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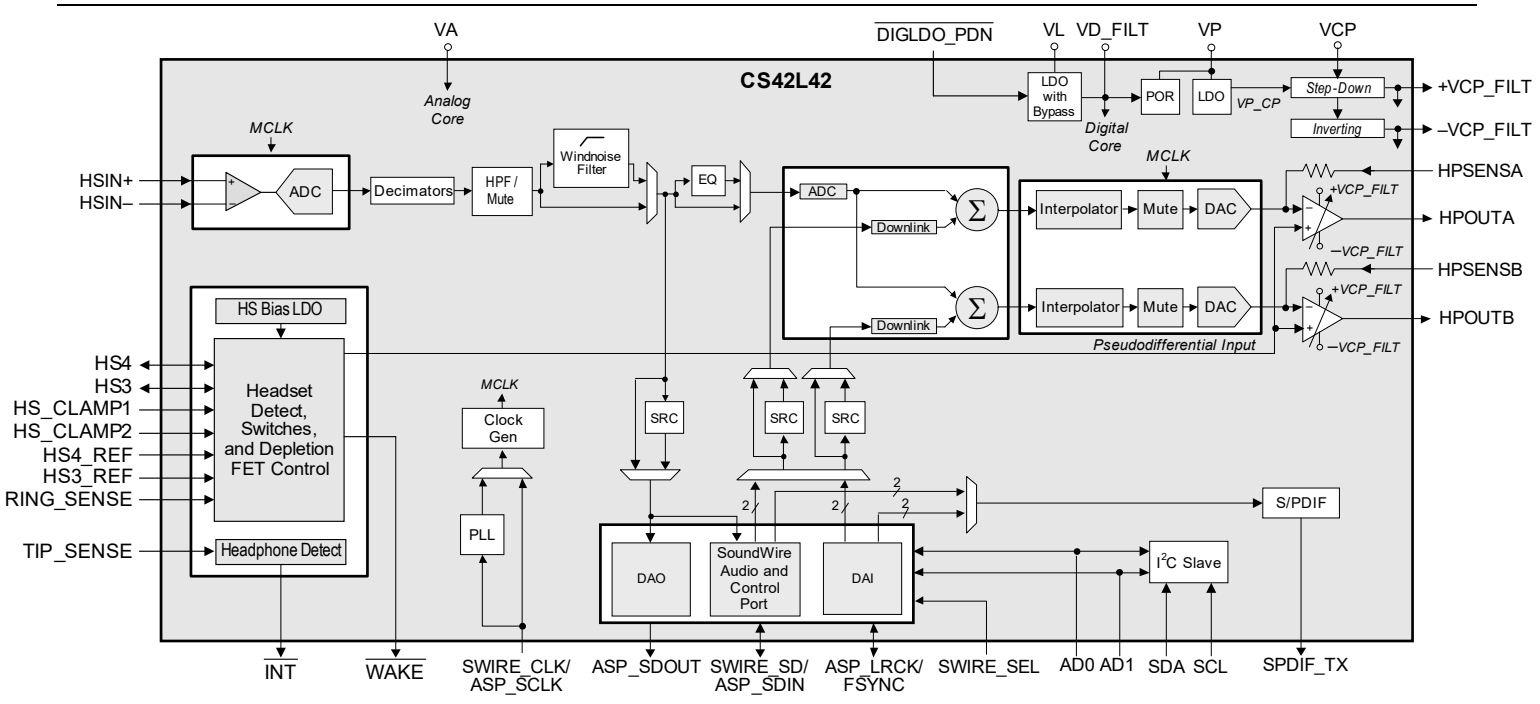
Low-Power Audio Codec with SoundWire®–I²S/TDM and Audio Processing

System Features

- Stereo headphone (HP) output with 114-dB dynamic range
  - Class H HP amplifier with four-level automatic or manual supply adjust
  - Power output 2 x 35 mW into 30 Ω
- Mono mic input with 114-dB dynamic range
  - Low-noise headset bias with integrated bias resistor
  - 1-V_{RMS} input voltage
  - Integrated AC-coupling capacitors
- Integrated detect features
  - OMTP (Open Mobile Terminal Platform) and AHJ (American headset jack) headset-type detection and configuration with low-impedance internal switches
  - Mic short (S0 Button) detect with ADC automute
  - Automatic Hi-Z of headset bias output to ground on headset bias current rise or HP/headset unplug
- System wake from headset/headphone plug/unplug or S0 button press
- Interrupt output
- Mono equalizer for side-tone mix
- MIPI® SoundWire® or I²C/I²S/TDM control and audio interface
- S/PDIF transmit (Sony/Philips digital interface format)
- Integrated fractional-N PLL
  - Increases system-clock flexibility for audio processing
  - Reference clock sourced from either I²S/TDM bit clock or MIPI SoundWire clock
- Audio serial port (ASP)
  - I²S (two channels) or TDM (up to four channels)
  - Slave or Hybrid-Master Mode (bit-clock slave and LRCK/FSYNC derived from bit clock)
  - Sample-rate converter (SRC) for two input channels, with bypass
  - SRC for one output channel, with bypass
  - User isochronous audio transport support
  - Supports up to 192-kHz sample rate to S/PDIF output
  - Sample rate support for 8 to 192 kHz
- Integrated power management
  - Digital core operates from either an external 1.2-V supply or LDO from a 1.8-V supply.
  - Step-down charge pump improves HP efficiency
  - Independent peripheral power-down controls
  - Standby operation from VP with all other supplies powered off
  - VP monitor to detect and report brownout conditions
  - Low-impedance switching suppresses ground-noise

Applications

- Ultrabooks, tablets, and smartphones
- Digital headsets



General Description

The CS42L42 is a low-power audio codec with integrated MIPI SoundWire interface or I²C/I²S/TDM interfaces designed for portable applications. It provides a high-dynamic range, stereo DAC for audio playback and a mono high-dynamic-range ADC for audio capture.

The CS42L42 provides high performance (up to 24-bit) audio for ADC and DAC audio playback and capture functions as well as for the S/PDIF transmitter. The CS42L42 architecture includes bypassable SRCs and a bypassable, three-band, 32-bit parametric equalizer that allows processing of digital audio data.

A digital mixer is used to mix the ADC or serial ports to the DACs. There is independent attenuation on each mixer input.

The processing along the output paths from the ADC or serial port to the two stereo DACs includes volume adjustment and mute control.

The CS42L42 is available in a 49-ball WLCSP package and a 48-pin QFN package for extended temperature range grade of –40°C to +85°C.

Table of Contents

1 Pin Assignments and Descriptions

This section shows pin assignments and describes pin functions.

1.1 WLCSP Pin Out (Through-Package View)

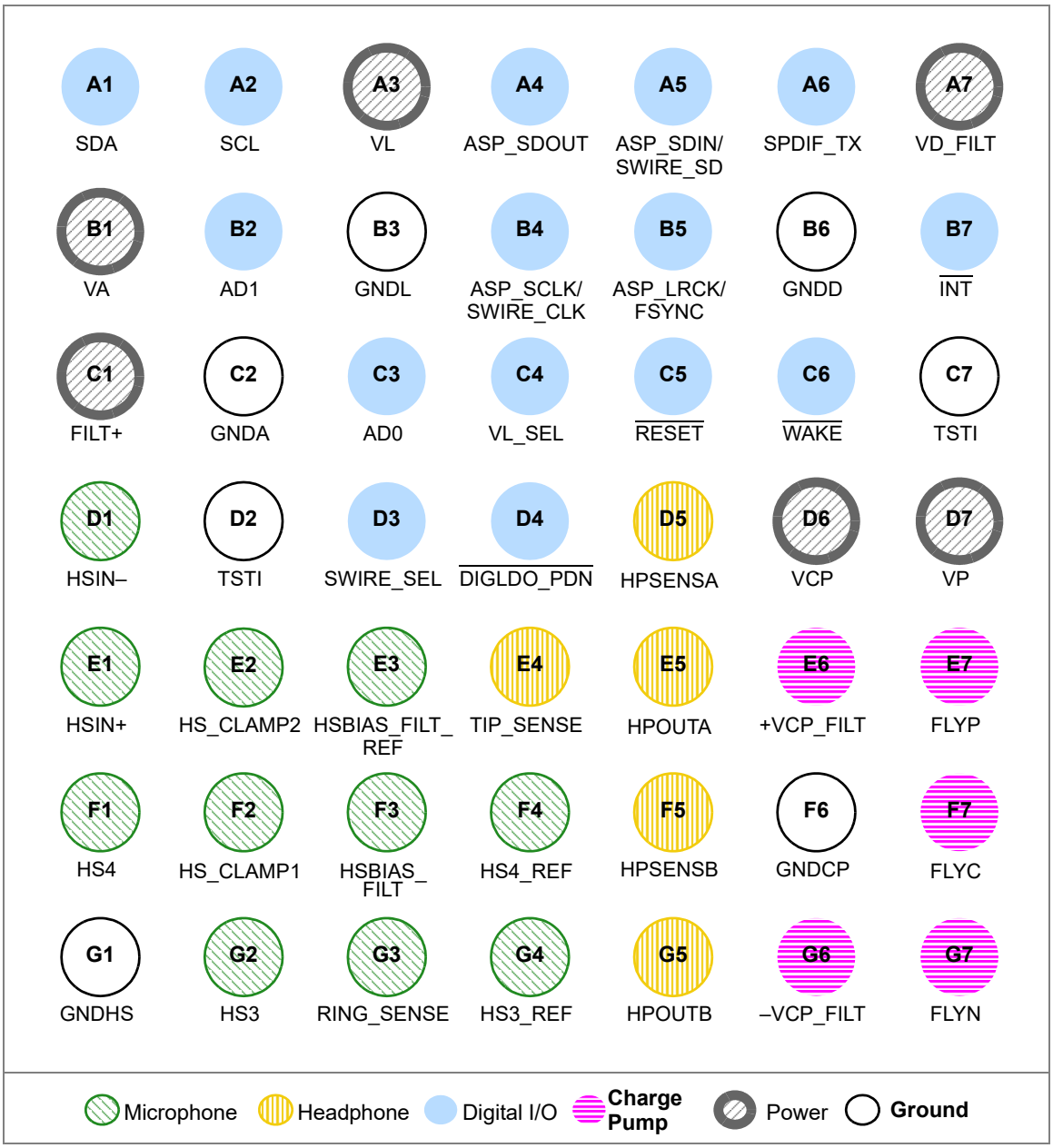


Figure 1-1. WLCSP Pin Diagram (Through-Package View)

1.2 QFN Pin Out (Through-Package View)

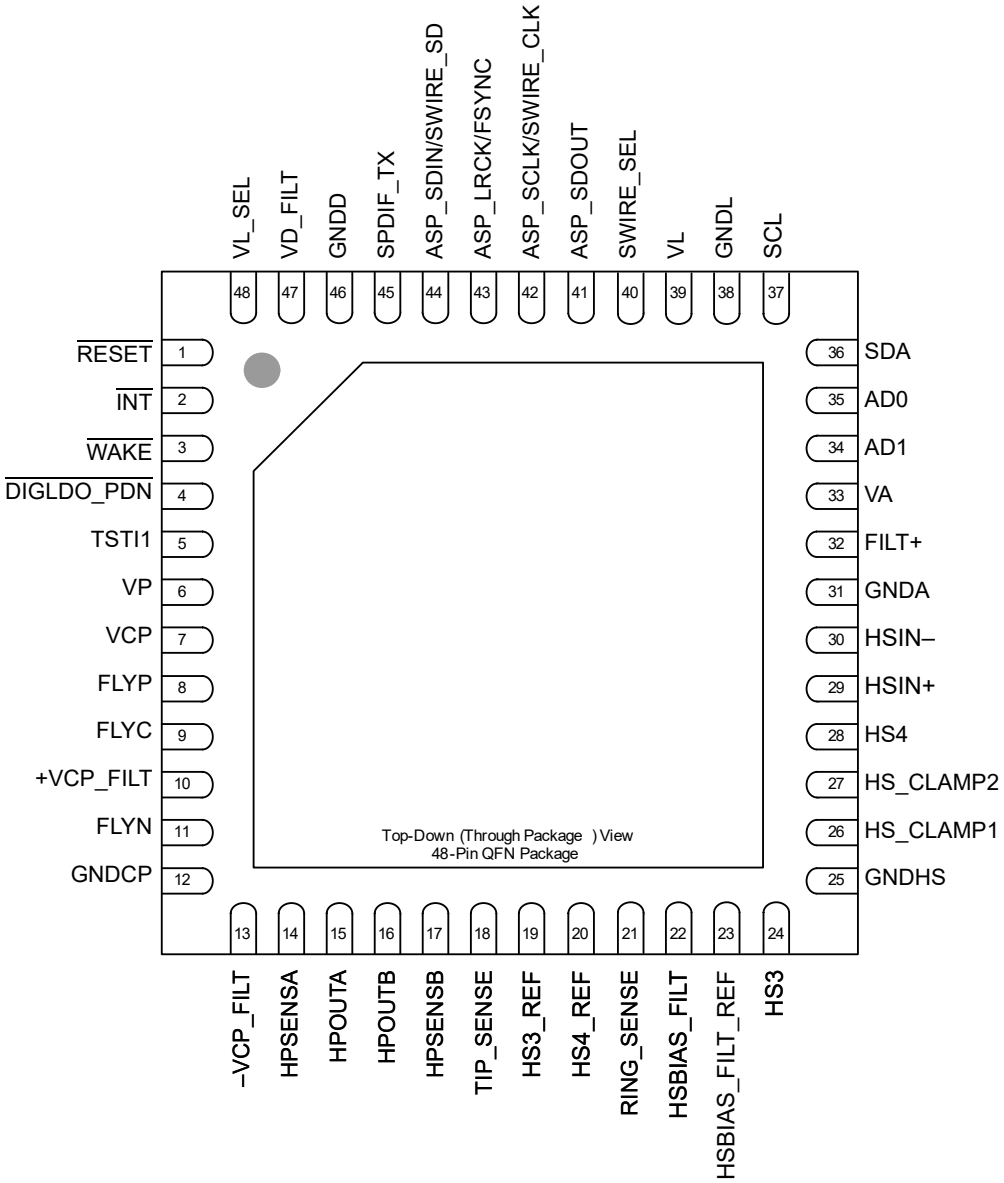


Figure 1-2. QFN Pin Diagram

1.3 Pin Descriptions

Table 1-1. Pin Descriptions

Pin Name	CSP Pin #	QFN Pin #	Power Supply	I/O	Pin Description	Internal Connection	Driver	Receiver	State at Reset
					Microphone				
HS_CLAMP1 HS_CLAMP2	F2 E2	26 27	VP	I	**Headset Depletion FET Connections.** Input to drain of integrated depletion FET for ground-noise rejection.	—	—	—	Input
HS3_REF HS4_REF	G4 F4	19 20	VP	I	**Headset Connection Reference**. Input to pseudodifferential HP output reference	—	—	—	Input
HS3 HS4	G2 F1	24 28	VP	I	**Headset Connections**. Input to headset and mic-button detection functions	—	—	—	Input
HSBIAS_FILT	F3	22	VP	I	**Headset Bias Source Voltage Filter.** Filter connection for the internal quiescent voltage used for headset bias generation.	—	—	—	Input
HSBIAS_FILT_REF	E3	23	VP	I	**Headset Bias Source Voltage Filter Reference.** Input of filter connection for the internal quiescent voltage used for headset-bias generation.	—	—	—	Input
HSIN–	D1	30	VP	I	**Inverting Mic Inputs.** Inverting analog input for the ADC.	—	—	—	Input
HSIN+	E1	29	VP	I	**Noninverting Mic Inputs.** Noninverting analog input for the ADC.	—	—	—	Input
RING_SENSE	G3	21	VP	I	**Ring Sense Input.** Sense pin to detect S/PDIF or headphone plug. Can be configured to be debounced on plug and unplug events independently.	—	—	—	Input
					Headphone				
HPOUTA HPOUTB	E5 G5	15 16	±VCP_FILT	O	**Headphone Audio Output.** Ground-centered audio output.	—	—	—	—
HPSENSA HPSENSB	D5 F5	14 17	±VCP_FILT	I	**Headphone Audio Sense Input.** Audio sense input.	—	—	—	Input
TIP_SENSE	E4	18	VP	I	**Tip Sense.** Output can be set to wake the system. Independently configurable to be debounced on plug and unplug events.	—	Hi-Z	—	—
					Digital I/O				
AD0 AD1	C3 B2	35 34	VL	I	**I²C Address Input/SoundWire Instance ID Input.** Address pins for I²C or SoundWire Instance ID [1:0] input.	—	—	Hysteresis on CMOS input	Input
ASP_LRCK/FSYNC	B5	43	VL	I/O	**ASP Left/Right Clock or Frame Sync.** Left or right word select, or frame start sync for the ASP interface.	—	CMOS output	Hysteresis on CMOS input	Input
ASP_SCLK/SWIRE_CLK	B4	42	VL	I	**ASP/SoundWire Serial Data Clock.** SoundWire data-shift clock in SoundWire Mode or serial data-shift clock for the ASP interface in I²S/TDM Mode. Source clock used for internal master clock generation.	—	—	Hysteresis on CMOS input	Input
ASP_SDIN/SWIRE_SD	A5	44	VL	I/O	**ASP Serial Data Input/SoundWire Serial Data Input and Output.** Serial data input and output in SoundWire mode or serial data input for the ASP interface in I²S/TDM mode.	—	CMOS output	Hysteresis on CMOS input	Input
ASP_SDOUT	A4	41	VL	O	**ASP Serial Data Output.** Serial data output for the ASP interface.	Weak pull-down	CMOS output	—	Output
$\overline{\text{DIGLDO\_PDN}}$	D4	4	VP	I	**Digital LDO Power Down.** Digital core logic LDO power down.	—	—	Hysteresis on CMOS input	Input
$\overline{\text{INT}}$	B7	2	VP	O	**Interrupt output.** Programmable, open-drain, active-low programmable interrupt output.	—	CMOS open-drain output	—	Output
$\overline{\text{RESET}}$	C5	1	VP	I	**Reset.** Hardware reset.	—	—	Hysteresis on CMOS input	Input
SCL	A2	37	VL	I	**I²C Clock.** Clock input for the I²C interface.	—	—	Hysteresis on CMOS input	Input

Table 1-1. Pin Descriptions *(Cont.)*

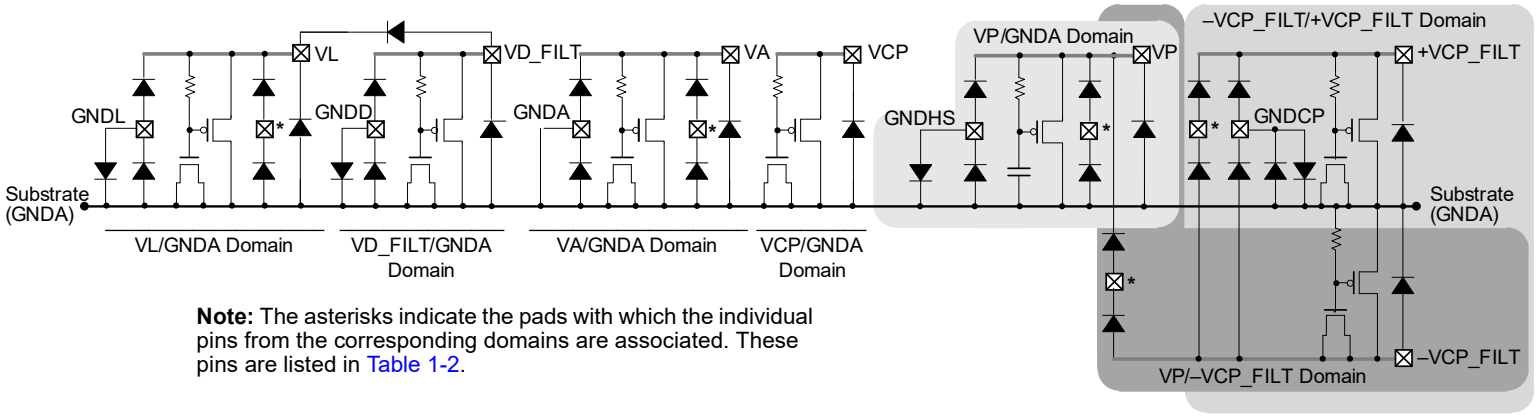
Pin Name	CSP Pin #	QFN Pin #	Power Supply	I/O	Pin Description	Internal Connection	Driver	Receiver	State at Reset
SDA	A1	36	VL	I/O	**I²C Input/Output.** I²C input and output.	—	CMOS open-drain output	Hysteresis on CMOS input	Input
SPDIF_TX	A6	45	VL	O	**S/PDIF Audio Serial Data Output.** Serial data output for S/PDIF interface.	—	CMOS output	—	Output
SWIRE_SEL	D3	40	VL	I	**SoundWire Select.** SoundWire interface selection input. Defines the serial and audio interface type. If asserted, SoundWire is the control and audio interface, otherwise I²C is control and TDM/I²S is used for audio data.	—	—	Hysteresis on CMOS input	Input
VL_SEL	C4	48	VP	I	**VL Supply Voltage Select.** Select for VL power supply voltage level. Connect to VP for 1.8-V VL supply, connect to GNDD for 1.2-V VL supply	—	—	Hysteresis on CMOS input	Input
$\overline{\text{WAKE}}$	C6	3	VP	O	**Wake up.** Programmable, open-drain, active-low output. This outputs the state of the Mic S0 or HP wake detect.	—	Hi-Z, CMOS open-drain output	—	Output
Charge Pump									
–VCP_FILT	G6	13	VCP/ VP[1]	O	**Inverting Charge Pump Filter Connection.** Power supply for the inverting charge pump that provides the negative rail for the HP amplifier.	—	—	—	—
+VCP_FILT	E6	10	VCP/ VP[1]	O	**Step Down Charge Pump Filter Connection.** Power supply for the step down charge pump that provides the positive rail for the HP amplifier.	—	—	—	—
FLYC	F7	9	VCP/ VP[1]	O	**Charge Pump Cap Common Node.** Common positive node for the HP amplifiers' step-down and inverting charge pumps' flying capacitors.	—	—	—	—
FLYN	G7	11	VCP/ VP[1]	O	**Charge Pump Cap Negative Node.** Negative node for the inverting charge pump's flying capacitor.	—	—	—	—
FLYP	E7	8	VCP/ VP[1]	O	**Charge Pump Cap Positive Node.** Positive node for HP amps' step-down charge pump's flying capacitor.	—	—	—	—
Power									
FILT+	C1	32	VA	I	**Positive Voltage Reference.** Positive reference voltage for internal sampling circuits.	—	—	—	—
VA	B1	33	N/A	I	**Analog Power Supply.** Power supply for the internal analog section.	—	—	—	—
VCP	D6	7	N/A	I	**Charge Pump Power.** Power supply for the internal HP amplifiers charge pump.	—	—	—	—
VD_FILT	A7	47	N/A	I	**1.2-V Digital Core Power Supply.** Power supply for internal digital logic.	—	—	—	—
VL	A3	39	N/A	I	**I/O Power Supply.** Power supply for external interface and internal digital logic.	—	—	—	—
VP	D7	6	N/A	I	**High Voltage Interface Supply.** Power supply for high voltage interface.	—	—	—	—
Ground									
GNDA	C2	31	N/A	I	**Analog Ground.** Ground reference for the internal analog section.	—	—	—	—
GNDL	B3	38	N/A	I	**Digital Ground.** Ground reference for interface section.	—	—	—	—
GNDHS	G1	25	N/A	I	**Headset Ground.** Ground reference for the internal analog section.	—	—	—	—
GNDCP	F6	12	N/A	I	**Charge Pump Ground.** Ground reference for the internal HP amplifiers charge pump.	—	—	—	—
GNDD	B6	46	N/A	I	**Digital Ground.** Ground reference for the internal digital circuits.	—	—	—	—
Test									
TSTI	D2, C7	—	N/A	I	**Test input.** Connect to GNDA.	—	—	—	—

1. The power supply is determined by ADPTPWR setting (see Section 7.14.1). VP is used if ADPTPWR = 001 (VP_CP Mode) or when necessary for ADPTPWR = 111 (Adapt-to-Signal Mode).

1.4 Electrostatic Discharge (ESD) Protection Circuitry

ESD-sensitive device. The CS42L42 is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to current JEDEC ESD standards.

Fig. 1-3 provides a composite view of the ESD domains showing the ESD protection paths between each pad and the substrate (GNDA) and the interrelations between some domains. Note that this figure represents the structure for the internal protection devices and that additional protections can be implemented as part of the integration into the board.



Note: The asterisks indicate the pads with which the individual pins from the corresponding domains are associated. These pins are listed in Table 1-2.

Figure 1-3. Composite ESD Topology

Table 1-2 shows the individual ESD domains and lists the pins associated with each domain.

Table 1-2. ESD Domains

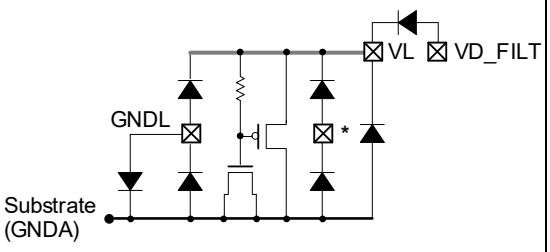
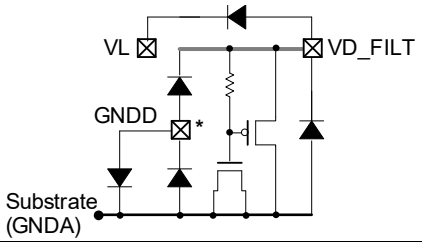
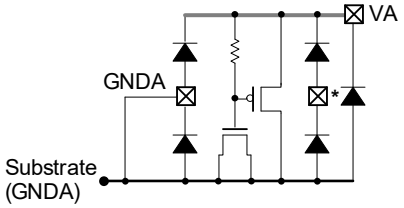
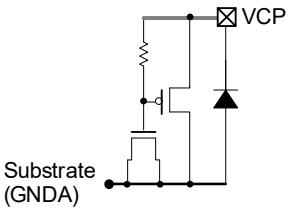
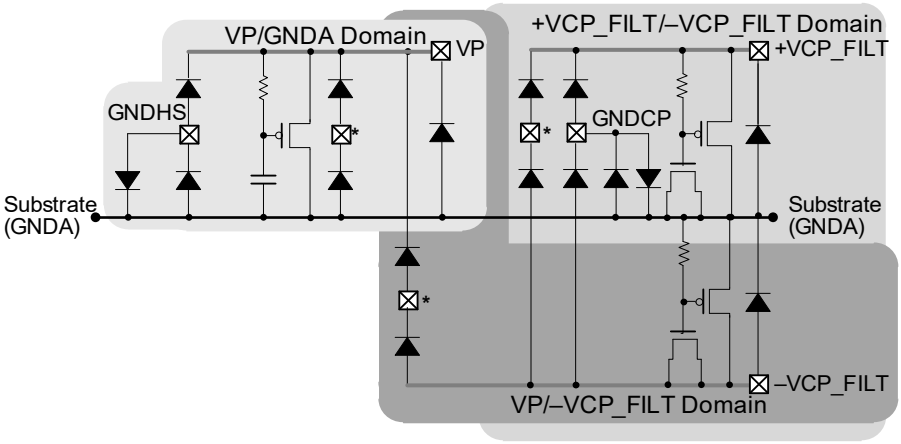
ESD Domain	Signal Name (CSP/QFN) (See * in Topology Figures for Pad)	Topology
VL/ GNDA [1]	AD0 AD1 ASP_LRCK/FSYNC GNDL SCL SDA ASP_SDOUT SPDIF_TX SWIRE_SEL ASP_SCLK/SWIRE_CLK SWIRE_SD/ASP_SDIN VD_FILT VL	
VD_FILT/ GNDA	VD_FILT GNDD TSTI	
VA/ GNDA	FILT+ GNDA VA	

Table 1-2. ESD Domains *(Cont.)*

ESD Domain	Signal Name (CSP/QFN) (See * in Topology Figures for Pad)	Topology
VCP/ GNDA	VCP	
VP/ GNDA	GNDHS HS3 HS4 HS_CLAMP1 HS_CLAMP2 HSBIAS_FILT HSBIAS_FILT_REF HSIN+ HSIN– VP VL_SEL $\overline{\text{INT}}$ $\overline{\text{WAKE}}$ $\overline{\text{RESET}}$ DIGLDO_PDN	
+VCP_ FILT/ –VCP_ FILT	+VCP_FILT –VCP_FILT FLYN HPSENSA HPSENSB HPOUTA HPOUTB GNDCP	
VP/ –VCP_ FILT	FLYC FLYP HS3_REF HS4_REF RING_SENSE TIP_SENSE	

1. See Section 5.8 for additional information regarding VD_FILT andVL.

2 Typical Connections

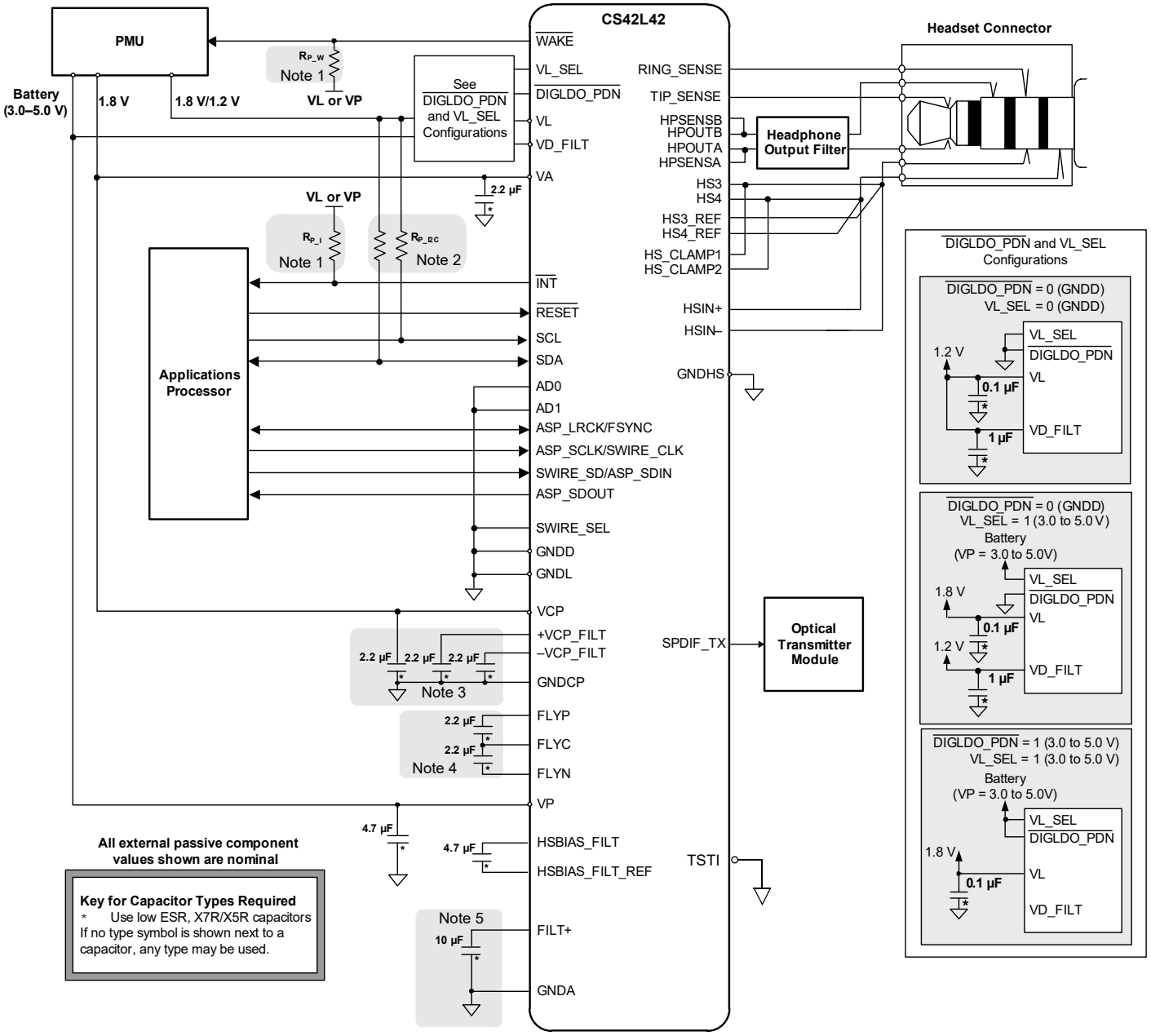


Figure 2-1. Typical Connection Diagram for I²C, I²S, or TDM

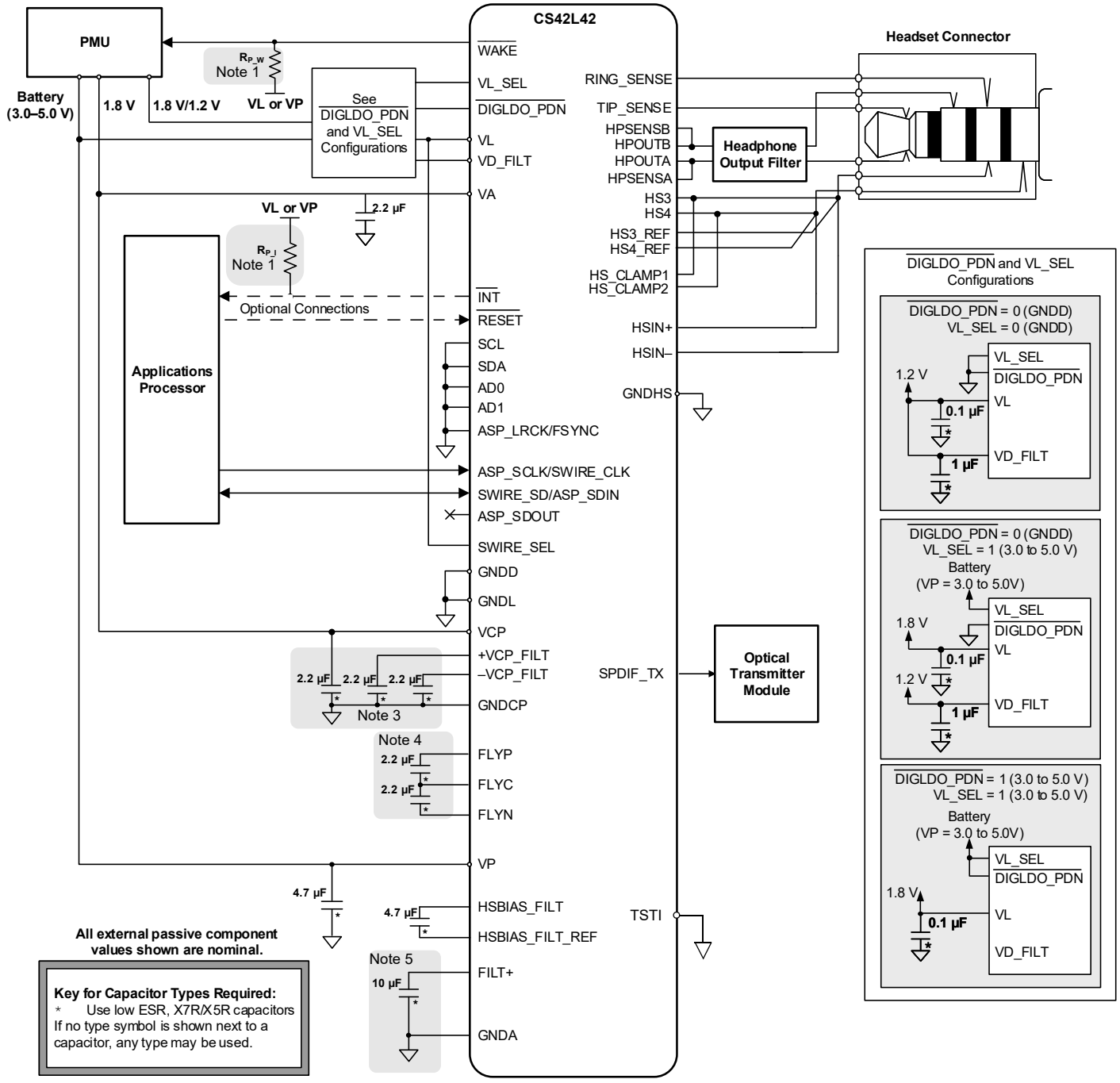


Figure 2-2. Typical Connection Diagram for SoundWire

Notes:

1. R_{P_I} and R_{P_W} values can be determined by the $\overline{INT}$ and $\overline{WAKE}$ pin specifications in Table 3-25.
2. R_{P_I2C} values can be determined by the I^2C pull-up resistance specification in Table 3-24.
3. The headphone amplifier's output power and distortion ratings use the nominal capacitances shown. Larger capacitance reduces ripple on the internal amplifiers' supplies and, in turn, reduces distortion at high-output power levels. Smaller capacitance may not reduce ripple enough to achieve output power and distortion ratings. Because actual values of typical X7R/X5R ceramic capacitors deviate from nominal values by a percentage specified in the manufacturer's data sheet, capacitors must be selected for minimum output power and maximum distortion required. Higher value capacitors than those shown may be used, however lower value capacitors must not (values can vary from the nominal by ±20%). See Section 2.1.2 for additional details.
4. Series resistance in the path of the power supplies must be avoided. Any voltage drop on VCP directly affects the negative charge-pump supply (–VCP_FILT) and clips the audio output.
5. Lowering capacitance below the value shown affects PSRR, THD+N performance, ADC–DAC isolation and intermodulation, and interchannel isolation and intermodulation.

2.1 Electromagnetic Compatibility (EMC) Circuitry

The circuit in Fig. 2-3 may be applied to signals not local to the CS42L42 (i.e., that traverse significant distances) for EMC.

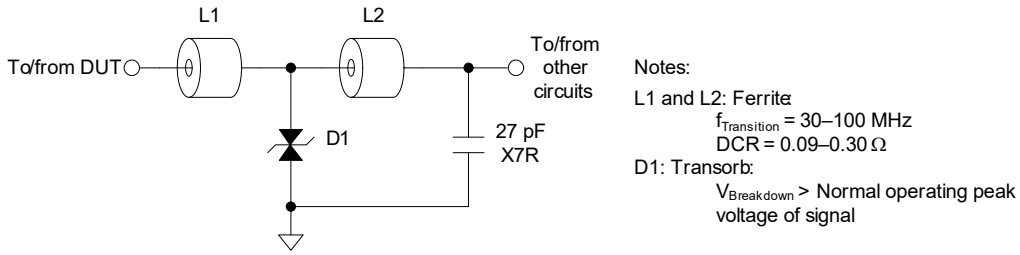


Figure 2-3. Optional EMC Circuit

2.1.1 Low-Profile Charge-Pump Capacitors

In the typical connection for analog mics (Fig. 2-1), the recommended capacitor values for the charge-pump circuitry are 2.2 µF, rated as X7R/X5R or better. The following low-profile versions of these capacitors are suitable for the application:

- Description: 2.2 µF ±20%, 6.3 V, X5R, 0201
- Manufacturer, Part Number: Murata, GRM033R60J225ME47, nominal height = 0.3 mm
- Manufacturer, Part Number: AVX, 02016D225MAT2A, nominal height = 0.33 mm

Note: Although the 0201 capacitors described are suitable, larger capacitors such as 0402 or larger may provide acceptable performance.

2.1.2 Ceramic Capacitor Derating

Note 3 in Fig. 2-1 highlights that ceramic capacitor derating factors can significantly affect in-circuit capacitance values and, in turn, CS42L42 performance. Under typical conditions, numerous types and brands of large-value ceramic capacitors in small packages exhibit effective capacitances well below their ±20% tolerance, with some being derated by as much as –50%. These same capacitors, when tested by a multimeter, read much closer to their rated value. A similar derating effect has not been observed with tantalum capacitors.

The derating observed varied with manufacturer and physical size: Larger capacitors performed better, as did ones from Kemet Electronics Corp. and TDK Corp. of any size. This derating effect is described in data sheets and in applications notes from capacitor manufacturers. For instance, as DC and AC voltages are varied from the standard test points (applied DC and AC voltages for standard test points versus PSRR test are 0 and 1 V_{RMS} @ 1 kHz versus 0.9 V and ~1 mV_{RMS} @ 20 Hz–20 kHz), it is documented that the capacitances vary significantly.

3 Characteristics and Specifications

Table 3-1 defines parameters as they are characterized in this section.

Table 3-1. Parameter Definitions

Parameter	Definition
Dynamic range	The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. A signal-to-noise ratio measurement over the specified bandwidth made with a –60 dB signal; 60 dB is added to resulting measurement to refer the measurement to full scale. This technique ensures that distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17–1991, and the Electronic Industries Association of Japan, EIAJ CP–307. Dynamic range is expressed in decibel units.
Idle channel noise	The rms value of the signal with no input applied (properly back-terminated analog input, digital zero, or zero modulation input). Measured over the specified bandwidth.
Interchannel isolation	A measure of cross talk between the left and right channel pairs. Interchannel isolation is measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Interchannel isolation is expressed in decibel units.
Load resistance and capacitance	The recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. The load capacitance effectively moves the band-limiting pole of the amp in the output stage. Increasing load capacitance beyond the recommended value can cause the internal op-amp to become unstable.
Offset error	The deviation of the midscale transition (111…111 to 000…000) from the ideal.
Output offset voltage	The DC offset voltage present at the amplifier's output when its input signal is in a mute state. The offset exists due to CMOS process limitations and is proportional to analog volume settings. When measuring the offset out the headphone amplifier, the headphone amplifier is ON.
Total harmonic distortion + noise (THD+N)	The ratio of the rms sum of distortion and noise spectral components across the specified bandwidth (typically 20 Hz–20 kHz) relative to the rms value of the signal. THD+N is measured at –1 and –20 dBFS for the analog input and at 0 and –20 dB for the analog output, as suggested in AES17–1991 Annex A. THD+N is expressed in decibel units.

Table 3-2. Recommended Operating Conditions

Test conditions: GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground.

Parameters			Symbol	Minimum [1]	Maximum [1]	Unit
DC power supply	Charge pump		VCP	1.66	1.94	V
	LDO regulator for digital [2]	$\overline{\text{DIGLDO\_PDN}}$ = 0 and VL_SEL = 0	VD_FILT	1.10	1.30	V
	Serial interface control port and S/PDIF transmitter	$\overline{\text{DIGLDO\_PDN}}$ = 0 and VL_SEL = 0 VL_SEL = 1	VL VL	1.10 1.66	1.30 1.94	V V
	Analog		VA	1.66	1.94	V
	Battery supply		VP	2.50 [3]	5.25	V
External voltage applied to pin [4,5]		TIP_SENSE pin ±VCP_FILT domain pins [6] VL domain pins VA domain pins VP domain pins	V_{INHI} V_{VCPF} V_{VL} V_{VA} V_{VP}	–VCP_FILT – 0.3 –VCP_FILT – 0.3 –0.3 –0.3 –0.3	VP + 0.3 +VCP_FILT + 0.3 VL + 0.3 VA + 0.3 VP + 0.3	V V V V V
Ambient temperature			T_A	–40	+85	°C

1. Device functional operation is guaranteed within these limits; operation outside them is not guaranteed or implied and may reduce device reliability.
2. If $\overline{\text{DIGLDO\_PDN}}$ is deasserted, no external voltage must be applied to VD_FILT.
3. Although device operation is guaranteed down to 2.5 V, device performance is guaranteed only down to 3.0 V. The following are affected when VP < 3.0 V: HSBIAS, charge pump LDO, TIP_SENSE threshold, RING_SENSE threshold.
4. The maximum over/undervoltage is limited by the input current.
5. Table 1-1 lists the power supply domain in which each CS42L42 pin resides.
6. ±VCP_FILT is specified in Table 3-16.

Table 3-3. Absolute Maximum Ratings

Test conditions: GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground.

Parameters		Symbol	Minimum	Maximum	Unit
DC power supply	Charge pump, LDO, serial/control, analog (see Section 4.15)	VL, VA, VCP	–0.3	2.33	V
	Digital core	VD_FILT	–0.3	1.55	V
	Battery	VP	–0.3	6.3	V
Input current [1]		I_{in}	—	±10	mA
Ambient operating temperature (power applied)		T_A	–50	+115	°C
Storage temperature		T_{stg}	–65	+150	°C

Caution: Stresses beyond "Absolute Maximum Ratings" levels may cause permanent damage to the device. These levels are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Table 3-2, "Recommended Operating Conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. Any pin except supply pins. Transient currents of up to ±100 mA on analog input pins do not cause SCR latch-up.

Table 3-4. Output Fault Rating

Test conditions: GNDA = GNDCP = 0 V; VA = 1.8 V; VP = 3.6 V; voltages are with respect to ground.

Source [1]	Fault Supply	Expected Years [2]
HPOUT(A,B)	VA GNDA +VCP_FILT –VCP_FILT VP	1.5 2 0.5 1.5 1.5
HS3/HS4 (HSx switch to ground)	HPOUT(A,B)[3]	3.2
HS3/HS4 (HSx switches to HSBIAS)	HPOUT(A,B)[3]	0.75
HS3_REF/HS4_REF (HSx connected to ground)	HPOUT(A,B)	3.2
HS3_REF/HS4_REF (HSx not connected to ground)	HPOUT(A,B)	0.75

1. Each source is individually connected directly to the specified supply during a fault condition.
2. The rating is based on foundry electromigration design rules when a perpetual fault exists on the HP outputs. When the specified time expires, analog performance is expected to degrade.
3. HPOUTx = 1 Vrms. If shorted to HSx, the headphone may be current limited in this configuration.

Table 3-5. Combined High-Performance ADC On-Chip Analog and Digital Filter Characteristics

Test conditions (unless specified otherwise): T_A = +25°C; MCLK = 12 MHz; MCLK_SRC_SEL = 0; Fs_{INT} = 48 kHz; path is HSIN to internal routing engine. All gains are set to 0 dB; HPF disabled.

Parameter [1,2]		Min	Typical	Max	Unit
Notch filter on (ADC_NOTCH_DIS = 0)	Passband (normalized to 0.417x10^{-3} Fs_{INT}) –0.18-dB corner	—	0.390	—	Fs_{int}
	Passband (normalized to 0.417x10^{-3} Fs_{INT}) –3.0-dB corner	—	0.410	—	Fs_{int}
	Passband ripple (0.417x10^{-3} Fs_{INT} to 0.390 Fs_{INT}; normalized to 0.417x10^{-3} Fs_{int})	–0.23	—	0.15	dB
	Stopband attenuation 1 (0.5 Fs_{INT} to 0.524 Fs_{INT})	45	—	—	dB
	Stopband attenuation 2 (0.524 Fs_{INT} to 3 Fs_{INT})	70	—	—	dB
	Total group delay [3]	—	5.6/Fs_{int}	—	s
Notch filter off (ADC_NOTCH_DIS = 1)	Passband (normalized to 0.417x10^{-3} Fs_{INT}) –0.05-dB corner	—	0.390	—	Fs_{int}
	Passband (normalized to 0.417x10^{-3} Fs_{INT}) –3.0-dB corner	—	0.500	—	Fs_{int}
	Passband ripple (0.417x10^{-3} Fs_{INT} to 0.417 Fs_{INT}; normalized to 0.417x10^{-3} Fs_{INT})	–0.29	—	0.15	dB
	Stopband attenuation (0.64 Fs_{INT} to 3 Fs_{INT})	70	—	—	dB
	Total group delay [3]	—	5.6/Fs_{int}	—	s

1. Response scales with Fs_{int} (internal sample rate, based on MCLK). Specifications are normalized to Fs_{int} and are denormalized by multiplying by Fs_{int}.
2. Measurements with HPF disabled require either differential configuration or single-ended configuration with –30 dBFS input signal.
3. Informational only; group delay cannot be measured for this block by itself.Total group delay includes delay through the entire ADC and decimator path total-group delay is measured at 1 kHz.

Table 3-6. ADC High-Pass Filter (HPF) Characteristics

Test conditions (unless specified otherwise): ADC_HPF_CF = 00; all gains are set to 0 dB; specifications represent the frequency response of the entire path with ADC_NOTCH_DIS = 1, SRC_ADC_BYPASS = 1, ADC_WNF_EN = 0, and ADC_HPF_EN = 1.

Parameter [1]		Minimum	Typical	Maximum	Unit
Passband (normalized to 0.2083 FS_{INT})	–0.05-dB corner	—	0.666 x 10^{-3}	—	Fs_{INT}
	–3.0-dB corner	—	77.0 x 10^{-6}	—	Fs_{INT}
Phase deviation @ 0.453 x 10^{-3} Fs_{INT} [2]		—	12.37	—	Deg
Filter settling time [3]	ADC_HPF_CF = 00 (38.8 x 10^{-6} x Fs_{INT} mode)	—	2900/Fs_{INT}	—	s
	ADC_HPF_CF = 01 (2.5 x 10^{-3} x Fs_{INT} mode)	—	170/Fs_{INT}	—	s
	ADC_HPF_CF = 10 (4.9 x 10^{-3} x Fs_{INT} mode)	—	90/Fs_{INT}	—	s
	ADC_HPF_CF = 11 (9.7 x 10^{-3} x Fs_{INT} mode)	—	50/Fs_{INT}	—	s

1. Response scales with Fs_{INT} (based on internal MCLK). Specifications are normalized to Fs_{INT} and are denormalized by multiplying by Fs_{INT}.
2. An additional –2° phase deviation may be present through the total path from HSIN to SDOUT.
3. Required time for the magnitude of the DC component present at the output of the HPF to reach 5% of the applied DC signal.

Table 3-7. Combined DAC Digital, On-Chip Analog, and HPOUTx Filter Characteristics

Test conditions (unless specified otherwise): T_A = +25°C; MCLK = 12 MHz, MCLK_SRC_SEL = 0, Fs_{INT} = 48 kHz; path is internal routing engine to HPOUTx, analog and digital gains are all set to 0 dB; HPF disabled.

Parameter [1]		Minimum	Typical	Maximum	Unit
Passband	–0.05-dB corner	—	0.48	—	Fs_{INT}
	–3.0-dB corner	—	0.50	—	Fs_{INT}
Passband ripple (0.417x10^{-3} Fs_{INT} to 0.417 Fs_{INT}; normalized to 0.417x10^{-3} Fs_{INT})		–0.04	—	0.063	dB
Stopband attenuation (0.545 Fs_{INT} to Fs_{INT})		60	—	—	dB
Total group delay [2]		—	5.35/Fs_{INT}	—	s

1. Response scales with Fs_{INT} (based on internal MCLK). Specifications are normalized to Fs_{INT} and denormalized by multiplying by Fs_{INT}.
2. Informational only; group delay cannot be measured for this block by itself. An additional 5.5/Fs_{int} group delay may be present through the serial ports and internal audio bus.

Table 3-8. DAC High-Pass Filter (HPF) Characteristics

Test conditions (unless specified otherwise) Analog and digital gains are all set to 0 dB; T_A = +25°C.

Parameter [1]		Minimum	Typical	Maximum	Unit
Passband	–0.05-dB corner –3.0-dB corner	— —	$0.180x10^{-3}$ $19.5x10^{-6}$	— —	Fs_{INT} Fs_{INT}
Passband ripple ($0.417x10^{-3}$ Fs_{INT} to 0.417 Fs_{INT}; normalized to 0.417 Fs_{INT})		—	—	0.01	dB
Phase deviation @ $0.453x10^{-3}$ Fs_{INT}		—	2.45	—	°
Filter settling time [2]		—	$24.5x10^{3}/Fs_{INT}$	—	s

1. Response scales with Fs_{INT} (internal sample rate, based on MCLK). Specifications are normalized to Fs_{INT} and are denormalized by multiplying by Fs_{INT}.
2. Required time for the magnitude of the DC component present at the output of the HPF to reach 5% of the applied DC signal.

Table 3-9. HSINx to SDOUT with SRC-Enabled Datapath Characteristics

Test conditions (unless specified otherwise): LRCK = Fs_{INT} = Fs_{EXT} = 48 kHz; MCLK = 12 MHz; HPF disabled; passband/stopband levels normalized to 20 Hz; entire path characteristics including AFE + ADC + SRC + serial port.

Parameters [1,2]			Minimum	Typical	Maximum	Unit
ADC notch filter enabled	Passband	–0.22-dB corner –3.0-dB corner	— —	0.390 0.410	— —	Fs_{EXT} Fs_{EXT}
	Passband ripple ($0.417x10^{-3}$ Fs_{EXT} to 0.390 Fs_{EXT}; normalized to 20 Hz)		–0.30	—	0.15	dB
	Stopband rejection from 0.477 Fs_{EXT} to 3 Fs_{EXT}		70	—	—	dB
	Square wave overshoot		—	—	3.1	dB
	Group delay, bark-weighted average		—	—	$38.5/Fs_{EXT}$	s
	Group delay	$Fs_{EXT} \le 44.1$ kHz $Fs_{EXT} \ge 48$ kHz)	— —	$17.4/Fs_{INT} + (13.2 \pm 1.5)/Fs_{EXT}$ $(12.4 \pm 0.5)/Fs_{INT} + (11.9 \pm 1)/Fs_{EXT}$	— —	s s
	SRC-disabled group delay [3]		—	(13.9±1)/Fs	—	s
ADC notch filter disabled	Passband	–0.22-dB corner –3.0-dB corner	— —	0.444 0.466	— —	Fs_{EXT} Fs_{EXT}
	Passband ripple ($0.417x10^{-3}$ Fs_{EXT} to 0.417 Fs_{EXT}; normalized to 20 Hz)		–0.30	—	0.15	dB
	Stopband rejection from 0.480 Fs_{EXT} to 0.521 Fs_{EXT}		55	—	—	dB
	Stopband rejection from 0.521 Fs_{EXT} to 0.640 Fs_{EXT}		14	—	—	dB
	Stopband rejection from 0.640 Fs_{EXT} to 3 Fs_{EXT}		70	—	—	dB
	Square wave overshoot		—	—	3.1	dB
	Group delay, bark-weighted average		—	—	$38.5/Fs_{EXT}$	s
	Group delay	$Fs_{EXT} \le 44.1$ kHz $Fs_{EXT} \ge 48$ kHz)	— —	$17.4/Fs_{INT} + (13.2 \pm 1.5)/Fs_{EXT}$ $(12.4 \pm 0.5)/Fs_{INT} + (11.9 \pm 1)/Fs_{EXT}$	— —	s s
	SRC disabled group delay [3]		—	(13.9±1)/Fs	—	s

1. Fs_{EXT} is the external sample rate (LRCK/FSYNC frequency). Response scales with Fs_{EXT}.
2. Measurements with HPF disabled require either differential configuration or single-ended configuration with –30 dBFS input signal.
3. This value varies by up to 1 Fs. If SRC is disabled, Fs = Fs_{OUT} = Fs_{IN}.

Table 3-10. SDIN to HPOUTx with SRC-Enabled Datapath Characteristics

Test conditions (unless specified otherwise): LRCK = Fs_{INT} = Fs_{EXT} = 48 kHz; MCLK = 12 MHz; HPF disabled; passband/stopband levels normalized to $0.417x10^{-3}$ Fs_{EXT}; entire path characteristics including serial port + SRC + DAC + HPOUT.

Parameters [1]		Minimum	Typical	Maximum	Unit
Passband	–0.2-dB corner –3.0-dB corner	— —	0.463 0.466	— —	Fs_{EXT} Fs_{EXT}
Passband ripple ($0.417x10^{-3}$ Fs_{EXT} to 0.417 Fs_{EXT}; normalized to $0.417x10^{-3}$ Fs_{EXT})		–0.16	—	0.02	dB
Response at 0.5 Fs_{EXT}		—	—	–54.9	dB
Stopband rejection from 0.480 Fs_{EXT} to 0.524 Fs_{EXT}		55	—	—	dB
Stopband rejection from 0.524 Fs_{EXT} to 0.545 Fs_{EXT}		39	—	—	dB
Stopband rejection from 0.545 Fs_{EXT} to 3 Fs_{EXT}		60	—	—	dB
Square wave overshoot		—	—	3.1	dB
Group delay, bark-weighted average		—	—	$34/Fs_{EXT}$	s
Group delay	$Fs_{EXT} \le 48$ kHz $Fs_{EXT} \ge 88.2$ kHz)	— —	$(15.8 \pm 1.5)/Fs_{EXT} + 10.3/Fs_{INT}$ $(20.1 \pm 1)/Fs_{EXT} + (11.6 \pm 0.5)/Fs_{INT}$	— —	s s
SRC disabled group delay [2]		—	(15±1)/Fs	—	s

1. Fs_{EXT} is the external sample rate (LRCK/FSYNC frequency). Response scales with Fs_{EXT}.
2. This value varies by up to 1 Fs. If SRC is disabled, Fs = Fs_{OUT} = Fs_{IN}.

Table 3-11. Wind-Noise Digital Filter Characteristics

Test conditions (unless specified otherwise): MCLK = 12 MHz; MCLK_SRC_SEL = 0; Fs_{INT} = 48 kHz; ADC HPF disabled.

Parameters [1,2]		Minimum	Typical	Maximum	Unit
Passband –3.0-dB corner	ADC_WNF_CF = 000	—	160	—	Hz
	ADC_WNF_CF = 001	—	180	—	Hz
	ADC_WNF_CF = 010	—	200	—	Hz
	ADC_WNF_CF = 011	—	220	—	Hz
	ADC_WNF_CF = 100	—	240	—	Hz
	ADC_WNF_CF = 101	—	260	—	Hz
	ADC_WNF_CF = 110	—	280	—	Hz
	ADC_WNF_CF = 111	—	300	—	Hz
Passband –0.05-dB corner	ADC_WNF_CF = 000	—	280	—	Hz
	ADC_WNF_CF = 001	—	315	—	Hz
	ADC_WNF_CF = 010	—	350	—	Hz
	ADC_WNF_CF = 011	—	385	—	Hz
	ADC_WNF_CF = 100	—	420	—	Hz
	ADC_WNF_CF = 101	—	455	—	Hz
	ADC_WNF_CF = 110	—	490	—	Hz
	ADC_WNF_CF = 111	—	525	—	Hz
Passband ripple (–0.05-dB corner to 0.417 Fs_{INT}; normalized to 0.417 Fs_{INT})		—	—	0.15	dB
Filter settling time	ADC_WNF_CF = 000	—	731/Fs_{INT}	—	s
	ADC_WNF_CF = 001	—	650/Fs_{INT}	—	s
	ADC_WNF_CF = 010	—	585/Fs_{INT}	—	s
	ADC_WNF_CF = 011	—	532/Fs_{INT}	—	s
	ADC_WNF_CF = 100	—	487/Fs_{INT}	—	s
	ADC_WNF_CF = 101	—	450/Fs_{INT}	—	s
	ADC_WNF_CF = 110	—	418/Fs_{INT}	—	s
	ADC_WNF_CF = 111	—	390/Fs_{INT}	—	s

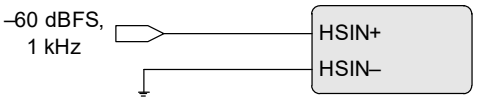
1. Responses are clock dependent and scale with Fs_{INT}. The full-band response plot (Fig. 9-28) is normalized to Fs_{INT} and is denormalized by multiplying the x-axis scale by Fs. Passband frequencies above the transition-band response plot (Fig. 9-29) are for a Fs_{INT} of 48 kHz. Frequencies for other Fs_{INT} values are determined by multiplying the x-axis scale shown in the transition band plot and passband frequencies above by a factor of Fs_{INT}/48 kHz.
2. Wind-noise HPF characteristics apply only if the given filter is enabled (ADC_WNF_EN = 1). Otherwise, the signal is unaffected by this block.

Table 3-12. HSIN-to-Serial Data Out Characteristics

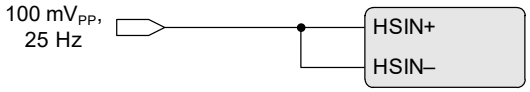
Test conditions (unless specified otherwise): Fig. 2-1 and Fig. 2-2 show CS42L42 connections; input is a full-scale 1-kHz sine wave; GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground; parameters and can vary with VA; typical performance data taken with VL = VA = 1.8 V, VP = 3.6 V; min/max performance data taken with VA = 1.66–1.94 V; VL = 1.8 V, VP = 3.6 V; T_A = +25°C; measurement bandwidth is 20 Hz–20 kHz; ASP_LRCK = Fs = 48 kHz; MCLK = 12 MHz; SRC bypassed in data path; mixer attenuation and digital volume = 0 dB. ADC_HPF_EN = 1. Specifications valid for pseudodifferential and fully differential inputs.

Parameter [1]			Minimum	Typical	Maximum	Unit
Dynamic range [2] (defined in Table 3-1)		A-weighted	108	114	—	dB
		Unweighted	105	111	—	dB
THD+N [3] (defined in Table 3-1)		Differential, –1-dBFS input	—	–85	–79	dB
		Single-ended, –1-dBFS input	—	–80	–74	dB
Common-mode rejection [4]			—	72	—	dB
DC voltage on HSIN with pin floating			—	1.35	—	V
Accuracy	Offset error (defined in Table 3-1) [5]			127		LSB
	Gain drift		—	±100	—	ppm/°C
Input	HP amp-to-analog input isolation	R_L = 3 kΩ	—	90	—	dB
		R_L = 30 Ω	—	83	—	dB
	Full-scale signal input voltage [6]		1.5•VA	1.57•VA	1.64•VA	Vpp
	Input impedance [7]		45	50	—	kΩ
	Turn-on time [8]	ADC_SOFTRAMP_EN = 0	—	—	25	ms

1. Parameters in this table are described in detail in Table 3-1.
2. (HSIN dynamic range test configuration (pseudodifferential). Input signal is –60 dB down from the corresponding full-scale voltage.



3. ADC_HPF_EN must remain asserted for proper functionality. Failure to do so may cause clipping of the ADC digital output.
4. HSIN CMRR test configuration



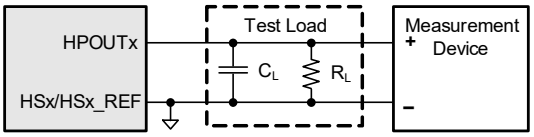
5. SDOUT code with ADC_HPF_EN = 1 (see p. 155), ADC_DIG_BOOST = 0 (see p. 154).
6. ADC full-scale input voltage is measured on between HSIN+ and HSIN–. This is for single-ended or pseudodifferential input signals.
7. Measured between HSIN+ and HSIN–.
8. Turn-on time is measured from the ADC_PDN = 0 ACK signal to when data comes through the DAO port or SoundWire port. In most cases, enabling the SRC increases the turn-on time and may exceed the maximum value specified.

Table 3-13. Serial Data In-to-HPOUTx Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 and Fig. 2-2 show CS42L42 connections; input test signal is a 24-bit full-scale 997-Hz sine wave with 1 LSB of triangular PDF dither applied; GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground; parameters can vary with VA; typical performance data taken with VL = VA = 1.8 V, VP = 3.6 V; min/max performance data taken with VA = 1.66–1.94 V; VL = 1.8 V, VP = 3.6 V; VCP Mode; T_A = +25°C; measurement bandwidth is 20 Hz–20 kHz; ASP_LRCK = Fs_{INT} = 48-kHz mode; MCLK = 12 MHz, MCLK_SRC_SEL = 0; mixer attenuation and digital volume = 0 dB; FULL_SCALE_VOL = 0 (0dB); HP load: R_L = 30 Ω, C_L = 1 nF (HPOUT_LOAD = 0) and R_L = 3 kΩ, C_L = 10 nF (HPOUT_LOAD = 1)SRC bypassed.

Parameter [1]				Minimum	Typical	Maximum	Unit
R_L = 3 kΩ VP_CP Mode	Dynamic range (defined in Table 3-1)	18–24 bit	A-weighted	108	114	—	dB
			unweighted	105	111	—	dB
	THD+N [2] (defined in Table 3-1)	18–24 bit	0 dB	—	–90	–84	dB
			–20 dB	—	–83	—	dB
			–60 dB	—	–51	–48	dB
		16 bit	0 dB	—	–88	–82	dB
			–20 dB	—	–73	—	dB
			–60 dB	—	–33	–27	dB
	Idle channel noise (A-weighted)			—	2.0	—	µV
	Full-scale output voltage [3]			1.50•VA	1.58•VA	1.66•VA	V_{PP}
R_L = 30 Ω VP_CP Mode	Dynamic range (defined in Table 3-1)	18–24 bit	A-weighted	108	114	—	dB
			unweighted	105	111	—	dB
	THD+N [2] (defined in Table 3-1)		Pout = 10 mW	—	–98	—	dB
			Pout = 35 mW	—	–75	–69	dB
	Full-scale output voltage [3]			1.50•VA	1.58•VA	1.66•VA	V_{PP}
	Output power [2]			—	35.0	—	mW
R_L = 15 Ω VCP Mode (FULL_SCALE_VOL = 1 [–6 dB])	Dynamic range (defined in Table 3-1)	18–24 bit	A-weighted	102	108	—	dB
			unweighted	99	105	—	dB
	THD+N [2] (defined in Table 3-1)		Pout = 17.3 mW	—	–75	–69	dB
	Full-scale output voltage [3]			0.71•VA	0.79•VA	0.86•VA	V_{PP}
	Output power [2]			—	17.3	—	mW
R_L = 15 Ω VP_CP Mode	Dynamic range	18–24 bit	A-weighted	102	108	—	dB
			unweighted	99	105	—	dB
Other characteristics (Table 3-1 gives parameter definitions.)	Interchannel isolation [3] (3 kΩ)		217 Hz	—	90	—	dB
			1 kHz	—	90	—	dB
			20 kHz	—	80	—	dB
	Interchannel isolation [3] (30 Ω)		217 Hz	—	90	—	dB
			1 kHz	—	90	—	dB
			20 kHz	—	70	—	dB
	Output offset voltage: mute [3,4] (ANA_MUTE_x = 1, see p. 156)		HPOUTx	—	±0.5	±1.0	mV
	Output offset voltage [3,4]		HPOUTx	—	±0.5	±2.5	mV
	Load resistance (R_L)		Normal operation [3]	15	—	—	Ω
	Load capacitance (C_L) [3,5]		HPOUT_LOAD = 0	—	—	1	nF
			HPOUT_LOAD = 1	—	—	10	nF
	Turn-on time [6]		SLOW_START_EN = 000	—	—	25	ms

1. One LSB of triangular PDF dither is added to data.
2. Because VCP settings lower than VA reduce the HP amplifier headroom, the specified THD+N performance at full-scale output voltage and power may not be achieved.
3. HP output test configuration. Symbolized component values are specified in the test conditions above.



4. Assumes no external impedance on HSx/HSx_REF. External impedance on HSx/HSx_REF affects the offset and step deviation. See Section 4.4.1.
5. Amplifier is guaranteed to be stable with either headphone load setting.
6. Turn-on time is measured from when the HP_PDN = 0 ACK signal is received to when the signal appears on the HP output. In most cases, enabling the SRC increases the turn-on time and may exceed the maximum specified value.

Table 3-14. HSBIAS Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 and Fig. 2-2 show CS42L42 connections; GNDHS = GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground; parameters can vary with VA and VP; typical performance data taken with VL = VA = 1.8 V, VP = 3.6 V; min/max performance data taken with VA = 1.66–1.94 V, VL = 1.8 V, VP = 3.0–5.25; I_{OUT} = 500 µA; T_A = +25°C; PDN_ALL = 0, HSBIAS_CTRL = 2.7-V Mode.

Parameters [1]				Minimum	Typical	Maximum	Unit
Output voltage [2]	PDN_ALL	DETECT_MODE	HSBIAS_CTRL				
	0/1	0x (inactive/short detect only)	10 (2.0-V Mode)	1.40	1.86	2.15	V
	0/1	01 (short detect only)	11 (2.7-V Mode)	1.75	2.30	2.70	V
	0	11 (Normal Mode)	10 (2.0-V Mode) [3]	1.80	2.00	2.10	V
	0	00/11 (inactive/Normal Mode)	11 (2.7-V Mode)	2.61	2.75	2.86	V
DC output current, I_{OUT2} [4]			HSBIAS_CTRL = 10 (2.0-V Mode)	—	0.91	—	mA
			HSBIAS_CTRL = 11 (2.7-V Mode)	—	1.2	—	mA
Integrated output noise (measured at HSx)			f = 100 Hz–20 kHz	—	—	4	µVrms
Output resistance, R_{OUTx}				2.19	2.21	2.23	kΩ
Output resistance temperature variation			–40°C to +85°C		±3		%
Current-sense trip point			HSBIAS_SENSE_TRIP = 000	—	12	—	µA
			HSBIAS_SENSE_TRIP = 001	—	23	—	µA
			HSBIAS_SENSE_TRIP = 010	—	41	—	µA
			HSBIAS_SENSE_TRIP = 011	—	52	—	µA
			HSBIAS_SENSE_TRIP = 100	—	64	—	µA
			HSBIAS_SENSE_TRIP = 101	—	75	—	µA
			HSBIAS_SENSE_TRIP = 110	—	93	—	µA
			HSBIAS_SENSE_TRIP = 111	—	104	—	µA
Capacitive load				—	—	100	µF

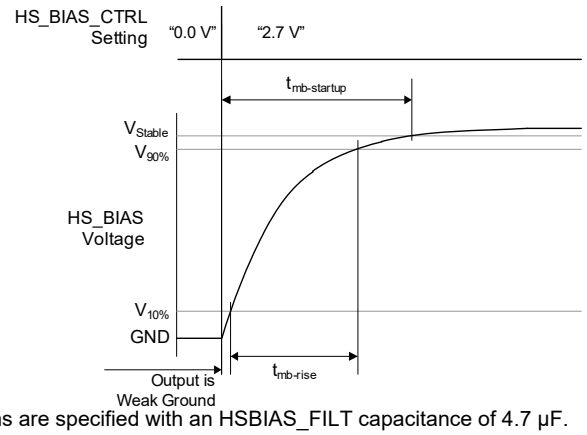
1. If HSBIAS_CTRL = 01, the internal HSBIAS node is to be shorted to ground. Output is pulled down to ground via an internal resistance of R_{OUT} to the HS3/HS4 pins, which is, in turn, connected internally or externally to ground (per Fig. 2-1).
2. The output voltage is the unloaded, open-circuit voltage present at the HSx pin selected as HSBIAS output.
3. No audio is allowed on HSIN/HSx if DETECT_MODE = 11 and HSBIAS_CTRL = 10.
4. Specifies use limits for the normal operation and HSIN short conditions.

Table 3-15. Switching Specifications—HSBIAS

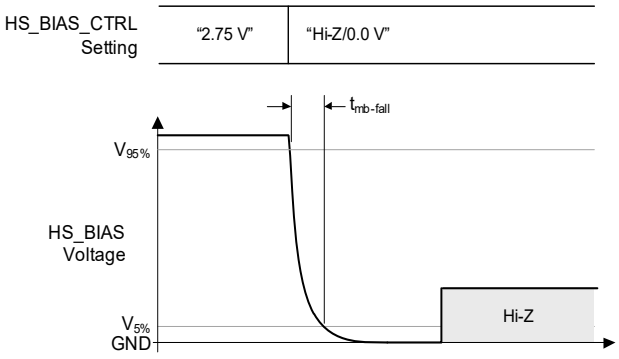
Test conditions (unless specified otherwise): Fig. 2-1 shows CS42L42 connections; GNDA = GNDP = GNDCP = GNDD = 0 V; voltages are with respect to ground; parameters can vary with VA and VP; typical performance data taken with VL = VA = VCP = 1.8 V, VP = 3.6 V; min/max performance data taken with VA = 1.66–1.94 V; VL = VCP = 1.8 V; VP = 3.0–5.25; I_{OUT} = 500 µA (not valid for fall time); T_A = +25°C; PDN_ALL = 0, DETECT_MODE = Normal Mode.

Parameters [1]			Symbol	Minimum	Typical	Maximum	Unit
HS bias rise time [2, 3]		HSBIAS_RAMP = 00	$t_{mb-rise}$	—	0.002	—	ms
		HSBIAS_RAMP = 01		—	10	—	ms
		HSBIAS_RAMP = 10		—	25	—	ms
		HSBIAS_RAMP = 11		—	50	—	ms
HS bias fall time [4]		HSBIAS_RAMP = 00	$t_{mb-fall}$	—	3	—	ms
		HSBIAS_RAMP = 01		—	15	—	ms
		HSBIAS_RAMP = 10		—	37	—	ms
		HSBIAS_RAMP = 11		—	75	—	ms
HS bias transition time [5]	Condition 1 [6]	1.8 V → Hi-Z	$t_{mb-tran}$	—	92	—	µs
		2.0 V → Hi-Z		—	92	—	µs
		2.3 V → Hi-Z		—	93	—	µs
	Condition 2 [7]	2.7 V → 2.3 V	$t_{mb-tran}$	—	23	—	µs
		1.8 V → 2.3 V		—	20	—	µs
		2.0 V → 2.3 V		—	18	—	µs
		2.0 V → 2.7 V		—	1	—	µs
	Condition 3 [8]	Hi-Z → 1.8 V	$t_{mb-tran}$	—	96	—	µs
		Hi-Z → 2.3 V		—	96	—	µs
	Condition 4 [8,9]		$t_{mb-tran}$	—	10	—	ms
	Condition 5 [10]	Hi-Z → 2.7 V, HSBIAS_RAMP = 01	$t_{mb-tran}$	—	183	—	µs
		Hi-Z → 2.3 V, HSBIAS_RAMP = 10		—	198	—	µs
		Hi-Z → 2.3 V, HSBIAS_RAMP = 11		—	220	—	µs
HS bias droop		Condition 2 [7]	$V_{mb-droop}$	—	—	500	mV
HS bias startup-to-stable time [11]		HSBIAS_RAMP = 00	$t_{mb-startup}$	—	0.01	—	ms
		HSBIAS_RAMP = 01		—	14	—	ms
		HSBIAS_RAMP = 10		—	36	—	ms
		HSBIAS_RAMP = 11		—	65	—	ms

1. HSBIAS startup timing example

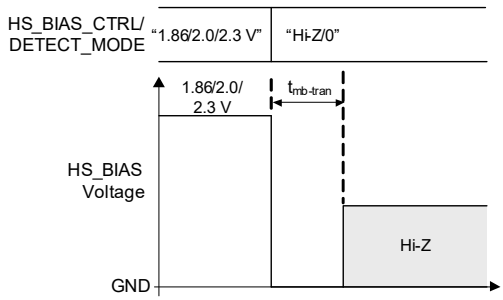


2. HSBIAS rise time is measured from 10% to 90% of the final output voltage. Transitions are specified with an HSBIAS_FILT capacitance of 4.7 µF.
3. Under the specified configuration, the HSBIAS transitions with an exponential rise time.
4. HS bias fall time is the time associated with HSBIAS falling from 95% to 5% of the programmed typical output voltage. If transitioning to Hi-Z, the output does not enter Hi-Z state until the internal digital counter completes, as determined by the HSBIAS_RAMP setting.

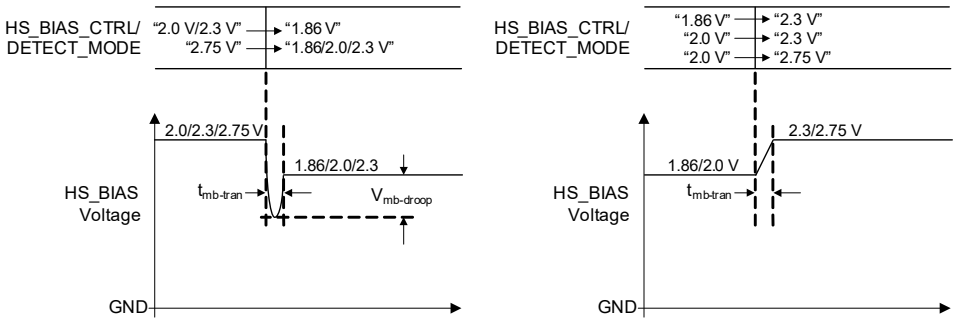


5. HS bias transitions between the GND mode and ON modes occur with no transition state.

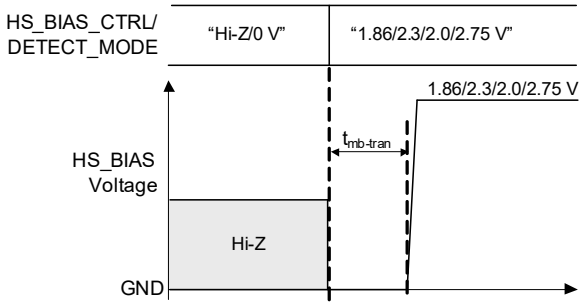
6. Condition 1 transition timing.



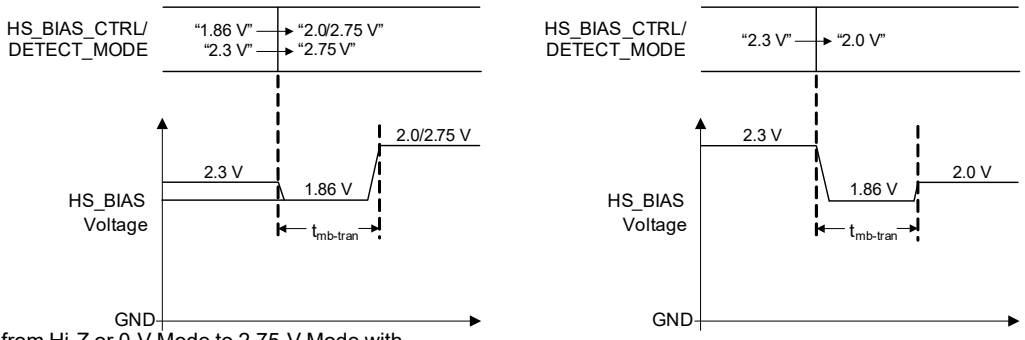
7. Condition 2 transition timing.



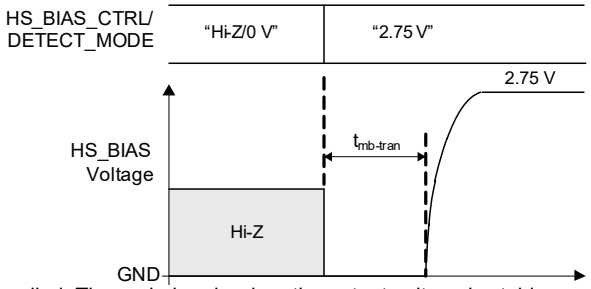
8. Due to isolation between HSBIAS internal node and HSx pins, the following is informational only and cannot be measured externally. Condition 3 applies when transitioning from Hi-Z or 0-V Mode to 1.86- or 2.30-V Mode.
Condition 4 applies when transitioning from Hi-Z or 0-V Mode to 2.0- or 2.75-V Mode with HSBIAS_RAMP = 00.



9. Condition 4 also applies when transitioning from 1.86- or 2.3-V Mode to 2.0- or 2.75-V Mode.



10. Condition 5 applies when transitioning from Hi-Z or 0-V Mode to 2.75-V Mode with HSBIAS_RAMP = 01/10/11.



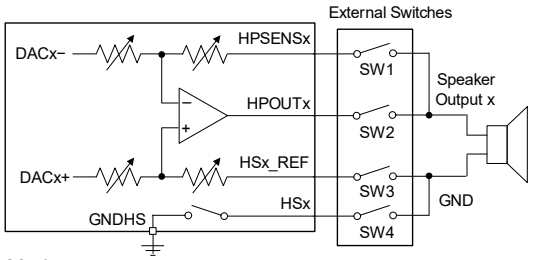
11. Mic bias startup to stable time period begins when the mic bias voltage starts to be applied. The period ends when the output voltage is stable (output voltage is at 95% of its programmed typical value).

Table 3-16. DC Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 and Fig. 2-2 show CS42L42 connections; GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground; VL = VCP = VA = 1.8 V, VP = 3.6 V; T_A = +25°C.

Parameters			Minimum	Typical	Maximum	Unit
VCP_FILT (No load connected to HPOUTx.)	VP_CP Mode (ADPTPWR = 001)	+VCP_FILT	—	2.6	—	V
		–VCP_FILT	—	–2.6	—	V
	VCP Mode (ADPTPWR = 010)	+VCP_FILT	—	VCP	—	V
		–VCP_FILT	—	–VCP	—	V
	VCP/2 Mode (ADPTPWR = 011)	+VCP_FILT	—	VCP/2	—	V
		–VCP_FILT	—	–VCP/2	—	V
	VCP/3 Mode (ADPTPWR = 100)	+VCP_FILT	—	VCP/3	—	V
		–VCP_FILT	—	–VCP/3	—	V
HS3/HS4 ground switch resistance (Typical values have ±25% tolerance.)			—	0.5	—	Ω
HS_CLAMPx depletion FET ground switch resistance			—	1	—	Ω
Closed-loop external switch configuration	External switch allowable ON-resistance (R_{ON}) [1]		—	—	1	Ω
	External switch ON-resistance flatness over common-mode voltage appearing at switch [1]	SW1, SW2 R_{ON} flatness	—	—	0.075	Ω
		SW3, SW4 R_{ON} flatness	—	—	0.02	Ω
	External switch + PCB stray capacitance (C_{ON} + C_{OFF} + PCB_{STRAY} – C) [1]		—	100	—	pF
Other DC filter	FILT+ voltage		—	VA	—	V
	HP output current limiter on threshold. See Section 4.6.4. [2]		80	115	160	mA
	VD_FILT and VL power-on reset threshold (V_{POR})	Up	—	0.777	—	V
		Down	—	0.628	—	V
HPOUT pull-down resistance [3,4]		HPOUT_PULLDOWN = 0000–0111, 1100	—	0.9	—	kΩ
		HPOUT_PULLDOWN = 1001	—	9.3	—	kΩ
		HPOUT_PULLDOWN = 1010	—	5.8	—	kΩ
Headset-Detect Comparator 1 level (Step size = 0.05 V)		HSDET_COMP1_LVL = 0000	—	0.65	—	V
		HSDET_COMP1_LVL = 0111	—	1.0	—	V
		HSDET_COMP1_LVL = 1111	—	1.4	—	V
Headset-Detect Comparator 2 level (Step size = 0.05 V)		HSDET_COMP2_LVL = 0000	—	1.65	—	V
		HSDET_COMP2_LVL = 0111	—	2.0	—	V
		HSDET_COMP2_LVL = 1111	—	2.4	—	V

1. External switches. See Section 4.4.2 for additional details.



2. The HP output current limiter threshold spec is valid only while the Class H rails are in VCP Mode.
3. Typical values have ±20% tolerance.
4. Clamp is disabled (HPOUT_CLAMP = 1) and channel is powered down (HPOUT_PDN = 1).

Table 3-17. Power-Supply Rejection Ratio (PSRR) Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 and Fig. 2-2 show CS42L42 connections; input test signal held low (all zero data); GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground; VL = VA = 1.8 V, VP = 3.6 V; T_A = +25°C.

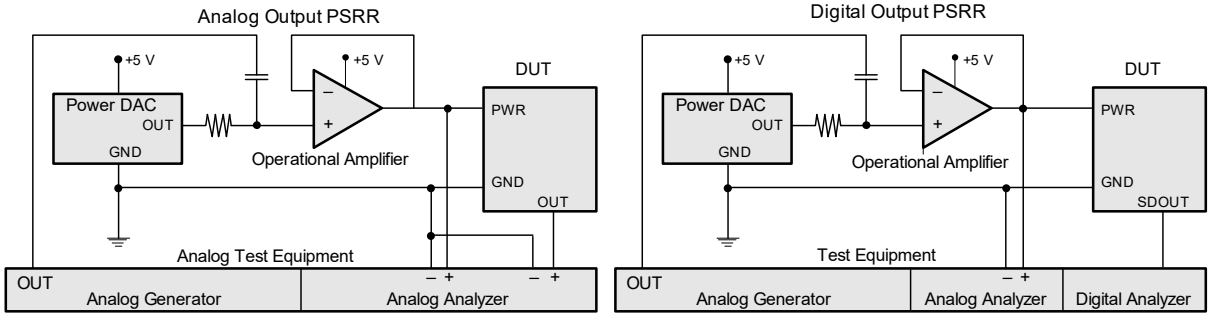
Parameters [1]		Minimum	Typical	Maximum	Unit
HSIN PSRR with 100-mVpp signal AC-coupled to VP supply	217 Hz	—	88	—	dB
	1 kHz	—	83	—	dB
	20 kHz	—	73	—	dB
HSIN PSRR with 100-mVpp signal AC-coupled to VA supply	217 Hz	—	70	—	dB
	1 kHz	—	70	—	dB
	20 kHz	—	55	—	dB
HPOUTx (–6-dB analog gain) PSRR with 100-mVpp signal AC coupled to VA supply [2]	217 Hz	—	75	—	dB
	1 kHz	—	75	—	dB
	20 kHz	—	70	—	dB
HPOUTx (–6-dB analog gain) PSRR with 100-mVpp signal AC-coupled to VCP supply [2]	217 Hz	—	85	—	dB
	1 kHz	—	85	—	dB
	20 kHz	—	65	—	dB
HPOUTx (0-dB analog gain) PSRR with 100-mVpp signal AC coupled to VP supply	217 Hz	—	80	—	dB
	1 kHz	—	80	—	dB
	20 kHz	—	60	—	dB

Table 3-17. Power-Supply Rejection Ratio (PSRR) Characteristics *(Cont.)*

Test conditions (unless specified otherwise): Fig. 2-1 and Fig. 2-2 show CS42L42 connections; input test signal held low (all zero data); GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground; VL = VA = 1.8 V, VP = 3.6 V; T_A = +25°C.

Parameters [1]		Minimum	Typical	Maximum	Unit
HSBIAS (HSBIAS = 2.7-V mode, I_{OUT} = 500 µA) PSRR with 100-mVpp signal AC coupled to VA supply [3,4]	217 Hz	—	105	—	dB
	1 kHz	—	100	—	dB
	20 kHz	—	83	—	dB
HSBIAS (HSBIAS = 2.7-V mode, I_{OUT} = 500 µA) PSRR with 1-Vpp signal AC coupled to VP supply [4]	217 Hz	—	108	—	dB
	1 kHz	—	95	—	dB
	20 kHz	—	70	—	dB
HSBIAS (Normal Mode, HSBIAS = 2.0-V mode, I_{OUT} = 500 µA) PSRR with 100-mVpp signal AC coupled to VA supply [3,4]	217 Hz	—	75	—	dB
	1 kHz	—	70	—	dB
	20 kHz	—	55	—	dB
HSBIAS (Normal Mode, HSBIAS = 2.0-V mode, I_{OUT} = 500 µA) PSRR with 100-mVpp signal AC coupled to VP supply [4]	217 Hz	—	75	—	dB
	1 kHz	—	70	—	dB
	20 kHz	—	55	—	dB

1. PSRR test configuration: Typical PSRR can vary by approximately 6 dB below the indicated values.



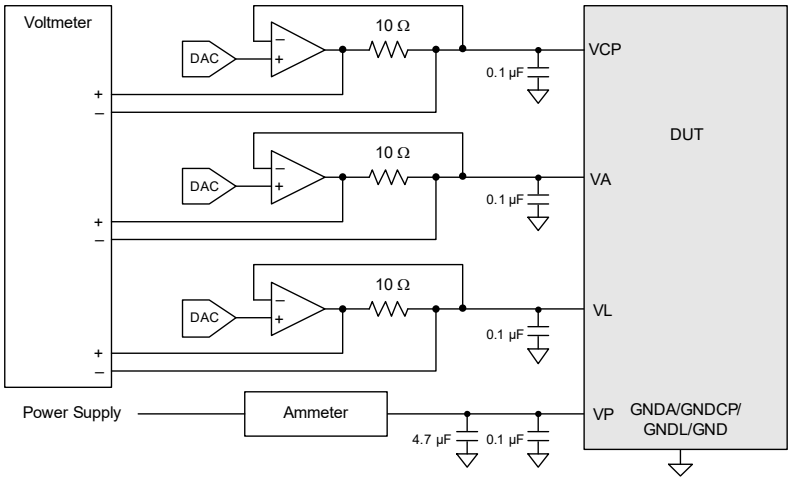
2. No load connected to any analog outputs.
3. The accurate reference, which sets the HSBIAS output voltage, is powered from VA.
4. If HS_CLAMP1/2 are connected to HS3/4, PSRR is reduced by 6 dB.

Table 3-18. Power Consumption

Test conditions (unless specified otherwise): Fig. 2-1 shows CS42L42 connections; GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground; performance data taken with VA = VCP = VL = 1.8 V; DIGLDO_PDN is deasserted; VP = 3.6 V; T_A = +25°C; ASP_LRCK = 48-kHz Mode; Fs_{INT} = 48 kHz; SCLK = 12 MHz, MCLK_SRC_SEL = 0;mixer attenuation = 0 dB; FULL_SCALE_VOL = 1 (–6 dB) for HPOUTx, TIP_SENSE_CTRL = 11, all other fields are set to defaults; no signal on any input; control port inactive; input clock/data are held low when not required; test load is R_L = 30 Ω and C_L = 1 nF for HPOUTx; measured values include currents consumed by the codec and do not include current delivered to external loads unless specified otherwise (e.g., HPOUTx); see Fig. 3-1.

Use Cases			Class H Mode	Typical Current (µA)				Total Power (µW)
				i_{VA}	i_{VCP}	i_{VL}	i_{VP}	
1	A	Off [1]	—	0	0	0	3.1	11.16
2	A	Standby [2,3] Depletion FETs on	—	0	0	0	20	72.0
	B	S0 Detect and tip sense active, Depletion FETs off	—	0	0	0	28	100.8
3	A	Standby (RCO Mode) [4,5] Depletion FETs on	—	0	0	343	31	729
	B	S0 Detect and tip sense active, Depletion FETs off	—	0	0	343	37	751
4	A	Record	—	1483	0	663	58	4072
5	A	Playback Stereo HPOUT (no signal, HPOUT_LOAD = 0)	VCP/3	1413	1204	858	58	6464
	B	Stereo HPOUT (0.1 mW, HPOUT_LOAD = 0)	VCP/3	1441	2336	965	58	8744
6	A	S/PDIF Tx (SCLK = 12.288 MHz, 48-kHz data rate, 24-bit, no S/PDIF transmitter load) [6]	—	0	0	418	26	846
7	A	Voice call Headset (HSIN, HSBIAS_CTRL = 10)	—	3032	1200	1569	270	11414
	B	Voice call (SoundWire) Headset (HSIN, HSBIAS_CTRL = 10)	—	3032	1200	1815	270	11857

1. Off configuration: Clock/data lines held low; RESET = LOW; VA = VL = VCP = 0 V; VP = 3.6 V.
2. Standby configuration: Clock/data lines held low; VA = VL = VCP = 0 V; VP = 3.6 V; M_MIC_WAKE = 0, M_HP_WAKE = 0 (unmasked).
3. SCLK_PRESENT = 1.
4. SCLK_PRESENT = 0 (RCO clocking).
5. Standby configuration (RCO clocking): Clock/data lines held low; VA = 0 V; VL = 1.8 V, VCP = 0 V, VP = 3.6 V; M_MIC_WAKE = 0, M_HP_WAKE = 0 (unmasked).
6. SCLK = 12.288 MHz, PLL off, SPDIF_CLK_DIV = 001 (divide factor = 2); data lines held low.



Note: The current draw on the VA, VCP, and VL power supply pins is derived from the measured voltage drop across a 10-Ω series resistor between the associated supply source and each voltage supply pin. Given the larger currents that are possible on the VP supply, an ammeter is used for the measurement.

Figure 3-1. Power Consumption Test Configuration

Table 3-19. Register Field Settings

Use Cases		Register Fields and Settings																Class H Mode p. 42
		PDN_ALL	ASP_DAO_PDN	ASP_DAI_PDN	ASP_DAI1_PDN	ADC_PDN	MIXER_PDN	EQ_PDN	HP_PDN	SPDIF_TX_PDN	PLL_START	RING_SENSE_PDNB	DETECT_MODE [1]	TIP_SENSE_CTRL [1]	HSBIAS_CTRL [1]	HS_CLAMP_DISABLE		
1	A	—	—	—	—	—	—	—	—	—	—	—	00	00	01	—		—
2	A	1	—	—	—	—	—	—	—	1	0	—	01	01	10	0		—
	B	1	—	—	—	—	—	—	—	1	0	—	01	01	10	1		—
3	A	1	—	—	—	—	—	—	—	1	0	—	01	01	10	0		—
	B	1	—	—	—	—	—	—	—	1	0	—	01	01	10	1		—
4	A	0	0	1	1	0	1	1	1	1	0	0	00	00	00	0		—
5	A	0	1	0	1	1	0	1	0	1	0	0	01	00	10	1		VCP/3
	B	0	1	0	1	1	0	1	0	1	0	0	01	00	10	1		VCP/3
6	A	0	1	0	1	1	1	1	1	0	0	0	00	00	00	1		—
7	A	Individual power downs. See definitions in Table 3-18.																—

1.LATCH_TO_VP must be set for the following settings to take effect: TIP_SENSE_CTRL, DETECT_MODE, HS_CLAMP_DISABLE, HSBIAS_CTRL.

Table 3-20. S0 Button Detect Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows CS42L42 connections; GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground; parameters can vary with VA and VP; typical performance data taken with VL = VA = 1.8 V, VP = 3.6 V; min/max performance data taken with VA = 1.66–1.94 V, VL = 1.8 V, VP = 3.0–5.25 V; T_A = +25°C.

Parameters		Minimum	Typical	Maximum	Unit
HS DC-detection parameters	Short-detect threshold (S0 button)	100	150	200	mV
	Total group delay	—	5	—	ms
	HS DC detect threshold [1]	—	(M+1) x 1.5625	—	%
	DC level detect power-up time [2]	—	11	—	ms

1.The variable M refers to the decimal representation of the HS_DETECT_LEVEL setting (see p. 152).
2.Time for the DC level detector circuits to completely power up after PDN_MIC_LVL_DETECT transitions from 1 to 0 (see p. 151).

Table 3-21. Switching Specifications—SoundWire Port

Test conditions (unless specified otherwise): GND = 0 V; SWIRE_SEL pin = VL; voltages are with respect to ground; VD_FILT = 1.2 V; VA = 1.8 V; VP = 3.6 V; TA = +25°C; logic 0 = ground, logic 1 = VL; input timings are measured at V_{IL} and V_{IH} thresholds; output timings are measured at V_{OL} and V_{OH} thresholds for VL logic (as shown in Table 3-25).

Parameter			Symbol	Minimum	Maximum	Unit
VL = 1.2	SWIRE_CLK frequency	Small data bus (10- to 60-pF capacitance)	F_{SWSCLK}	—	12.3	MHz
		Large data bus (10- to 100-pF capacitance)		—	11.0	MHz
	Input clock slew time	Small data bus	—	2.0	5.0	ns
		Large data bus	—	2.0	6.0	ns
	Data output slew time [1]		T_{SLEW}	2.0	—	ns
	Data driver disable time [2]		T_{DZ}	—	5.0	ns
	Delay from clock to active state		T_{ZD}	8.1	—	ns
	Time for data output valid	Small data bus (10- to 60-pF capacitance)	T_{OV_DATA}	—	27.9	ns
		Large data bus (10- to 100-pF capacitance)		—	29.0	ns
	Data output hold time		T_{OH_DATA}	6.7	—	ns
	Data input minimum setup time [2]		$T_{ISETUP\_MIN\_DATA}$	—	0.0	ns
	Data input minimum hold time		$T_{IHOLD\_MIN\_DATA}$	—	4.0	ns
	Clock input duty cycle		—	45	55	%
	VL logic (SWIRE_CLK and SWIRE_SD pins)	High-level output voltage	V_{OH}	0.8*VL	—	V
		Low-level output voltage	V_{OL}	—	0.2*VL	V
		High-level input voltage	V_{IH}	0.65*VL	—	V
		Low-level input voltage	V_{IL}	—	0.35*VL	V
		Input voltage threshold (rising edge)	V_{TP}	0.5*VL	0.65*VL	V
		Input voltage threshold (falling edge)	V_{TN}	0.35*VL	0.5*VL	V
		Hysteresis voltage	V_{HYST}	0.1*VL	—	V