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CS42L51

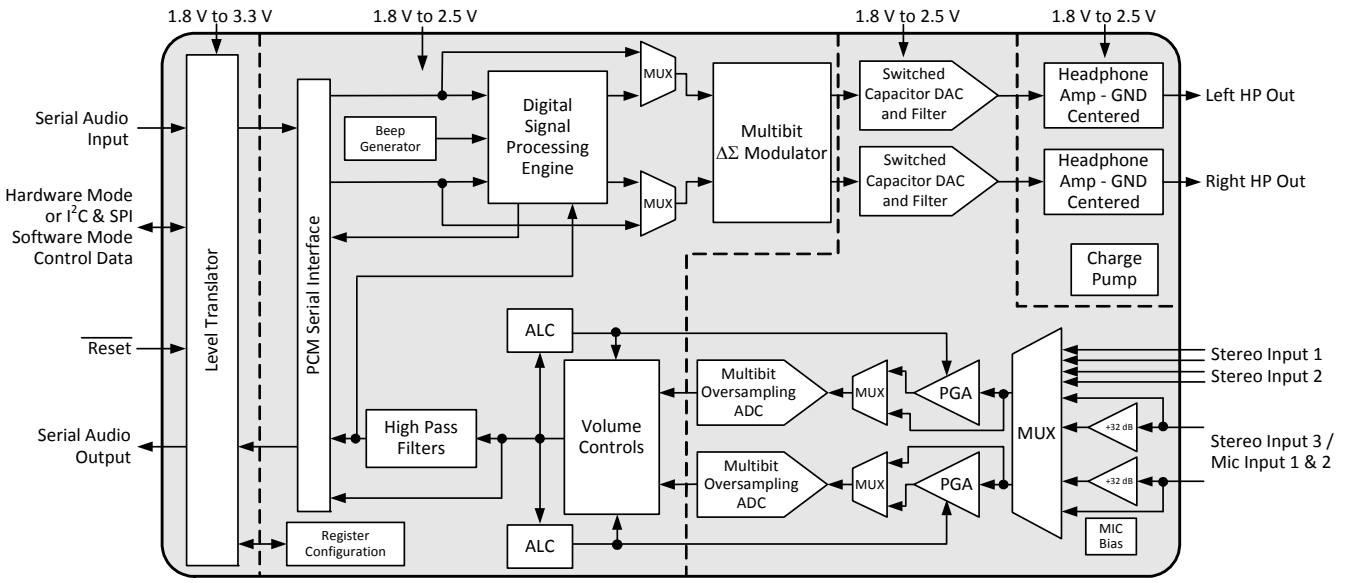
Low-Power, Stereo Codec with Headphone Amp

DIGITAL-TO-ANALOG FEATURES

- 98-dB dynamic range (A-weighted)
- -86-dB THD+N
- Headphone amplifier - GND centered
  - On-chip charge pump provides –VA_HP
  - No DC-blocking capacitor required
  - 46-mW power into stereo 16 Ω @ 1.8 V
  - 88-mW power into stereo 16 Ω @ 2.5 V
  - -75 dB THD+N
- Digital signal processing engine
  - Bass & treble tone control, de-emphasis
  - PCM + ADC mix with independent volume control
  - Master digital volume control
  - Soft ramp & zero-cross transitions
- Beep generator
  - Tone selections across two octaves
  - Separate volume control
  - Programmable on & off time intervals
  - Continuous, periodic or one-shot beep selections
- Programmable peak-detect and limiter
- Pop and click suppression

ANALOG-TO-DIGITAL FEATURES

- 98-dB dynamic range (A-weighted)
- -88-dB THD+N
- Analog gain controls
  - +32-dB or +16-dB mic preamplifiers
  - Analog programmable gain amplifier (PGA)
- +20-dB digital boost
- Programmable automatic level control (ALC)
  - Noise gate for noise suppression
  - Programmable threshold and attack/release rates
- Independent channel control
- Digital volume control
- High-pass filter disable for DC measurements
- Stereo 3:1 analog input MUX
- Dual mic inputs
  - Programmable, low noise mic bias levels
  - Differential mic mix for common mode noise rejection
- Very low 64 Fs oversampling clock reduces power consumption



SYSTEM FEATURES

- 24-bit converters
- 4–96-kHz sample rate
- Multibit delta–sigma architecture
- Low power operation
  - Stereo playback: 12.93 mW @ 1.8 V
  - Stereo record and playback: 20.18 mW @ 1.8 V
- Variable power supplies
  - 1.8–2.5 V digital & analog
  - 1.8–3.3 V interface logic
- Power down management
  - ADC, DAC, codec, mic preamplifier, PGA
- Software Mode (I²C™ and SPI™ control)
- Hardware mode (stand-alone control)
- Digital routing/mixes:
  - Analog out = ADC + Digital In
  - Digital out = ADC + Digital In
  - Internal digital loopback
  - Mono mixes
- Flexible clocking options
  - Master or slave operation
  - High-impedance digital output option (for easy MUXing between the codec and other data sources)
  - Quarter-speed mode (i.e., Allows 8 kHz Fs while maintaining a flat noise floor up to 16 kHz)

APPLICATIONS

- HDD and flash-based portable audio players
- MD players/recorders
- PDAs
- Personal media players
- Portable game consoles
- Digital voice recorders
- Digital camcorders
- Digital cameras
- Smart phones

GENERAL DESCRIPTION

The CS42L51 is a highly integrated, 24-bit, 96-kHz, low power stereo codec. Based on multi-bit, delta-sigma modulation, it allows infinite sample rate adjustment between 4 kHz and 96 kHz. Both the ADC and DAC offer many features suitable for low power, portable system applications.

The ADC input path allows independent channel control of a number of features. An input multiplexer selects between line-level or microphone level inputs for each channel. The microphone input path includes a selectable programmable-gain pre-amplifier stage and a low noise MIC bias voltage supply. A PGA is available for line or microphone inputs and provides analog gain with soft ramp and zero-cross transitions. The ADC also features a digital volume attenuator with soft ramp transitions. A programmable ALC and Noise Gate monitor the input signals and adjust the volume levels appropriately.

The DAC output path includes a digital signal processing engine. Tone Control provides bass and treble adjustment of four selectable corner frequencies. The Mixer allows independent volume control for both the ADC mix and the PCM mix, as well as a master digital volume control for the analog output. All volume level changes may be configured to occur on soft ramp and zero-cross transitions. The DAC also includes de-emphasis, limiting functions and a beep generator delivering tones selectable across a range of two full octaves.

The stereo headphone amplifier is powered from a separate positive supply and the integrated charge pump provides a negative supply. This allows a ground-centered analog output with a wide signal swing and eliminates external DC-blocking capacitors.

In addition to its many features, the CS42L51 operates from a low-voltage analog and digital core, making this codec ideal for portable systems that require extremely low power consumption in a minimal amount of space.

The CS42L51 is available in a 32-pin QFN package in both Commercial (-10 to +70° C) and Automotive grades (-40 to +85° C). The CDB42L51 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please see "Ordering Information" on page 83 for complete details.

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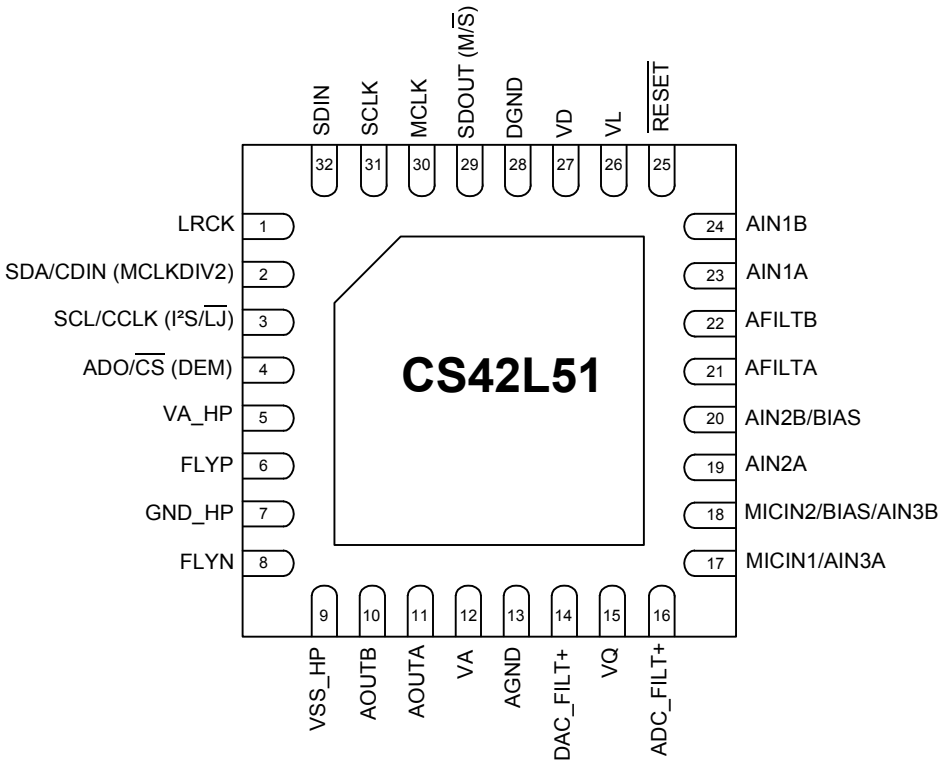
1. PIN DESCRIPTIONS - SOFTWARE (HARDWARE) MODE



Pin Name	#	Pin Description
LRCK	1	**Left Right Clock** (*Input/Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
SDA/CDIN (MCLKDIV2)	2	**Serial Control Data** (*Input*/*Output*) - SDA is a data I/O in I²C Mode. CDIN is the input data line for the control port interface in SPI Mode.
		MCLK Divide by 2 (*Input*) - Hardware Mode: Divides the MCLK by 2 prior to all internal circuitry.
SCL/CCLK (I²S/LJ)	3	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port.
		Interface Format Selection (*Input*) - Hardware Mode: Selects between I²S & Left-Justified interface formats for the ADC & DAC.
AD0/CS (DEM)	4	**Address Bit 0 (I²C) / Control Port Chip Select (SPI)** (*Input*) - AD0 is a chip address pin in I²C Mode; CS is the chip-select signal for SPI format.
		De-Emphasis *(Input)* - Hardware Mode: Enables/disables the de-emphasis filter.
VA_HP	5	**Analog Power For Headphone** *(Input)* **-** Positive power for the internal analog headphone section.
FLYP	6	**Charge Pump Cap Positive Node** *(Input)* **-** Positive node for the external charge pump capacitor.
GND_HP	7	**Analog Ground** (*Input*) - Ground reference for the internal headphone/charge pump section.
FLYN	8	**Charge Pump Cap Negative Node** *(Input)* **-** Negative node for the external charge pump capacitor.
VSS_HP	9	**Negative Voltage From Charge Pump** *(Output)* **-** Negative voltage rail for the internal analog headphone section.

AOUTB AOUTA	10 11	**Analog Audio Output** (*Output*) - The full-scale output level is specified in the DAC Analog Characteristics specification table
VA	12	**Analog Power** (*Input*) - Positive power for the internal analog section.
AGND	13	**Analog Ground** (*Input*) - Ground reference for the internal analog section.
DAC_FILT+	14	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.
VQ	15	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage.
ADC_FILT+	16	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.
MICIN1/ AIN3A	17	**Microphone Input 1** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table.
MICIN2/ BIAS/AIN3B	18	**Microphone Input 2** (*Input/Output*) - The full-scale level is specified in the ADC Analog Characteristics specification table. This pin can also be configured as an output to provide a low noise bias supply for an external microphone. Electrical characteristics are specified in the DC Electrical Characteristics table.
AIN2A	19	**Analog Input** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table.
AIN2B/BIAS	20	**Analog Input** (*Input/Output*) - The full-scale level is specified in the ADC Analog Characteristics specification table. This pin can also be configured as an output to provide a low noise bias supply for an external microphone. Electrical characteristics are specified in the DC Electrical Characteristics table.
AFILTA AFILTB	21 22	**Filter Connection** (*Output*) - Filter connection for the ADC inputs.
AIN1A AIN1B	23 24	**Analog Input** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table.
$\overline{\text{RESET}}$	25	**Reset** (*Input*) - The device enters a low power mode when this pin is driven low.
VL	26	**Digital Interface Power** (*Input*) - Determines the required signal level for the serial audio interface and host control port. Refer to the Recommended Operating Conditions for appropriate voltages.
VD	27	**Digital Power** (*Input*) - Positive power for the internal digital section.
DGND	28	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
SDOUT (M/$\overline{\text{S}}$)	29	**Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data. **Serial Port Master/Slave** (*Input/Output*) - Hardware Mode Startup Option: Selects between Master and Slave Mode for the serial port.
MCLK	30	**Master Clock** (*Input*) - Clock source for the delta-sigma modulators.
SCLK	31	**Serial Clock** *(Input/Output*) - Serial clock for the serial audio interface.
SDIN	32	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
Thermal Pad	-	Thermal relief pad for optimized heat dissipation. See "QFN Thermal Pad" on page 79.

1.1 Digital I/O Pin Characteristics

The logic level for each input should not exceed the maximum ratings for the VL power supply.

Pin Name SW/(HW)	I/O	Driver	Receiver
$\overline{\text{RESET}}$	Input	-	1.8 V - 3.3 V
SCL/CCLK ($I^2S/\overline{LJ}$)	Input	-	1.8 V - 3.3 V, with Hysteresis
SDA/CDIN (MCLKDIV2)	Input/Output	1.8 V - 3.3 V, CMOS/Open Drain	1.8 V - 3.3 V, with Hysteresis
AD0/$\overline{\text{CS}}$ (DEM)	Input	-	1.8 V - 3.3 V
MCLK	Input	-	1.8 V - 3.3 V
LRCK	Input/Output	1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V
SCLK	Input/Output	1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V
SDOUT ($M/\overline{S}$)	Input/Output	1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V
SDIN	Input	-	1.8 V - 3.3 V

Table 1. I/O Power Rails

2. TYPICAL CONNECTION DIAGRAMS

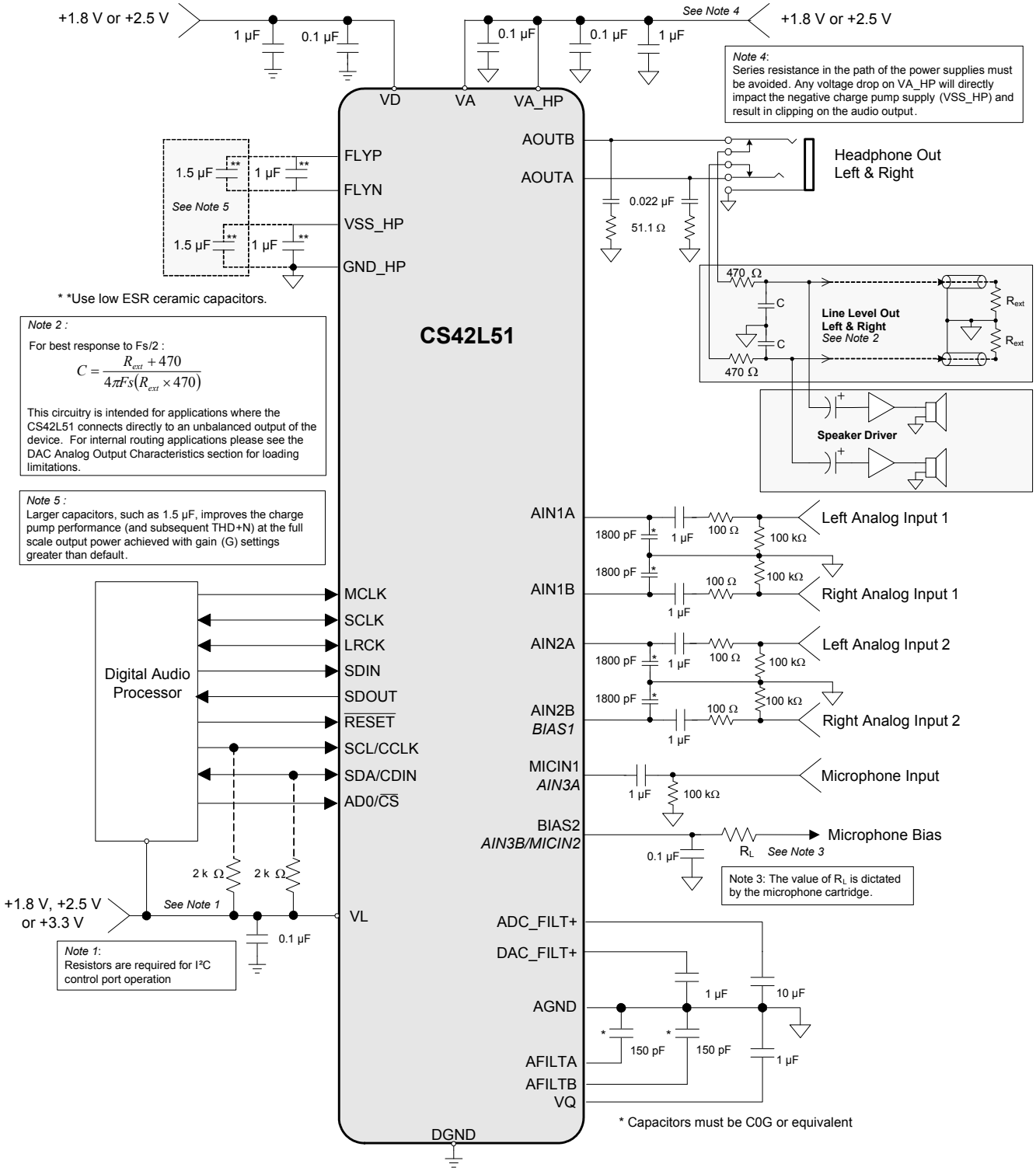


Figure 1. Typical Connection Diagram (Software Mode)

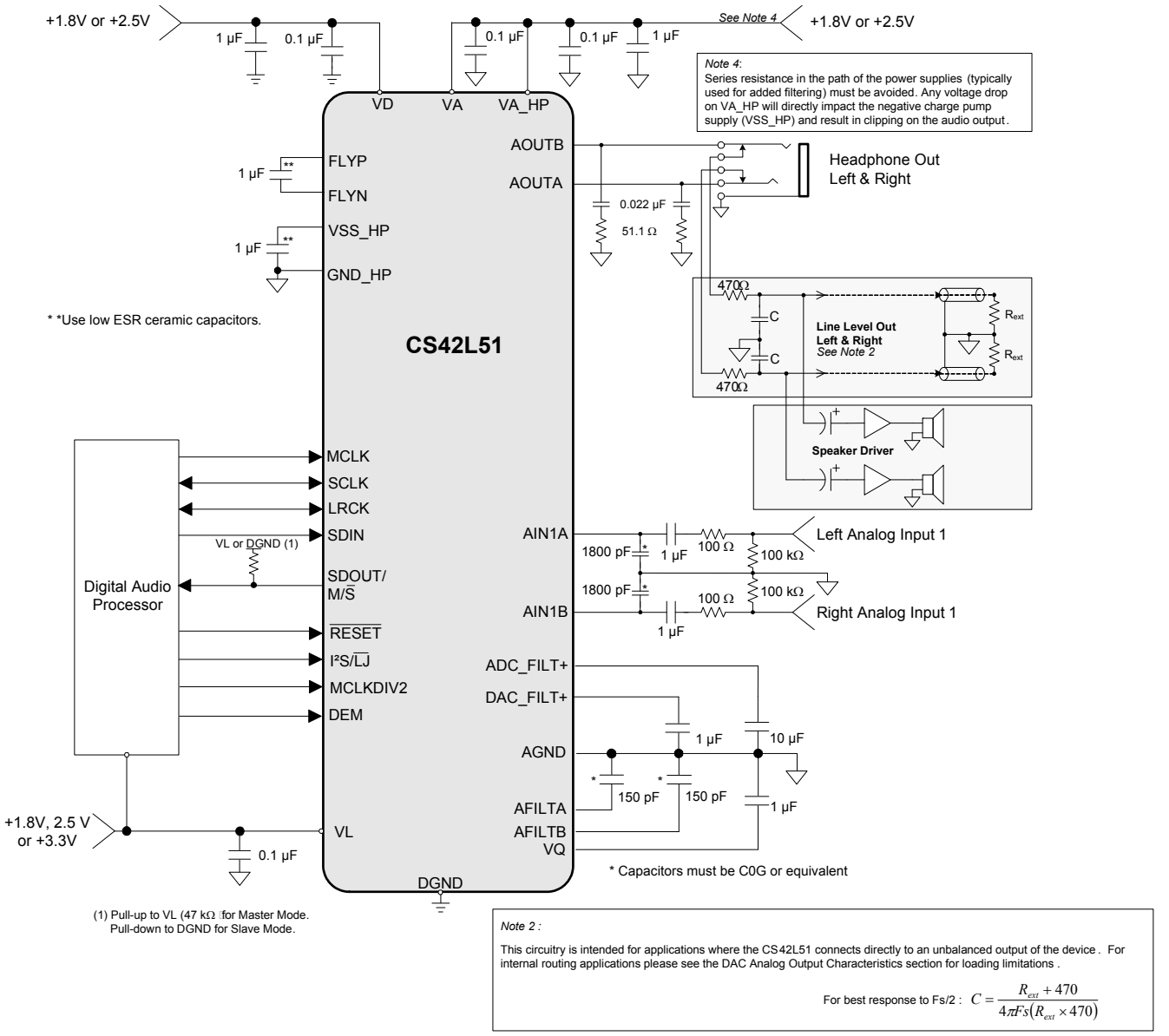


Figure 2. Typical Connection Diagram (Hardware Mode)

3. CHARACTERISTIC AND SPECIFICATION TABLES

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25° C.)

SPECIFIED OPERATING CONDITIONS

(AGND=DGND=0 V, all voltages with respect to ground.)

Parameters		Symbol	Min	Max	Units
DC Power Supply (Note 1)					
Analog Core		VA	1.65	2.63	V
Headphone Amplifier		VA_HP	1.65	2.63	V
Digital Core		VD	1.65	2.63	V
Serial/Control Port Interface		VL	1.65	3.47	V
Ambient Temperature	Commercial - CNZ Automotive - DNZ	T_A	-10 -40	+70 +85	°C °C

Note:

1. The device will operate properly over the full range of the analog, headphone amplifier, digital core and serial/control port interface supplies.

ABSOLUTE MAXIMUM RATINGS

(AGND = DGND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Max	Units
DC Power Supply	Analog Digital Serial/Control Port Interface	VA, VA_HP VD VL	-0.3 -0.3 -0.3	3.0 3.0 4.0	V V V
Input Current	(Note 2)	I_{in}	-	±10	mA
External Voltage Applied to Analog Input	(Note 3)	V_{IN}	AGND-0.3	VA+0.3	V
External Voltage Applied to Analog Output		V_{IN}	-VA_HP - 0.3	+VA_HP + 0.3	V
External Voltage Applied to Digital Input	(Note 3)	V_{IND}	-0.3	VL+ 0.3	V
Ambient Operating Temperature (power applied)		T_A	-50	+115	°C
Storage Temperature		T_{stg}	-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:

2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.
3. The maximum over/under voltage is limited by the input current.

ANALOG INPUT CHARACTERISTICS (COMMERCIAL - CNZ)

(Test Conditions (unless otherwise specified): Input sine wave (relative to digital full scale): 1 kHz through passive input filter; Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. Sample Frequency = 48 kHz)

Parameter (Note 4)		VA = 2.5 V (nominal) Min	Typ	Max	VA = 1.8 V (nominal) Min	Typ	Max	Unit
Analog In to ADC (PGA bypassed)								
Dynamic Range	A-weighted	93	99	-	90	96	-	dB
	unweighted	90	96	-	87	93	-	dB
Total Harmonic Distortion + Noise	-1 dBFS	-	-86	-80	-	-84	-78	dB
	-20 dBFS	-	-76	-	-	-73	-	dB
	-60 dBFS	-	-36	-	-	-33	-	dB
Analog In to PGA to ADC								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	92	98	-	89	95	-	dB
	unweighted	89	95	-	86	92	-	dB
PGA Setting: +12 dB	A-weighted	85	91	-	82	88	-	dB
	unweighted	82	88	-	79	85	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-1 dBFS	-	-88	-81	-	-86	-80	dB
	-60 dBFS	-	-35	-	-	-32	-	dB
PGA Setting: +12 dB	-1 dBFS	-	-85	-79	-	-83	-77	dB
Analog In to MIC Pre-Amp (+16 dB) to PGA to ADC								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	-	86	-	-	83	-	dB
	unweighted	-	83	-	-	80	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-1 dBFS	-	-76	-	-	-74	-	dB
Analog In to MIC Pre-Amp (+32 dB) to PGA to ADC								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	-	78	-	-	75	-	dB
	unweighted	-	74	-	-	71	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-1 dBFS	-	-74	-	-	-71	-	dB
Other Characteristics								
DC Accuracy								
Interchannel Gain Mismatch		-	0.2	-	-	0.2	-	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Offset Error	SDOUT Code with HPF On	-	352	-	-	352	-	LSB
Input								
Interchannel Isolation		-	90	-	-	90	-	dB
DAC Isolation (Note 5)		-	70	-	-	70	-	dB
Full-scale Input Voltage	ADC	0.74•VA	0.78•VA	0.82•VA	0.74•VA	0.78•VA	0.82•VA	Vpp
	PGA (0 dB)	0.75•VA	0.794•VA	0.83•VA	0.75•VA	0.794•VA	0.83•VA	Vpp
	MIC (+16 dB)		0.129•VA			0.129•VA		Vpp
	MIC (+32 dB)		0.022•VA			0.022•VA		Vpp
Input Impedance (Note 6)	ADC	-	20	-	-	20	-	kΩ
	PGA	-	39	-	-	39	-	kΩ
	MIC	-	50	-	-	50	-	kΩ

Notes:

4. Referred to the typical full-scale voltage. Applies to all THD+N and Dynamic Range values in the table.
5. Measured with DAC delivering full-scale output power into 16 Ω.
6. Measured between AINxx and AGND.

ANALOG INPUT CHARACTERISTICS (AUTOMOTIVE - DNZ)

(Test Conditions (unless otherwise specified): Input sine wave (relative to full scale): 1 kHz through passive input filter; Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. Sample Frequency = 48 kHz)

Parameter (Note 4)		VA = 2.5 V (nominal) Min	Typ	Max	VA = 1.8 V (nominal) Min	Typ	Max	Unit
Analog In to ADC								
Dynamic Range	A-weighted	91	99	-	88	96	-	dB
	unweighted	78	96	-	85	93	-	dB
Total Harmonic Distortion + Noise	-1 dBFS	-	-86	-78	-	-84	-76	dB
	-20 dBFS	-	-76	-	-	-73	-	dB
	-60 dBFS	-	-36	-	-	-33	-	dB
Analog In to PGA to ADC								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	90	98	-	87	95	-	dB
	unweighted	87	95	-	84	92	-	dB
PGA Setting: +12 dB	A-weighted	83	91	-	80	88	-	dB
	unweighted	80	88	-	77	85	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-1 dBFS	-	-88	-80	-	-86	-78	dB
	-60 dBFS	-	-35	-	-	-32	-	dB
PGA Setting: +12 dB	-1 dBFS	-	-85	-77	-	-83	-75	dB
Analog In to MIC Pre-Amp (+16 dB) to PGA to ADC								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	-	86	-	-	83	-	dB
	unweighted	-	83	-	-	80	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-1 dBFS	-	-76	-	-	-74	-	dB
Analog In to MIC Pre-Amp (+32 dB) to PGA to ADC								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	-	78	-	-	75	-	dB
	unweighted	-	74	-	-	71	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-1 dBFS	-	-74	-	-	-71	-	dB
Other Characteristics								
DC Accuracy								
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Offset Error	SDOUT Code with HPF On	-	352	-	-	352	-	LSB
Input								
Interchannel Isolation		-	90	-	-	90	-	dB
DAC Isolation (Note 5)		-	70	-	-	70	-	dB

Parameter (Note 4)		VA = 2.5 V (nominal) Min	Typ	Max	VA = 1.8 V (nominal) Min	Typ	Max	Unit
Full-scale Input Voltage	ADC	0.74•VA	0.78•VA	0.82•VA	0.74•VA	0.78•VA	0.82•VA	Vpp
	PGA (0 dB)	0.75•VA	0.794•VA	0.83•VA	0.75•VA	0.794•VA	0.83•VA	Vpp
	MIC (+16 dB)		0.129•VA			0.129•VA		Vpp
	MIC (+32 dB)		0.022•VA			0.022•VA		Vpp
Input Impedance (Note 6)	ADC	18	-	-	18	-	-	kΩ
	PGA	40	-	-	40	-	-	kΩ
	MIC	50	-	-	50	-	-	kΩ

ADC DIGITAL FILTER CHARACTERISTICS

Parameter (Note 7)		Min	Typ	Max	Unit
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.46	Fs
Passband Ripple		-0.09	-	0.17	dB
Stopband		0.6	-	-	Fs
Stopband Attenuation		33	-	-	dB
Total Group Delay		-	7.6/Fs	-	s
High-Pass Filter Characteristics (48 kHz Fs)					
Frequency Response	-3.0 dB	-	3.7	-	Hz
	-0.13 dB	-	24.2	-	Hz
Phase Deviation	@ 20 Hz	-	10	-	Deg
Passband Ripple		-	-	0.17	dB
Filter Settling Time		-	10^5/Fs	0	s

Note:

7. Response is clock-dependent and will scale with Fs. Note that the response plots (Figure 33 to Figure 41) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs. HPF parameters are for Fs = 48 kHz.

ANALOG OUTPUT CHARACTERISTICS (COMMERCIAL - CNZ)

(Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; Sample Frequency = 48 kHz; test load R_L = 10 kΩ, C_L = 10 pF for the line output (see Figure 3), and test load R_L = 16 Ω, C_L = 10 pF (see Figure 3) for the headphone output. HP_GAIN[2:0] = 011.)

Parameter (Note 8)		VA = 2.5V (nominal) Min	Typ	Max	VA = 1.8V (nominal) Min	Typ	Max	Unit
R_L = 10 kΩ								
Dynamic Range								
18 to 24-Bit	A-weighted	92	98	-	89	95	-	dB
	unweighted	89	95	-	86	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-86	-78	-	-88	-82	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-	-	-32	-	dB
16-Bit	0 dB	-	-86	-	-	-88	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
R_L = 16 Ω								
Dynamic Range								
18 to 24-Bit	A-weighted	92	98	-	89	95	-	dB
	unweighted	89	95	-	86	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-75	-69	-	-75	-69	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-	-	-32	-	dB
16-Bit	0 dB	-	-75	-	-	-75	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
Other Characteristics for R_L = 16 Ω or 10 kΩ								
Output Parameters (Note 9)	Modulation Index (MI)	-	0.6787	-	-	0.6787	-	
	Analog Gain Multiplier (G)		0.6047			0.6047		
Full-scale Output Voltage (2•G•MI•VA) (Note 9)		See Line Output Voltage Characteristics, page 17						Vpp
Full-scale Output Power (Note 9)		See Headphone Output Power Characteristics, page 18,						mW
Interchannel Isolation (1 kHz)	16 Ω	-	80	-	-	80	-	dB
	10 kΩ	-	95	-	-	93	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
AC-Load Resistance (R_L)	(Note 10)	16	-	-	16	-	-	Ω
Load Capacitance (C_L)	(Note 10)	-	-	150	-	-	150	pF

Notes:

8. One LSB of triangular PDF dither is added to data.
9. Full-scale output voltage and power is determined by the gain setting, G, in register "Headphone Analog Gain (HP_GAIN[2:0])" on page 56. High gain settings at certain VA and VA_HP supply levels may cause clipping when the audio signal approaches full-scale, maximum power output. See Figures 27–30.

10. See Figure 3. R_L and C_L reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. In this circuit topology, C_L will effectively move the band-limiting pole of the amp in the output stage. Increasing this value beyond the recommended 150 pF can cause the internal op-amp to become unstable.

ANALOG OUTPUT CHARACTERISTICS (AUTOMOTIVE - DNZ)

(Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; Sample Frequency = 48 kHz and 96 kHz; test load R_L = 10 kΩ, C_L = 10 pF for the line output (see Figure 3), and test load R_L = 16 Ω, C_L = 10 pF (see Figure 3) for the headphone output. HP_GAIN[2:0] = 011.)

Parameter (Note 8)		**VA = 2.5V** (nominal) Min	Typ	Max	**VA = 1.8V** (nominal) Min	Typ	Max	Unit
R_L = 10 kΩ								
Dynamic Range								
18 to 24-Bit	A-weighted	90	98	-	87	95	-	dB
	unweighted	87	95	-	84	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-86	-73	-	-88	-80	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-	-	-32	-	dB
16-Bit	0 dB	-	-86	-	-	-88	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
R_L = 16 Ω								
Dynamic Range								
18 to 24-Bit	A-weighted	90	98	-	87	95	-	dB
	unweighted	87	95	-	84	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-75	-67	-	-75	-67	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-	-	-32	-	dB
16-Bit	0 dB	-	-75	-	-	-75	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
Other Characteristics for R_L = 16 or 10 kΩ								
Output Parameters (Note 9)	Modulation Index (MI)	-	0.6787	-	-	0.6787	-	
	Analog Gain Multiplier (G)		0.6047			0.6047		
Full-scale Output Voltage (2•G•MI•VA) (Note 9)		See Line Output Voltage Characteristics, page 17						Vpp
Full-scale Output Power (Note 9)		See Headphone Output Power Characteristics, page 18,						mW
Interchannel Isolation (1 kHz)	16 Ω	-	80	-	-	80	-	dB
	10 kΩ	-	95	-	-	93	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
AC-Load Resistance (R_L)	(Note 10)	16	-	-	16	-	-	Ω
Load Capacitance (C_L)	(Note 10)	-	-	150	-	-	150	pF

LINE OUTPUT VOLTAGE CHARACTERISTICS

Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; Sample Frequency = 48 kHz; test load R_L = 10 kΩ, C_L = 10 pF (see Figure 3).

Parameter			VA = 2.5V (nominal)			VA = 1.8V (nominal)			Unit
			Min	Typ	Max	Min	Typ	Max	
AOUTx Voltage Into R_L = 10 kΩ									
HP_GAIN[2:0]	Analog Gain (G)	VA_HP							
000	0.3959	1.8 V	-	1.34	-	-	0.97	-	V_{pp}
		2.5 V	-	1.34	-	-	0.97	-	V_{pp}
001	0.4571	1.8 V	-	1.55	-	-	1.12	-	V_{pp}
		2.5 V	-	1.55	-	-	1.12	-	V_{pp}
010	0.5111	1.8 V	-	1.73	-	-	1.25	-	V_{pp}
		2.5 V	-	1.73	-	-	1.25	-	V_{pp}
011 (default)	0.6047	1.8 V	-	2.05	-	1.41	1.48	1.55	V_{pp}
		2.5 V	1.95	2.05	2.15	-	1.48	-	V_{pp}
100	0.7099	1.8 V	-	2.41	-	-	1.73	-	V_{pp}
		2.5 V	-	2.41	-	-	1.73	-	V_{pp}
101	0.8399	1.8 V	-	2.85	-		2.05		V_{pp}
		2.5 V	-	2.85	-	-	2.05	-	V_{pp}
110	1.0000	1.8 V	-	3.39	-	-	2.44	-	V_{pp}
		2.5 V	-	3.39	-	-	2.44	-	V_{pp}
111	1.1430	1.8 V	(See (Note 11)				2.79		V_{pp}
		2.5 V	-	3.88	-	-	2.79	-	V_{pp}

Note:

11. VA_HP settings lower than VA reduces the headroom of the headphone amplifier. As a result, the DAC may not achieve the full THD+N performance at full-scale output voltage and power.

HEADPHONE OUTPUT POWER CHARACTERISTICS

Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; Sample Frequency = 48 kHz; test load R_L = 16 Ω, C_L = 10 pF (see Figure 3).

Parameter			VA = 2.5V (nominal)			VA = 1.8V (nominal)			Unit
			Min	Typ	Max	Min	Typ	Max	
AOUTx Power Into R_L = 16 Ω									
HP_GAIN[2:0]	Analog Gain (G)	VA_HP							
000	0.3959	1.8 V	-	14	-	-	7	-	mW_{rms}
		2.5 V	-	14	-	-	7	-	mW_{rms}
001	0.4571	1.8 V	-	19	-	-	10	-	mW_{rms}
		2.5 V	-	19	-	-	10	-	mW_{rms}
010	0.5111	1.8 V	-	23	-	-	12	-	mW_{rms}
		2.5 V	-	23	-	-	12	-	mW_{rms}
011 (default)	0.6047	1.8 V		(Note 11)		-	17	-	mW_{rms}
		2.5 V	-	32	-	-	17	-	mW_{rms}
100	0.7099	1.8 V		(Note 11)		-	23	-	mW_{rms}
		2.5 V	-	44	-	-	23	-	mW_{rms}
101	0.8399	1.8 V					(Note 9)		mW_{rms}
		2.5 V				-	32	-	mW_{rms}
110	1.0000	1.8 V							mW_{rms}
		2.5 V							mW_{rms}
111	1.1430	1.8 V							mW_{rms}
		2.5 V							mW_{rms}

(Note 9, 11)

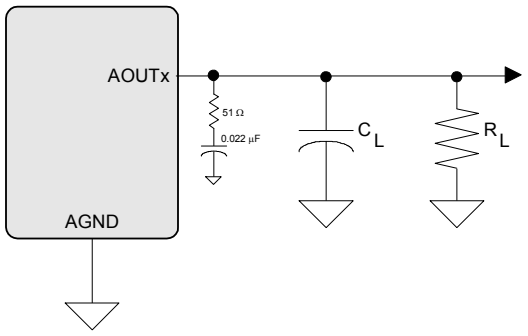


Figure 3. Headphone Output Test Load

COMBINED DAC INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

Parameter (Note 12)		Min	Typ	Max	Unit
Frequency Response 10 Hz to 20 kHz		-0.01	-	+0.08	dB
Passband	to -0.05 dB corner to -3 dB corner	0 0	- -	0.4780 0.4996	Fs Fs
StopBand		0.5465	-	-	Fs
StopBand Attenuation (Note 13)		50	-	-	dB
Group Delay		-	10.4/Fs	-	s
De-emphasis Error	Fs = 32 kHz Fs = 44.1 kHz Fs = 48 kHz	- - -	- - -	+1.5/+0 +0.05/-0.25 -0.2/-0.4	dB dB dB

Notes:

12. Response is clock dependent and will scale with Fs. Note that the response plots (Figure 38 to Figure 41 on page 80) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
13. Measurement Bandwidth is from Stopband to 3 Fs.

SWITCHING SPECIFICATIONS - SERIAL PORT

(Inputs: Logic 0 = DGND, Logic 1 = VL, SDOUT C_{LOAD} = 15 pF.)

Parameters		Symbol	Min	Max	Units
$\overline{\text{RESET}}$ pin Low Pulse Width (Note 14)			1	-	ms
MCLK Frequency			1.024	38.4	MHz
MCLK Duty Cycle (Note 15)			45	55	%
Slave Mode					
Input Sample Rate (LRCK)	Quarter-Speed Mode Half-Speed Mode Single-Speed Mode Double-Speed Mode	F_s F_s F_s F_s	4 8 4 50	12.5 25 50 100	kHz kHz kHz kHz
LRCK Duty Cycle			45	55	%
SCLK Frequency		$1/t_P$	-	$64 \cdot F_s$	Hz
SCLK Duty Cycle			45	55	%
LRCK Setup Time Before SCLK Rising Edge		$t_{s(LK-SK)}$	40	-	ns
LRCK Edge to SDOUT MSB Output Delay		$t_{d(MSB)}$	-	52	ns
SDOUT Setup Time Before SCLK Rising Edge		$t_{s(SDO-SK)}$	20	-	ns
SDOUT Hold Time After SCLK Rising Edge		$t_{h(SK-SDO)}$	30	-	ns
SDIN Setup Time Before SCLK Rising Edge		$t_{s(SD-SK)}$	20	-	ns
SDIN Hold Time After SCLK Rising Edge		t_h	20	-	ns

Parameters		Symbol	Min	Max	Units
Master Mode (Note 16)					
Output Sample Rate (LRCK)	All Speed Modes (Note 17)	F_s	-	$\frac{MCLK}{128}$	Hz
LRCK Duty Cycle			45	55	%
SCLK Frequency		$1/t_P$	-	$64 \cdot F_s$	Hz
SCLK Duty Cycle			45	55	%
LRCK Edge to SDOUT MSB Output Delay		$t_{d(MSB)}$	-	52	ns
SDOUT Setup Time Before SCLK Rising Edge		$t_{s(SDO-SK)}$	20	-	ns
SDOUT Hold Time After SCLK Rising Edge		$t_{h(SK-SDO)}$	30	-	ns
SDIN Setup Time Before SCLK Rising Edge		$t_{s(SD-SK)}$	20	-	ns
SDIN Hold Time After SCLK Rising Edge		t_h	20	-	ns

14. After powering up the CS42L51, $\overline{\text{RESET}}$ should be held low after the power supplies and clocks are settled.
15. See "Example System Clock Frequencies" on page 77 for typical MCLK frequencies.
16. See"Master" on page 38.
17. "MCLK" refers to the external master clock applied.

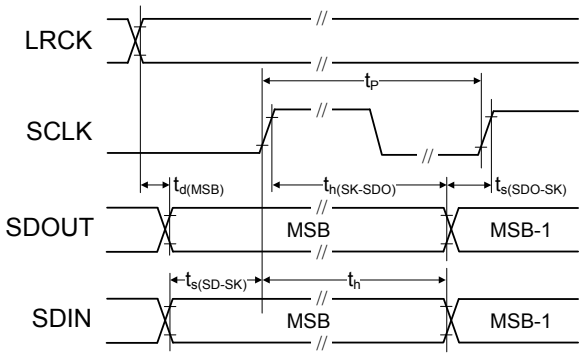


Figure 5. Serial Audio Interface Master Mode Timing

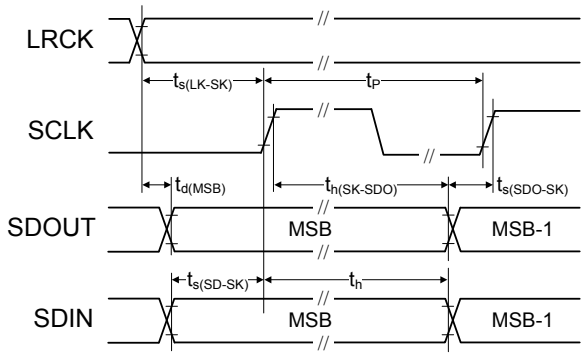


Figure 4. Serial Audio Interface Slave Mode Timing

SWITCHING SPECIFICATIONS - I²C CONTROL PORT

(Inputs: Logic 0 = DGND, Logic 1 = VL, SDA C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{\text{RESET}}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 18)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}	-	1	µs
Fall Time SCL and SDA	t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	3450	ns

18. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

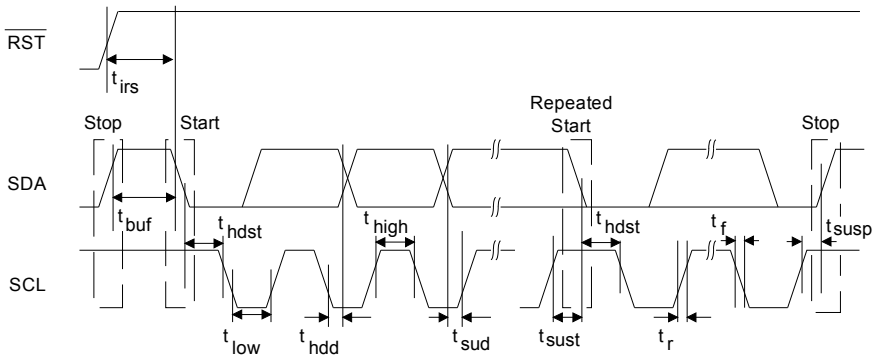


Figure 6. Control Port Timing - I²C

SWITCHING CHARACTERISTICS - SPI CONTROL PORT

(Inputs: Logic 0 = DGND, Logic 1 = VL)

Parameter		Symbol	Min	Max	Units
CCLK Clock Frequency		f_{sck}	0	6.0	MHz
$\overline{\text{RESET}}$ Rising Edge to $\overline{\text{CS}}$ Falling		t_{srs}	20	-	ns
$\overline{\text{CS}}$ Falling to CCLK Edge		t_{css}	20	-	ns
$\overline{\text{CS}}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 19)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN	(Note 20)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 20)	t_{f2}	-	100	ns

19. Data must be held for sufficient time to bridge the transition time of CCLK.
20. For f_{sck} <1 MHz.

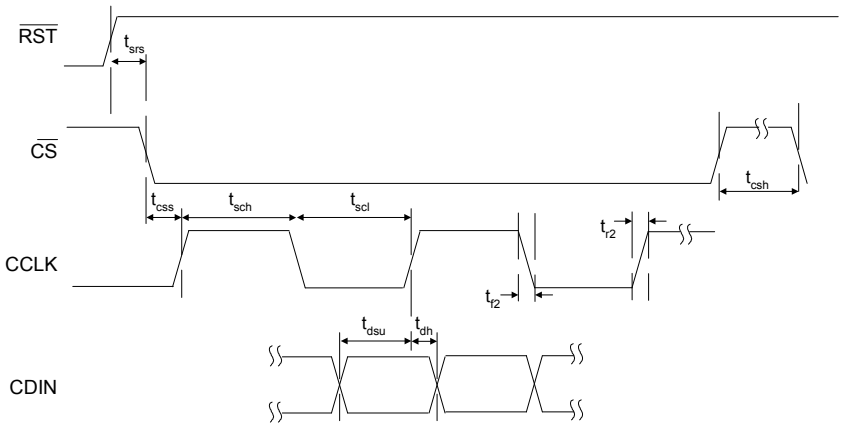


Figure 7. Control Port Timing - SPI Format

DC ELECTRICAL CHARACTERISTICS

(AGND = 0 V; all voltages with respect to ground.)

Parameters		Min	Typ	Max	Units
VQ Characteristics					
Nominal Voltage		-	0.5•VA	-	V
Output Impedance		-	23	-	kΩ
DC Current Source/Sink (Note 21)		-	-	10	µA
DAC_FILT+ Nominal Voltage		-	VA	-	V
ADC_FILT+ Nominal Voltage		-	VA	-	V
VSS_HP Characteristics					
Nominal Voltage		-	-0.8•(VA_HP)	-	V
DC Current Source		-		10	µA
MIC BIAS Characteristics					
Nominal Voltage	MICBIAS_LVL[1:0] = 00	-	0.8•VA	-	V
	MICBIAS_LVL[1:0] = 01	-	0.7•VA	-	V
	MICBIAS_LVL[1:0] = 10	-	0.6•VA	-	V
	MICBIAS_LVL[1:0] = 11	-	0.5•VA	-	V
DC Current Source		-	-	1	mA
Power Supply Rejection Ratio (PSRR)	1 kHz	-	50	-	dB
Power Supply Rejection Ratio (PSRR) (Note 22)	1 kHz	-	60	-	dB

21. The DC current draw represents the allowed current draw from the VQ pin due to typical leakage through electrolytic de-coupling capacitors.
22. Valid with the recommended capacitor values on DAC_FILT+, ADC_FILT+ and VQ. Increasing the capacitance will also increase the PSRR.

DIGITAL INTERFACE SPECIFICATIONS & CHARACTERISTICS

Parameters (Note 23)	Symbol	Min	Max	Units
Input Leakage Current	I_{in}	-	±10	µA
Input Capacitance		-	10	pF
1.8 V - 3.3 V Logic				
High-Level Output Voltage (I_{OH} = -100 µA)	V_{OH}	VL - 0.2	-	V
Low-Level Output Voltage (I_{OL} = 100 µA)	V_{OL}	-	0.2	V
High-Level Input Voltage	V_{IH}	0.68•VL	-	V
Low-Level Input Voltage	V_{IL}	-	0.32•VL	V

23. See “Digital I/O Pin Characteristics” on page 8 for serial and control port power rails.

POWER CONSUMPTION

See (Note 24)

	Operation	Power Control Registers 02h PDN_DACB	PDN_DACA	PDN_PGAB	PDN_PGAA	PDN_ADCB	PDN_ADCA	PDN	03h PDN_MICB	PDN_MICA	PDN_MICBIAS	V	Typical Current (mA) i_{VA_HP}	i_{VA}	i_{VD}	i_{VL} (Note 25)	Total Power (mW_{rms})
1	Off (Note 26)	x	x	x	x	x	x	x	x	x	x	1.8	0	0	0	0	0
												2.5	0	0	0	0	0
2	Standby (Note 27)	x	x	x	x	x	x	1	x	x	x	1.8	0	0.01	0.02	0	0.05
												2.5	0	0.01	0.03	0	0.10
3	Mono Record ADC	1	1	1	1	1	0	0	1	1	1	1.8	0	1.85	2.03	0.03	7.05
												2.5	0	2.07	3.05	0.05	12.94
	PGA to ADC	1	1	1	0	1	0	0	1	1	1	1.8	0	2.35	2.03	0.03	7.95
												2.5	0	2.58	3.08	0.05	14.29
	MIC to PGA to ADC (with Bias)	1	1	1	0	1	0	0	1	0	0	1.8	0	3.67	2.05	0.03	10.36
												2.5	0	3.95	3.09	0.05	17.71
	MIC to PGA to ADC (no Bias)	1	1	1	0	1	0	0	1	0	1	1.8	0	3.27	2.03	0.03	9.61
												2.5	0	3.52	3.08	0.05	16.62
4	Stereo Record ADC	1	1	1	1	0	0	0	1	1	1	1.8	0	2.69	2.12	0.03	8.72
												2.5	0	2.93	3.18	0.04	15.40
	PGA to ADC	1	1	0	0	0	0	0	1	1	1	1.8	0	3.65	2.12	0.03	10.45
												2.5	0	3.91	3.17	0.04	17.84
	MIC to PGA to ADC (no Bias)	1	1	0	0	0	0	0	0	0	1	1.8	0	5.48	2.11	0.03	13.73
												2.5	0	5.76	3.17	0.04	22.45
5	Mono Playback	1	0	1	1	1	1	0	1	1	1	1.8	1.66	1.40	2.35	0.01	9.74
												2.5	2.03	1.71	3.48	0.02	18.08
6	Stereo Playback	0	0	1	1	1	1	0	1	1	1	1.8	2.77	2.05	2.35	0.01	12.93
												2.5	3.21	2.50	3.49	0.02	23.02
7	Mono Record & Playback PGA in (no MIC) to Mono Out	1	0	1	0	1	0	0	1	1	1	1.8	1.66	3.63	2.73	0.03	14.49
												2.5	2.03	4.16	4.08	0.05	25.79
8	Phone Monitor MIC (with bias) in to Mono Out	1	0	1	0	1	0	0	1	0	0	1.8	1.66	4.95	2.75	0.03	16.90
												2.5	2.03	5.52	4.08	0.05	29.20
9	Stereo Record & Playback PGA in (no MIC) to Stereo Out	0	0	0	0	0	0	0	1	1	1	1.8	2.77	5.59	2.82	0.03	20.18
												2.5	3.21	6.28	4.19	0.04	34.30

24. Unless otherwise noted, test conditions are as follows: All zeros input, slave mode, sample rate = 48 kHz; No load. Digital (VD) and logic (VL) supply current will vary depending on speed mode and master/slave operation.
25. VL current will slightly increase in master mode.
26. $\overline{\text{RESET}}$ pin 25 held LO, all clocks and data lines are held LO.
27. $\overline{\text{RESET}}$ pin 25 held HI, all clocks and data lines are held HI.

4. APPLICATIONS

4.1 Overview

4.1.1 Architecture

The CS42L51 is a highly integrated, low power, 24-bit audio CODEC comprised of stereo analog-to-digital converters (ADC), and stereo digital-to-analog converters (DAC) designed using multi-bit delta-sigma techniques. The DAC operates at an oversampling ratio of 128Fs and the ADC operates at 64Fs, where Fs is equal to the system sample rate. The different clock rates maximize power savings while maintaining high performance. The CODEC operates in one of four sample rate speed modes: Quarter, Half, Single and Double. It accepts and is capable of generating serial port clocks (SCLK, LRCK) derived from an input Master Clock (MCLK).

4.1.2 Line & MIC Inputs

The analog input portion of the CODEC allows selection from and configuration of multiple combinations of stereo and microphone (MIC) sources. Six line inputs with configuration for two MIC inputs (or one MIC input with common mode rejection), two MIC bias outputs and independent channel control (including a high-pass filter disable function) are available. A Programmable Gain Amplifier (PGA), MIC boost, and Automatic Level Control (ALC), with noise gate settings, provide analog gain and adjustment. Digital volume controls, including gain, boost, attenuation and inversion are also available.

4.1.3 Line & Headphone Outputs

The analog output portion of the D/A includes a headphone amplifier capable of driving headphone and line-level loads. An on-chip charge pump creates a negative headphone supply allowing a full-scale output swing centered around ground. This eliminates the need for large DC-Blocking capacitors and allows the amplifier to deliver more power to headphone loads at lower supply voltages. Eight gain settings for the headphone amplifier are available.

4.1.4 Signal Processing Engine

A signal processing engine is available to process serial input D/A data before output to the DAC. The D/A data has independent volume controls and mixing functions such as mono mixes and left/right channel swaps. A Tone Control provides bass and treble at four selectable corner frequencies. An automatic level control provides limiting capabilities at programmable attack and release rates, maximum thresholds and soft ramping. A 15/50 μs de-emphasis filter is also available at a 44.1 kHz sample rate.

4.1.5 Beep Generator

A beep may be generated internally at select frequencies across approximately two octave major scales and configured to occur continuously, periodically or at single time intervals controlled by the user. Volume may be controlled independently.

4.1.6 Device Control (Hardware or Software Mode)

In Software Mode, all functions and features may be controlled via a two-wire I²C or three-wire SPI control port interface. In Hardware Mode, a limited feature set may be controlled via stand-alone control pins.

4.1.7 Power Management

Two Software Mode control registers provide independent power-down control of the ADC, DAC, PGA, MIC pre-amp and MIC bias, allowing operation in select applications with minimal power consumption.