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CS42L52

Low-Power, Stereo CODEC with Headphone and Speaker Amps

Stereo CODEC

- High Performance Stereo ADC and DAC
  - 99 dB (ADC), 98 dB (DAC) Dyn. Range (A-wtd)
  - -88 dB THD+N
- Flexible Stereo Analog Input Architecture
  - 4:1 Analog Input MUX
  - Analog Input Mixing
  - Analog Passthrough with Volume Control
  - Analog Programmable Gain Amplifier (PGA)
- Programmable Automatic Level Control (ALC)
  - Noise Gate for Noise Suppression
  - Programmable Threshold and Attack/Release Rates
- Dual MIC Inputs
  - Differential or Single-ended
  - +16 dB to +32 dB with 1-dB step Mic Pre-Amplifiers
  - Programmable, Low-noise MIC Bias Levels
- Digital Signal Processing Engine
  - Bass and Treble Tone Control, De-emphasis
  - Master Vol. and Independent PCM SDIN + ADC SDOUT Mix Volume Control
  - Soft-Ramp and Zero-Cross Transitions
  - Programmable Peak-detect and Limiter
  - Beep Generator w/Full Tone Control

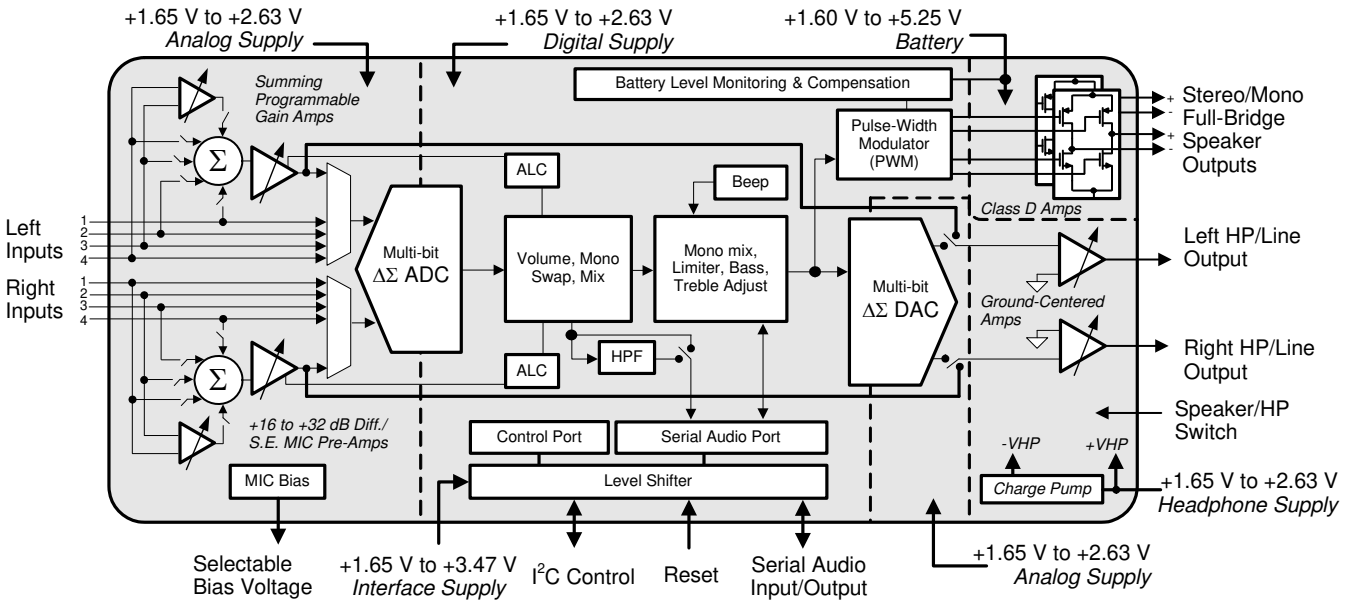
Class D Stereo/Mono Speaker Amplifier

- No External Filter Required
- High-power Stereo Output at 10% THD+N
  - 2 x 1.00 W into 8 Ω @ 5.0 V
  - 2 x 550 mW into 8 Ω @ 3.7 V
  - 2 x 230 mW into 8 Ω @ 2.5 V
- High-power Mono Output at 10% THD+N
  - 1 x 1.90 W into 4 Ω @ 5.0 V
  - 1 x 1.00 W into 4 Ω @ 3.7 V
  - 1 x 350 mW into 4 Ω @ 2.5 V
- Direct Battery-powered Operation
  - Battery Level Monitoring and Compensation
- 81% Efficiency at 800 mW
- Phase-aligned PWM Output Reduces Idle Channel Current
- Spread Spectrum Modulation
- Low Quiescent Current

Stereo Headphone Amplifier

- Ground-centered Outputs
  - No DC-Blocking Capacitors Required
  - Integrated Negative Voltage Regulator
- High-power Output at -75 dB THD+N
  - 2 x 23 mW Into 16 Ω @ 1.8 V
  - 2 x 44 mW Into 16 Ω @ 2.5 V

(**Features** continued on page 2)



System Features

- 12, 24, and 27 MHz Master Clock Support in Addition to Typical Audio Clock Rates
- High-performance 24-bit Converters
  - Multi-bit Delta-Sigma Architecture
  - Very Low 64Fs Oversampling Clock Reduces Power Consumption
- Low-power Operation
  - Stereo Analog Passthrough: 10 mW @ 1.8 V
  - Stereo Playback: 14 mW @ 1.8 V
  - Stereo Rec. and Playback: 23 mW @ 1.8 V
- Variable Power Supplies
  - 1.8 V to 2.5 V Digital and Analog
  - 1.6 V to 5 V Class D Amplifier
  - 1.8 V to 2.5 V Headphone Amplifier
  - 1.8 V to 3.3 V Interface Logic
- Power-down Management
  - ADC, DAC, CODEC, MIC Pre-Amplifier, PGA, Headphone Amplifier, Speaker Amplifier
- Analog and Digital Routing/Mixes:
  - Line/Headphone Out = Analog In (ADC Bypassed)
  - Line/Headphone/Speaker Out = ADC + Digital In
  - Digital Out = ADC + Digital In
  - Internal Digital Loopback
  - Mono Mixes
- Flexible Clocking Options
  - Master or Slave Operation
  - High-impedance Digital Output Option (for easy MUXing between CODEC and other data sources)
  - Quarter-speed Mode - (i.e. allows 8 kHz Fs while maintaining a flat noise floor up to 16 kHz)
  - 4 kHz to 96 kHz Sample Rates
- I^2C^{TM} Control Port Operation
- Headphone/Speaker Detection Input
- Pop and Click Suppression

Applications

- Digital Voice Recorders, Digital Cameras, and Camcorders
- PDA's
- Personal Media Players
- Portable Game Consoles

General Description

The CS42L52 is a highly integrated, low-power stereo CODEC with headphone and Class D speaker amplifiers. The CS42L52 offers many features suitable for low-power, portable system applications.

The **ADC input path** allows independent channel control of a number of features. Input summing amplifiers mix and select line-level and/or microphone-level inputs for each channel. The microphone input path includes a selectable programmable-gain pre-amplifier stage and a low-noise MIC bias voltage supply. A PGA is available for line or microphone inputs and provides analog gain with soft-ramp and zero-cross transitions. The ADC also features a digital volume control with soft ramp transitions. A programmable ALC and Noise Gate monitor the input signals and adjust the volume levels appropriately. To conserve power, the ADC may be bypassed while still allowing full analog volume control.

The **DAC output path** includes a digital signal processing engine with various fixed-function controls. Tone Control provides bass and treble adjustment of four selectable corner frequencies. The Digital Mixer provides independent volume control for both the ADC output and PCM input signal paths, as well as a master volume control. Digital Volume controls may be configured to change on soft-ramp transitions while the analog controls can be configured to occur on every zero crossing. The DAC also includes de-emphasis, limiting functions and a BEEP generator, delivering tones selectable across a range of two full octaves.

The **stereo headphone amplifier** is powered from a separate positive supply and the integrated **charge pump** provides a negative supply. This allows a ground-centered, analog output with a wide signal swing and eliminates external DC-blocking capacitors.

The **Class D stereo speaker amplifier** does not require an external filter and provides the high-efficiency amplification required by power-sensitive portable applications. The speaker amplifier may be powered directly from a battery while the internal DC supply monitoring and compensation provides a constant gain level as the battery's voltage decays.

In addition to its many features, the CS42L52 operates from a low-voltage analog and digital core making it ideal for portable systems that require extremely low power consumption in a minimal amount of space.

The CS42L52 is available in a 40-pin QFN package in Commercial (-40 to +85 °C) grade. The CS42L52 Customer Demonstration board is also available for device evaluation and implementation suggestions. Refer to "Ordering Information" on page 81 for complete ordering information.

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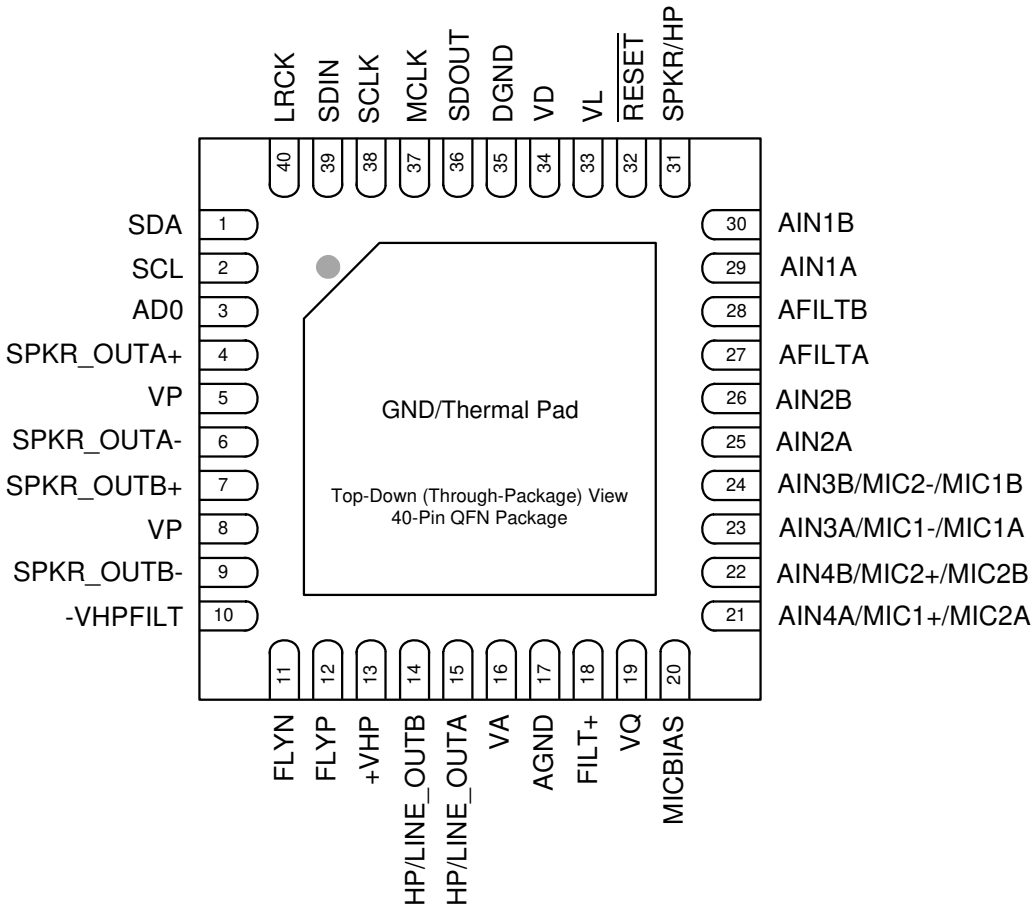
1. PIN DESCRIPTIONS



Pin Name	#	Pin Description
SDA	1	**Serial Control Data** (*Input/Output*) - SDA is a data I/O in I²C Mode.
SCL	2	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port.
AD0	3	**Address Bit 0** (*Input*) - Chip address bit 0.
SPKR_OUTA+ SPKR_OUTA- SPKR_OUTB+ SPKR_OUTB-	4 6 7 9	**PWM Speaker Output** (*Output*) - Full-bridge amplified PWM speaker outputs.
VP	5 8	**Power for PWM Drivers** (*Input*) - Power supply for the PWM output driver stages.
-VHPFILT	10	**Inverting Charge Pump Filter Connection** *(Output)* - Power supply from the inverting charge pump that provides the negative rail for the headphone/line amplifiers.
FLYN	11	**Charge Pump Cap Negative Node** *(Output)* - Negative node for the inverting charge pump's flying capacitor.
FLYP	12	**Charge Pump Cap Positive Node** *(Output)* - Positive node for the inverting charge pump's flying capacitor.
+VHP	13	**Positive Analog Power for Headphone** (*Input*) - Positive voltage rail and power for the internal headphone amplifiers and inverting charge pump.
HP/LINE_OUTB, A	14,15	**Headphone/Line Audio Output** (*Output*) - Stereo headphone or line level analog outputs.
VA	16	**Analog Power** (*Input*) - Positive power for the internal analog section.

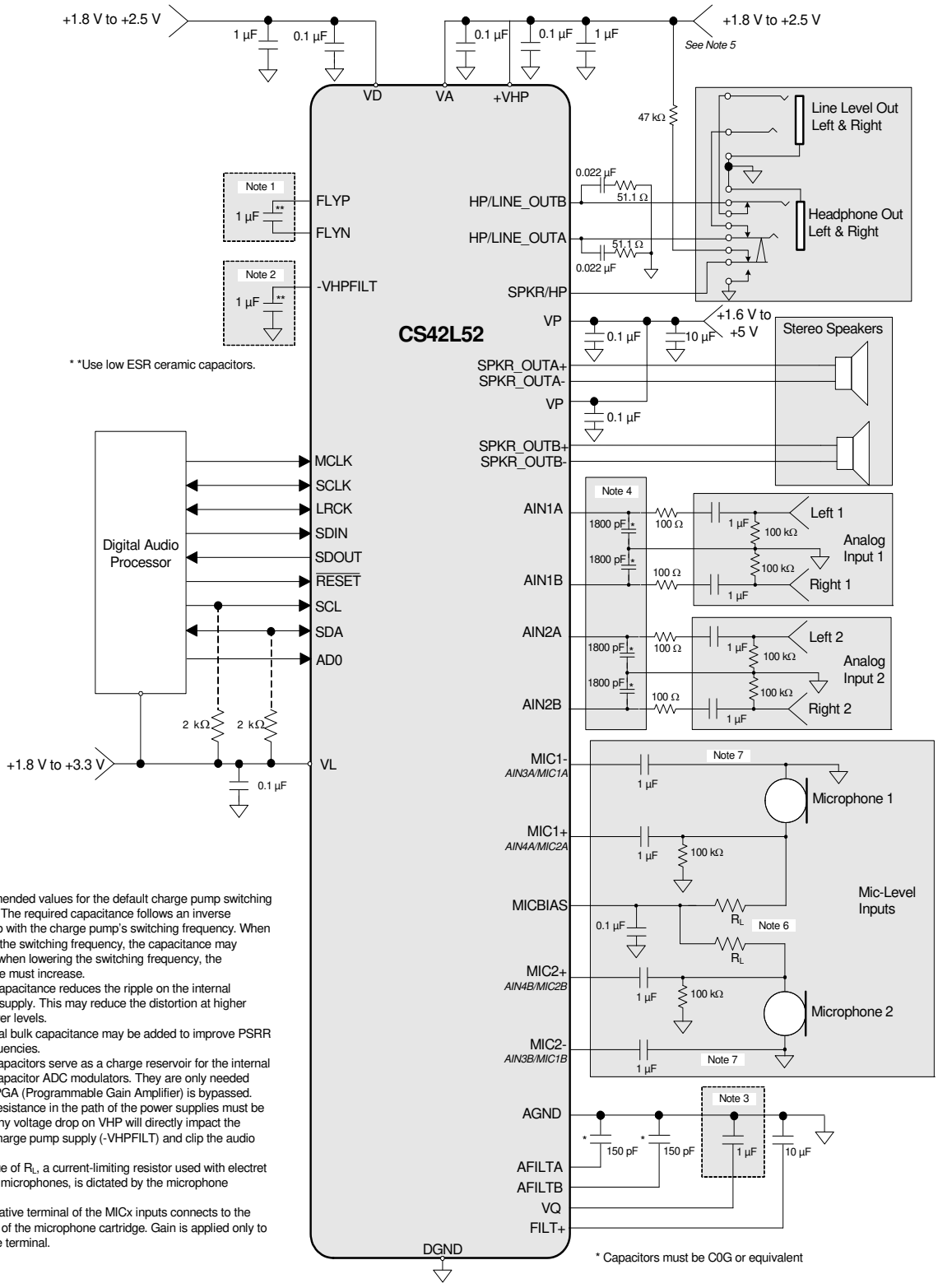
AGND	17	**Analog Ground** (*Input*) - Ground reference for the internal analog section.
FILT+	18	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits.
VQ	19	**Quiescent Voltage** (*Output*) - Filter connection for the internal quiescent voltage.
MICBIAS	20	**Microphone Bias** (*Output*) - Low noise bias supply for an external microphone. Electrical characteristics are specified in the DC Electrical Characteristics table.
AIN4A,B AIN3A,B	21,22 23,24	**Line-Level Analog Inputs** (*Input*) - Single-ended stereo line-level analog inputs.
MIC1+,- MIC2+,-	21,23 22,24	**Differential Microphone Inputs** (*Input*) - Differential stereo microphone inputs.
MIC2A,B MIC1A,B	21,22 23,24	**Single-Ended Microphone Inputs** (*Input*) - Single-ended stereo microphone inputs.
AIN2A,B AIN1A,B	25,26 29,30	**Line-Level Analog Inputs** (*Input*) - Single-ended stereo line-level analog inputs.
AFILTA,B	27,28	**Anti-alias Filter Connection** (*Output*) - Anti-alias filter connection for the ADC inputs.
SPKR/HP	31	**Speaker/Headphone Switch** (*Input*) - Powers down the left and/or right channel of the speaker and/or headphone outputs.
$\overline{\text{RESET}}$	32	**Reset** (*Input*) - The device enters a low power mode when this pin is driven low.
VL	33	**Digital Interface Power** (*Input*) - Determines the required signal level for the serial audio interface and host control port.
VD	34	**Digital Power** (*Input*) - Positive power for the internal digital section.
DGND	35	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
SDOUT	36	**Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data.
MCLK	37	**Master Clock** (*Input*) - Clock source for the delta-sigma modulators.
SCLK	38	**Serial Clock** (*Input/Output*) - Serial clock for the serial audio interface.
SDIN	39	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
LRCK	40	**Left Right Clock** (*Input/Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
GND/Thermal Pad	-	Ground reference for PWM power FETs and charge pump; thermal relief pad for optimized heat dissipation.

1.1 I/O Pin Characteristics

Input and output levels and associated power supply voltage are shown in the table below. Logic levels should not exceed the corresponding power supply voltage.

Power Supply	Pin Name	I/O	Internal Connections	Driver	Receiver
VL	$\overline{\text{RESET}}$	Input	-	-	1.65 V - 3.47 V, with Hysteresis
	AD0	Input	-	-	1.65 V - 3.47 V, with Hysteresis
	SCL	Input	-	-	1.65 V - 3.47 V, with Hysteresis
	SDA	Input/ Output	-	1.65 V - 3.47 V, CMOS/Open Drain	1.65 V - 3.47 V, with Hysteresis
	MCLK	Input	-	-	1.65 V - 3.47 V
	LRCK	Input/ Output	Weak Pullup (~1 MΩ)	1.65 V - 3.47 V, CMOS	1.65 V - 3.47 V
	SCLK	Input/ Output	Weak Pullup (~1 MΩ)	1.65 V - 3.47 V, CMOS	1.65 V - 3.47 V
	SDOUT	Output	Weak Pullup (~1 MΩ)	1.65 V - 3.47 V, CMOS	
	SDIN	Input	-	-	1.65 V - 3.47 V
VA	SPKR/HP	Input	-	-	1.65 V - 2.63 V
VP	SPKR_OUTA+	Output	-	1.6 V - 5.25 V Power MOSFET	-
	SPKR_OUTA-	Output	-	1.6 V - 5.25 V Power MOSFET	-
	SPKR_OUTB+	Output	-	1.6 V - 5.25 V Power MOSFET	-
	SPKR_OUTB-	Output	-	1.6 V - 5.25 V Power MOSFET	-

2. TYPICAL CONNECTION DIAGRAM



Notes:

1. Recommended values for the default charge pump switching frequency. The required capacitance follows an inverse relationship with the charge pump's switching frequency. When increasing the switching frequency, the capacitance may decrease; when lowering the switching frequency, the capacitance must increase.

2. Larger capacitance reduces the ripple on the internal amplifier's supply. This may reduce the distortion at higher output power levels.

3. Additional bulk capacitance may be added to improve PSRR at low frequencies.

4. These capacitors serve as a charge reservoir for the internal switched capacitor ADC modulators. They are only needed when the PGA (Programmable Gain Amplifier) is bypassed.

5. Series resistance in the path of the power supplies must be avoided. Any voltage drop on VHP will directly impact the negative charge pump supply (-VHPFILT) and clip the audio output.

6. The value of R_L, a current-limiting resistor used with electret condenser microphones, is dictated by the microphone cartridge.

7. The negative terminal of the MICx inputs connects to the ground pin of the microphone cartridge. Gain is applied only to the positive terminal.

Figure 1. Typical Connection Diagram

3. CHARACTERISTIC AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

AGND=DGND=0 V, All voltages with respect to ground.

Parameters	Symbol	Min	Max	Units
DC Power Supply				
Analog	VA	1.65	2.63	V
Headphone Amplifier	+VHP	1.65	2.63	V
Speaker Amplifier	VP	1.60	5.25	V
Digital	VD	1.65	2.63	V
Serial/Control Port Interface	VL	1.65	3.47	V
Ambient Temperature Commercial - CNZ	T_A	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS

AGND = DGND = 0 V; All voltages with respect to ground.

Parameters		Symbol	Min	Max	Units
DC Power Supply	Analog	VA, VHP	-0.3	3.0	V
	Speaker	VP	-0.3	6.0	V
	Digital	VD	-0.3	3.0	V
	Serial/Control Port Interface	VL	-0.3	4.0	V
Input Current	(Note 1)	I_{in}	-	±10	mA
External Voltage Applied to Analog Input	(Note 2)	V_{IN}	AGND-0.3	VA+0.3	V
External Voltage Applied to Analog Output		V_{IN}	-VHP - 0.3	+VHP + 0.3	V
External Voltage Applied to Digital Input	(Note 2)	V_{IND}	-0.3	VL+ 0.3	V
Ambient Operating Temperature	(power applied)	T_A	-50	+115	°C
Storage Temperature		T_{stg}	-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:

1. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.
2. The maximum over/under voltage is limited by the input current.

ANALOG INPUT CHARACTERISTICS

Test Conditions (unless otherwise specified): Input sine wave (relative to digital full scale): 1 kHz through passive input filter; All Supplies = VA; T_A = +25°C; Sample Frequency = 48 kHz; Measurement Bandwidth is 20 Hz to 20 kHz unless otherwise specified; "Required Initialization Settings" on page 37 written on power up.

Parameters		VA = 2.5V Min	VA = 2.5V Typ	VA = 2.5V Max	VA = 1.8V Min	VA = 1.8V Typ	VA = 1.8V Max	Unit
Analog In to ADC (PGA bypassed)								
Dynamic Range	A-weighted	93	99	-	90	96	-	dB
	unweighted	90	96	-	87	93	-	dB
Total Harmonic Distortion + Noise	-1 dBFS	-	-86	-80	-	-84	-78	dB
	-20 dBFS	-	-76	-	-	-73	-	dB
	-60 dBFS	-	-36	-30	-	-33	-27	dB
Analog In to PGA to ADC								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	92	96	-	89	95	-	dB
	unweighted	89	93	-	86	92	-	dB
PGA Setting: +12 dB	A-weighted	85	91	-	82	88	-	dB
	unweighted	82	88	-	79	85	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-1 dBFS	-	-88	-82	-	-86	-80	dB
	-60 dBFS	-	-33	-27	-	-32	-26	dB
PGA Setting: +12 dB	-1 dBFS	-	-85	-79	-	-83	-77	dB
Analog In to MIC Pre-Amp (+16 dB) to PGA to ADC								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	-	86	-	-	83	-	dB
	unweighted	-	83	-	-	80	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-1 dBFS	-	-76	-	-	-74	-	dB
Analog In to MIC Pre-Amp (+32 dB) to PGA to ADC								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	-	76	-	-	74	-	dB
	unweighted	-	73	-	-	71	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-2 dBFS	-	-74	-	-	-71	-	dB
Other Characteristics								
DC Accuracy								
Interchannel Gain Mismatch		-	0.2	-	-	0.2	-	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Offset Error	SDOUT Code with HPF On	-	352	-	-	352	-	LSB
Input								
Interchannel Isolation		-	90	-	-	90	-	dB
HP Amp to Analog Input Isolation	R_L = 10 kΩ	-	100	-	-	100	-	dB
(Note 3)	R_L = 16 Ω	-	70	-	-	70	-	dB
Speaker Amp to Analog Input Isolation		-	60	-	-	60	-	dB
Full-scale Input Voltage	ADC	0.73•VA	0.769•VA	0.83•VA	0.73•VA	0.769•VA	0.83•VA	Vpp
	PGA (0 dB)	0.73•VA	0.770•VA	0.83•VA	0.73•VA	0.770•VA	0.83•VA	Vpp
	PGA (+12 dB)		0.194•VA			0.194•VA		Vpp
	MIC (+16 dB)		0.115•VA			0.115•VA		Vpp
	MIC (+32 dB)		0.019•VA			0.019•VA		Vpp
Input Impedance (Note 4)	ADC	-	20	-	-	20	-	kΩ
	PGA	-	39	-	-	39	-	kΩ
	MIC	-	50	-	-	50	-	kΩ

3. Measured with DAC delivering full-scale output into specified load.
4. Measured between analog input and AGND.

ADC DIGITAL FILTER CHARACTERISTICS

Parameters (Note 5)		Min	Typ	Max	Unit
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.4948	Fs
Passband Ripple		-0.09	-	0.17	dB
Stopband		0.6	-	-	Fs
Stopband Attenuation		33	-	-	dB
Total Group Delay		-	7.6/Fs	-	s
High-Pass Filter Characteristics (48 kHz Fs)					
Frequency Response	-3.0 dB -0.13 dB	- -	3.6 24.2	- -	Hz Hz
Phase Deviation	@ 20 Hz	-	10	-	Deg
Passband Ripple		-	-	0.17	dB
Filter Settling Time		-	10^5/Fs	0	s

5. Response is clock-dependent and will scale with Fs. Note that the response plots (Figures 26 to 29 on page 78) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs. HPF parameters are for Fs = 48 kHz.

ANALOG OUTPUT CHARACTERISTICS

Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; All Supplies = VA; T_A = +25°C; Sample Frequency = 48 kHz; Measurement bandwidth is 20 Hz to 20 kHz; Test load R_L = 10 kΩ, C_L = 10 pF for the line output (see Figure 2); Test load R_L = 16 Ω, C_L = 10 pF (see Figure 2) for the headphone output; HP_GAIN[2:0] = 011; "Required Initialization Settings" on page 37 written on power up.

Parameters (Note 6)		VA = 2.5 V Min	VA = 2.5 V Typ	VA = 2.5 V Max	VA = 1.8 V Min	VA = 1.8 V Typ	VA = 1.8 V Max	Unit
R_L = 10 kΩ								
Dynamic Range								
18- to 24-Bit	A-weighted	92	98	-	89	95	-	dB
	unweighted	89	95	-	86	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18- to 24-Bit	0 dB	-	-86	-80	-	-88	-82	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-29	-	-32	-26	dB
16-Bit	0 dB	-	-86	-	-	-88	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
R_L = 16 Ω								
Dynamic Range								
18- to 24-Bit	A-weighted	92	98	-	89	95	-	dB
	unweighted	89	95	-	86	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18- to 24-Bit	0 dB	-	-75	-69	-	-75	-69	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-29	-	-32	-26	dB
16-Bit	0 dB	-	-75	-	-	-75	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
Other Characteristics for R_L = 16 Ω or 10 kΩ								
Output Parameters (Note 7)	Modulation Index (MI)	-	0.6787	-	-	0.6787	-	
	Analog Gain Multiplier (G)	-	0.6047	-	-	0.6047	-	
Full-scale Output Voltage (2•G•MI•VA) (Note 7)		See "Line Output Voltage Level Characteristics" on page 19						Vpp
Full-scale Output Power (Note 7)		See "Headphone Output Power Characteristics" on page 18						
Interchannel Isolation (1 kHz)	16 Ω	-	80	-	-	80	-	dB
	10 kΩ	-	95	-	-	93	-	dB
Speaker Amp to HP Amp Isolation		-	80	-	-	80	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
AC Load Resistance (R_L)	(Note 8)	16	-	-	16	-	-	Ω
Load Capacitance (C_L)	(Note 8)	-	-	150	-	-	150	pF

6. One (least-significant bit) LSB of triangular PDF dither is added to data.
7. Full-scale output voltage and power is determined by the gain setting, G, in register "Headphone Analog Gain" on page 51. High gain settings at certain VA and VHP supply levels may cause clipping when the audio signal approaches full-scale, maximum power output, as shown in Figures 22 - 25 on page 75.

8. See Figure 2. R_L and C_L reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. In this circuit topology, C_L will effectively move the band-limiting pole of the amp in the output stage. Increasing this value beyond the recommended 150 pF can cause the internal op-amp to become unstable.

ANALOG PASSTHROUGH CHARACTERISTICS

Test Conditions (unless otherwise specified): Input sine wave (relative to full-scale): 1 kHz through passive input filter; PGA and HP/Line Gain = 0 dB; All Supplies = VA; T_A = +25°C; Sample Frequency = 48 kHz; Measurement Bandwidth is 20 Hz to 20 kHz; "Required Initialization Settings" on page 37 written on power up.

Parameters		VA = 2.5 V Min	VA = 2.5 V Typ	VA = 2.5 V Max	VA = 1.8 V Min	VA = 1.8 V Typ	VA = 1.8 V Max	Unit
Analog In to HP/Line Amp (ADC is powered down)								
R_L = 10 kΩ								
Dynamic Range	A-weighted	-	-96	-	-	-94	-	dB
	unweighted	-	-93	-	-	-91	-	dB
Total Harmonic Distortion + Noise	-1 dBFS	-	-70	-	-	-70	-	dB
	-20 dBFS	-	-73	-	-	-71	-	dB
	-60 dBFS	-	-33	-	-	-31	-	dB
Full-scale Input Voltage		-	0.91•VA	-	-	0.91•VA	-	Vpp
Full-scale Output Voltage		-	0.84•VA	-	-	0.84•VA	-	Vpp
Passband Ripple		-	0/-0.3	-	-	0/-0.3	-	dB
R_L = 16 Ω								
Dynamic Range	A-weighted	-	-96	-	-	-94	-	dB
	unweighted	-	-93	-	-	-91	-	dB
Total Harmonic Distortion + Noise	-1 dBFS	-	-70	-	-	-70	-	dB
	-20 dBFS	-	-73	-	-	-71	-	dB
	-60 dBFS	-	-33	-	-	-31	-	dB
Full-scale Input Voltage		-	0.91•VA	-	-	0.91•VA	-	Vpp
Full-scale Output Voltage		-	0.84•VA	-	-	0.84•VA	-	Vpp
Output Power		-	32	-	-	17	-	mW
Passband Ripple		-	0/-0.3	-	-	0/-0.3	-	dB

PWM OUTPUT CHARACTERISTICS

Test conditions (unless otherwise specified): Input test signal is a full scale 997 Hz signal; MCLK = 12.2880 MHz; Measurement Bandwidth is 20 Hz to 20 kHz; Sample Frequency = 48 kHz; Test load R_L = 8 Ω for stereo full-bridge, R_L = 4 Ω for mono parallel full-bridge; VD = VL = VA = VHP = 1.8 V; PWM Modulation Index of 0.85; PWM Switch Rate = 384 kHz; "Required Initialization Settings" on page 37 written on power up. (Note 9)

Parameters (Note 10)	Symbol	Conditions	Min	Typ	Max	Units
VP = 5.0 V						
Power Output per Channel	P_O					
Stereo Full-Bridge		THD+N < 10% THD+N < 1%	- -	1.00 0.80	- -	W_{rms} W_{rms}
Mono Parallel Full-Bridge		THD+N < 10% THD+N < 1%	- -	1.90 1.50	- -	W_{rms} W_{rms}
Total Harmonic Distortion + Noise	THD+N					
Stereo Full-Bridge		P_O = 0 dBFS = 0.8W	-	0.52	-	%
Mono Parallel Full-Bridge		P_O = -3 dBFS = 0.75 W P_O = 0 dBFS = 1.5 W	- -	0.10 0.50	- -	% %
Dynamic Range	DR					
Stereo Full-Bridge		P_O = -60 dBFS, A-Weighted P_O = -60 dBFS, Unweighted	- -	91 88	- -	dB dB
Mono Parallel Full-Bridge		P_O = -60 dBFS, A-Weighted P_O = -60 dBFS, Unweighted	- -	91 88	- -	dB dB
VP = 3.7 V						
Power Output per Channel	P_O					
Stereo Full-Bridge		THD+N < 10% THD+N < 1%	- -	0.55 0.45	- -	W_{rms} W_{rms}
Mono Parallel Full-Bridge		THD+N < 10% THD+N < 1%	- -	1.00 0.84	- -	W_{rms} W_{rms}
Total Harmonic Distortion + Noise	THD+N					
Stereo Full-Bridge		P_O = 0 dBFS = 0.43 W	-	0.54	-	%
Mono Parallel Full-Bridge		P_O = -3 dBFS = 0.41 W P_O = 0 dBFS = 0.81 W	- -	0.09 0.45	- -	% %
Dynamic Range	DR					
Stereo Full-Bridge		P_O = -60 dBFS, A-Weighted P_O = -60 dBFS, Unweighted	- -	91 88	- -	dB dB
Mono Parallel Full-Bridge		P_O = -60 dBFS, A-Weighted P_O = -60 dBFS, Unweighted	- -	95 92	- -	dB dB
VP =2.5 V						
Power Output per Channel	P_O					
Stereo Full-Bridge		THD+N < 10% THD+N < 1%	- -	0.23 0.19	- -	W_{rms} W_{rms}
Mono Parallel Full-Bridge		THD+N < 10% THD+N < 1%	- -	0.44 0.35	- -	W_{rms} W_{rms}
Total Harmonic Distortion + Noise	THD+N					
Stereo Full-Bridge		P_O = 0 dBFS = 0.18 W	-	0.50	-	%
Mono Parallel Full-Bridge		P_O = -3 dBFS = 0.17 W P_O = 0 dBFS = 0.35 W	- -	0.08 0.43	- -	% %
Dynamic Range	DR					
Stereo Full-Bridge		P_O = -60 dBFS, A-Weighted P_O = -60 dBFS, Unweighted	- -	91 88	- -	dB dB
Mono Parallel Full-Bridge		P_O = -60 dBFS, A-Weighted P_O = -60 dBFS, Unweighted	- -	94 91	- -	dB dB
MOSFET On Resistance	$R_{DS(ON)}$	VP = 5.0V, I_d = 0.5 A	-	600	-	mΩ

Parameters (Note 10)	Symbol	Conditions	Min	Typ	Max	Units
MOSFET On Resistance	$R_{DS(ON)}$	VP = 3.7V, I_d = 0.5 A	-	640	-	mΩ
MOSFET On Resistance	$R_{DS(ON)}$	VP = 2.5V, I_d = 0.5 A	-	760	-	mΩ
Efficiency	η	VP = 5.0 V, P_O = 2 x 0.8 W, R_L = 8 Ω	-	81	-	%
Output Operating Peak Current	I_{PC}		-	-	1.5	A
VP Input Current During Reset	I_{VP}	$\overline{\text{RESET}}$, pin 32, is held low	-	0.8	5.0	µA

9. The PWM driver should be used in captive speaker systems only.

10. Optimal PWM performance is achieved when MCLK > 12 MHz.

HEADPHONE OUTPUT POWER CHARACTERISTICS

Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; Sample Frequency = 48 kHz; Measurement Bandwidth is 20 Hz to 20 kHz; Test load R_L = 16 Ω, C_L = 10 pF (see Figure 2); "Required Initialization Settings" on page 37 written on power up.

Parameters			VA = 2.5V Min	VA = 2.5V Typ	VA = 2.5V Max	VA = 1.8V Min	VA = 1.8V Typ	VA = 1.8V Max	Unit
AOUTx Power Into R_L = 16 Ω									
HP_GAIN[2:0]	Analog Gain (G)	VHP							
000	0.3959	1.8 V	-	14	-	-	7	-	mW_{rms}
		2.5 V	-	14	-	-	7	-	mW_{rms}
001	0.4571	1.8 V	-	19	-	-	10	-	mW_{rms}
		2.5 V	-	19	-	-	10	-	mW_{rms}
010	0.5111	1.8 V	-	23	-	-	12	-	mW_{rms}
		2.5 V	-	23	-	-	12	-	mW_{rms}
011 (default)	0.6047	1.8 V		(Note 11)		-	17	-	mW_{rms}
		2.5 V	-	32	-	-	17	-	mW_{rms}
100	0.7099	1.8 V		(Note 11)		-	23	-	mW_{rms}
		2.5 V	-	44	-	-	23	-	mW_{rms}
101	0.8399	1.8 V				(Note 7), Figure 22 on page 74			mW_{rms}
		2.5 V				-	32	-	mW_{rms}
110	1.0000	1.8 V	(Note 7, 11) See Figures 22 and 23 on page 74						mW_{rms}
		2.5 V							mW_{rms}
111	1.1430	1.8 V							mW_{rms}
		2.5 V							mW_{rms}

11. VHP settings lower than VA reduces the headroom of the headphone amplifier. As a result, the DAC may not achieve the full THD+N performance at full-scale output voltage and power.

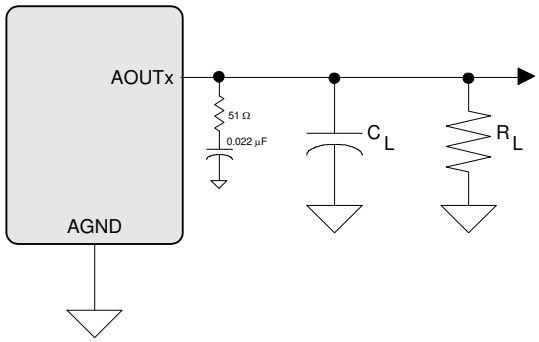


Figure 2. Headphone Output Test Load

LINE OUTPUT VOLTAGE LEVEL CHARACTERISTICS

Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; measurement bandwidth is 20 Hz to 20 kHz; Sample Frequency = 48 kHz; Test load R_L = 10 kΩ, C_L = 10 pF (see Figure 2); "Required Initialization Settings" on page 37 written on power up.

Parameters			VA = 2.5V			VA = 1.8V			Unit
			Min	Typ	Max	Min	Typ	Max	
AOUTx Voltage Into R_L = 10 kΩ									
HP_GAIN[2:0]	Analog Gain (G)	VHP							
000	0.3959	1.8 V	-	1.34	-	-	0.97	-	V_{pp}
		2.5 V	-	1.34	-	-	0.97	-	V_{pp}
001	0.4571	1.8 V	-	1.55	-	-	1.12	-	V_{pp}
		2.5 V	-	1.55	-	-	1.12	-	V_{pp}
010	0.5111	1.8 V	-	1.73	-	-	1.25	-	V_{pp}
		2.5 V	-	1.73	-	-	1.25	-	V_{pp}
011 (default)	0.6047	1.8 V	-	2.05	-	1.41	1.48	1.55	V_{pp}
		2.5 V	1.95	2.05	2.15	-	1.48	-	V_{pp}
100	0.7099	1.8 V	-	2.41	-	-	1.73	-	V_{pp}
		2.5 V	-	2.41	-	-	1.73	-	V_{pp}
101	0.8399	1.8 V	-	2.85	-		2.05		V_{pp}
		2.5 V	-	2.85	-	-	2.05	-	V_{pp}
110	1.0000	1.8 V	-	3.39	-	-	2.44	-	V_{pp}
		2.5 V	-	3.39	-	-	2.44	-	V_{pp}
111	1.1430	1.8 V	(See Note 11)			-	2.79	-	V_{pp}
		2.5 V	-	3.88	-	-	2.79	-	V_{pp}

COMBINED DAC INTERPOLATION AND ONCHIP ANALOG FILTER RESPONSE

Parameters (Note 12)		Min	Typ	Max	Unit
Frequency Response 10 Hz to 20 kHz		-0.01	-	+0.08	dB
Passband	to -0.05 dB corner	0	-	0.4780	Fs
	to -3 dB corner	0	-	0.4996	Fs
StopBand		0.5465	-	-	Fs
StopBand Attenuation (Note 13)		50	-	-	dB
Group Delay		-	9/Fs	-	s
De-emphasis Error	Fs = 32 kHz	-	-	+1.5/+0	dB
	Fs = 44.1 kHz	-	-	+0.05/-0.25	dB
	Fs = 48 kHz	-	-	-0.2/-0.4	dB

12. Response is clock dependent and scales with Fs. Note that the response plots (Figures 30 and 33 on page 78) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
13. Measurement Bandwidth is from Stopband to 3 Fs.

SWITCHING SPECIFICATIONS - SERIAL PORT

Inputs: Logic 0 = DGND, Logic 1 = VL, SDOUT C_{LOAD} = 15 pF.

Parameters		Symbol	Min	Max	Units
$\overline{\text{RESET}}$ pin Low Pulse Width (Note 14)			1	-	ms
MCLK Frequency (Note 15)			(See "Serial Port Clocking" on page 33)		MHz
MCLK Duty Cycle			45	55	%
Slave Mode					
Input Sample Rate (LRCK)		F_s	(See "Serial Port Clocking" on page 33)		kHz
LRCK Duty Cycle			45	55	%
SCLK Frequency		$1/t_P$	-	$64 \cdot F_s$	Hz
SCLK Duty Cycle			45	55	%
LRCK Setup Time Before SCLK Rising Edge		$t_{s(LK-SK)}$	40	-	ns
LRCK Edge to SDOUT MSB Output Delay		$t_{d(MSB)}$	-	52	ns
SDOUT Setup Time Before SCLK Rising Edge		$t_{s(SDO-SK)}$	20	-	ns
SDOUT Hold Time After SCLK Rising Edge		$t_{h(SK-SDO)}$	30	-	ns
SDIN Setup Time Before SCLK Rising Edge		$t_{s(SD-SK)}$	20	-	ns
SDIN Hold Time After SCLK Rising Edge		t_h	20	-	ns
Master Mode					
Output Sample Rate (LRCK)	All Speed Modes	F_s	(See "Serial Port Clocking" on page 33)		Hz
LRCK Duty Cycle			45	55	%
SCLK Frequency	SCLK=MCLK mode	$1/t_P$	-	12.0000	MHz
	MCLK=12.0000 MHz	$1/t_P$	-	$68 \cdot F_s$	Hz
	all other modes	$1/t_P$	-	$64 \cdot F_s$	Hz
SCLK Duty Cycle			45	55	%
LRCK Edge to SDOUT MSB Output Delay		$t_{d(MSB)}$	-	52	ns
SDOUT Setup Time Before SCLK Rising Edge		$t_{s(SDO-SK)}$	20	-	ns
SDOUT Hold Time After SCLK Rising Edge		$t_{h(SK-SDO)}$	30	-	ns
SDIN Setup Time Before SCLK Rising Edge		$t_{s(SD-SK)}$	20	-	ns
SDIN Hold Time After SCLK Rising Edge		t_h	20	-	ns

14. After powering up the CS42L52, $\overline{\text{RESET}}$ should be held low after the power supplies and clocks are settled.
15. See "Example System Clock Frequencies" on page 76 for typical MCLK frequencies.

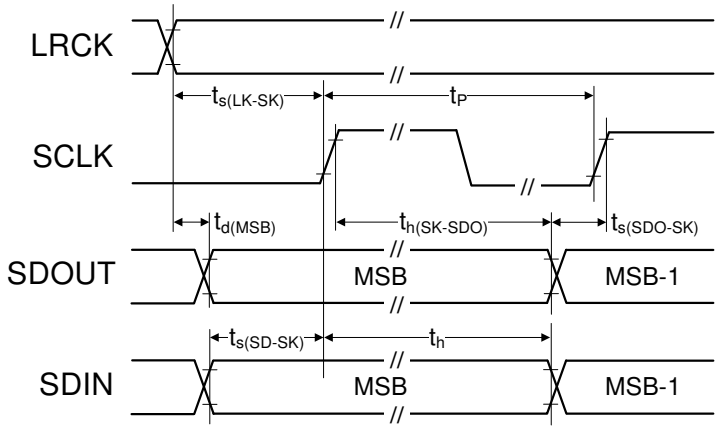


Figure 3. Serial Audio Interface Timing

SWITCHING SPECIFICATIONS - I²C CONTROL PORT

Inputs: Logic 0 = DGND, Logic 1 = VL, SDA C_L = 30 pF.

Parameters	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{\text{RESET}}$ Rising Edge to Start	t_{irs}	550	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 16)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}	-	1	µs
Fall Time SCL and SDA	t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	1000	ns

16. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

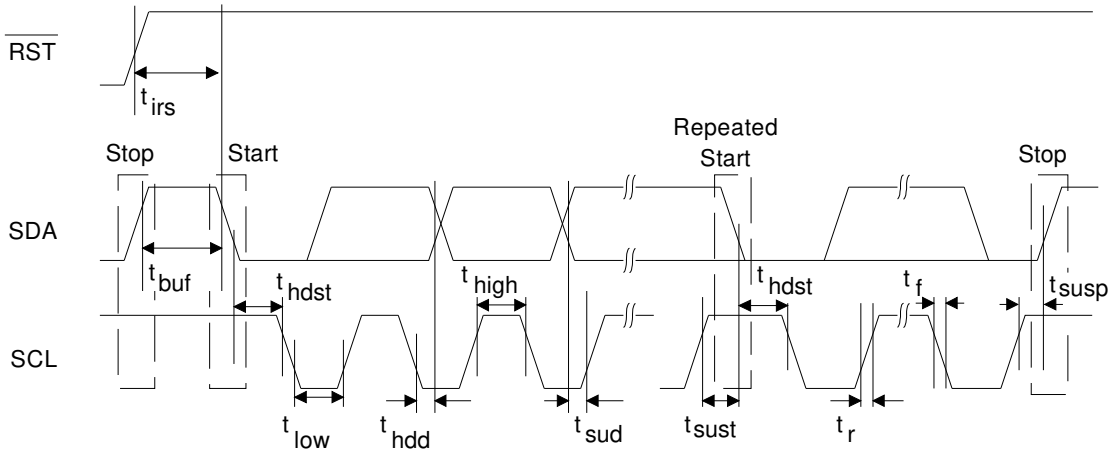


Figure 4. Control Port Timing - I²C

DC ELECTRICAL CHARACTERISTICS

AGND = 0 V; All voltages with respect to ground.

Parameters		Min	Typ	Max	Units
VQ Characteristics					
Nominal Voltage		-	0.5•VA	-	V
Output Impedance		-	23	-	kΩ
DC Current Source/Sink		-	-	1	µA
MIC BIAS Characteristics					
Nominal Voltage	BIASLVL[2:0] = 000	-	0.5•VA	-	V
	BIASLVL[2:0] = 001	-	0.6•VA	-	V
	BIASLVL[2:0] = 010	-	0.7•VA	-	V
	BIASLVL[2:0] = 011	-	0.8•VA	-	V
	BIASLVL[2:0] = 100	-	0.83•VA	-	V
	BIASLVL[2:0] = 101	-	0.91•VA	-	V
DC Output Current		-	-	1	mA
Power Supply Rejection Ratio (PSRR)	1 kHz	-	50	-	dB
Power Supply Rejection Ratio Characteristics					
PSRR @1 kHz (Note 17)	PGA to ADC	-	44	-	dB
	ADC	-	60	-	dB
	DAC (HP and Line Amps)	-	60	-	dB
PSRR @60 Hz (Note 17)	PGA to ADC(Note 18)	-	22	-	dB
	ADC	-	42	-	dB
	DAC (HP and Line Amps)	-	60	-	dB
PSRR @217 Hz	Full-Bridge PWM Outputs	-	56	-	dB

17. Valid with the recommended capacitor values on FILT+ and VQ. Increasing the capacitance will also increase the PSRR.
18. The PGA is biased with VQ, created from a resistor divider from the VA supply. Increasing the capacitance on VQ will also increase the PSRR at low frequencies. A 10 µF capacitor on VQ improves the PSRR to 42 dB.

DIGITAL INTERFACE SPECIFICATIONS AND CHARACTERISTICS

Parameters (Note 19)		Symbol	Min	Max	Units
Input Leakage Current		I_{in}	-	±10	µA
Input Capacitance			-	10	pF
1.8 V - 3.3 V Logic					
High-Level Output Voltage (I_{OH} = -100 µA)		V_{OH}	VL - 0.2	-	V
Low-Level Output Voltage (I_{OL} = 100 µA)		V_{OL}	-	0.2	V
High-Level Input Voltage	VL = 1.65 V	V_{IH}	0.85•VL	-	V
	VL = 1.8 V		0.77•VL	-	V
	VL = 2.0 V		0.68•VL	-	V
	VL > 2.0 V		0.65•VL	-	V
Low-Level Input Voltage		V_{IL}	-	0.30•VL	V

19. See "I/O Pin Characteristics" on page 10 for serial and control port power rails.

POWER CONSUMPTION See (Note 20).

	Operation	Power Ctl. Registers												V	Typical Current (mA)					Total Power (mW_{rms})
		02h					03h			04h					i_{VHP}	i_{VA}	i_{VD}	i_{VL} VL=3.3V (Note 23)	i_{VP} VP=3.7V	
		PDN_PGAB	PDN_PGAA	PDN_ADCB	PDN_ADCA	PDN	PDN_MICB	PDN_MICA	PDN_MICBIAS	PDN_HPB[1:0]		PDN_HPA[1:0]		PDN_SPKB[1:0]	PDN_SPKA[1:0]						
1	Off (Note 21)	x	x	x	x	x	x	x	x	x		x		x	x	1.8	0.00	0.00	0.00	0.00	0.00	**0.00**
																2.5	0.00	0.00	0.00			**0.00**
2	Standby (Note 22)	x	x	x	x	1	x	x	x	x		x		x	x	1.8	0.00	0.00	0.01	0.00	0.00	**0.02**
																2.5	0.00	0.00	0.02			**0.05**
3	Mono Record ADC	1	1	1	0	0	1	1	1	11		11		11	11	1.8	0.00	1.67	2.32	0.03	0.00	**7.24**
																2.5	0.00	1.87	3.72			**14.05**
	PGA to ADC	1	0	1	0	0	1	1	1	11		11		11	11	1.8	0.00	2.1	2.31	0.03	0.00	**7.99**
																2.5	0.00	2.3	3.72			**15.13**
	MIC to PGA to ADC (with Bias)	1	0	1	0	0	1	0	0	11		11		11	11	1.8	0.00	3.48	2.32	0.03	0.00	**10.49**
																2.5	0.00	3.71	3.72			**18.65**
	MIC to PGA to ADC (no Bias)	1	0	1	0	0	1	0	1	11		11		11	11	1.8	0.00	3.15	2.32	0.03	0.00	**9.90**
																2.5	0.00	3.37	3.73			**17.83**
4	Stereo Record ADC	1	1	0	0	0	1	1	1	11		11		11	11	1.8	0.00	2.31	2.37	0.03	0.00	**8.48**
																2.5	0.00	2.53	3.82			**15.95**
	PGA to ADC	0	0	0	0	0	1	1	1	11		11		11	11	1.8	0.00	3.18	2.37	0.03	0.00	**10.04**
																2.5	0.00	3.42	3.81			**18.15**
	MIC to PGA to ADC (no Bias)	0	0	0	0	0	0	0	1	11		11		11	11	1.8	0.00	5.32	2.37	0.03	0.00	**13.90**
																2.5	0.00	5.57	3.81			**23.53**
5	Mono Playback to Headphone	1	1	1	1	0	1	1	1	10		11		11	11	1.8	1.59	1.99	2.72	0.01	0.00	**11.36**
																2.5	2.07	2.62	4.27			**22.43**
6	Mono Playback to Speaker	1	1	1	1	0	1	1	1	11		11		10	10	1.8	0.00	0.20	4.42	0.01	1.00	**12.05**
																2.5	0.00	0.22	6.77			**21.21**
7	Stereo Playback to Headphone	1	1	1	1	0	1	1	1	10		10		11	11	1.8	2.77	2.00	2.91	0.01	0.00	**13.84**
																2.5	3.27	2.63	4.28			**25.48**
8	Stereo Playback to Speaker	1	1	1	1	0	1	1	1	11		11		10	10	1.8	0.00	0.20	4.38	0.01	1.00	**11.98**
																2.5	0.00	0.22	6.80			**21.28**
9	Stereo Passthrough to Headphone	1	1	1	1	0	1	1	1	10		10		11	11	1.8	2.79	1.91	1.06	0.01	0.00	**10.39**
																2.5	3.18	2.14	1.81			**17.85**
10	Mono Record and Playback PGA in (no MIC) to Mono HP	1	0	1	0	0	1	1	1	11		10		11	11	1.8	1.77	3.95	4.28	0.03	0.00	**18.05**
																2.5	2.13	4.77	6.63			**33.90**
11	Phone Monitor MIC (w/bias) in to Mono Out	1	0	1	0	0	1	0	0	11		10		11	11	1.8	1.76	5.33	4.28	0.03	0.00	**20.52**
																2.5	2.15	6.19	6.69			**37.65**
12	Stereo Record and Playback PGA in (no MIC) to St. HP Out	0	0	0	0	0	1	1	1	10		10		11	11	1.8	2.76	5.05	4.64	0.03	0.00	**22.46**
																2.5	3.21	5.90	7.17			**40.78**
13	Stereo Rec. and Full Playback PGA (no MIC) to St. HP and SPK	0	0	0	0	0	1	1	1	10		10		10	10	1.8	3.49	5.24	7.20	0.03	1.00	**32.47**
																2.5	3.95	6.10	10.46			**55.07**

20. Unless otherwise noted, test conditions are as follows: All zeros input, slave mode, sample rate = 48 kHz; No load. Digital (VD) and logic (VL) supply current will vary depending on speed mode and master/slave operation. "Required Initialization Settings" on page 37 written on power up.
21. $\overline{\text{RESET}}$ pin 25 held LO, all clocks and data lines are held LO.
22. $\overline{\text{RESET}}$ pin 25 held HI, all clocks and data lines are held HI.
23. VL current will slightly increase in master mode.

4. APPLICATIONS

4.1 Overview

4.1.1 Basic Architecture

The CS42L52 is a highly integrated, low-power, 24-bit audio CODEC comprised of a stereo analog-to-digital converter (ADC), a stereo digital-to-analog converter (DAC), a digital PWM modulator and two full-bridge power back-ends. The ADC and DAC are designed using multibit delta-sigma techniques - the DAC operates at an oversampling ratio of 128Fs and the ADC operates at 64Fs, where Fs is equal to the system sample rate.

The different clock rates maximize power savings while maintaining high performance. The PWM modulator operates at a fixed frequency of 384 kHz. The power FETs are configured for either stereo full-bridge or mono parallel full-bridge output. The CODEC operates in one of four sample rate speed modes: Quarter, Half, Single, and Double. It accepts and is capable of generating serial port clocks (SCLK, LRCK) derived from an input Master Clock (MCLK).

4.1.2 Line and MIC Inputs

The analog input portion of the CODEC allows selection from and configuration of multiple combinations of stereo and microphone (MIC) sources. Eight line inputs with an option for two balanced MIC inputs, a MIC bias output, and a Programmable Gain Amplifier (PGA) comprise the analog front-end.

4.1.3 Line and Headphone Outputs

The analog output portion of the CODEC includes a headphone amplifier capable of driving headphone and line-level loads. An on-chip charge pump creates a negative headphone supply allowing a full-scale output swing centered around ground. This eliminates the need for large DC-Blocking capacitors and allows the amplifier to deliver more power to headphone loads at lower supply voltages.

4.1.4 Speaker Driver Outputs

The Class D power amplifiers drive 8 ohm (stereo) and 4 ohm (mono) speakers directly, without the need for an external filter. The power MOSFETS are powered directly from a battery eliminating the efficiency loss associated with an external regulator. Battery level monitoring and compensation maintains a steady output as battery levels fall. **NOTE**: The CS42L52 should only be used in captive speaker systems where the outputs are permanently tied to the speaker terminals.

4.1.5 Fixed Function DSP Engine

The fixed-function digital signal processing engine processes both the PCM serial input data and ADC output data, allowing a mix between the two. Independent volume control, left/right channel swaps, mono mixes, tone control, and limiting functions also comprise the DSP engine.

4.1.6 Beep Generator

The beep generator delivers tones at select frequencies across approximately two octave major scales. With independent volume control, beeps may be configured to occur continuously, periodically, or at single time intervals.

4.1.7 Power Management

Three control registers provide independent power-down control of the ADC, DAC, PGA, MIC pre-amp, MIC bias, Headphone, and Speaker outputs, allowing operation in select applications with minimal power consumption.

4.2 Analog Inputs

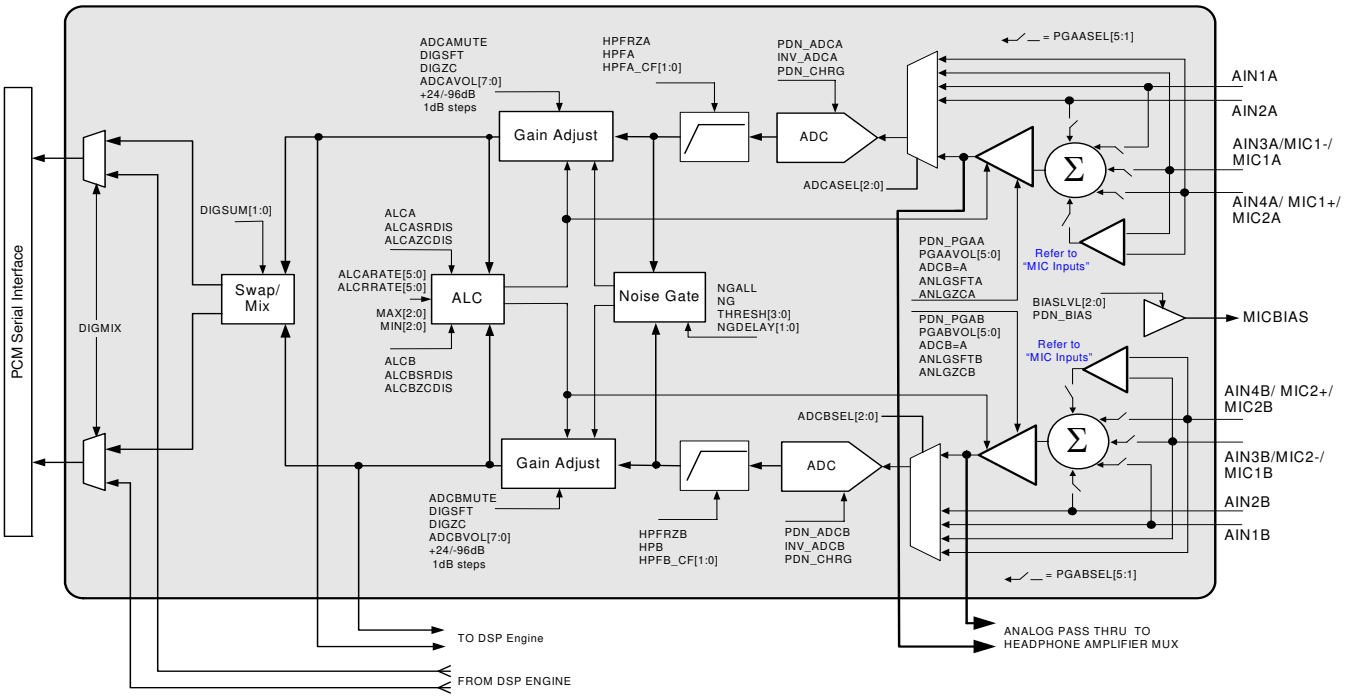


Figure 5. Analog Input Signal Flow

Referenced Control	Register Location
Analog Front End	
PDN_PGAx	"Power Down PGAx" on page 42
PGAxVOL[5:0]	"PGAx Volume" on page 56
ADCB=A	"Analog Front-End Volume Setting B=A" on page 50
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