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CS42L55

Ultra Low Power, Stereo CODEC w/Class H Headphone Amp

DIGITAL to ANALOG FEATURES

- 5 mW Stereo Playback Power Consumption
- 99 dB Dynamic Range (A-wtd)
- -86 dB THD+N
- Digital Signal Processing Engine
  - Bass & Treble Tone Control, De-Emphasis
  - Master Volume Control (+12 to -102 dB in 0.5 dB steps)
  - Soft-Ramp & Zero-Cross Transitions
  - Programmable Peak-Detect and Limiter
  - Beep Generator w/Full Tone Control

Stereo Headphone and Line Amplifiers

- Step-Down/Inverting Charge Pump
- Class H Amplifier - Automatic Supply Adj.
  - High Efficiency
  - Low EMI
- Pseudo-Differential Ground-Centered Outputs
- High HP Power Output at -75 dB THD+N
  - 2 x 20 mW Into 32 Ω @1.8 V
  - 2 x 20 mW Into 16 Ω @1.8 V
- 1 V_{RMS} Line Output @1.8 V
- Analog Vol. Ctl. (+12 to -55 dB in 1 dB steps)
- Analog In to Analog Out Passthrough
- Pop and Click Suppression

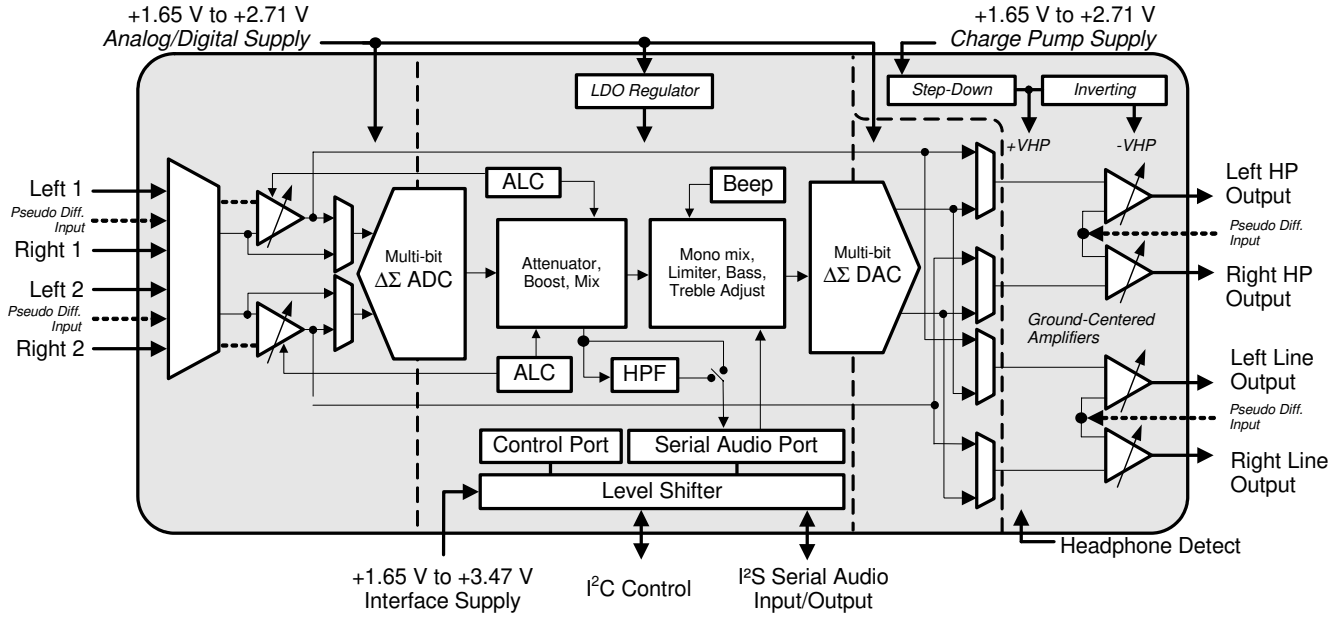
ANALOG to DIGITAL FEATURES

- 3.5 mW Stereo Record Power Consumption
- 95 dB Dynamic Range (A-wtd)
- -87 dB THD+N
- 2:1 Stereo Input MUX
- Analog Programmable Gain Amplifier (PGA) (+12 to -6 dB in 0.5 dB steps)
- +20 dB Boost
- Programmable Automatic Level Control (ALC)
  - Noise Gate for Noise Suppression
  - Programmable Threshold & Attack/Release Rates
- Independent ADC Channel Control
- Digital Vol. Ctl. (0 to -96 dB in 1 dB steps)
- High-Pass Filter Disable for DC Measurements
- Pseudo Differential Inputs

SYSTEM FEATURES

- 12 MHz USB Master Clock Input
- Low Power Operation
  - Stereo Anlg. Passthrough: 3.3 mW @1.8 V
  - Stereo Rec. and Playback: 8.3 mW @1.8 V
- Headphone Detect Input

(SYSTEM FEATURES continued on page 2)



SYSTEM FEATURES

- High Performance 24-bit Converters
  - Multi-bit Delta Sigma Architecture
- Integrated High Efficient Power Management Reduces Power Consumption
  - Step-Down Charge Pump Improves Efficiency
  - Inverting Charge Pump Accommodates Low System Voltage by Providing Negative Rail for HP/Line Amp
  - LDO Reg. Provides Low Digital Supply Voltage
- Digital Power Reduction
  - Very Low Oversampling Rate for Converters
  - Bursted Serial Clock Providing 24 Bits per Sample
- Power Down Management
  - ADC, DAC, CODEC, PGA, DSP
- Analog & Digital Routing/Mixes
  - Line/Headphone Out = Analog In (ADC Bypassed)
  - Line/Headphone Out = ADC Out
  - Internal Digital Loopback
  - Mono Mixes
- I²C® Control Port
- I²S Digital Interface Format
- Flexible Clocking Options
  - Master or Slave Operation
  - High-Impedance Digital Output Select *(used for easy MUXing between CODEC and other data sources)*
  - 8.000, 11.029, 12.000, 16.000, 22.059, 24.000, 32.000, 44.118 and 48.000 kHz Sample Rates

APPLICATIONS

- HDD & Flash-Based Portable Audio Players
- MD Players/Recorders
- PDAs
- Personal Media Players
- Portable Game Consoles
- Digital Voice Recorders
- Digital Camcorders
- Digital Cameras
- Smart Phones

GENERAL DESCRIPTION

The CS42L55 is a highly integrated, 24-bit, ultra-low power stereo CODEC based on multi-bit delta-sigma modulation. Both the ADC and DAC offer many features suitable for low power portable system applications.

The **analog input path** allows independent channel control of a variety of features. The Programmable Gain Amplifier (PGA) provides analog gain with zero cross transitions. The ADC path includes a digital volume attenuator with soft ramp transitions and a programmable ALC and noise gate monitor the input signals and adjust the volume appropriately. An **analog passthrough** also exists, accommodating a lower noise, lower power analog in to analog out path to the headphone and line amplifiers, bypassing the ADC and DAC.

The **DAC output path** includes a fixed-function digital signal processing engine. Tone control provides bass and treble adjustment at four selectable corner frequencies. The digital mixer provides independent volume control for both the ADC output and PCM input signal paths, as well as a master volume control. Digital volume controls may be configured to change on soft ramp transitions while the analog controls can be configured to occur on every zero crossing. The DAC path also includes de-emphasis, limiting functions and a beep generator delivering tones selectable across a range of two full octaves.

The Class H stereo headphone amplifier combines the efficiency of an integrated **step-down and inverting charge pump** with the linearity and low EMI of a Class AB amplifier. A step-down/inverting charge pump operates in two modes: +/-VCP mode or +/-(VCP/2) mode. Based on the amplifier's output signal, internal logic automatically adjusts the output of the charge pump, +VHPFILT and –VHPFILT, to optimize efficiency. With these features, the amplifier delivers a ground-centered output with a large signal swing even at low voltages and eliminates the need for external DC-blocking capacitors.

These features make the CS42L55 the ideal solution for portable applications that require extremely low power consumption in a minimal amount of space.

The CS42L55 is available in a 36-pin QFN package for the Commercial (-40°C to +85°C) grade. The CDB42L55 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please see "Ordering Information" on page 73 for complete details.

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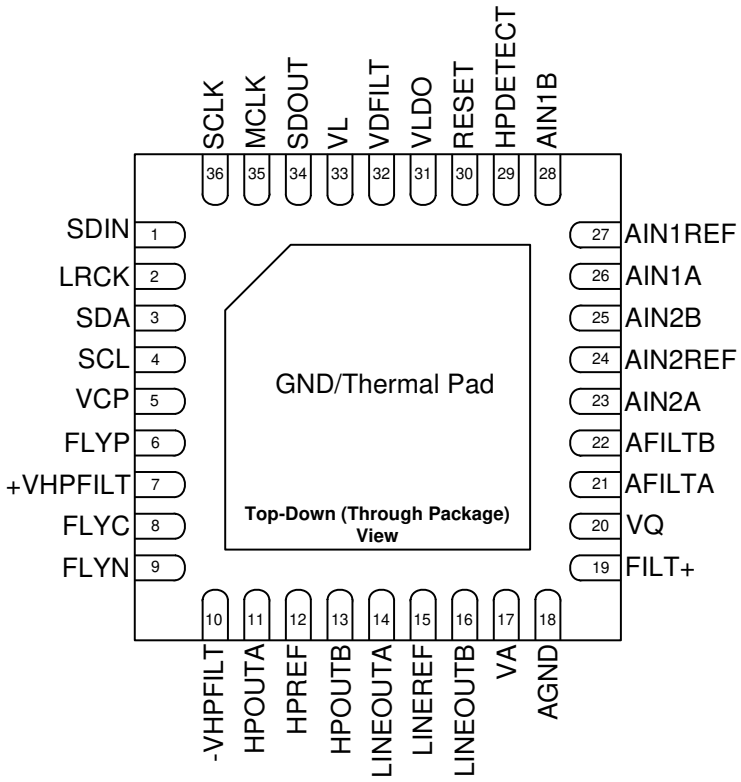
1. PIN DESCRIPTIONS



Pin Name	#	Pin Description
SDIN	1	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
LRCK	2	**Left Right Clock** *(Input/Output)* - Determines which channel, Left or Right, is currently active on the serial audio data lines.
SDA	3	**Serial Control Data** (*Input*/*Output*) - Serial data for the I²C serial control port.
SCL	4	**Serial Control Port Clock** (*Input*) - Serial clock for the I²C serial control port.
VCP	5	**Step-Down Charge Pump Power** *(Input)* - Power supply for the step-down charge pump.
FLYP	6	**Charge Pump Cap Positive Node** *(Output)* - Positive node for the step-down charge pump's flying capacitor.
+VHPFILT	7	**Step-Down Charge Pump Filter Connection** *(Output)* - Power supply from the step-down charge pump that provides the positive rail for the headphone and line amplifiers
FLYC	8	**Charge Pump Cap Common Node** *(Output)* - Common positive node for the step-down and inverting charge pumps' flying capacitors.
FLYN	9	**Charge Pump Cap Negative Node** *(Output)* - Negative node for the inverting charge pump's flying capacitor.
-VHPFILT	10	**Inverting Charge Pump Filter Connection** *(Output)* - Power supply from the inverting charge pump that provides the negative rail for the headphone and line amplifiers.
HPOUTA HPOUTB	11 13	**Headphone Audio Output** (*Output*) - The full-scale output level is specified in the HP Output Characteristics specification table
HPREF	12	**Pseudo Diff. Headphone Output Reference** (*Input*) - Ground reference for the headphone amplifiers
LINEOUTA LINEOUTB	14 16	**Line Audio Output** (*Output*) - The full-scale output level is specified in the Line Output Characteristics specification table
LINEREF	15	**Pseudo Diff. Line Output Reference** (*Input*) - Ground reference for the line amplifiers.

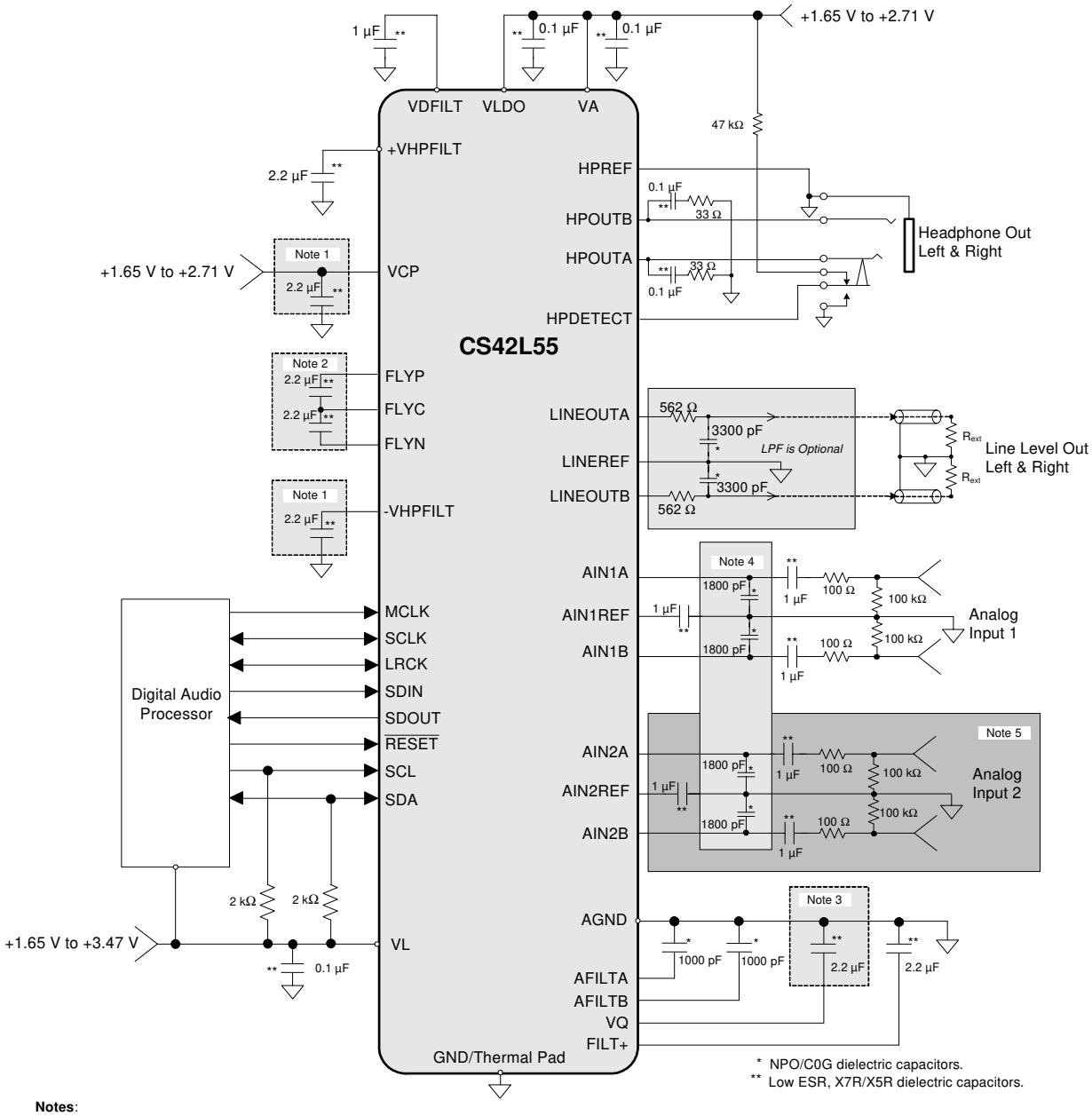
VA	17	**Analog Power** *(Input)* - Power supply for the internal analog section.
AGND	18	**Analog Ground** (*Input*) - Ground reference for the internal analog section.
FILT+	19	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.
VQ	20	**Quiescent Voltage** (*Output*) **-** Filter connection for the internal quiescent voltage.
AFILTA AFILTB	21 22	**Antialias Filter Connection** (*Output*) - Antialias filter connection for the ADC inputs.
AIN2A AIN2B AIN1A AIN1B	23 25 26 28	**Analog Input** (*Input*) **-** The full-scale level is specified in the Analog Input Characteristics specification table.
AIN2REF AIN1REF	24 27	**Pseudo Diff. Analog Input Reference** (*Input*) - Ground reference for the programmable gain amplifiers (PGA).
HPDETECT	29	**Headphone Detect** (*Input*) - Powers down the left and/or right channel of the line and/or headphone outputs as described in "Headphone Power Control" on page 43 and "Line Power Control" on page 43.
$\overline{\text{RESET}}$	30	**Reset** (*Input*) - The device enters a low power mode when this pin is driven low.
VLDO	31	**Low Dropout Regulator (LDO) Power** *(Input)* - Power supply for the LDO regulator.
VDFILT	32	**Low Dropout Regulator (LDO) Filter Connection** *(Output)* - Power supply from the LDO regulator that provides the low voltage power to the digital section.
VL	33	**Digital Interface Power** (*Input*) - Determines the required signal level for the serial audio interface and I²C control port.
SDOUT	34	**Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data.
MCLK	35	**Master Clock** (*Input*) - Clock source for the delta-sigma modulators.
SCLK	36	**Serial Clock** *(Input/Output)* **-** Serial clock for the serial audio interface.
GND/ Thermal Pad	-	Ground reference for the internal charge pump and digital section; thermal relief pad. See "QFN Thermal Pad" on page 68 for more information.

1.1 I/O Pin Characteristics

Input and output levels and associated power supply voltage are shown in the table below. Logic levels should not exceed the corresponding power supply voltage.

Power Supply	Pin Name	I/O	Internal Connections	Driver	Receiver
VL	$\overline{\text{RESET}}$	Input	-	-	1.8 V - 3.3 V, with Hysteresis
	SCL	Input	-	-	1.8 V - 3.3 V, with Hysteresis
	SDA	Input/Output	-	CMOS/Open Drain	1.8 V - 3.3 V, with Hysteresis
	MCLK	Input	-	-	1.8 V - 3.3 V
	LRCK	Input/Output	Weak Pull-up (~1 MΩ)	1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V
	SCLK	Input/Output	Weak Pull-up (~1 MΩ)	1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V
	SDOUT	Output	-	1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V
	SDIN	Input	-	-	1.8 V - 3.3 V
VA	HPDETECT	Input	-	-	1.8 V - 2.5 V, with Hysteresis

2. TYPICAL CONNECTION DIAGRAM



Notes:
1. The headphone amplifier's output power and distortion are rated using the nominal capacitance shown. Larger capacitance reduces the ripple on the internal amplifiers' supplies and in turn reduces the amplifier's distortion at high output power levels. Smaller capacitance may not sufficiently reduce ripple to achieve the rated output power and distortion. Since the actual value of typical X7R/X5R ceramic capacitors deviates from the nominal value by a percentage specified in the manufacturer's data sheet, capacitors should be selected based on the minimum output power and maximum distortion required.
2. The headphone amplifier's output power and distortion are rated using the nominal capacitance shown and using the default charge pump switching frequency. The required capacitance follows an inverse relationship with the charge pump's switching frequency. When increasing the switching frequency, the capacitance may decrease; when lowering the switching frequency, the capacitance must increase. Since the actual value of typical X7R/X5R ceramic capacitors deviates from the nominal value by a percentage specified in the manufacturer's data sheet, capacitors should be selected based on the minimum output power, maximum distortion and maximum charge pump switching frequency required.
3. Additional bulk capacitance may be added to improve PSRR at low frequencies.
4. These capacitors serve as a charge reservoir for the internal switched capacitor ADC modulators and should be placed as close as possible to the inputs. They are only needed when the PGA (Programmable Gain Amplifier) is bypassed.
5. Input pairs (such as AIN2A, AIN2REF and AIN2B) may be left floating if they are not used.

Figure 1. Typical Connection Diagram

3. CHARACTERISTIC AND SPECIFICATION TABLES

RECOMMENDED OPERATING CONDITIONS

GND = AGND = 0 V, all voltages with respect to ground.

Parameters		Symbol	Min	Max	Units
DC Power Supply					
Analog		VA	1.65	2.71	V
Charge Pump		VCP	1.65	VA	V
LDO Regulator for Digital		VLDO	1.65	2.71	V
Serial/Control Port Interface		VL	1.65	3.47	V
Ambient Temperature	Commercial - CNZ	T_A	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS

GND = AGND = 0 V; all voltages with respect to ground.

Parameters		Symbol	Min	Max	Units
DC Power Supply	Analog, Charge Pump, LDO	VA, VCP, VLDO	-0.3	3.0	V
	Serial/Control Port Interface	VL	-0.3	4.0	V
Input Current	(Note 2)	I_{in}	-	±10	mA
Analog Input Voltage	(Note 3)	V_{IN}	AGND-0.7	VA+0.7	V
Digital Input Voltage	(Note 3)	V_{IND}	-0.3	VL+0.4	V
Ambient Operating Temperature (power applied)		T_A	-50	+115	°C
Storage Temperature		T_{stg}	-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:

1. Due to the existence of parasitic body diodes between VCP and VA, current flows from VCP to VA whenever the VA power supply is lower than VCP. This causes a “back-powering” effect on the VA power supply rails internal to the part. Hence VA should be maintained at an equal or greater voltage than VCP at all times. While “back-powering” does not have any adverse effects on device operation with respect to performance and reliability, it does lead to extra power consumption and therefore should be avoided.
2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.
3. The maximum over/under voltage is limited by the input current.

ANALOG INPUT CHARACTERISTICS

Test Conditions (unless otherwise specified): Connections to the CS42L55 are shown in the Figure 1. "Typical Connection Diagram" on page 10; Input is a 1 kHz sine wave through the passive input filter, PGA = 0 dB; All Supplies = VA; GND = AGND = 0 V; T_A = +25°C; Measurement bandwidth is 20 Hz to 20 kHz. Sample Frequency = 48 kHz.

Parameter (Note 4)		VA = 2.5 V Min	VA = 2.5 V Typ	VA = 2.5 V Max	VA = 1.8 V Min	VA = 1.8 V Typ	VA = 1.8 V Max	Unit
Analog In to ADC (PGA bypassed)								
Dynamic Range	A-weighted	89	95	-	86	92	-	dB
	unweighted	86	92	-	83	89	-	dB
Total Harmonic Distortion + Noise	-1 dBFS	-	-85	-79	-	-85	-79	dB
	-20 dBFS	-	-72	-	-	-69	-	dB
	-60 dBFS	-	-32	-26	-	-29	-23	dB
Analog In to PGA to ADC								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	88	94	-	85	91	-	dB
	unweighted	85	91	-	82	88	-	dB
PGA Setting: +12 dB	A-weighted	81	87	-	78	84	-	dB
	unweighted	78	84	-	75	81	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-1 dBFS	-	-87	-81	-	-85	-79	dB
	-60 dBFS	-	-31	-25	-	-28	-22	dB
PGA Setting: +12 dB	-1 dBFS	-	-83	-77	-	-81	-75	dB
Common Mode Rejection (Note 5)		-	40	-	-	40	-	dB
DC Accuracy								
Interchannel Gain Mismatch		-	0.2	-	-	0.2	-	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Offset Error	(Note 6)	-	352	-	-	352	-	LSB
Input								
Interchannel Isolation (1 kHz)		-	90	-	-	90	-	dB
HP Amp to Analog Input Isolation	R_L = 10 kΩ	-	90	-	-	90	-	dB
	R_L = 16 Ω	-	83	-	-	83	-	dB
Full-scale Input Voltage	ADC	0.76•VA	0.80•VA	0.84•VA	0.76•VA	0.80•VA	0.84•VA	Vpp
	PGA (0 dB)	0.78•VA	0.82•VA	0.86•VA	0.78•VA	0.82•VA	0.86•VA	Vpp
	PGA (+12 dB)		0.198•VA			0.198•VA		Vpp
Input Impedance (Note 7)	ADC	-	60	-	-	60	-	kΩ
	PGA	-	40	-	-	40	-	kΩ

4. Referred to the typical full-scale voltage. Applies to all THD+N and Dynamic Range values in the table.
5. See test figure shown below.
6. SDOUT Code with HPFx=1;HPFRZx=0.
7. Measured between AINxx and AGND.

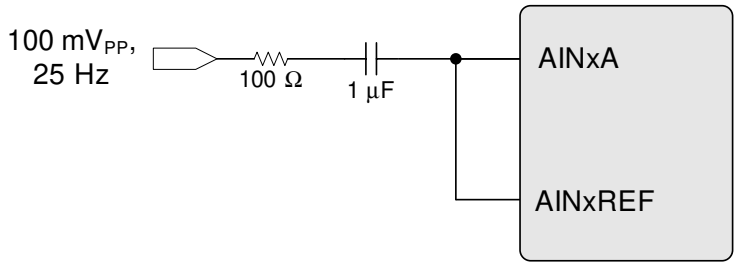


Figure 2. CMRR Test Configuration

ADC DIGITAL FILTER CHARACTERISTICS

Parameter (Note 8)		Min	Typ	Max	Unit
Frequency Response (20 Hz to 20 kHz)		-0.07	-	+0.02	dB
Passband	to -0.05 dB corner	-	0.421	-	Fs
	to -3 dB corner	-	0.495	-	Fs
Stopband		0.52	-	-	Fs
Stopband Attenuation		33	-	-	dB
Total Group Delay		-	7.6/Fs	-	s
High-Pass Filter Characteristics (48 kHz Fs) (Note 9)					
Passband	to -3.0 dB corner	-	1.87	-	Hz
	to -0.05 dB corner	-	17.15	-	Hz
Passband Ripple		-	-	0.15	dB
Phase Deviation	@ 20 Hz	-	5.3	-	Deg
Filter Settling Time (Note 10)		-	10^5/Fs	-	s

Notes:

8. Response is clock-dependent and will scale with Fs. Note that the response plots (Figures 27 to 30 on page 70) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs. HPF parameters are for Fs = 48 kHz.
9. Characteristics are based on the default setting in register "HPF Control (Address 09h)" on page 47.
10. Settling time decreases at higher corner frequency settings.

HP OUTPUT CHARACTERISTICS

Test conditions (unless otherwise specified): Connections to the CS42L55 are shown in the "Typical Connection Diagram" on page 10; Input test signal is a full-scale 997 Hz sine wave; All Supplies = VA, VCP Mode; GND = AGND = 0 V; T_A = +25°C; Measurement bandwidth is 20 Hz to 20 kHz; Sample Frequency = 48 kHz; Test load R_L = 3 kΩ, C_L = 150 pF for a Line Load, and test load R_L = 16 Ω, C_L = 150 pF for a headphone load. (See Figure 3 on page 15).

Parameter (Note 11)		VA = 2.5 V Min	VA = 2.5 V Typ	VA = 2.5 V Max	VA = 1.8 V Min	VA = 1.8 V Typ	VA = 1.8 V Max	Unit
Line Load R_L = 3 kΩ (+2 dB Analog Gain) (Note 12)								
Dynamic Range								
18 to 24-Bit	A-weighted	92	98	-	90	96	-	dB
	unweighted	89	95	-	87	93	-	dB
16-Bit	A-weighted	-	96	-	-	94	-	dB
	unweighted	-	93	-	-	91	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-84	-78	-	-85	-79	dB
	-20 dB	-	-76	-	-	-74	-	dB
	-60 dB	-	-36	-30	-	-34	-28	dB
16-Bit	0 dB	-	-82	-	-	-83	-	dB
	-20 dB	-	-74	-	-	-72	-	dB
	-60 dB	-	-34	-	-	-32	-	dB
Full-scale Output Voltage (Note 13)		1.56•VA	1.64•VA	1.73•VA	1.56•VA	1.64•VA	1.73•VA	V_{PP}
HP Load R_L = 16 Ω (-4 dB Analog Gain) (Note 12)								
Dynamic Range								
18 to 24-Bit	A-weighted	89	95	-	88	94	-	dB
	unweighted	86	92	-	85	91	-	dB
16-Bit	A-weighted	-	93	-	-	92	-	dB
	unweighted	-	90	-	-	89	-	dB
Total Harmonic Distortion + Noise		-	-75	-69	-	-75	-69	dB
Full-scale Output Voltage		0.76•VA	0.82•VA	0.88•VA	0.76•VA	0.82•VA	0.88•VA	V_{PP}
Output Power (Note 13)		-	32	-	-	17	-	mW
Other Characteristics for R_L = 16 Ω or 3 kΩ								
Interchannel Isolation	3 kΩ	-	90	-	-	90	-	dB
	16 Ω	-	90	-	-	90	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Output Offset Voltage (Note 14)	DAC to HPOUT	-	0.5	1.0	-	0.5	1.0	mV
Gain Drift		-	±100	-	-	±100	-	ppm/°C
AC-Load Resistance (R_L)	(Note 14)	16	-	-	16	-	-	Ω
Load Capacitance (C_L)	(Note 14)	-	-	150	-	-	150	pF

LINE OUTPUT CHARACTERISTICS

Test conditions (unless otherwise specified): Connections to the CS42L55 are shown in the "Typical Connection Diagram" on page 10; Input test signal is a full-scale 997 Hz sine wave; All Supplies = VA, VCP Mode; GND = AGND = 0 V; T_A = +25 °C; Measurement bandwidth is 20 Hz to 20 kHz; Sample Frequency = 48 kHz; Test load R_L = 3 kΩ, C_L = 150 pF (see Figure 3 on page 15).

Parameter (Note 11)		VA = 2.5 V Min	VA = 2.5 V Typ	VA = 2.5 V Max	VA = 1.8 V Min	VA = 1.8 V Typ	VA = 1.8 V Max	Unit
(+2 dB Analog Gain) (Note 12)								
Dynamic Range								
18 to 24-Bit	A-weighted	93	99	-	91	97	-	dB
	unweighted	90	96	-	88	94	-	dB
16-Bit	A-weighted	-	96	-	-	94	-	dB
	unweighted	-	93	-	-	91	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-84	-78	-	-86	-80	dB
	-20 dB	-	-76	-	-	-74	-	dB
	-60 dB	-	-36	-30	-	-34	-28	dB
16-Bit	0 dB	-	-82	-	-	-84	-	dB
	-20 dB	-	-74	-	-	-72	-	dB
	-60 dB	-	-34	-	-	-32	-	dB
Full-scale Output Voltage (Note 13)		1.50•VA	1.58•VA	1.66•VA	1.50•VA	1.58•VA	1.66•VA	V_{PP}
Other Characteristics								
Interchannel Isolation		-	90	-	-	90	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Output Offset Voltage (Note 14)	DAC to LINEOUT	-	0.5	1.0	-	0.2	1.0	mV
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Output Impedance		-	100	-	-	100	-	Ω
AC-Load Resistance (R_L)	(Note 14)	3	-	-	3	-	-	kΩ
Load Capacitance (C_L)	(Note 14)	-	-	150	-	-	150	pF

Notes:

11. One-half LSB of triangular PDF dither is added to data.
12. The Analog Gain setting (refer to "Headphone Volume Control" on page 57 or "Line Volume Control" on page 58) must be configured as indicated to achieve the specified output characteristics. High gain settings at certain VA and VCP supply levels may cause clipping when the audio signal approaches full-scale, maximum power output.
13. VCP settings lower than VA reduces the headroom of the headphone amplifier. As a result, the specified THD+N performance at full-scale output voltage and power may not be achieved.
14. See Figure 3 and Figure 4 on page 15. Refer to "Parameter Definitions" on page 71.

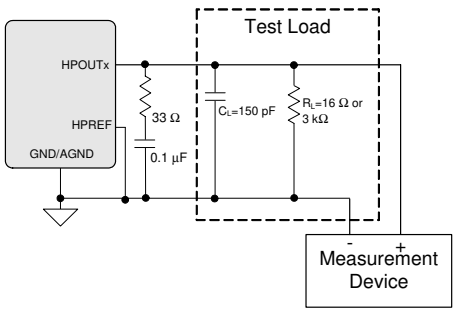


Figure 3. HP Output Test Configuration

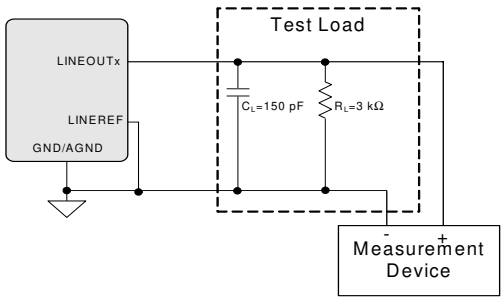


Figure 4. Line Output Test Configuration

ANALOG PASSTHROUGH CHARACTERISTICS

Test Conditions (unless otherwise specified): Connections to the CS42L55 are shown in the "Typical Connection Diagram" on page 10; Input is a 1 kHz sine wave through the passive input filter shown in Figure 1, PGA and HP/Line gain = 0 dB; All Supplies = VA, VCP Mode; GND = AGND = 0 V; T_A = +25 °C; Measurement bandwidth is 20 Hz to 20 kHz. Sample Frequency = 48 kHz.

Parameter		VA = 2.5 V Min	VA = 2.5 V Typ	VA = 2.5 V Max	VA = 1.8 V Min	VA = 1.8 V Typ	VA = 1.8 V Max	Unit
Analog In to HP Amp (ADC is powered down)								
R_L = 3 kΩ (+2 dB Output Analog Gain)(Note 12)								
Dynamic Range	A-weighted	-	94	-	-	91	-	dB
	unweighted	-	91	-	-	88	-	dB
Total Harmonic Distortion + Noise	-1 dB	-	-70	-	-	-80	-	dB
	-20 dB	-	-71	-	-	-68	-	dB
	-60 dB	-	-31	-	-	-28	-	dB
Full-scale Input Voltage		-	0.80•VA	-	-	0.80•VA	-	Vpp
Full-scale Output Voltage		-	0.93•VA	-	-	0.93•VA	-	Vpp
Passband Ripple			0/-0.3			0/-0.3		dB
R_L = 16 Ω (-4 dB Output Analog Gain)(Note 12)								
Dynamic Range	A-weighted	-	94	-	-	91	-	dB
	unweighted	-	91	-	-	88	-	dB
Total Harmonic Distortion + Noise	-1 dB	-	-70	-	-	-80	-	dB
	-20 dB	-	-71	-	-	-68	-	dB
	-60 dB	-	-31	-	-	-28	-	dB
Full-scale Input Voltage		-	0.80•VA	-	-	0.80•VA	-	Vpp
Output Power (Note 13)		-	12	-	-	6.5	-	mW
Passband Ripple		-	0/-0.3	-	-	0/-0.3	-	dB
Analog In to Line Amp (ADC is powered down)								
R_L = 3 kΩ (+2 dB Output Analog Gain) (Note 12)								
Dynamic Range	A-weighted	-	94	-	-	91	-	dB
	unweighted	-	91	-	-	88	-	dB
Total Harmonic Distortion + Noise	-1 dB	-	-70	-	-	-80	-	dB
	-20 dB	-	-71	-	-	-68	-	dB
	-60 dB	-	-31	-	-	-28	-	dB
Full-scale Input Voltage		-	0.80•VA	-	-	0.80•VA	-	Vpp
Full-scale Output Voltage		-	0.89•VA	-	-	0.89•VA	-	Vpp
Passband Ripple			0/-0.3			0/-0.3		dB

COMBINED DAC INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

Parameter (Note 15)		Min	Typ	Max	Unit
Frequency Response 20 Hz to 20 kHz	Fs = 48.000 kHz	-0.04	-	+0.04	dB
	Fs = 44.118 kHz	-0.14	-	+0.14	dB
Passband	to -0.05 dB corner	-	0.48	-	Fs
	to -3 dB corner	-	0.49	-	Fs
Stopband		0.55	-	-	Fs
Stopband Attenuation (Note 16)		49	-	-	dB
Total Group Delay		-	9/Fs	-	s
De-emphasis Error	Fs = 44.118 kHz	-	-	+0.05/-0.25	dB

Notes:

15. Response is clock dependent and will scale with Fs. Note that the response plots (Figures 31 to 34 on page 70) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
16. Measurement bandwidth is from Stopband to 3 Fs.

SWITCHING SPECIFICATIONS - SERIAL PORT

Inputs: Logic 0 = GND = AGND, Logic 1 = VL, LRCK, SCLK, SDOUT C_{LOAD} = 15 pF.

Parameters		Symbol	Min	Max	Units
$\overline{\text{RESET}}$ pin Low Pulse Width (Note 17)			1	-	ms
MCLK Frequency			(See "Serial Port Clocking" on page 34)		MHz
MCLK Duty Cycle			45	55	%
Slave Mode (Figure 5)					
Input Sample Rate (LRCK)		F_s	(See "Serial Port Clocking" on page 34)		kHz
LRCK Duty Cycle			45	55	%
SCLK Frequency		$1/t_{Ps}$	-	$68 \cdot F_s$	Hz
SCLK Duty Cycle			45	55	%
LRCK Setup Time Before SCLK Rising Edge		$t_{ss(LK-SK)}$	40	-	ns
SDOUT Setup Time Before SCLK Rising Edge		$t_{ss(SDO-SK)}$	20	-	ns
SDOUT Hold Time After SCLK Rising Edge		$t_{hs(SK-SDO)}$	30	-	ns
SDIN Setup Time Before SCLK Rising Edge		$t_{ss(SD-SK)}$	20	-	ns
SDIN Hold Time After SCLK Rising Edge		t_{hs}	20	-	ns
Master Mode (Figure 6)					
Output Sample Rate (LRCK)	All Speed Modes	F_s	(See "Serial Port Clocking" on page 34)		Hz
LRCK Duty Cycle			45	55	%
SCLK Frequency	SCLK = MCLK mode	$1/t_{Pm}$	-	12.0000	MHz
	All Other Modes	$1/t_{Pm}$	-	$68 \cdot F_s$	Hz
SCLK Duty Cycle	RATIO[1:0] = '11'		45	55	%
	RATIO[1:0] = '01' (Note 18)		33	66	%
LRCK Time Before SCLK Falling Edge		$t_{sm(LK-SK)}$	-	±2	ns
SDOUT Setup Time Before SCLK Rising Edge		$t_{sm(SDO-SK)}$	20	-	ns
SDOUT Hold Time After SCLK Rising Edge		$t_{hm(SK-SDO)}$	30	-	ns
SDIN Setup Time Before SCLK Rising Edge		$t_{sm(SD-SK)}$	20	-	ns
SDIN Hold Time After SCLK Rising Edge		t_{hm}	20	-	ns

Notes: 17. After powering up the CS42L55, $\overline{\text{RESET}}$ should be held low after the power supplies and clocks are settled. This specification is valid with the recommended capacitor on VDFILT.

18. The device will periodically extend the SCLK high time to compensate for the fractional MCLK/SCLK ratio.

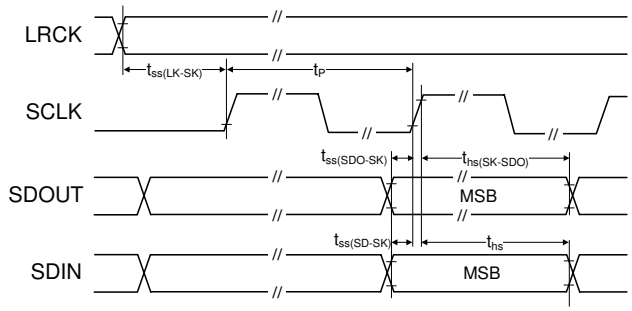


Figure 5. Serial Port Timing (Slave Mode)

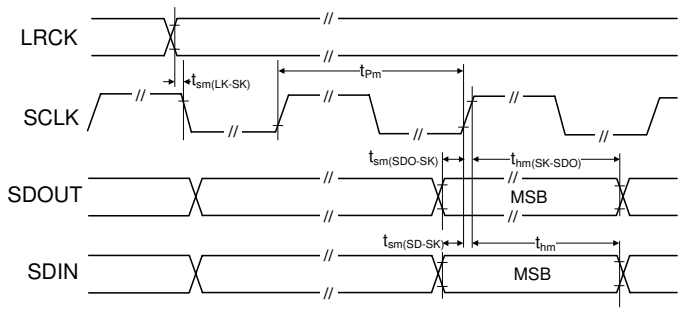


Figure 6. Serial Port Timing (Master Mode)

SWITCHING SPECIFICATIONS - CONTROL PORT

Inputs: Logic 0 = GND = AGND, Logic 1 = VL, SDA C_L = 30 pF.

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{\text{RESET}}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 19)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}	-	1	µs
Fall Time SCL and SDA	t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	1000	ns

Notes:

19. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

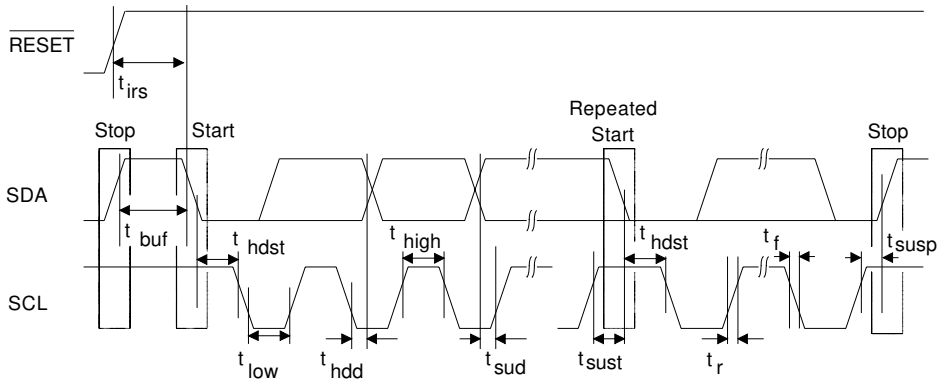


Figure 7. I²C Control Port Timing

POWER SUPPLY REJECTION (PSRR) CHARACTERISTICS

Test Conditions (unless otherwise specified): Connections to the CS42L55 are shown in the "Typical Connection Diagram" on page 10; GND = AGND = 0 V; all voltages with respect to ground.

Parameters		Min	Typ	Max	Units
PSRR with 100 mVpp, 1 kHz signal (Note 20)	PGA to ADC	-	55	-	dB
	ADC	-	50	-	dB
	PGA to HP & Line Amps	-	50	-	dB
	DAC to HP & Line Amps	-	50	-	dB
PSRR with 100 mVpp, 60 Hz signal (Note 20)	PGA to ADC (Note 21)	-	35	-	dB
	ADC	-	25	-	dB
	PGA to HP & Line Amps	-	50	-	dB
	DAC to HP & Line Amps	-	60	-	dB

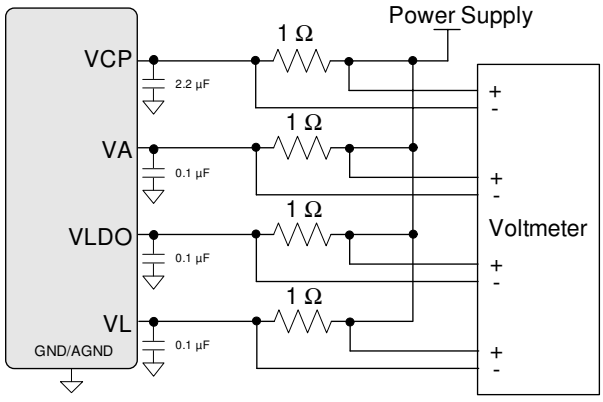
Notes:

20. Valid with the recommended capacitor values on FILT+ and VQ, no load on HP and Line. Increasing the capacitance on FILT+ and VQ will also increase the PSRR.
21. The PGA is biased with VQ, created by a resistor divider from the VA supply.

DIGITAL INTERFACE SPECIFICATIONS & CHARACTERISTICS

Parameters (Note 22)		Symbol	Min	Max	Units
Input Leakage Current		I_{in}	-	±10	µA
Input Capacitance			-	10	pF
1.8 V - 3.3 V Logic					
High-Level Output Voltage (I_{OH} = -100 µA)		V_{OH}	VL - 0.2	-	V
Low-Level Output Voltage (I_{OL} = 100 µA)		V_{OL}	-	0.2	V
High-Level Input Voltage	VL = 1.65 V	V_{IH}	0.83•VL	-	V
	VL = 1.8 V		0.76•VL	-	
	VL = 2.0 V		0.68•VL	-	
	VL > 2.0 V		0.65•VL	-	
Low-Level Input Voltage		V_{IL}	-	0.30•VL	V
HPDETECT Input					
High-Level Input Voltage		$HPDV_{IH}$	0.65•VA	-	V
Low-Level Input Voltage		$HPDV_{IL}$	-	0.35•VA	V

22. See "I/O Pin Characteristics" on page 9 for serial and control port power rails.



Note: Current is derived from the voltage drop across a 1 Ω resistor in series with each supply input.

Figure 8. Power Consumption Test Configuration

POWER CONSUMPTION - ALL SUPPLIES = 1.8 V

	Operation Test Conditions (unless otherwise specified): All zeros input, slave mode, sample rate = 48 kHz; No load. Refer to Figure 8 on page 19.		**Power Ctl. Registers**								**ADC, Line, HP Sel. Registers**						**0Fh** page 50	**Class H Mode** page 45	**Typical Current (mA)**				**Total Power (mW)**
			02h page 42				**03h** page 43				**08h** page 46												
			PDN_CHRG	PDN_ADCB	PDN_ADCA	PDN	PDN_HPB[1:0]	PDN_HPA[1:0]	PDN_LINB[1:0]	PDN_LINA[1:0]	ADCBMUX[1:0]	ADCAMUX[1:0]	LINEBMUX	LINEAMUX	HPBMUX	HPAMUX	PDN_DSP		i_{VCP}	i_{VA}	i_{VLDO}	i_{VL}	
1	Off (Note 23)		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-	0.002	0.003	0.002	0.001	**0.01**
2	Standby	MCLKDIS=1	x	x	x	1	x	x	x	x	x	x	x	x	x	x	x	-	0.003	0.002	0.039	0.006	**0.09**
		MCLKDIS=0	x	x	x	1	x	x	x	x	x	x	x	x	x	x	x	-	0.002	0.005	0.223	0.006	**0.43**
	(Note 23)	MCLKDIS=x	x	x	x	1	x	x	x	x	x	x	x	x	x	x	x	-	0.002	0.002	0.010	0.002	**0.03**
3	Mono Record (Note 24)	ADC	0	1	0	0	11	11	11	11	xx	01	x	x	x	x	x	-	0.003	0.859	0.650	0.017	**2.75**
		PGA to ADC	0	1	0	0	11	11	11	11	xx	00	x	x	x	x	x	-	0.002	1.053	0.650	0.018	**3.10**
4	Stereo Record (Note 24)	ADC	0	0	0	0	11	11	11	11	01	01	x	x	x	x	x	-	0.002	1.116	0.795	0.022	**3.48**
		PGA to ADC	0	0	0	0	11	11	11	11	00	00	x	x	x	x	x	-	0.002	1.470	0.800	0.022	**4.13**
5	Mono Play to HP	No Effects	1	1	1	0	11	10	11	11	xx	xx	x	x	x	0	1	VCP/2	0.450	1.007	0.686	0.006	**3.87**
																		VCP	0.928	1.014	0.690	0.006	**4.75**
		Effects	1	1	1	0	11	10	11	11	xx	xx	x	x	x	0	0	VCP/2	0.452	1.008	0.964	0.006	**4.37**
																		VCP	0.936	1.014	0.972	0.006	**5.27**
6	Mono Play to Line	No Effects	1	1	1	0	11	11	11	10	xx	xx	x	0	x	x	1	VCP/2	0.394	1.008	0.704	0.006	**3.80**
																		VCP	0.822	1.015	0.692	0.005	**4.56**
		Effects	1	1	1	0	11	11	11	10	xx	xx	x	0	x	x	0	VCP/2	0.394	1.008	0.977	0.006	**4.29**
																		VCP	0.822	1.015	0.969	0.006	**5.06**
7	Stereo Play to HP	No Effects	1	1	1	0	10	10	11	11	xx	xx	x	x	0	0	1	VCP/2	0.697	1.434	0.688	0.006	**5.08**
																		VCP	1.405	1.441	0.692	0.006	**6.38**
		Effects	1	1	1	0	10	10	11	11	xx	xx	x	x	0	0	0	VCP/2	0.693	1.435	1.023	0.006	**5.68**
																		VCP	1.429	1.442	1.031	0.006	**7.04**
8	Stereo Play to Line	No Effects	1	1	1	0	11	11	10	10	xx	xx	0	0	x	x	1	VCP/2	0.572	1.437	0.697	0.006	**4.88**
																		VCP	1.182	1.443	0.698	0.005	**5.99**
		Effects	1	1	1	0	11	11	10	10	xx	xx	0	0	x	x	0	VCP/2	0.572	1.437	1.025	0.006	**5.47**
																		VCP	1.182	1.445	1.025	0.006	**6.58**
9	Stereo Passthrough to HP		0	1	1	0	10	10	11	11	xx	xx	x	x	1	1	x	VCP/2	0.562	1.083	0.190	0.005	**3.31**
																		VCP	1.159	1.090	0.190	0.006	**4.40**
10	Stereo Passthrough to Line		0	1	1	0	11	11	10	10	xx	xx	1	1	x	x	x	VCP/2	0.572	1.084	0.190	0.006	**3.33**
																		VCP	1.181	1.093	0.190	0.006	**4.44**
11	Mono Rec. & Play PGA In, HP Out	No Effects	0	1	0	0	11	10	11	11	xx	00	x	x	x	0	1	VCP/2	0.450	1.838	1.063	0.017	**6.06**
																		VCP	0.931	1.846	1.061	0.017	**6.94**
		Effects	0	1	0	0	11	10	11	11	xx	00	x	x	x	0	0	VCP/2	0.453	1.839	1.346	0.017	**6.58**
																		VCP	0.937	1.846	1.345	0.018	**7.46**
12	Stereo Rec. & Play PGA In, HP Out	No Effects	0	0	0	0	10	10	11	11	00	00	x	x	0	0	1	VCP/2	0.689	2.682	1.209	0.023	**8.29**
																		VCP	1.417	2.690	1.218	0.022	**9.63**
		Effects	0	0	0	0	10	10	11	11	00	00	x	x	0	0	0	VCP/2	0.693	2.682	1.560	0.022	**8.92**
																		VCP	1.420	2.691	1.561	0.023	**10.25**

POWER CONSUMPTION - ALL SUPPLIES = 2.5 V

	Operation Test Conditions (unless otherwise specified): /All zeros input, slave mode, sample rate = 48 kHz; No load. Refer to Figure 8 on page 19.		**Power Ctl. Registers**								**MUX Registers**							**Class H Mode** page 45	**Typical Current (mA)**				**Total Power (mW)**
			02h page 42				**03h**page 43				**08h** page 46						**0Fh** page 50		i_{VCP}	i_{VA}	i_{VLDO}	i_{VL}	
			PDN_CHRG	PDN_ADCB	PDN_ADCA	PDN	PDN_HPB[1:0]	PDN_HPA[1:0]	PDN_LINB[1:0]	PDN_LINA[1:0]	ADCBMUX[1:0]	ADCAMUX[1:0]	LINEBMUX	LINEAMUX	HPBMUX	HPAMUX	PDN_DSP						
1	Off (Note 23)		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-	0.001	0.001	0.001	0.000	**0.01**
2	Standby	MCLKDIS=1	x	x	x	1	x	x	x	x	x	x	x	x	x	x	x	-	0.000	0.000	0.064	0.007	**0.18**
		MCLKDIS=0	x	x	x	1	x	x	x	x	x	x	x	x	x	x	x	-	0.000	0.013	0.385	0.007	**1.01**
	(Note 23)	MCLKDIS=x	x	x	x	1	x	x	x	x	x	x	x	x	x	x	x	-	0.000	0.000	0.018	0.000	**0.05**
3	Mono Record (Note 24)	ADC	1	1	0	0	11	11	11	11	xx	01	x	x	x	x	x	-	0.000	0.752	0.743	0.019	**3.79**
		PGA to ADC	1	1	0	0	11	11	11	11	xx	00	x	x	x	x	x	-	0.000	0.997	0.750	0.019	**4.42**
4	Stereo Record (Note 24)	ADC	1	0	0	0	11	11	11	11	01	01	x	x	x	x	x	-	0.000	1.031	0.918	0.025	**4.94**
		PGA to ADC	1	0	0	0	11	11	11	11	00	00	x	x	x	x	x	-	0.000	1.511	0.926	0.024	**6.15**
5	Mono Play to HP	No Effects	1	1	1	0	11	10	11	11	xx	xx	x	x	x	0	1	VCP/2	0.676	1.327	0.705	0.007	**6.79**
																		VCP	1.694	1.339	0.709	0.007	**9.37**
		Effects	1	1	1	0	11	10	11	11	xx	xx	x	x	x	0	0	VCP/2	0.677	1.325	1.032	0.007	**7.60**
																		VCP	1.728	1.337	1.049	0.007	**10.30**
6	Mono Play to Line	No Effects	1	1	1	0	11	11	11	10	xx	xx	x	0	x	x	1	VCP/2	0.585	1.328	0.738	0.007	**6.65**
																		VCP	1.516	1.339	0.739	0.007	**9.00**
		Effects	1	1	1	0	11	11	11	10	xx	xx	x	0	x	x	0	VCP/2	0.585	1.324	1.030	0.006	**7.36**
																		VCP	1.515	1.338	1.030	0.007	**9.73**
7	Stereo Play to HP	No Effects	1	1	1	0	10	10	11	11	xx	xx	x	x	0	0	1	VCP/2	0.943	1.833	0.711	0.007	**8.74**
																		VCP	2.250	1.850	0.744	0.007	**12.13**
		Effects	1	1	1	0	10	10	11	11	xx	xx	x	x	0	0	0	VCP/2	0.945	1.835	1.090	0.007	**9.69**
																		VCP	2.237	1.846	1.121	0.007	**13.03**
8	Stereo Play to Line	No Effects	1	1	1	0	11	11	10	10	xx	xx	0	0	x	x	1	VCP/2	0.760	1.835	0.730	0.007	**8.33**
																		VCP	1.888	1.848	0.740	0.006	**11.21**
		Effects	1	1	1	0	11	11	10	10	xx	xx	0	0	x	x	0	VCP/2	0.760	1.836	1.085	0.007	**9.22**
																		VCP	1.888	1.851	1.058	0.007	**12.01**
9	Stereo Passthrough to HP		1	1	1	0	10	10	11	11	xx	xx	x	x	1	1	x	VCP/2	0.751	1.174	0.212	0.007	**5.36**
																		VCP	1.880	1.188	0.212	0.007	**8.22**
10	Stereo Passthrough to Line		1	1	1	0	11	11	10	10	xx	xx	1	1	x	x	x	VCP/2	0.759	1.175	0.211	0.007	**5.38**
																		VCP	1.886	1.189	0.211	0.007	**8.23**
11	Mono Rec. & Play PGA In, HP Out	No Effects	1	1	0	0	11	10	11	11	xx	00	x	x	x	0	1	VCP/2	0.676	2.055	1.159	0.018	**9.77**
																		VCP	1.700	2.068	1.196	0.018	**12.46**
		Effects	1	1	0	0	11	10	11	11	xx	00	x	x	x	0	0	VCP/2	0.678	2.055	1.462	0.018	**10.53**
																		VCP	1.696	2.066	1.463	0.018	**13.11**
12	Stereo Rec. & Play PGA In, HP Out	No Effects	1	0	0	0	10	10	11	11	00	00	x	x	0	0	1	VCP/2	0.945	3.071	1.340	0.024	**13.45**
																		VCP	2.254	3.089	1.358	0.023	**16.81**
		Effects	1	0	0	0	10	10	11	11	00	00	x	x	0	0	0	VCP/2	0.950	3.074	1.702	0.024	**14.38**
																		VCP	2.254	3.090	1.705	0.023	**17.68**

Notes:

23. When “Off”, $\overline{\text{RESET}}$ pin and clock/data lines held LO; when in “standby”, lines are held HI.
24. Either inputs 1 or 2 may be selected. Input 1 is shown for simplicity.

4. APPLICATIONS

4.1 Overview

4.1.1 Basic Architecture

The CS42L55 is a highly integrated, ultra-low power, 24-bit audio CODEC comprised of stereo A/D and D/A converters with pseudo-differential stereo input and output amplifiers. The ADC and DAC are designed using multi-bit delta-sigma techniques; both converters operate at a low oversampling ratio of 64xFs, maximizing power savings while maintaining high performance. The CODEC operates in one of three sample rate speed modes: Quarter, Half and Single. It accepts and is capable of generating serial audio clocks (SCLK, LRCK) derived from a 12 or 6 MHz input Master Clock (MCLK). Designed with a very low voltage digital core and low voltage Class H amplifiers (powered from an integrated low-dropout regulator and a step-down/inverting charge pump, respectively), the CS42L55 provides significant reduction in overall power consumption.

4.1.2 Line Inputs

The analog input portion of the CODEC allows selection from two stereo line-level sources into a Programmable Gain Amplifier (PGA). The optional pseudo-differential configuration provides noise-rejection for single-ended inputs.

4.1.3 Line and Headphone Outputs (Class H, Ground-Centered Amplifiers)

The analog output portion of the CODEC includes separate pseudo-differential headphone and line out Class H amplifiers. An on-chip step-down/inverting charge pump creates a positive and negative voltage equal to the input or one-half the input supply for the amplifiers, allowing an adaptable, full-scale output swing centered around ground. The inverting architecture eliminates the need for large DC-blocking capacitors and allows the amplifier to deliver more power to headphone loads at lower supply voltages. The step-down architecture allows the amplifier's power supply to adapt to the required output signal. This adaptive power supply scheme converts traditional Class AB amplifiers into more power-efficient Class H amplifiers.

4.1.4 Fixed-Function DSP Engine

The fixed function digital signal processing engine processes both the PCM serial input data and ADC output data allowing a mix between the two. Independent volume control, left/right channel swaps, mono mixes, tone control comprise the DSP engine.

4.1.5 Beep Generator

The beep generator delivers tones at select frequencies across approximately two octave major scales. With independent volume control, beeps may be configured to occur continuously, periodically or at single time intervals.

4.1.6 Power Management

Several control registers and bits provide independent power down control of the ADC, PGA, DSP, headphone and line outputs, allowing operation in select applications with minimal power consumption.

4.2 Analog Inputs

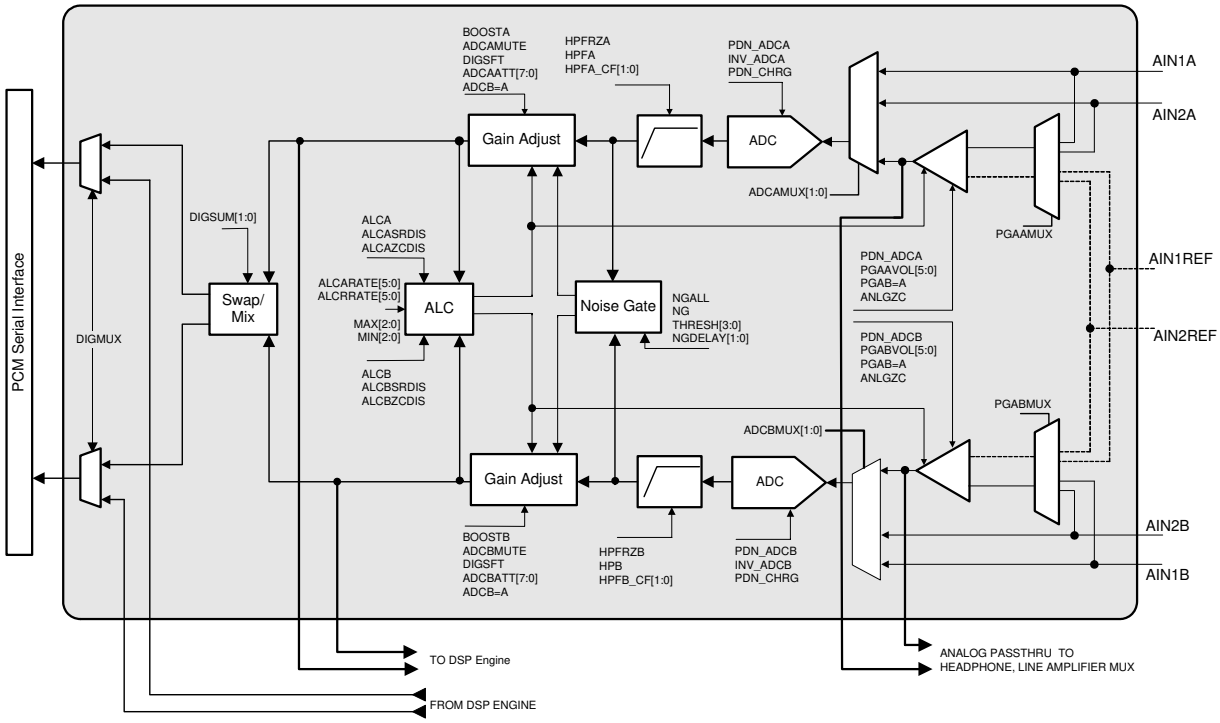


Figure 9. Analog Input Signal Flow

Referenced Control	Register Location
Analog Front End	
PGAxMUX	"PGA x Input Select" on page 49
PDN_ADCx	"Power Down ADC x" on page 42
PGAxVOL[5:0]	"PGAx Volume" on page 49
PGAB=A	"PGA Channel B=A" on page 48
ANLGZCx	"Analog Zero Cross" on page 46
ADCxMUX[1:0]	"ADC x Input Select" on page 46
INV_ADCx	"Invert ADC Signal Polarity" on page 48
PDN_CHRG	"Power Down ADC Charge Pump" on page 42
HPFRZx	"ADCx High-Pass Filter Freeze" on page 47
HPFx	"ADCx High-Pass Filter" on page 47
HPFx_CF[1:0]	"HPF x Corner Frequency" on page 47
Digital Volume	
BOOSTx	"Boostx" on page 49
ADCxMUTE	"ADC Mute" on page 48
ADCxATT[7:0]	"ADCx Volume" on page 50
DIGSFT	"Digital Soft Ramp" on page 46
ADCB=A	"ADC Channel B=A" on page 48
ALCx	"ALCx" on page 62
ALCxSRDIS	"ALCx Soft Ramp Disable" on page 65
ALCxZCDIS	"ALCx Zero Cross Disable" on page 65
ALCARATE[5:0]	"ALC Attack Rate" on page 63
ALCRRATE[5:0]	"ALC Release Rate" on page 63
MAX[2:0]	"ALC Maximum Threshold" on page 64
MIN[2:0]	"ALC Minimum Threshold" on page 64
NGALL	"Noise Gate All Channels" on page 64
NG	"Noise Gate Enable" on page 65
THRESH[3:0]	"Noise Gate Threshold and Boost" on page 65
NGDELAY[1:0]	"Noise Gate Delay Timing" on page 65
Miscellaneous	
DIGSUM[1:0]	"Digital Sum" on page 48
DIGMUX	"Digital MUX" on page 45

4.2.1 Pseudo-Differential Inputs

The CS42L55 implements a pseudo-differential input stage. The AINxREF inputs are intended to be used as a pseudo-differential reference signal. This feature provides 0 noise rejection with single-ended signals. Figure 10 shows a basic diagram outlining the internal implementation of the pseudo-differential input stage, including a recommended stereo pseudo-differential input topology. If pseudo-differential input functionality is not required, simply leave the AINxREF pin floating.

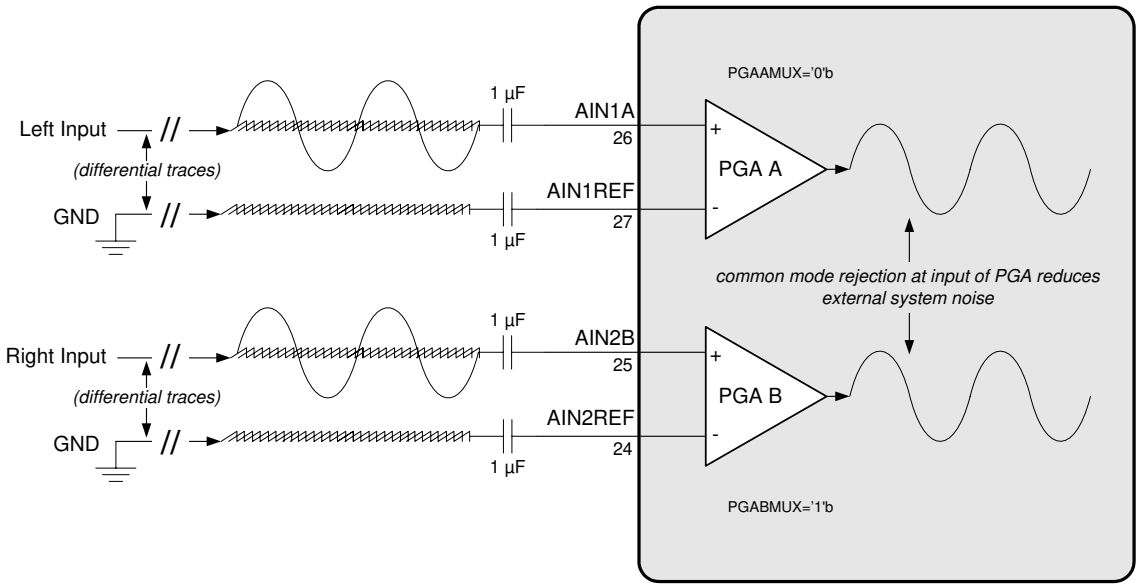


Figure 10. Stereo Pseudo-Differential Input

Referenced Control	Register Location
PGAxMUX	"PGA x Input Select" on page 49

4.2.2 Automatic Level Control (ALC)

When enabled, the ALC monitors the analog input signal after the digital attenuator. The ALC then detects when peak levels exceed the maximum threshold settings and first lowers the PGA gain settings and then increases the digital attenuation levels at a programmable attack rate and maintains the resulting level below the maximum threshold.

When input signal levels fall below the minimum threshold, digital attenuation levels are decreased first and the PGA gain is then increased at a programmable release rate and maintains the resulting level above the minimum threshold.

Attack and release rates are affected by the ADC soft ramp/zero cross settings and sample rate, Fs. ALC soft ramp and zero cross dependency may be independently enabled/disabled.

Recommended settings: Best level control may be realized with the fastest attack and slowest release setting with soft ramp enabled in the control registers.

Notes:

1. When ALC x is enabled and the PGAxVOL[5:0] is set to +12 dB, the ADCxATT[7:0] should not be set below 0 dB.
2. The maximum desired gain must be set in the PGAxVOL register. The ALC will only apply the gain set in PGAxVOL.
3. The ALC maintains the output signal between the MIN and MAX thresholds. As the input signal level changes, the level-controlled output may not always be the same but will always fall between the thresholds.

Referenced Control	Register Location
PGAxVOL[5:0]	"PGAx Volume" on page 49
ADCxATT[7:0].....	"ADCx Volume" on page 50
MAX[2:0], MIN[2:0]	"ALC Threshold (Address 26h)" on page 64

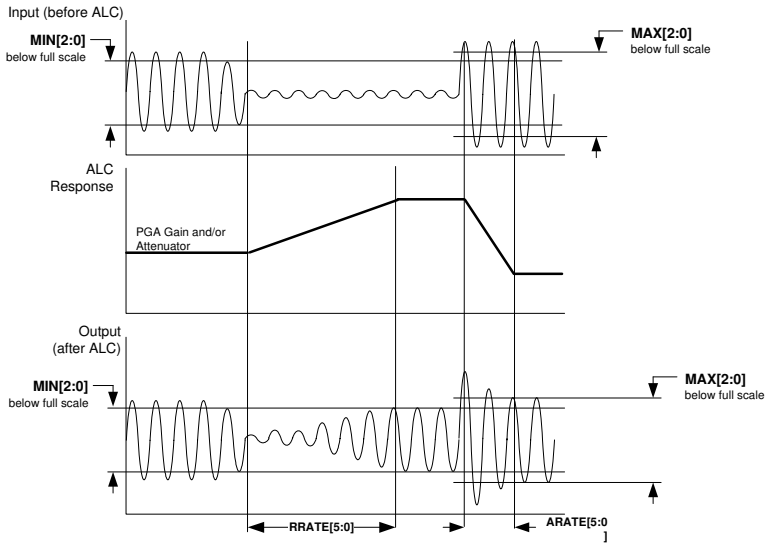


Figure 11. ALC Operation

4.3 Analog In to Analog Out Passthrough

The CS42L55 accommodates analog routing of the analog input signal directly to the headphone and line out amplifiers. This feature is useful in applications that utilize an FM tuner where audio recovered over-the-air must be transmitted to the headphone amplifier without digital conversion in the ADC and DAC. This analog passthrough path reduces power consumption and is immune to modulator switching noise that could interfere with some tuners. This path is selected using the Line and/or HP mux bits and powering down the ADC.

Referenced Control	Register Location
PDN_ADCx	"Power Down ADC x" on page 42
HPxMUX.....	"Headphone Input Select" on page 47
LINExMUX.....	"Line Input Select" on page 47