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CS42L73

Ultralow Power Mobile Audio and Telephony CODEC

Product Overview

- Stereo analog-to-digital converter (ADC)
- Dual analog or digital mic support
- Dual mic bias generators
- Four digital-to-analog converters (DACs) coupled to five outputs
  - Ground-centered stereo headphone amp.
  - Ground-centered stereo line output
  - Mono ear speaker amplifier
  - Mono 1-W speakerphone amplifier
  - Mono speakerphone line output for stereo speakerphone expansion
- Three serial ports with asynchronous sample rate converters
- Digital audio mixing and routing

Ultralow Power Consumption

- 3.8-mW quiescent headphone playback

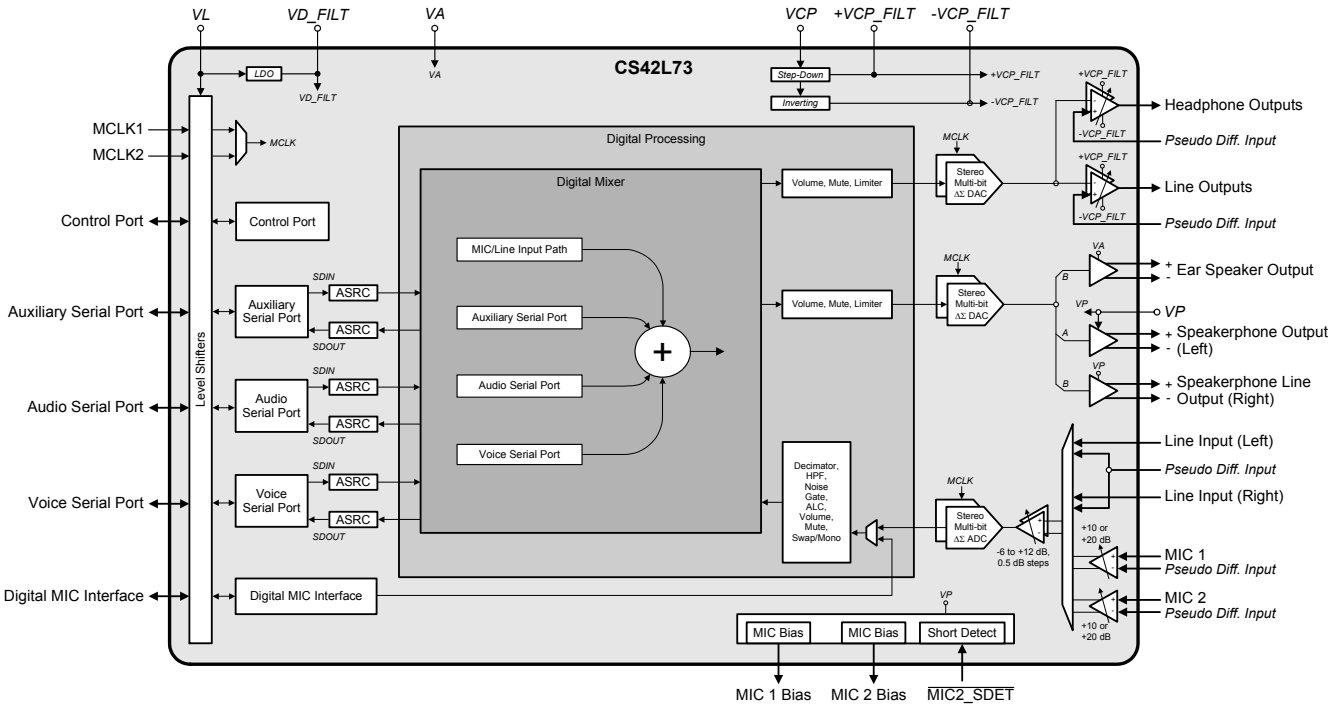
Applications

- Smart phones, ultramobile PCs, and mobile Internet devices

System Features

- Native (no PLL required) support for 6/12/24 MHz, 13/26 MHz, and 19.2/38.4 MHz master clock rates and typical audio clock rates
- Integrated high-efficiency power management reduces power consumption
  - Internal LDO regulator to reduce internal digital operating voltage to VL/2 V
  - Step-down charge pump provides low headphone/line out supply voltage
  - Inverting charge pump accommodates low system voltage by providing negative rail for HP and line amplifier
- Flexible speakerphone amplifier powering
  - 3.00–5.25 V range
  - Independent cycling
- Power-down management
  - Individual controls for ADCs, digital mic interface, mic bias generators, serial ports, and output amplifiers and associated DACs
- Programmable thermal overload notification
- High-speed I²C™ control port (400 kHz)

(**Features** continued on page 2)



Stereo Analog-to-Digital Features

- 91-db dynamic range (A-weighted)
- -85 dB THD+N
- Independent ADC channel control
- 2:1 stereo analog input MUX
- Stereo line input: Shared pseudodifferential reference input
- Dual analog mic inputs
  - Pseudodifferential or single-ended
  - Two, independent, programmable, low-noise mic bias outputs
  - Mic short detect to support headset button
- Analog programmable gain amplifier (PGA) (+12 to -6 dB in 0.5 dB steps)
- +10 dB or +20 dB analog mic boost in addition to PGA gain settings
- Programmable automatic level control (ALC)
  - Noise gate for noise suppression
  - Programmable threshold and attack/release rates

Dual Digital Microphone Interface

- Programmable clock rate: Integer divide by 2 or 4 of internal MCLK

Stereo DAC to Headphone Amplifier

- 94-dB dynamic range (A-weighted)
- -81 dB THD+N into 32 Ω
- Integrated step-down/inverting charge pump
- Class H amplifier, automatic supply adjustment
  - High efficiency
  - Low EMI
- Pseudodifferential ground-centered outputs
- High HP power output at -70/-81 dB THD+N
  - 2 x 16/8.1 mW into 16/32 Ω @ 1.8 V
- Pop and click suppression
- Analog volume control (+12 to -50 dB in 1 dB steps; to -76 dB in 2 dB steps) with zero-cross transitions
- Digital volume control (+12 to -102 dB in 0.5 dB steps) with soft-ramp transitions
- Programmable peak-detect and limiter

Stereo DAC to Line Outputs

- 97 dB dynamic range (A-weighted)
- -86 dB THD+N
- Class-H amplifier
- Pseudodifferential ground-centered outputs
- 1-V_{RMS} line output @ 1.8 V
- Pop and click suppression
- Analog volume control (+12 to -50 dB in 1 dB steps; to -76 dB in 2 dB steps) with zero-cross transitions
- Digital volume control (+12 to -102 dB in 0.5 dB steps) with soft-ramp transitions
- Programmable peak-detect and limiter

Mono DAC to Ear Speaker Amplifier

- High-power output at -70 dB (0.032%) THD+N: 45 mW into 16 Ω @ 1.8 V
- Pop and click suppression
- Digital volume control (+12 to -102 dB in 0.5 dB steps) with soft-ramp transitions
- Programmable peak-detect and limiter

Mono DAC to Speakerphone Amplifier

- High output power at ≤1% THD+N: 1.06/0.76/0.59 W into 8 Ω @ 5.0/4.2/3.7 V
- Direct battery-powered operation
- Pop and click suppression
- Digital volume control (+12 to -102 dB in 0.5 dB steps) with soft-ramp transitions
- Programmable peak-detect and limiter

Mono DAC-to-Speakerphone Line Output

- 84 dB dynamic range (A-weighted)
- -65 dB THD+N
- High voltage (2 V_{RMS} @ VA = 1.8 V, VP = 3.7 V) line output to ensure maximum output from a wide variety of external amplifiers
- Pop and click suppression
- Digital volume control (+12 to -102 dB in 0.5 dB steps) with soft-ramp transitions
- Programmable peak-detect and limiter

Serial Ports

- Three independent serial ports: auxiliary serial port (XSP), audio serial port (ASP), and voice serial port (VSP)
- 8.00, 11.025, 12.00, 16.00, 22.05, 24.00, 32.00, 44.10, and 48.00 kHz sample rates
- All ports support master or slave operation with I²S interface
- XSP and VSP support slave operation with PCM interface
- XSP and ASP are stereo-input/stereo-output to/from digital mixer
- VSP is mono-input/stereo-output to/from digital mixer
- Integrated asynchronous sample rate converters

General Description

The CS42L73 is a highly integrated, low-power, audio and telephony CODEC for portable applications such as smartphones and ultramobile personal computers.

The CS42L73 features a **flexible clocking architecture**, allowing the device to use reference clock frequencies of 6, 12, 24, 13, 26, 19.2, or 38.4 MHz, or any standard audio master clock. As many as two reference/master clock sources may be connected; either one can be selected to drive the internal clocks and processing rate of the CS42L73. Thus, multiple master clock sources within a system can be dynamically activated and deactivated to minimize system-level power consumption.

Three asynchronous bidirectional serial ports (auxiliary, audio, and voice serial ports (XSP, ASP, and VSP, respectively) support multiple clock domains of various digital audio sources or destinations. Three low-latency, fast-locking, integrated **high-performance asynchronous sample rate converters** synchronize and convert the audio samples to the internal processing rate of the CS42L73.

A stereo line input or two mono (one stereo) mic inputs are routed to a **stereo ADC**. The mic inputs may be selectively preamplified by +10 or +20 dB. Two independent, low-noise mic bias voltage supplies are also provided. A PGA is applied to the inputs before they reach the ADC.

The **stereo input path** that follows the stereo ADC begins with a multiplexer to selectively choose data from a **digital mic interface**. Following the multiplexer, the data is decimated, selectively DC high-pass filtered, channel-swapped or mono-to-stereo routed (fanned-out), and volume adjusted or muted. The volume levels can be automatically adjusted via a programmable ALC and noise gate.

A **digital mixer** is used to mix and route the CS42L73's inputs (analog inputs to ADC, digital mic, or serial ports) to outputs (DAC-fed amplifiers or serial ports). There is independent attenuation on each mixer input for each output.

The processing along the **output paths** from the digital mixer to the **two stereo DACs** includes volume adjustment and mute control. A peak-detector can be used to automatically adjust the volume levels via a programmable limiter.

The first stereo DAC feeds the **stereo headphone and line output amplifiers**, which are powered from a dedicated positive supply. An integrated **charge pump** provides a negative supply. This allows a ground-centered analog output with a wide signal swing, and eliminates external DC-blocking capacitors while reducing pops and clicks. Tri-level Class H amplification is used to reduce power consumption under low-signal-level conditions. Analog volume controls are provided on the stereo headphone and line outputs.

The second stereo DAC feeds several mono outputs. The left channel of the DAC sources a **mono, differential-drive, speakerphone amplifier** for driving the handset speakerphone. The right channel sources a **mono, differential-drive, earphone amplifier** for driving the handset earphone. The right channel is also routed to a **mono, differential-drive, speakerphone line output**, which may be connected to an external amplifier to implement a stereo speakerphone configuration when it is used in conjunction with the integrated speakerphone amplifier.

The CS42L73 implements **robust power management** to achieve ultralow power consumption. High granularity in power-down controls allows individual functional blocks to be powered down when unused. The internal low-dropout regulator (LDO) saves power by running the internal digital circuits at half the logic interface supply voltage (VL/2).

A high-speed **I^2C control port** interface capable of up to 400 kHz operation facilitates register programming.

The CS42L73 is available in space-saving 64-ball WLCSP and 65-ball FBGA packages for the commercial (-40° to +85° C) grade.

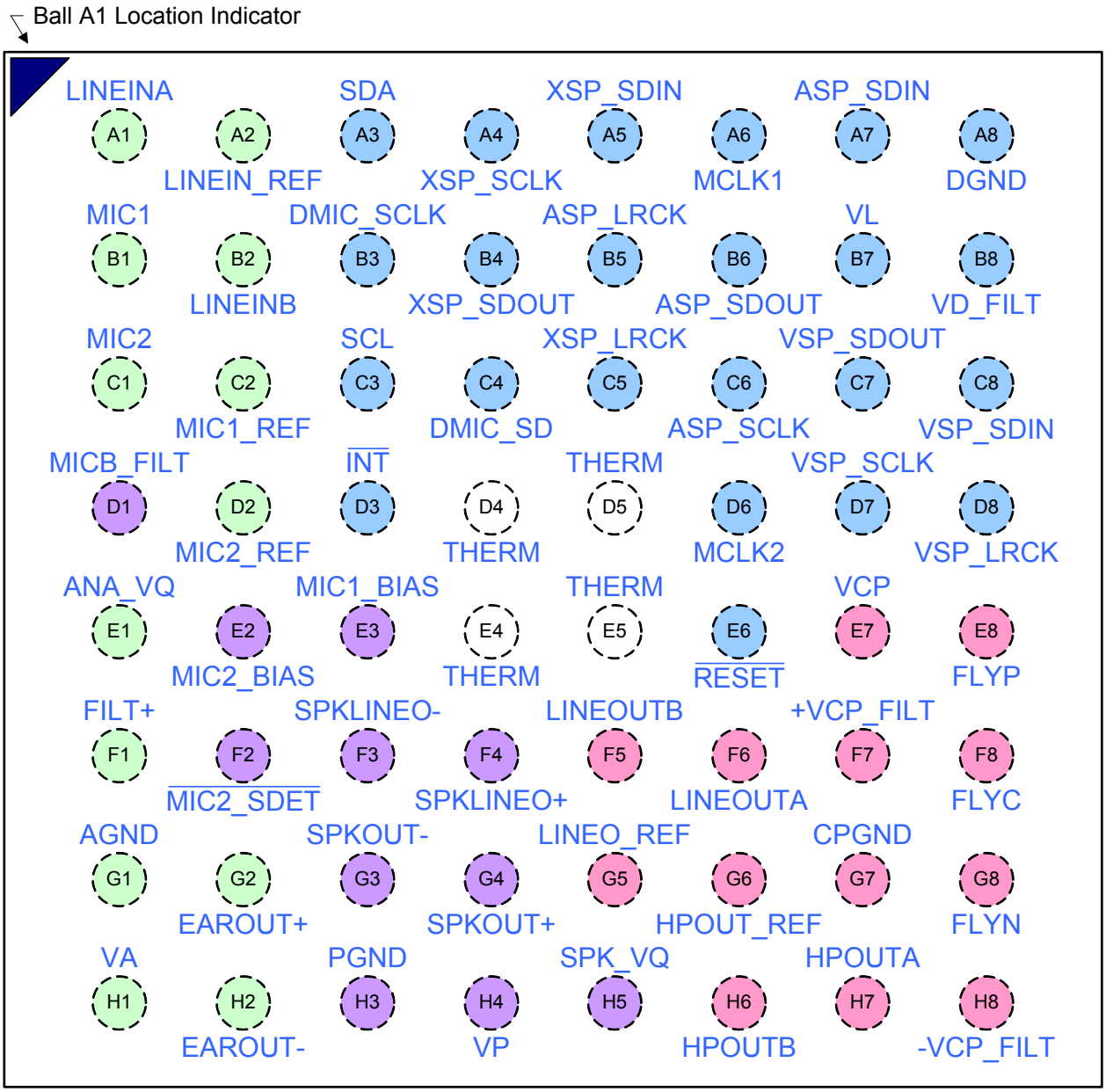
TABLE OF CONTENTS

LIST OF FIGURES

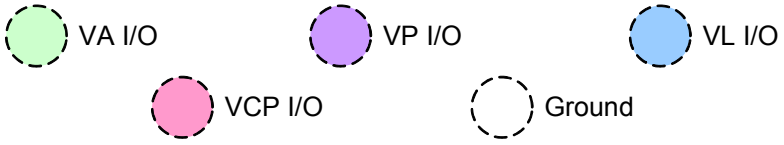
LIST OF TABLES

1. PACKAGE PIN/BALL ASSIGNMENTS AND CONFIGURATIONS

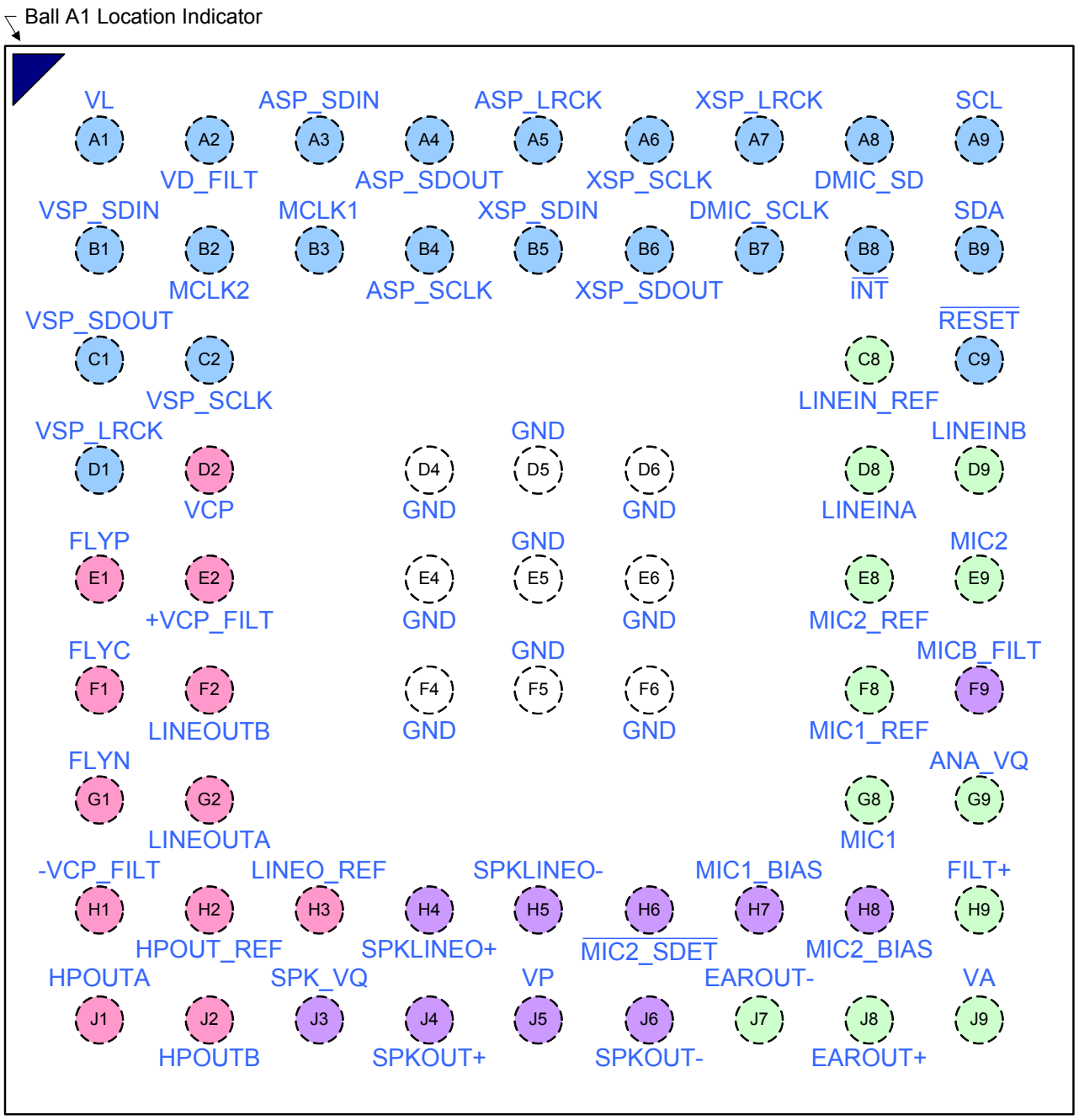
1.1 64-Ball Wafer-Level Chip Scale Package (WLCSP)



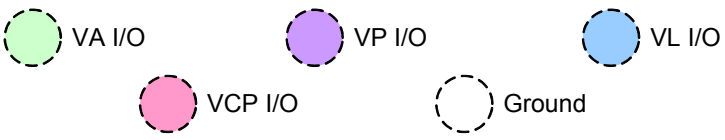
Top-Down
(Though Package)
View



1.2 65-Ball Fine-Pitch Ball Grid Array (FBGA) Package



Top-Down
(Though Package)
View



1.3 Pin/Ball Descriptions

Name	Location		Description
	WLCSP	FBGA	
MCLK1 MCLK2	A6 D6	B3 B2	**High Speed Clock** (*Input*). Potential clock sources for the converters and the device core. Clock source for optional serial port mastering.
$\overline{\text{RESET}}$	E6	C9	**Reset** (*Input*). The device enters a low-power mode when this pin is driven low.
SCL	C3	A9	**Serial Control Port Clock** (*Input*). Serial clock for the I²C control interfaces.
SDA	A3	B9	**Serial Control Data** (*Input*/*Output*). SDA is the bidirectional data pin for the I²C control interface.
$\overline{\text{INT}}$	D3	B8	**Interrupt Request** (*Output*). Open-drain active low interrupt request output.
LINEINA LINEINB	A1 B2	D8 D9	**Analog Line Inputs, A and B (LEFT and RIGHT)** (*Input*). The full-scale level is specified in the Analog Input Characteristics specification table.
LINEIN_REF	A2	C8	**Analog Line Input Pseudodifferential Reference** (*Input*). Ground reference for the analog line input buffers LINEINA and LINEINB.
MIC1 MIC2	B1 C1	G8 E9	**Microphone Inputs 1 and 2** (*Input*). The handset (MIC1) and headset (MIC2) microphone signal inputs. The full-scale level is specified in the Analog Input Characteristics specification table.
MIC1_REF MIC2_REF	C2 D2	F8 E8	**Microphone Inputs 1 and 2 Pseudodifferential References** (*Input*). Ground references for the microphone inputs MIC1 and MIC2.
MIC1_BIAS MIC2_BIAS	E3 E2	H7 H8	**Microphone Bias Voltages 1 and 2** (*Output*). Bias voltage for the microphones MIC1 and MIC2.
$\overline{\text{MIC2\_SDET}}$	F2	H6	**Microphone 2 Short Detect** (*Input*). Transitions on this input can be configured to cause interrupts that represent the pressing and releasing of a button that shorts the headset microphone to ground.
DMIC_SCLK	B3	B7	**Digital Mic Serial Clock** (*Output*). The high-speed clock output to the digital microphone(s).
DMIC_SD	C4	A8	**Digital Mic Serial Data** (*Input*). The serialized data input from the digital microphone(s).
XSP_SCLK	A4	A6	**Auxiliary Serial Port (XSP), Serial Clock** (*Input/Output*). Serial shift clock for the interface.
XSP_LRCK	C5	A7	**XSP, Left/Right Clock** (*Input/Output*). Identifies the start of each serialized PCM data word. When the I²S interface format is selected, this signal also indicates which channel, Left or Right, is currently active on the serial PCM audio data lines.
XSP_SDIN	A5	B5	**XSP, Data Input** (*Input*). Input for two's complement serial PCM audio data.
XSP_SDOUT	B4	B6	**XSP, Data Output** (*Output*). Output for two's complement serial PCM audio data.
ASP_SCLK	C6	B4	**Audio Serial Port (ASP), Serial Clock** (*Input/Output*). Serial shift clock for the interface.
ASP_LRCK	B5	A5	**ASP, Left/Right Clock** (*Input/Output*). Identifies the start of each serialized PCM data word and indicates which channel, Left or Right, is currently active on the serial PCM audio data lines.
ASP_SDIN	A7	A3	**ASP, Data Input** (*Input*). Input for two's complement serial PCM audio data.
ASP_SDOUT	B6	A4	**ASP, Data Output** (*Output*). Output for two's complement serial PCM audio data.
VSP_SCLK	D7	C2	**Voice Serial Port (VSP), Serial Clock** (*Input/Output*). Serial shift clock for the interface.
VSP_LRCK	D8	D1	**Voice Serial Port, Left/Right Clock** (*Input/Output*). Identifies the start of each serialized PCM data word. When the I²S interface format is selected, this signal also indicates which channel, Left or Right, is currently active on the serial PCM audio data lines.
VSP_SDIN	C8	B1	**VSP, Data Input** (*Input*). Input for two's complement serial PCM audio data.
VSP_SDOUT	C7	C1	**VSP, Data Output** (*Output*). Output for two's complement serial PCM audio data.
HPOUTA HPOUTB	H7 H6	J1 J2	**Headphone Audio Output** (*Output*). The full-scale output level is specified in the HP Output Characteristics specification table.
HPOUT_REF	G6	H2	**Pseudodifferential Headphone Output Reference** (*Input*). Ground reference for the headphone amplifiers.

Name	Location		Description
	WLCSP	FBGA	
LINEOUTA LINEOUTB	F6 F5	G2 F2	**Line Audio Output** (*Output*). The full-scale output level is specified in the Line Output Characteristics specification table.
LINEO_REF	G5	H3	**Pseudodifferential Line Output Reference** (*Input*). Ground reference for the line amplifiers.
EAROUT+ EAROUT-	G2 H2	J8 J7	**Ear Speaker Audio Output** (*Output*). The full-scale output level is specified in the Ear Speaker Output Characteristics specification table.
SPKOUT+ SPKOUT-	G4 G3	J4 J6	**Speakerphone Audio Output** (*Output*). The full-scale output level is specified in the Speakerphone Output Characteristics specification table.
SPKLINEO+ SPKLINEO-	F4 F3	H4 H5	**Speakerphone Audio Line Output** (*Output*). The full-scale output level is specified in the Speakerphone Line Output Characteristics specification table.
VA	H1	J9	**Analog Power** (*Input*). Power supply for the internal analog section.
VP	H4	J5	**Speakerphone Power** (*Input*). Power supply for the speakerphone output amplifier and mic bias generators.
VCP	E7	D2	**Step-down Charge Pump Power** (*Input*). Power supply for the step-down charge pump.
VL	B7	A1	**Digital Interface/Core Power** (*Input*). Power Supply for the serial PCM audio ports, I²C control port, and digital mic interface. Power supply for the digital core logic step-down regulator.
+VCP_FILT	F7	E2	**Step-down Charge Pump Filter Connection** (*Output*). Power supply from the step-down charge pump that provides the positive rail for the headphone and line amplifiers.
-VCP_FILT	H8	H1	**Inverting Charge Pump Filter Connection** (*Output*). Power supply from the inverting charge pump that provides the negative rail for the headphone and line amplifiers.
FLYP	E8	E1	**Charge Pump Cap Positive Node** (*Output*). Positive node for the headphone and line amplifiers' step-down charge pump's flying capacitor.
FLYC	F8	F1	**Charge Pump Cap Common Node** (*Output*). Common positive node for the headphone and line amplifiers' step-down and inverting charge pumps' flying capacitors.
FLYN	G8	G1	**Charge Pump Cap Negative Node** (*Output*). Negative node for the headphone and line amplifiers' inverting charge pump's flying capacitor.
VD_FILT	B8	A2	**Regulator Filter Connection** (*Output*). Power supply filter connection for the step-down regulator that provides the low voltage power to the digital section.
ANA_VQ	E1	G9	**Quiescent Voltage, Analog** (*Output*). Filter connection for the internal VA quiescent voltage.
SPK_VQ	H5	J3	**Quiescent Voltage, Speaker** (*Output*). Filter connection for the internal VP quiescent voltage.
FILT+	F1	H9	**Positive Voltage Reference** (*Output*). Positive reference voltage for the internal sampling circuits.
MICB_FILT	D1	F9	**Microphone Bias Source Voltage Filter** (*Output*). Filter connection for the internal quiescent voltage used for the MICx_BIAS outputs.
AGND	G1	N/A	**Analog Ground** (*Input*). Ground reference for the internal analog section.
PGND	H3	N/A	**Speakerphone Ground** (*Input*). Ground reference for the speakerphone and speakerphone line output amplifiers. Connect to ground plane(s) on board to conduct heat away from the part.
CPGND	G7	N/A	**Charge Pump Ground** (*Input*). Ground reference for the internal headphone and line amplifiers charge pump.
DGND	A8	N/A	**Digital Ground** (*Input*). Ground reference for the internal digital section.
GND	N/A	D4, D5, D6, E4, E5, E6, F4, F5, F6	**Ground**. Ground reference for internal analog (AGND), speakerphone and speakerphone line output amplifiers (PGND), internal headphone and line amplifiers (CPGND), and the internal digital section (DGND). These balls also provide thermal relief for the device. Connect to the Ground plane of the circuit board.
THERM	D4, D5, E4, E5	N/A	**Thermal Relief Balls**. Connect to the Ground plane of the circuit board. The Thermal Relief Balls are not electrically connected to the device.
NC	-	-	**No Connect**. No connection is required for these pins.

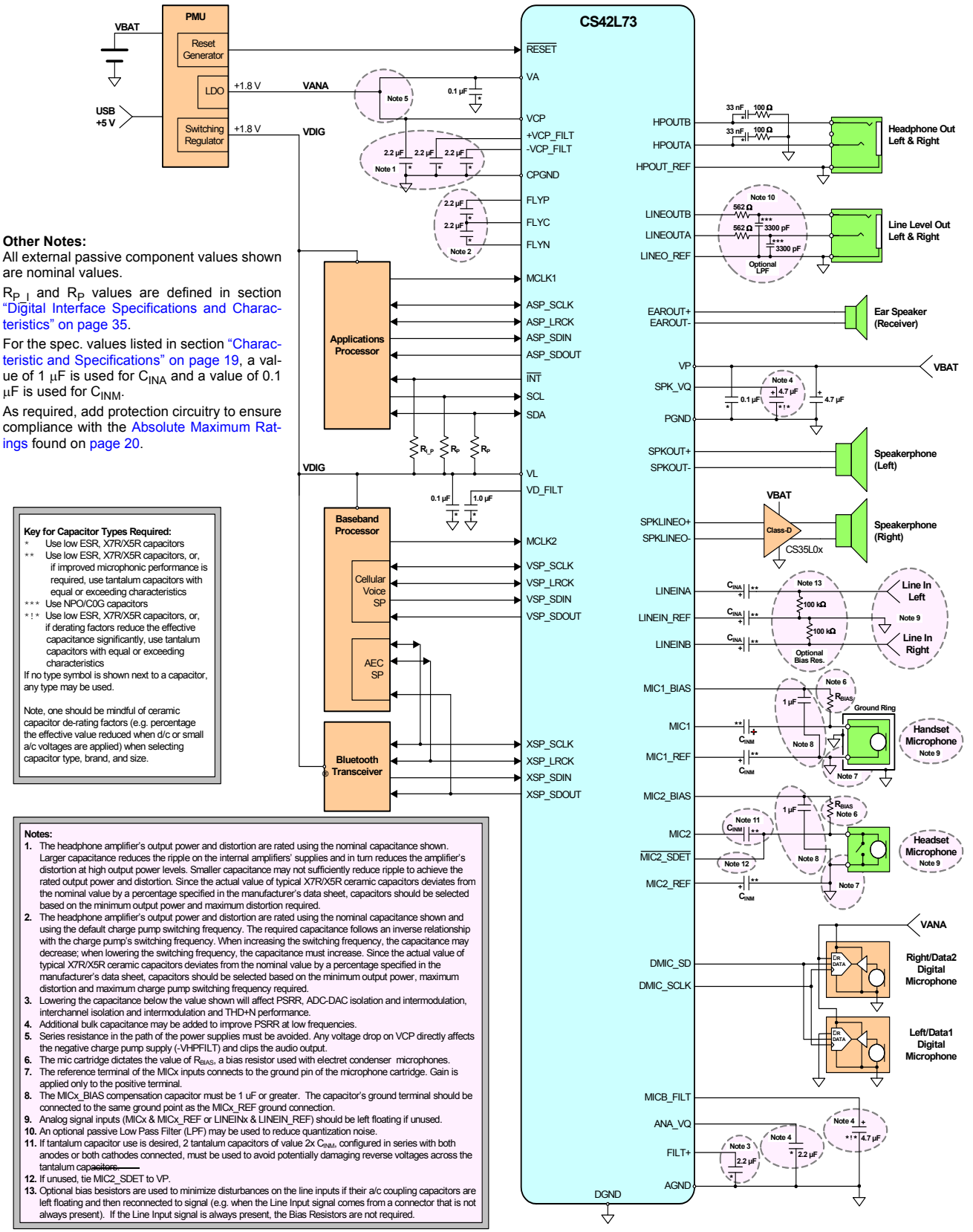
1.4 Digital Pin/Ball I/O Configurations

Power Supply	I/O Name	Direction	Internal Connections	Configuration
VL	MCLK1	Input	Weak Pull-down	Hysteresis on CMOS Input
	MCLK2	Input	Weak Pull-down	Hysteresis on CMOS Input
	$\overline{\text{RESET}}$	Input	-	Hysteresis on CMOS Input
	SCL	Input	-	Hysteresis on CMOS Input
	SDA	Input/Output	-	Hysteresis on CMOS Input/ CMOS Open-drain Output
	$\overline{\text{INT}}$	Output	Weak Pull-up	CMOS Open-drain Output
	XSP_SCLK	Input/Output	Weak Pull-down	Hysteresis on CMOS Input/CMOS Output
	XSP_LRCK	Input/Output	Weak Pull-down	Hysteresis on CMOS Input/CMOS Output
	XSP_SDIN	Input	Weak Pull-down	Hysteresis on CMOS Input
	XSP_SDOUT	Output	Weak Pull-down	Tristateable CMOS Output
	ASP_SCLK	Input/Output	Weak Pull-down	Hysteresis on CMOS Input/ CMOS Output
	ASP_LRCK	Input/Output	Weak Pull-down	Hysteresis on CMOS Input/CMOS Output
	ASP_SDIN	Input	Weak Pull-down	Hysteresis on CMOS Input
	ASP_SDOUT	Output	Weak Pull-down	Tristateable CMOS Output
	VSP_SCLK	Input/Output	Weak Pull-down	Hysteresis on CMOS Input/CMOS Output
	VSP_LRCK	Input/Output	Weak Pull-down	Hysteresis on CMOS Input/CMOS Output
	VSP_SDIN	Input	Weak Pull-down	Hysteresis on CMOS Input
	VSP_SDOUT	Output	Weak Pull-down	Tristateable CMOS Output
	DMIC_SCLK	Output	-	CMOS Output
	DMIC_SD	Input	Weak Pull-down	Hysteresis on CMOS Input

Notes:

- All outputs are disabled when $\overline{\text{RESET}}$ is active.
- Internal weak pull up/down minimum and typical resistances are 550 kΩ and 1 MΩ.
- Typical hysteresis is 500 mV within the 650 mV to 1.15 V window.
- The xSP_SCLK, xSP_LRCK, and xSP_SDOUT (x = X, A, or V) outputs may be disabled via register controls as described in sections “High-impedance Mode” on page 52 and “Master and Slave Timing” on page 52.
- Refer to specification table “Digital Interface Specifications and Characteristics” on page 35 for details on the digital I/O DC characteristics (output voltages/load-capacity, input switching threshold voltages, etc.). Inputs without integrated pull-ups/downs must not be left floating. All inputs must be driven or pulled (internally and/or externally) to a valid high or low level, as defined in the specification table.
- Refer to specification tables “Switching Specifications—Serial Ports—I²S Format” on page 38 on page 47, “Switching Specifications—Serial Ports—PCM Format” on page 39, and “Switching Specifications—Control Port” on page 40 for digital I/O AC characteristics (timing specifications).
- I/O voltage levels must not exceed the I/O’s corresponding power supply voltage. I/O voltage levels must not exceed the voltage listed in “Absolute Maximum Ratings” on page 20.

2. TYPICAL CONNECTION DIAGRAM



Other Notes:
All external passive component values shown are nominal values.

R_{P_I} and R_P values are defined in section "Digital Interface Specifications and Characteristics" on page 35.

For the spec. values listed in section "Characteristic and Specifications" on page 19, a value of 1 µF is used for C_{INA} and a value of 0.1 µF is used for C_{INM}.

As required, add protection circuitry to ensure compliance with the Absolute Maximum Ratings found on page 20.

Key for Capacitor Types Required:
* Use low ESR, X7R/X5R capacitors
** Use low ESR, X7R/X5R capacitors, or, if improved microphonic performance is required, use tantalum capacitors with equal or exceeding characteristics
*** Use NPO/C0G capacitors
! Use low ESR, X7R/X5R capacitors, or, if derating factors reduce the effective capacitance significantly, use tantalum capacitors with equal or exceeding characteristics
If no type symbol is shown next to a capacitor, any type may be used.

Note, one should be mindful of ceramic capacitor de-rating factors (e.g. percentage the effective value reduced when d/c or small a/c voltages are applied) when selecting capacitor type, brand, and size.

Notes:
1. The headphone amplifier's output power and distortion are rated using the nominal capacitance shown. Larger capacitance reduces the ripple on the internal amplifiers' supplies and in turn reduces the amplifier's distortion at high output power levels. Smaller capacitance may not sufficiently reduce ripple to achieve the rated output power and distortion. Since the actual value of typical X7R/X5R ceramic capacitors deviates from the nominal value by a percentage specified in the manufacturer's data sheet, capacitors should be selected based on the minimum output power and maximum distortion required.
2. The headphone amplifier's output power and distortion are rated using the nominal capacitance shown and using the default charge pump switching frequency. The required capacitance follows an inverse relationship with the charge pump's switching frequency. When increasing the switching frequency, the capacitance may decrease; when lowering the switching frequency, the capacitance must increase. Since the actual value of typical X7R/X5R ceramic capacitors deviates from the nominal value by a percentage specified in the manufacturer's data sheet, capacitors should be selected based on the minimum output power, maximum distortion and maximum charge pump switching frequency required.
3. Lowering the capacitance below the value shown will affect PSRR, ADC-DAC isolation and intermodulation, interchannel isolation and intermodulation and THD+N performance.
4. Additional bulk capacitance may be added to improve PSRR at low frequencies.
5. Series resistance in the path of the power supplies must be avoided. Any voltage drop on VCP directly affects the negative charge pump supply (-VHPFILT) and clips the audio output.
6. The mic cartridge dictates the value of R_{BIAS}, a bias resistor used with electret condenser microphones.
7. The reference terminal of the MICx inputs connects to the ground pin of the microphone cartridge. Gain is applied only to the positive terminal.
8. The MICx_BIAS compensation capacitor must be 1 uF or greater. The capacitor's ground terminal should be connected to the same ground point as the MICx_REF ground connection.
9. Analog signal inputs (MICx & MICx_REF or LINEINx & LINEIN_REF) should be left floating if unused.
10. An optional passive Low Pass Filter (LPF) may be used to reduce quantization noise.
11. If tantalum capacitor use is desired, 2 tantalum capacitors of value 2x C_{INM}, configured in series with both anodes or both cathodes connected, must be used to avoid potentially damaging reverse voltages across the tantalum capacitors.
12. If unused, tie MIC2_SDET to VP.
13. Optional bias besistors are used to minimize disturbances on the line inputs if their a/c coupling capacitors are left floating and then reconnected to signal (e.g. when the Line Input signal comes from a connector that is not always present). If the Line Input signal is always present, the Bias Resistors are not required.

Figure 1. Typical Connection Diagram

2.1 Low-Profile Charge-Pump Capacitors

The "Typical Connection Diagram" on page 17 shows that the recommended capacitor values for the charge pump circuitry are all 2.2 µF and the types are all X7R/X5R. Applications that require low-profile versions of these capacitors may use the following parts with a nominal height of only 0.5 mm:

Description: 2.2 µF ±20%, 6.3 V, X5R, 0402, Height = 0.5 mm
Manufacturer, Part Number:

- KEMET, C0402C225M9PAC

2.2 Ceramic Capacitor Derating

The Typical Connection Diagram Capacitor Key highlights that ceramic capacitor derating factors can significantly affect the in-circuit capacitance value and thus the performance of the CS42L73.

As is noted on the Typical Connection Diagram, the 4.7 µF ceramic capacitors used for ANA_VQ or SPKR_VQ affect low-frequency PSRR performance. Numerous types and brands of ceramic capacitors, under typical conditions, exhibit effective capacitances well below their tolerance of ±20%, with some being derated by as much as -50%. These same capacitors, when tested by a multimeter, read much closer to their rated value. A similar derating effect has not been observed with tantalum capacitors.

The amount of derating observed varied with manufacturer and physical size; larger capacitors performed better as did ones from Kemet Electronics Corp. and TDK Corp. of any size. This derating effect is described in datasheets and applications notes from capacitor manufacturers. For instance, as DC and AC voltages are varied from the standard test points (applied DC and AC voltages for standard test points vs. PSRR test are 0 V and 1 V_{RMS} @ 1 kHz vs. 0.9 V and ~1 mV_{RMS} @ 20 Hz to 20 kHz), it is documented that the capacitance varies significantly.

Based on these tests, the following ANA_VQ/SPKR_VQ capacitor parts are recommended for applications that require ceramic capacitors with the smallest PCB footprint:

Description: 4.7 µF ±20%, 6.3V, X5R, 0603
Manufacturer, Part Number:

- KEMET, C0603C475M9PAC
- TDK, C1608X5R0J475M

3. CHARACTERISTIC AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Test Conditions: GND = AGND = PGND = CPGND = DGND = 0 V; all voltages are with respect to ground (GND).

Parameters (Note 1) (Note 2)	Symbol	Min	Nom	Max	Units	Equivalent Tolerance from Nominal
DC Power Supplies						
Analog	VA	1.66	1.80	1.94	V	±7.8%
Speakerphone Amplifiers, Mic Bias Generators (Note 3) Mic Bias with High Voltage Selected and VP_MIN = 1b Otherwise	VP	 3.20 3.00	 - -	 5.25 5.25	 V	 - -
Charge Pump (Headphone and Lineout Amplifiers)	VCP	1.66	1.80	1.94	V	±7.8%
Digital Core, Serial/Control/Digital-Mic Interfaces	VL	1.66	1.80	1.94	V	±7.8%
Temperature						
Ambient Temperature (local to device) Commercial: CWZR	T_A	-40	-	+85	°C	-

Notes:

1. Device functional operation is guaranteed within these limits. Functionality is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.
2. "Parameter Definitions" on page 134 describes some parameters in detail.
3. The recommended operation range of the VP supply depends on how the CS42L73 is configured. If either mic bias is enabled (PDN_MIC1_BIAS = 0b or PDN_MIC2_BIAS = 0b) and the mic bias generators are set for their higher voltage (MIC_BIAS_CTRL = 1b), either VP must be held above 3.2 V or VP_MIN must be set to 0b. With this configuration and a VP level between 3.00 and 3.20 V, VP_MIN must be set to 0b to ensure the bias generators bypass one of their two LDO stages, ensuring there is enough headroom to avoid dropout. Refer to "Mic BIAS Characteristics" on page 26 for details on how much setting VP_MIN to 0b reduces PSRR performance.

ABSOLUTE MAXIMUM RATINGS

Test Conditions: GND = AGND = PGND = CPGND = DGND = 0 V; all voltages are with respect to ground (GND).

Parameters (Note 2)		Symbol	Min	Max	Units
DC Power Supply					
Analog, Charge Pump, Digital Core (LDO fed),		VA, VCP, VL	-0.3	2.22	V
Serial/Control/Digital-Mic Interfaces		VP (Note 4)	-0.3	5.6	V
Speakerphone Amplifiers, Mic Bias Generators					
Input Current	(Note 5)	I_{in}	-	±10	mA
Voltages Applied to I/Os					
External Voltage Applied	LINEINx, MICx, x_REF	V_{IN-AI}	AGND – 0.3	VA + 0.3	V
to Analog Input (Note 6)	$\overline{\text{MIC2\_SDET}}$	$V_{IN-AI-SD}$	PGND – 0.3	VP + 0.3	V
External Voltage	HPOUT, LINEOUT	V_{FLT-HP_LINE}	-VCP_FILT – 0.3	+VCP_FILT + 0.3	V
Applied to Analog	EAROUT	$V_{FLT-EAR}$	AGND – 0.3	VA + 0.3	V
Output (Note 7)	SPKOUT, SPKLINEO, MICx_BIAS	$V_{FLT-SPK\_MB}$	PGND – 0.3	VP + 0.3	V
External Voltage Applied to Digital Input	(Note 6)	V_{IN-DI}	-0.3	VL + 0.3	V
External Voltage Applied to Digital Output	(Note 7)	V_{FLT-DO}	-0.3	VL + 0.3	V
Temperature					
Ambient Operating Temperature	Commercial: CWZR	T_A	-50	+110	°C
(local to device, power applied)					
Storage Temperature (no power applied)		T_{stg}	-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:

4. VP must be applied before VA is applied. VP must be removed after VA is removed.
5. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.
6. The maximum over/under voltage is limited by the input current.
7. • V_{FLT-x} is the applied voltage that causes a contention fault condition between its source and the CS42L73 output.
   • ±VCPFILT are specified in "DC Electrical Characteristics" on page 21.
   • The specification applies to both the signal and pseudodifferential reference pins, where applicable.

DC ELECTRICAL CHARACTERISTICS

Test Conditions: Connections to the CS42L73 are shown in the "Typical Connection Diagram" on page 17; GND = AGND = PGND = CPGND = DGND = 0 V; all voltages are with respect to ground (GND); VA = VCP = 1.80 V, VP = 3.70 V; T_A = +25 °C.

Parameters (Note 2)		Min	Typ	Max	Units
ANA_VQ Characteristics					
Nominal Voltage		-	VA/2	-	V
SPK_VQ Characteristics					
Nominal Voltage		-	VP/2	-	V
VCPFILT Characteristics (Note 8)					
VCP Mode	+VCPFILT	-	VCP	-	V
	-VCPFILT	-	-VCP	-	V
VCP/2 Mode	+VCPFILT	-	VCP/2	-	V
	-VCPFILT	-	-VCP/2	-	V
VCP/3 Mode	+VCPFILT	-	VCP/3	-	V
	-VCPFILT	-	-VCP/3	-	V
FILT+ Characteristics					
Nominal Voltage		-	VA	-	V
VD_FILT Characteristics					
Nominal Voltage		-	0.9	-	V
MICB_FILT Characteristics					
Nominal Voltage	MIC_BIAS_CTRL = 0b	-	2.00	-	V
	MIC_BIAS_CTRL = 1b	-	2.75	-	V
Analog Output Current Limiter Characteristics					
Current Limiter On Threshold (Note 9)		100	120	150	mA

Notes:

8. No load (from specification tables "Serial Port to Stereo HP Output Characteristics" on page 27 and "Serial Port to Stereo Line Output Characteristics" on page 29, R_L = ∞ Ω and C_L = 0 pF) connected to Headphone and Line Outputs (HPOUTx and LINEOUTx). Headphone Zobel Network remains connected.
9. See "Analog Output Current Limiter" on page 51.

ANALOG INPUT TO SERIAL PORT CHARACTERISTICS

Test Conditions (unless otherwise specified): Connections to the CS42L73 are shown in the "Typical Connection Diagram" on page 17; Input is a 1-kHz sine wave through the passive input filter shown in Figure 1; GND = AGND = PGND = CPGND = DGND = 0 V; all voltages are with respect to ground (GND); VA = 1.80 V; T_A = +25 °C; Measurement Bandwidth is 20 Hz to 20 kHz; Fs = 48 kHz (Note 10); ASP is used and is in slave mode with Fs_{ext} = 48 kHz; MIC_PREAMPx = +10 dB, PGAxVOL = 0 dB; Mixer Attenuation and Digital Volume = 0 dB, Digital Mute is disabled.

Parameters (Note 2) (Note 11)		Min	Typ	Max	Units
LINEINA/LINEINB to PGA to ADC					
Dynamic Range					
PGA Setting: 0 dB	A-weighted	85	91	-	dB
	unweighted	82	88	-	dB
PGA Setting: +12 dB	A-weighted	78	84	-	dB
	unweighted	75	81	-	dB
Total Harmonic Distortion + Noise					
PGA Setting: 0 dB	-1 dBFS	-	-85	-79	dB
	-60 dBFS	-	-28	-22	dB
PGA Setting: +12 dB	-1 dBFS	-	-81	-75	dB
Common Mode Rejection (Note 12)		-	40	-	dB
MIC1/MIC2 to PREAMP to PGA to ADC, MIC_PREAMPx = +10 dB Gain					
Dynamic Range (Note 13)					
PGA Setting: 0 dB	A-weighted	-	88	-	dB
	unweighted	-	86	-	dB
PGA Setting: +12 dB	A-weighted	-	78	-	dB
	unweighted	-	75	-	dB
Total Harmonic Distortion + Noise					
PGA Setting: 0 dB	-1 dBFS	-	-77	-	dB
PGA Setting: +12 dB	-1 dBFS	-	-64	-	dB
Common Mode Rejection (Note 12)		-	40	-	dB
MIC1/MIC2 to PREAMP to PGA to ADC, MIC_PREAMPx = +20 dB Gain					
Dynamic Range (Note 13)					
PGA Setting: 0 dB	A-weighted	-	82	-	dB
	unweighted	-	79	-	dB
PGA Setting: +12 dB	A-weighted	-	70	-	dB
	unweighted	-	67	-	dB
Total Harmonic Distortion + Noise					
PGA Setting: 0 dB	-1 dBFS	-	-71	-	dB
PGA Setting: +12 dB	-1 dBFS	-	-63	-	dB
Common Mode Rejection (Note 12)		-	40	-	dB
DC Accuracy					
Interchannel Gain Mismatch		-	0.2	-	dB
Gain Drift		-	±100	-	ppm/°C
Offset Error		-	352	-	LSB

ANALOG INPUT TO SERIAL PORT CHARACTERISTICS (CONTINUED)

Test Conditions (unless otherwise specified): Connections to the CS42L73 are shown in the "Typical Connection Diagram" on page 17; Input is a 1-kHz sine wave through the passive input filter shown in Figure 1; GND = AGND = PGND = CPGND = DGND = 0 V; all voltages are with respect to ground (GND); VA = 1.80 V; T_A = +25 °C; Measurement Bandwidth is 20 Hz to 20 kHz; Fs = 48 kHz (Note 10); ASP is used and is in slave mode with Fs_{ext} = 48 kHz; MIC_PREAMPx = +10 dB, PGAxVOL = 0 dB; Mixer Attenuation and Digital Volume = 0 dB, Digital Mute is disabled.

Parameters (Note 2) (Note 11)		Min	Typ	Max	Units
Input					
Interchannel Isolation (1 kHz)	LINEINA to LINEINB, PGAxVOL = +12 dB	-	90	-	dB
	MIC1 to MIC2, MIC_PREAMPx = +20 dB, PGAxVOL = +12 dB	-	80	-	
HP Amp to Analog Input Isolation (Note 14)	R_L = 3 kΩ	84	90	-	dB
	R_L = 16 Ω	77	83	-	dB
Full-scale Signal Input Voltage LINEINA/LINEINB (Note 15)	PGAxVOL = 0 dB	0.78•VA	0.82•VA	0.86•VA	V_{PP}
	PGAxVOL = +12 dB	-	0.198•VA	-	V_{PP}
Full-scale Signal Input Voltage MIC1/MIC2 (Note 15)	MIC_PREAMPx = +10 dB, PGAxVOL = +0 dB	-	0.258•VA	-	V_{PP}
	MIC_PREAMPx = +20 dB, PGAxVOL = +0 dB	-	0.081•VA	-	V_{PP}
	MIC_PREAMPx = +10 dB, PGAxVOL = +12 dB	-	0.064•VA	-	V_{PP}
	MIC_PREAMPx = +20 dB, PGAxVOL = +12 dB	-	0.020•VA	-	V_{PP}
LINEIN_REF/MICx_REF Input Voltage (Note 16)		-	-	0.300	V_{PP}
Input Impedance (Note 17), LINEINA/LINEINB	1 kHz	-	50	-	kΩ
Input Impedance (Note 17), MIC1/MIC2	1 kHz	-	1.0	-	MΩ
DC Voltage at Analog Input (Pin Floating)		-	0.50•VA	-	V
LINEINA/LINEINAB PSRR					
- 100 mV_{PP} signal AC-coupled to VA supply (Note 18)	217 Hz	-	50	-	dB
- LINEINA and LINEINB connected to LINEIN_REF	1 kHz	-	65	-	dB
- PGAxVOL = 0 dB	20 kHz	-	40	-	dB
MIC1/MIC2 PSRR					
- 100 mV_{PP} signal AC-coupled to VA supply (Note 18)	217 Hz	-	50	-	dB
- MICx connected to MICx_REF	1 kHz	-	65	-	dB
- MIC_PREAMPx = +20 dB, PGAxVOL = +12 dB	20 kHz	-	35	-	dB

Notes:

10. Fs is the sampling frequency used by the core and the A/D and D/A converters. For specifications, a default value of 48 kHz is used. Refer to section "Applications" on page 41 for a description of how Fs relates to the CS42L73's clock inputs.
11. Measures are referred to the applicable typical full-scale voltages. Applies to all THD+N and dynamic range values in the table.
12. Refer to Figure 3 below.
13. Includes noise from MICx_BIAS output through series 2.21 kΩ series resistor to MICx. Refer to Figure 2 below. Input signal is -60 dB down from corresponding full-scale voltage.
14. Measurement taken with the following analog gain settings:
    - LINEINA/LINEINB: PGAxVOL = +12 dB
    - MIC1/MIC2: MIC_PREAMPx= + 20 dB, PGAxVOL = +12 dB
    - HPxAVOL = +2 dB for R_L = 3 kΩ, -4 dB for R_L = 16 Ω
15. The full-scale input voltages given refer to the maximum voltage difference between the LINEINx/MICx and LINEIN_REF/MICx_REF pins. Providing an input signal at these pins that exceeds the full-scale input voltage will result in the clipping of the analog signal.
16. The PGA output clips if the voltage difference between the LINEINx/MICx and LINEIN_REF/MICx_REF signals exceeds the full-scale voltage specification. If the LINEIN_REF/MICx_REF signal level exceeds the specified maximum value, PGA linearity may be degraded and analog input performance may be adversely affected. Refer to Figure 4 below.
17. Measured between LINEINx/MICy and AGND. Input impedance can vary from nominal value by ±20%.
18. The PGA is biased with ANA_VQ, created by a resistor divider from the VA supply. Increasing the capacitance on ANA_VQ will increase the PSRR at low frequencies.

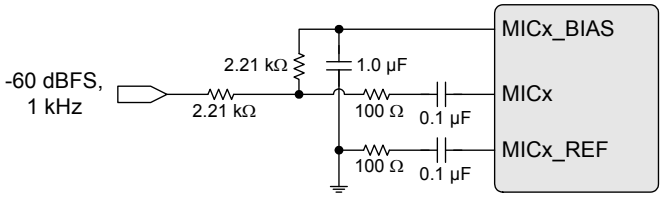


Figure 2. MICx Dynamic Range Test Configuration

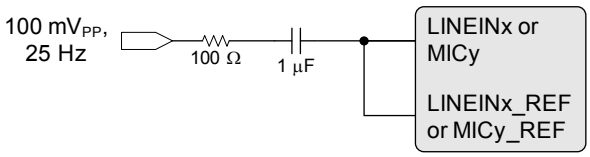


Figure 3. Analog Input CMRR Test Setup

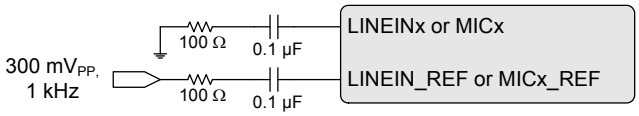


Figure 4. LINEIN_REF/MICx_REF Input Voltage Test Setup

STEREO-ADC AND DUAL-DIGITAL-MIC DIGITAL FILTER CHARACTERISTICS

Test Conditions (unless otherwise specified): Fs = 48 kHz (Note 10), f_{DMIC_SCLK} = 3.072 MHz (Note 19).

Parameters (Note 2)		Min	Typ	Max	Units
Low-Pass Filter Characteristics (Note 20)					
Frequency Response (20 Hz to 20 kHz)		-0.07	-	+0.02	dB
Passband	to -0.05 dB corner	-	0.41	-	Fs
	to -3.0 dB corner	-	0.49	-	Fs
Stopband (Note 21)		0.60	-	-	Fs
Stopband Attenuation		33	-	-	dB
Total Input Path Digital Filter Group Delay		-	4.3/Fs	-	s
High-Pass Filter Characteristics (Note 20) (Note 22)					
Passband	to -3.0 dB corner	-	$4.10x10^{-5}$	-	Fs
	to -0.05 dB corner	-	$3.57x10^{-4}$	-	Fs
Passband Ripple		-	-	0.01	dB
Phase Deviation @ 20 Hz		-	5.30	-	Deg
Filter Settling Time (input signal goes to 95% of its final value)		-	$12.2x10^{3}$/Fs	-	s

Notes:

19. Refer to section "Digital Microphone (DMIC) Interface" on page 60 for a description of how the digital mic shift clock frequency (f_{DMIC_SCLK}) relates to the CS42L73's internal master clock rate.
20. Responses are clock-dependent and will scale with Fs. Note that the response plots (Figures 48 to 52 on pages 127 and 128) have been normalized to Fs and can be denormalized by multiplying the X-axis scale by Fs.
21. Measurement Bandwidth is from Stopband to 3 Fs.
22. High-pass filter is applied after low-pass filter.

THERMAL OVERLOAD DETECT CHARACTERISTICS

Test Conditions: Connections to the CS42L73 are shown in the "Typical Connection Diagram" on page 17; GND = AGND = PGND = CPGND = DGND = 0 V; all voltages are with respect to ground (GND); VA = 1.80 V.

Parameters		Min	Typ	Max	Units
Thermal Overload Detect Threshold Characteristics					
Threshold Junction Temperature (T_J) (Note 23)	THMOVLD_THLD[1:0] = 00b	-	150	-	°C
	THMOVLD_THLD[1:0] = 01b	-	132	-	°C
	THMOVLD_THLD[1:0] = 10b	-	115	-	°C
	THMOVLD_THLD[1:0] = 11b	-	98	-	°C

Notes:

23. The thermal overload detect threshold temperature level can vary from the nominal value by ±10 °C.

ASRC DIGITAL FILTER CHARACTERISTICS

Test Conditions (unless otherwise specified): Fs = 48 kHz (Note 10); Fs_{ext} = 48 kHz (Note 24).

Parameters (Note 2) (Note 25)		Min	Typ	Max	Units
Low-Pass Filter Characteristics (Note 24)					
Frequency Response (0 Hz to 20 kHz)		-0.07	-	+0.04	dB
Passband	to -0.05 dB corner	-	0.48	-	Fs_{ext}
	to -3.0 dB corner	-	0.50	-	
Stopband		0.55	-	-	Fs_{ext}
Stopband Attenuation		125	-	-	dB
Total ASRC Group Delay		-	(Note 26)	-	s

Notes:

24. Fs_{ext} is the sample rate of the serial port (XSP, ASP, or VSP) interface.
25. Refer to Response plots in Figures 53 and 54 on page 129.
26. The equations for the group delay through the sample rate converters are:
    - Input (from the serial ports to the core): $6.9/Fs_{ext} + 3.0/Fs$
    - Output (from the core to the serial ports): $2.6/Fs_{ext} + 14.1/Fs$.

    A plot of ASRC group delay values for the extreme supported internal sample rates (Fs) and standard audio sample rates is found in section "Group Delay" on page 130.