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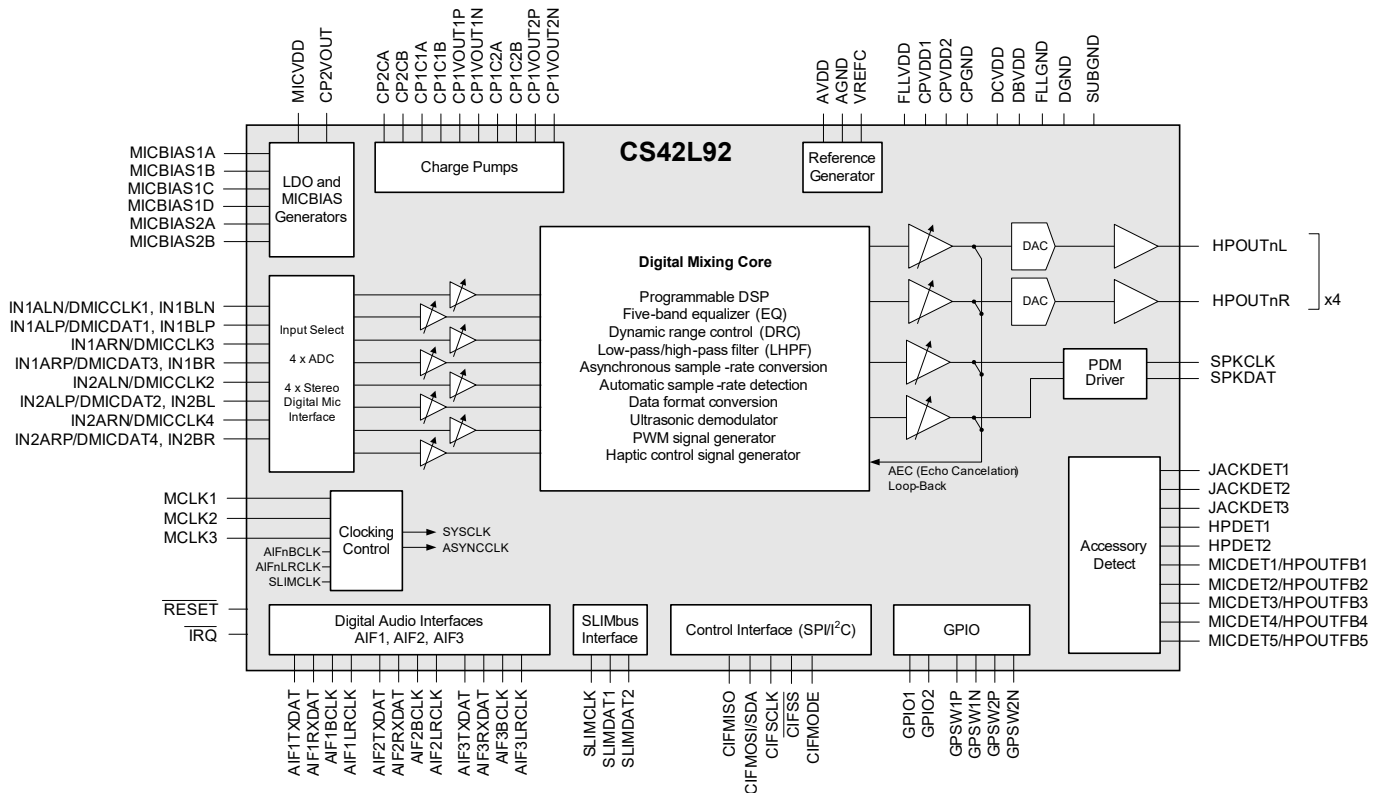# CS42L92

32-Bit 384-kHz Hi-Fi Audio Codec

Features

- Integrated multichannel 32-bit hi-fi audio hub codec
  — 99-dB signal-to-noise ratio (SNR) mic input (48 kHz)
  — 127-dB SNR headphone playback (48 kHz)
  — −100-dB total harmonic distortion + noise (THD+N)
  — Ultrasonic input- and output-path support
- Up to eight analog or digital microphone (DMIC) inputs
- Multipurpose headphone/earpiece/line output drivers
  — Support for balanced headphone output loads
  — 33 mW into 32-Ω load at 0.1% THD+N
  — Hi-fi filters for audiophile-quality playback
- Native audio playback up to 384 kHz sample rate, concurrent with voice and ultrasonic input signal paths
- Digital pulse-density modulation (PDM) output interface
- Multichannel asynchronous sample-rate conversion
- Multiline SLIMbus® audio and control interface
- Three multichannel digital-audio interfaces
  — Standard data formats up to 384 kHz, 32 bits
- Flexible clocking, derived from MCLK*n*, AIF*n*, or SLIMbus
  — Low-power frequency-locked loops (FLLs) support reference clocks down to 32 kHz.
- Advanced accessory detection functions
- Configurable functions on up to 16 general-purpose input/output (GPIO) pins
- Integrated regulators and charge pumps
- Small W-CSP package, 0.4-mm staggered ball array

Applications

- Smartphones, tablets, and multimedia handsets

Description

The CS42L92 is a highly integrated low-power audio system for smartphones, tablets, and other portable audio devices. Multiple input/output paths are supported by a fully flexible all-digital mixing and routing engine, incorporating sample rate converters and other signal-processing functions for wide use-case flexibility. The integrated DSP provides a general-purpose signal processing capability; this is supported by general-purpose timer and event-logger functions.

The digital audio interfaces and hi-fi DACs enable 32-bit playback through the entire signal chain. Native audio playback at sample rates up to 384 kHz is possible, concurrent with voice and ultrasonic input paths.

The CS42L92 supports up to eight analog inputs and up to eight PDM digital inputs. Low-power input modes are available for always-on (e.g., voice-trigger) functionality using either analog or digital input. A smart accessory interface, with multipurpose impedance sensing and measurement capability, supports detection of external headsets and push buttons. Dual headphone connections (e.g., 3.5-mm and USB-C™) can be detected simultaneously.

Four hi-fi quality stereo headphone drivers are provided, each supporting stereo ground-referenced or mono bridge-tied load (BTL) configurations. Multiple headphone/earpiece outputs can be supported, including balanced stereo headphone configurations. The output drivers offer noise levels as low as 0.63 μV_{RMS} into line or headphone loads. Selectable hi-fi filters support playback modes at sample rates up to 384 kHz.

Two channels of PDM output (one stereo interface) are available, and also an IEC-60958-3–compatible S/PDIF transmitter. A signal generator for controlling haptics devices is included; vibe actuators can connect directly to the PDM output interface. All inputs, outputs, and system interfaces can function concurrently.

A SLIMbus interface supports multichannel audio paths and host control register access. Three further digital audio interfaces are provided, each supporting a wide range of standard audio sample rates and serial interface formats. Automatic sample-rate detection enables seamless wideband/narrowband voice-call handover. Two FLLs are integrated, providing support for a wide range of system-clock frequencies.

The CS42L92 is configured using the SLIMbus, SPI™, or I2C interfaces. The device is powered from 1.8- and 1.2-V supplies. The power, clocking, and output driver architectures are designed to maximize battery life in voice, music, and standby modes. Low-power (10 μA) Sleep Mode is supported, with configurable wake-up events.

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1 Pin Descriptions

1.1 WLCSP Pinout

A2 CPVDD1	**A4** CP1VOUT2N	**A6** HPOUT4L	**A8** HPOUT3L	**A10** HPOUT2L	**A12** HPOUT1L	

Figure 1-1. Top-Down (Through-Package) View—104-Ball WLCSP Package

A2 CPVDD1 **A4** CP1VOUT2N **A6** HPOUT4L **A8** HPOUT3L **A10** HPOUT2L **A12** HPOUT1L

B1 CP2CA **B3** CPGND **B5** CP1C2B **B7** HPOUT3R **B9** HPOUT2R **B11** HPOUT1R **B13** MICDET4/HPOUTFB4

C2 CP1C2A **C4** CP1VOUT2P **C6** HPOUT4R **C8** MICDET5/HPOUTFB5 **C10** HPDET2 **C12** MICDET3/HPOUTFB3

D1 CP2CB **D3** CPVDD2 **D5** TRST **D7** JACKDET1 **D9** HPDET1 **D11** GPSW1N **D13**

E2 CP1C1A **E4** CP1VOUT1P **E6** MICBIAS2A **E8** GPSW2N **E10** MICDET2/HPOUTFB2 **E12** GPSW1P

F1 CP2VOUT **F3** CP1VOUT1N **F5** TDO **F7** GPSW2P **F9** MICDET1/HPOUTFB1 **F11** JACKDET2 **F13**

G2 MICBIAS1B **G4** MICBIAS1C **G6** CIFMODE **G8** JACKDET3 **G10** AGND2 **G12** **H13** AVDD2

H1 MICVDD **H3** MICBIAS1D **H5** MICBIAS2B **H7** GPIO2 **H9** GPIO1 **H11** IRQ

J2 IN1BLN **J4** IN1ALP/DMICDAT1 **J6** AIF3LRCLK/GPIO16 **J8** AIF3TXDAT/GPIO13 **J10** SPKCLK/GPIO3 **J12** RESET **K13** SUBGND

K1 IN1BLP **K3** IN1ARN/DMICCLK3 **K5** AIF1TXDAT/GPIO5 **K7** AIF2LRCLK/GPIO12 **K9** CIFSS **K11** SPKDAT/GPIO4 **L12** FLLGND

L2 IN1ARP/DMICDAT3 **L4** IN2BR **L6** AIF1RXDAT/GPIO7 **L8** CIFMISO **L10** MCLK3 **M11** FLLVDD **M13**

M1 IN1BR **M3** IN2ARN/DMICCLK4 **M5** VREFC **M7** AIF2BCLK/GPIO10 **M9** SLIMCLK **N10** MCLK2 **N12** DGND

N2 **N4** **N6** **N8** **P9** SLIMDAT1 **P11** MCLK1 **P13** DCVDD

P1 IN2BL **P3** IN2ALN/DMICCLK2 **P5** DGND **P7** AIF3BCLK/GPIO14 **R10** CIFSCLK **R12** DGND

R2 AGND1 **R4** SUBGND **R6** AIF2RXDAT/GPIO11 **R8** **T9** SLIMDAT2 **T11** DBVDD **T13** DGND

T1 NC **T3** AVDD1 **T5** DCVDD **T7** AIF2TXDAT/GPIO9 CIFMOSI/SDA

AIF1BCLK/GPIO6 AIF1LRCLK/GPIO8 AIF3RXDAT/GPIO15

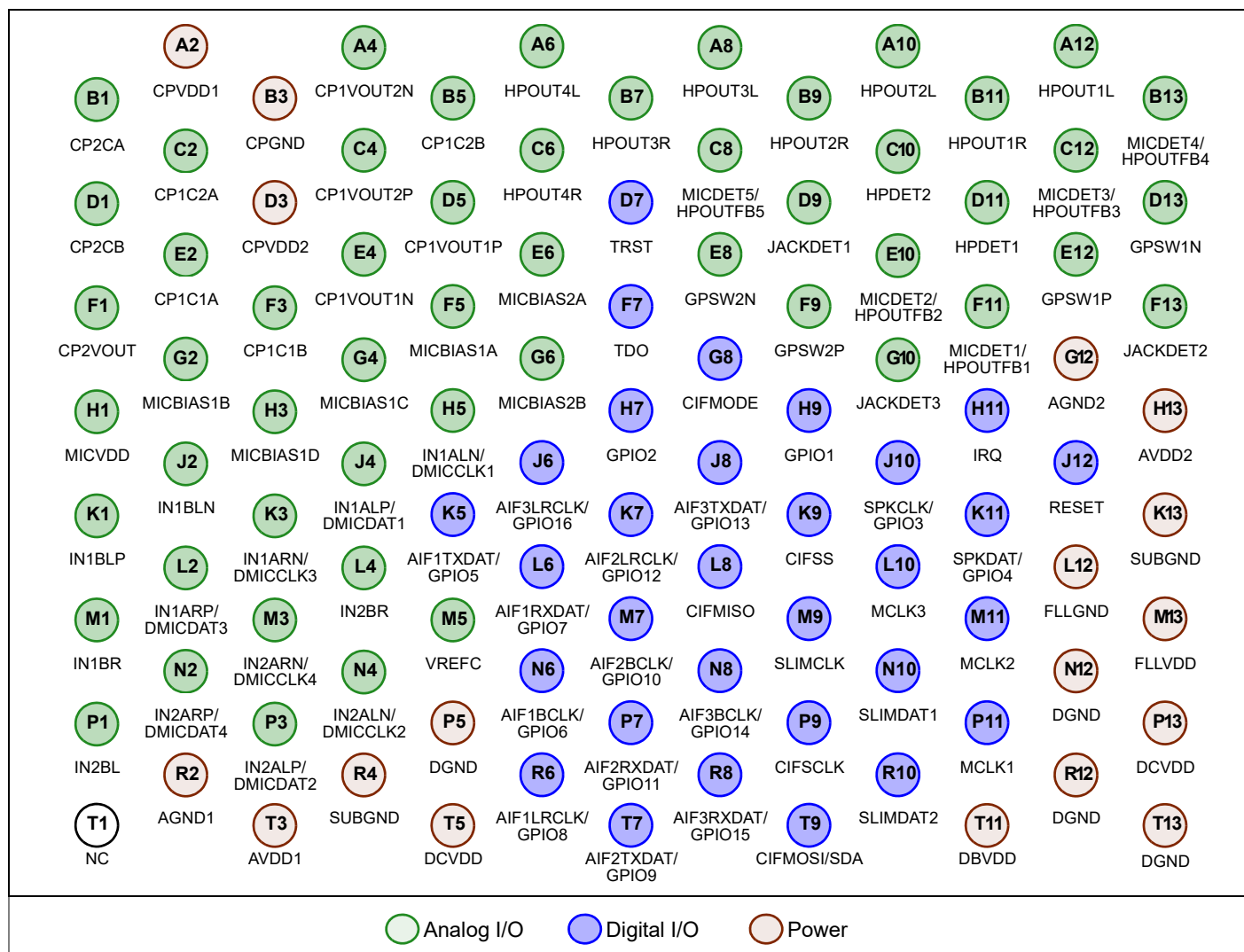🟢 Analog I/O   🔵 Digital I/O   🔴 Power

Figure 1-1. Top-Down (Through-Package) View—104-Ball WLCSP Package

1.2 Pin Descriptions

Table 1-1 describes each pin on the CS42L92. Note that pins that share a common name should be tied together on the printed circuit board (PCB).

Table 1-1. Pin Descriptions

PU = Pull-up, PD = Pull-down, K = Bus keeper, H = Hysteresis on CMOS input, Z = Hi-Z (High impedance), C = CMOS, OD = Open drain.

Pin Name	Pin #	Power Supply	I/O	Pin Description	Digital Pad Attributes	State at Reset [1]
				Analog I/O		
CP1C1A	E2	—	O	Charge Pump 1 fly-back capacitor 1 pin	—	—
CP1C1B	F3	—	O	Charge Pump 1 fly-back capacitor 1 pin	—	—
CP1C2A	C2	—	O	Charge Pump 1 fly-back capacitor 2 pin	—	—
CP1C2B	B5	—	O	Charge Pump 1 fly-back capacitor 2 pin	—	—
CP1VOUT1N	E4	—	O	Charge Pump 1 negative output 1 decoupling pin	—	Output
CP1VOUT1P	D5	—	O	Charge Pump 1 positive output 1 decoupling pin	—	Output
CP1VOUT2N	A4	—	O	Charge Pump 1 negative output 2 decoupling pin	—	Output
CP1VOUT2P	C4	—	O	Charge Pump 1 positive output 2 decoupling pin	—	Output
CP2CA	B1	—	O	Charge Pump 2 fly-back capacitor pin	—	Output
CP2CB	D1	—	O	Charge Pump 2 fly-back capacitor pin	—	Output
CP2VOUT	F1	—	O	Charge Pump 2 output decoupling pin/supply for LDO2	—	Output
GPSW1N	D13	—	I/O	General-purpose bidirectional switch 1 contact	—	—
GPSW1P	E12	—	I/O	General-purpose bidirectional switch 1 contact	—	—
GPSW2N	E8	—	I/O	General-purpose bidirectional switch 2 contact	—	—
GPSW2P	F9	—	I/O	General-purpose bidirectional switch 2 contact	—	—
HPDET1	D11	—	I/O	Headphone sense 1 input	—	Input
HPDET2	C10	—	I/O	Headphone sense 2 input	—	Input
HPOUT1L	A12	—	O	Left headphone 1 output	—	Output
HPOUT1R	B11	—	O	Right headphone 1 output	—	Output
HPOUT2L	A10	—	O	Left headphone 2 output	—	Output
HPOUT2R	B9	—	O	Right headphone 2 output	—	Output
HPOUT3L	A8	—	O	Left headphone 3 output	—	Output
HPOUT3R	B7	—	O	Right headphone 3 output	—	Output
HPOUT4L	A6	—	O	Left headphone 4 output	—	Output
HPOUT4R	C6	—	O	Right headphone 4 output	—	Output
IN1ALN/ DMICCLK1	H5	MICVDD or MICBIASn [2]	I	Left/right-channel negative differential mic/line input/ DMIC Clock Output 1. Also suitable for connection to external accessory interfaces.	—	IN1ALN input
IN1ALP/ DMICDAT1	J4	MICVDD or MICBIASn [2]	I	Left-channel single-ended mic/line input/positive differential mic/line input/DMIC Data Input 1. Also suitable for connection to external accessory interfaces.	PD/H	IN1ALP input
IN1ARN/ DMICCLK3	K3	MICVDD or MICBIASn [2]	I	Right-channel negative differential mic/line input/DMIC Clock Output 3. Also suitable for connection to external accessory interfaces.	—	IN1ARN input
IN1ARP/ DMICDAT3	L2	MICVDD or MICBIASn [2]	I/O	Right-channel single-ended mic/line input/positive differential mic/line input/DMIC Data Input 3. Also suitable for connection to external accessory interfaces.	PD/H	IN1ARP input
IN1BLN	J2	MICVDD	I	Negative differential mic/line input. Also suitable for connection to external accessory interfaces.	—	Input
IN1BLP	K1	MICVDD	I	Single-ended mic/line input/positive differential mic/line input. Also suitable for connection to external accessory interfaces.	—	Input

Table 1-1. Pin Descriptions *(Cont.)*

PU = Pull-up, PD = Pull-down, K = Bus keeper, H = Hysteresis on CMOS input, Z = Hi-Z (High impedance), C = CMOS, OD = Open drain.

Pin Name	Pin #	Power Supply	I/O	Pin Description	Digital Pad Attributes	State at Reset [1]
IN1BR	M1	MICVDD	I	Right-channel single-ended mic/line input/positive differential mic/line input.	—	Input
IN2ALN/ DMICCLK2	N4	MICVDD or MICBIASn [2]	I	Left-channel negative differential mic/line input/DMIC Clock Output 2. Also suitable for connection to external accessory interfaces.	—	IN2ALN input
IN2ALP/ DMICDAT2	P3	MICVDD or MICBIASn [2]	I/O	Left-channel single-ended mic/line input/positive differential mic/line input/DMIC Data Input 2. Also suitable for connection to external accessory interfaces.	PD/H	IN2ALP input
IN2ARN/ DMICCLK4	M3	MICVDD or MICBIASn [2]	I	Right-channel negative differential mic/line input/DMIC Clock Output 4. Also suitable for connection to external accessory interfaces.	—	IN2ARN input
IN2ARP/ DMICDAT4	N2	MICVDD or MICBIASn [2]	I/O	Right-channel single-ended mic/line input/positive differential mic/line input/DMIC Data Input 4. Also suitable for connection to external accessory interfaces.	PD/H	IN2ARP input
IN2BL	P1	MICVDD	I	Left-channel single-ended mic/line input	—	Input
IN2BR	L4	MICVDD	I	Right-channel single-ended mic/line input. Also suitable for connection to external accessory interfaces.	—	Input
JACKDET1	D9	AVDD	I	Jack detect input 1	—	Input
JACKDET2	F13	AVDD	I	Jack detect input 2	—	Input
JACKDET3	G10	AVDD	I	Jack detect input 3	—	Input
MICBIAS1A	F5	MICVDD	O	Microphone bias 1A	—	Output
MICBIAS1B	G2	MICVDD	O	Microphone bias 1B	—	Output
MICBIAS1C	G4	MICVDD	O	Microphone bias 1C	—	Output
MICBIAS1D	H3	MICVDD	O	Microphone bias 1D	—	Output
MICBIAS2A	E6	MICVDD	O	Microphone bias 2A	—	Output
MICBIAS2B	G6	MICVDD	O	Microphone bias 2B	—	Output
MICDET1/ HPOUTFB1	F11	—	I/O	Mic/accessory sense input 1/HPOUT ground feedback pin 1	—	Input
MICDET2/ HPOUTFB2	E10	—	I/O	Mic/accessory sense input 2/HPOUT ground feedback pin 2	—	Input
MICDET3/ HPOUTFB3	C12	—	I/O	Mic/accessory sense input 3/HPOUT ground feedback pin 3	—	Input
MICDET4/ HPOUTFB4	B13	—	I/O	Mic/accessory sense input 4/HPOUT ground feedback pin 4	—	Input
MICDET5/ HPOUTFB5	C8	—	I/O	Mic/accessory sense input 5/HPOUT ground feedback pin 5	—	Input
MICVDD	H1	—	O	LDO2 output decoupling pin (generated internally by CS42L92). (Can also be used as reference/supply for external microphones.)	—	Output
VREFC	M5	—	O	Band-gap reference external capacitor connection	—	Output
Digital I/O						
AIF1BCLK/ GPIO6	N6	DBVDD	I/O	Audio interface 1 bit clock/GPIO6	PU/PD/K/H/ Z/C/OD	GPIO6 input with bus-keeper
AIF1LRCLK/ GPIO8	R6	DBVDD	I/O	Audio interface 1 left/right clock/GPIO8	PU/PD/K/H/ Z/C/OD	GPIO8 input with bus-keeper
AIF1RXDAT/ GPIO7	L6	DBVDD	I/O	Audio interface 1 RX digital audio data/GPIO7	PU/PD/K/H/ C/OD	GPIO7 input with bus-keeper
AIF1TXDAT/ GPIO5	K5	DBVDD	I/O	Audio interface 1 TX digital audio data/GPIO5	PU/PD/K/H/ Z/C/OD	GPIO5 input with bus-keeper

Table 1-1. Pin Descriptions *(Cont.)*

PU = Pull-up, PD = Pull-down, K = Bus keeper, H = Hysteresis on CMOS input, Z = Hi-Z (High impedance), C = CMOS, OD = Open drain.

Pin Name	Pin #	Power Supply	I/O	Pin Description	Digital Pad Attributes	State at Reset [1]
AIF2BCLK/ GPIO10	M7	DBVDD	I/O	Audio interface 2 bit clock/GPIO10	PU/PD/K/H/ Z/C/OD	GPIO10 input with bus-keeper
AIF2LRCLK/ GPIO12	K7	DBVDD	I/O	Audio interface 2 left/right clock/GPIO12	PU/PD/K/H/ Z/C/OD	GPIO12 input with bus-keeper
AIF2RXDAT/ GPIO11	P7	DBVDD	I/O	Audio interface 2 RX digital audio data/GPIO11	PU/PD/K/H/ C/OD	GPIO11 input with bus-keeper
AIF2TXDAT/ GPIO9	T7	DBVDD	I/O	Audio interface 2 TX digital audio data/GPIO9	PU/PD/K/H/ Z/C/OD	GPIO9 input with bus-keeper
AIF3BCLK/ GPIO14	N8	DBVDD	I/O	Audio interface 3 bit clock/GPIO14. If the JTAG interface is configured, this pin provides the TCK input connection.	PU/PD/K/H/ Z/C/OD	GPIO14 input with bus-keeper
AIF3LRCLK/ GPIO16	J6	DBVDD	I/O	Audio interface 3 left/right clock/GPIO16	PU/PD/K/H/ Z/C/OD	GPIO16 input with bus-keeper
AIF3RXDAT/ GPIO15	R8	DBVDD	I/O	Audio interface 3 RX digital audio data/GPIO15. If the JTAG interface is configured, this pin provides the TDI input connection.	PU/PD/K/H/ C/OD	GPIO15 input with bus-keeper
AIF3TXDAT/ GPIO13	J8	DBVDD	I/O	Audio interface 3 TX digital audio data/GPIO13. If the JTAG interface is configured, this pin provides the TMS input connection.	PU/PD/K/H/ Z/C/OD	GPIO13 input with bus-keeper
CIFMISO	L8	DBVDD	O	Control interface (SPI) Master In Slave Out data. The CIFMISO is high impedance if CIF1SS is not asserted.	Z/C	Output
CIFMOSI/SDA	T9	DBVDD	I/O	Control interface (SPI) Master Out Slave In data/ Control interface (I2C) data input/output.	H/OD	Input
CIFSCLK	P9	DBVDD	I	Control interface clock input	H	Input
CIFSS	K9	DBVDD	I	Control interface (SPI) slave select (SS)	H	Input
CIFMODE	G8	DBVDD	I	Control interface mode select	H	Input
GPIO1	H9	DBVDD	I/O	GPIO1	PU/PD/K/H/ C/OD	GPIO1 input with bus-keeper
GPIO2	H7	DBVDD	I/O	GPIO2	PU/PD/K/H/ C/OD	GPIO2 input with bus-keeper
IRQ	H11	DBVDD	O	Interrupt request (IRQ) output (default is active low)	C/OD	Output
MCLK1	P11	DBVDD	I	Master clock 1	H	Input
MCLK2	M11	DBVDD	I	Master clock 2	H	Input
MCLK3	L10	DBVDD	I	Master clock 3	H	Input
RESET	J12	DBVDD	I	Digital reset input (active low)	PU/PD/K/H	Input with pull-up
SLIMCLK	M9	DBVDD	I/O	SLIMbus clock I/O	H/C	Input
SLIMDAT1	N10	DBVDD	I/O	SLIMbus data I/O	H/C	Input
SLIMDAT2	R10	DBVDD	I/O	SLIMbus data I/O	H/C	Input
SPKCLK/ GPIO3	J10	DBVDD	I/O	Digital speaker (PDM) clock output/GPIO3	PU/PD/K/H/ C/OD	GPIO3 input with bus-keeper
SPKDAT/ GPIO4	K11	DBVDD	I/O	Digital speaker (PDM) data output/GPIO4	PU/PD/K/H/ C/OD	GPIO4 input with bus-keeper
TDO	F7	DBVDD	O	JTAG data output	C	Output
TRST	D7	DBVDD	I	JTAG test access port reset (active low)	PD/H	Input with pull-down
Supply						
AGND1	R2	—	—	Analog ground (return path for AVDD1)	—	—
AGND2	G12	—	—	Analog ground (return path for AVDD2)	—	—
AVDD1	T3	—	—	Analog supply	—	—
AVDD2	H13	—	—	Analog supply	—	—

Table 1-1. Pin Descriptions *(Cont.)*

PU = Pull-up, PD = Pull-down, K = Bus keeper, H = Hysteresis on CMOS input, Z = Hi-Z (High impedance), C = CMOS, OD = Open drain.

Pin Name	Pin #	Power Supply	I/O	Pin Description	Digital Pad Attributes	State at Reset [1]
CPGND	B3	—	—	Charge pump ground (return path for CPVDD1, CPVDD2)	—	—
CPVDD1	A2	—	—	Supply for Charge Pump 1 and Charge Pump 2	—	—
CPVDD2	D3	—	—	Secondary supply for Charge Pump 1	—	—
DBVDD	T11	—	—	Digital buffer (I/O) supply	—	—
DCVDD	P13, T5	—	—	Digital core supply	—	—
DGND	N12, P5, R12, T13	—	—	Digital ground (return path for DCVDD and DBVDD)	—	—
FLLGND	L12	—	—	Analog ground (return path for FLLVDD)	—	—
FLLVDD	M13	—	—	Analog FLL supply	—	—
SUBGND	K13, R4	—	—	Substrate ground	—	—
No Connect						
NC	T1	—	—	—	—	—

1. Note that the default conditions described are not valid if modified by the boot sequence or by a wake-up control sequence.
2. The analog input functions on these pins are referenced to the MICVDD power domain. The digital input/output functions are referenced to the MICVDD or MICBIAS*n* power domain, as selected by the applicable IN*x*_DMIC_SUP field.
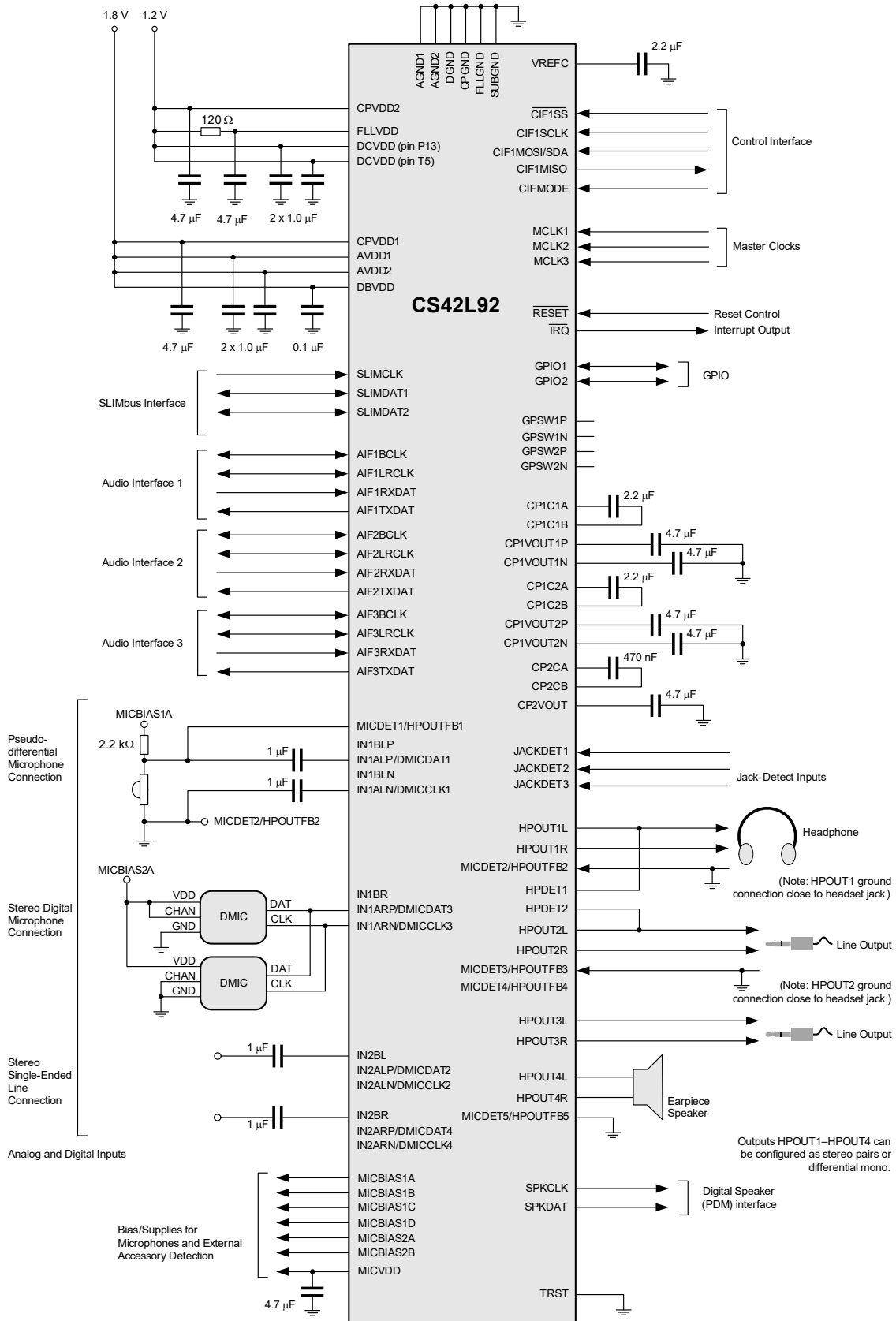
2 Typical Connection Diagram

Figure 2-1. Typical Connection Diagram

3 Characteristics and Specifications

Table 3-1 defines parameters as they are characterized in this section.

Table 3-1. Parameter Definitions

Parameter	Definition
Channel separation	Left-to-right and right-to-left channel separation is the difference in level between the active channel (driven to maximum full scale output) and the measured signal level in the idle channel at the test signal frequency. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel.
Common-mode rejection ratio (CMRR)	The ratio of a specified input signal (applied to both sides of a differential input), relative to the output signal that results from it.
Dynamic range (DR)	A measure of the difference between the maximum full scale output signal and the sum of all harmonic distortion products plus noise, with a low-level input signal applied. Typically, an input signal level 60 dB below full scale is used.
Power-supply rejection ratio (PSRR)	The ratio of a specified power supply variation relative to the output signal that results from it. PSRR is measured under quiescent signal path conditions.
Signal-to-noise ratio (SNR)	A measure of the difference in level between the maximum full scale output signal and the output with no input signal applied.
Total harmonic distortion (THD)	The ratio of the RMS sum of the harmonic distortion products in the specified bandwidth [1] relative to the RMS amplitude of the fundamental (i.e., test frequency) output.
Total harmonic distortion plus noise (THD+N)	The ratio of the RMS sum of the harmonic distortion products plus noise in the specified bandwidth [1] relative to the RMS amplitude of the fundamental (i.e., test frequency) output.

1. All performance measurements are specified with a 20-kHz, low-pass brick-wall filter and, where noted, an A-weighted filter. The low-pass filter removes out-of-band noise.

Table 3-2. Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under electrical characteristics at the test conditions specified.

Parameter	Symbol	Minimum	Maximum
Supply voltages	DCVDD [1], FLLVDD [1]	–0.3 V	1.6 V
	AVDD [2], CPVDD1, CPVDD2	–0.3 V	2.5 V
	DBVDD, MICVDD	–0.3 V	5.0 V
Voltage range digital inputs DBVDD domain	—	SUBGND – 0.3 V	DBVDD + 0.3 V
DMICDAT1–DMICDAT2	—	SUBGND – 0.3 V	MICVDD + 0.3 V
Voltage range analog inputs	IN1ARx, IN2Axx, IN2Bx	SUBGND – 0.3 V	MICVDD + 0.3 V
	IN1ALx, IN1BLx, IN1BR	SUBGND – 0.9 V	MICVDD + 0.3 V
	MICDETn 3	SUBGND – 0.3 V	MICVDD + 0.3 V
	HPOUTFBn 3	SUBGND – 0.3 V	SUBGND + 0.3 V
	JACKDET1, HPDET1, HPDET2	CP1VOUT2N – 0.3 V [5]	AVDD + 0.3 V
	JACKDET2 [4], JACKDET3 [4]	SUBGND – 0.3 V	MICVDD + 0.3 V
	GPSWnP, GPSWnN	SUBGND – 0.3 V	MICVDD + 0.3 V
Ground	AGND 6, DGND, CPGND, FLLGND	SUBGND – 0.3V	SUBGND + 0.3V
Operating temperature range	T_A	–40ºC	+85ºC
Operating junction temperature	T_J	–40ºC	+125ºC
Storage temperature after soldering	—	–65ºC	+150ºC

ESD-sensitive device. The CS42L92 is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device. This device is qualified to current JEDEC ESD standards.

1. The DCVDD and FLLVDD pins should be tied to a common supply rail. The associated power domain is referred to as DCVDD.
2. The AVDD1 and AVDD2 pins should be tied together. The associated power domain is referred to as AVDD.
3. The MICDETn and HPOUTFBn functions share common pins. The absolute maximum rating varies according to the applicable function of each pin. The HPOUTFBn ratings are applicable if any of the HPn_GND_SEL bits select the respective pin for HPOUT ground feedback.
4. If AVDD > MICVDD (e.g., if LDO2 is disabled), the maximum JACKDET2/JACKDET3 voltage is AVDD + 0.3 V.
5. CP1VOUT2N is an internal supply, generated by the CS42L92 charge pump (CP1). Its voltage can vary between CPGND and –CPVDD1.
6. The AGND1 and AGND2 pins should be tied together. The associated ground domain is referred to as AGND.

Table 3-3. Recommended Operating Conditions

Parameter		Symbol	Minimum	Typical	Maximum	Units
Digital supply range [1]	Core and FLL	DCVDD [2], FLLVDD [3]	1.14	1.2	1.26	V
Digital supply range	I/O	DBVDD	1.71	—	3.6 [4]	V
Charge pump supply range	CPVDD1	CPVDD1	1.71	1.8	1.89	V
	CPVDD2	CPVDD2	1.14	1.2	1.26	V
Analog supply range [5,6]		AVDD	1.71	1.8	1.89	V
Mic bias supply [7]		MICVDD	0.9	2.5	3.78	V
Ground [8]		DGND, AGND, CPGND, FLLGND, SUBGND	—	0	—	V
Power supply rise time [9,10]		DCVDD	10	—	2000	µs
		All other supplies	10	—	—	µs
Operating temperature range		T_A	–40	—	85	ºC

Note: There are no power sequencing requirements; the supplies may be enabled and disabled in any order.

1. The DCVDD and FLLVDD pins should be tied to a common supply rail. The associated power domain is referred to as DCVDD.
2. Sleep mode is supported for when DCVDD is below the limits noted, provided that AVDD and DBVDD are present.
3. It is recommended to connect a 120-Ω resistor in series with the FLLVDD pin connection. Note that the minimum voltage limit applies at the supply end of the 120-Ω resistor in this case.
4. If the SLIMbus interface is enabled, the maximum DBVDD voltage is 1.98 V.
5. The AVDD1 and AVDD2 pins should be tied together. The associated power domain is referred to as AVDD.
6. The AGND1 and AGND2 pins should be tied together. The associated ground domain is referred to as AGND.
7. An internal charge pump and LDO (powered by CPVDD1) provide the mic bias supply; the MICVDD pin must not be connected to an external supply.
8. The impedance between DGND, AGND, CPGND, FLLGND, and SUBGND must not exceed 0.1 Ω.
9. If the DCVDD rise time exceeds 2 ms, RESET must be asserted during the rise and held asserted until after DCVDD is within the recommended operating limits.
10. The specified minimum power supply rise times assume a minimum decoupling capacitance of 100 nF per pin. However, Cirrus Logic strongly advises that the recommended decoupling capacitors are present on the PCB and that appropriate layout guidelines are observed. The specified minimum power supply rise times also assume a maximum PCB inductance of 10 nH between decoupling capacitor and pin.

Table 3-4. Analog Input Signal Level—IN1xx, IN2xx

Test conditions (unless specified otherwise): AVDD = 1.8V; with the exception of the condition noted, the following electrical characteristics are valid across the full range of recommended operating conditions.

Parameter		Minimum	Typical	Maximum	Units
Full-scale input signal level (0 dBFS output)	Single-ended PGA input, 0 dB PGA gain	—	0.5	—	V_{RMS}
		—	–6	—	dBV
	Differential PGA input, 0 dB PGA gain	—	1	—	V_{RMS}
		—	0	—	dBV

Notes:
- The full-scale input signal level is also the maximum analog input level, before clipping occurs.
- The maximum input signal level is reduced by 6 dB if mid-power operation is selected (IN*n*_OSR = 100); the maximum signal level corresponds to –6 dBFS at the respective ADC outputs in this case.
- The full-scale input signal level changes in proportion with AVDD. For differential input, it is calculated as AVDD / 1.8.
- A 1.0V_{RMS} differential signal equates to 0.5V_{RMS}/–6dBV per input.
- A sinusoidal input signal is assumed.

Table 3-5. Analog Input Pin Characteristics

Test conditions (unless specified otherwise): T_A = +25ºC; with the exception of the condition noted, the following electrical characteristics are valid across the full range of recommended operating conditions.

Parameter		Minimum	Typical	Maximum	Units
Input resistance	Single-ended PGA input, All PGA gain settings	9	11	—	kΩ
	Differential PGA input, All PGA gain settings	17	22	—	kΩ
Input capacitance		—	—	5	pF

Table 3-6. Analog Input Gain—Programmable Gain Amplifiers (PGAs)

The following electrical characteristics are valid across the full range of recommended operating conditions.

Parameter		Minimum	Typical	Maximum	Units
Minimum programmable gain		—	0	—	dB
Maximum programmable gain		—	31	—	dB
Programmable gain step size	Guaranteed monotonic	—	1	—	dB

Table 3-7. Digital Input Signal Level—DMICDAT*n*

The following electrical characteristics are valid across the full range of recommended operating conditions.

Parameter		Minimum	Typical	Maximum	Units
Full-scale input level [1]	0 dBFS digital core input, 0 dB gain	—	–6	—	dBFS

1. The digital input signal level is measured in dBFS, where 0 dBFS is a signal level equal to the full-scale range (FSR) of the PDM input. The FSR is defined as the amplitude of a 1-kHz sine wave whose positive and negative peaks are represented by the maximum and minimum digital codes respectively—this is the largest 1-kHz sine wave that can fit in the digital output range without clipping.

Table 3-8. Output Characteristics

The following electrical characteristics are valid across the full range of recommended operating conditions.

Parameter			Minimum	Typical	Maximum	Units
Line/headphone/earpiece output driver (HPOUT*n*L, HPOUT*n*R)	Load resistance	Normal operation, Single-Ended Mode	6	—	—	Ω
		Normal operation, Differential (BTL) Mode	15	—	—	Ω
		Device survival with load applied indefinitely	0	—	—	Ω
	Load capacitance	Single-Ended Mode	—	—	500	pF
		Differential (BTL) Mode	—	—	200	pF
Digital speaker output (SPKDAT)	Full-scale output level [1]	0 dBFS digital core output, 0 dB gain	—	–6	—	dBFS

1. The digital output signal level is measured in dBFS, where 0 dBFS is a signal level equal to the full-scale range (FSR) of the PDM output. The FSR is defined as the amplitude of a 1-kHz sine wave whose positive and negative peaks are represented by the maximum and minimum digital codes respectively—this is the largest 1-kHz sine wave that can fit in the digital output range without clipping.

Table 3-9. Input/Output Path Characteristics

Test conditions (unless specified otherwise): DBVDD = CPVDD1 = AVDD = 1.8 V, DCVDD = FLLVDD = CPVDD2 = 1.2 V; MICVDD = 3.1 V (powered from internal LDO); T_A = +25ºC; 1 kHz sinusoid signal; Fs = 48 kHz; PGA gain = 0 dB, 24-bit audio data.

Parameter			Min	Typ	Max	Units
Line/headphone/earpiece output driver (HPOUT*n*L, HPOUT*n*R)	DC offset at Load	Single-ended mode	—	50	—	μV
		Differential (BTL) mode	—	75	—	μV
Analog input paths (IN1xx, IN2xx) to ADC (Differential Input Mode)	SNR (A-weighted), defined in Table 3-1	20 Hz to 20 kHz, 48 kHz sample rate	91	99	—	dB
		20 Hz to 8 kHz, 16 kHz sample rate	—	104	—	dB
	THD, defined in Table 3-1	–1 dBV input	—	–87	—	dB
	THD+N, defined in Table 3-1	–1 dBV input	—	–88	–79	dB
	Channel separation (L/R), defined in Table 3-1	100 Hz to 10 kHz	—	109	—	dB
	Input-referred noise floor	A-weighted, PGA gain = +20 dB	—	2.6	—	μV$_{RMS}$
	CMRR, defined in Table 3-1	PGA gain = +30 dB	—	83	—	dB
		PGA gain = 0 dB	—	72	—	dB
	PSRR (DBVDD, CPVDD1, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	99	—	dB
		100 mV (peak-peak) 10 kHz	—	84	—	dB
	PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	100	—	dB
		100 mV (peak-peak) 10 kHz	—	82	—	dB
Analog input paths (IN1xx, IN2xx) to ADC (Single-Ended Input Mode)	SNR (A-weighted), defined in Table 3-1	20 Hz to 20 kHz, 48 kHz sample rate	87	98	—	dB
		20 Hz to 8 kHz, 16 kHz sample rate	—	108	—	dB
	THD, defined in Table 3-1	–7dB V input	—	–84	—	dB
	THD+N, defined in Table 3-1	–7dB V input	—	–83	–78	dB
	Channel separation (L/R), defined in Table 3-1	100 Hz to 10 kHz	—	107	—	dB
	Input-referred noise floor	A-weighted, PGA gain = +20 dB	—	4	—	μV$_{RMS}$
	PSRR (DBVDD, CPVDD1, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	76	—	dB
		100 mV (peak-peak) 10 kHz	—	52	—	dB
	PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	96	—	dB
		100 mV (peak-peak) 10 kHz	—	87	—	dB

Table 3-9. Input/Output Path Characteristics *(Cont.)*

Test conditions (unless specified otherwise): DBVDD = CPVDD1 = AVDD = 1.8 V, DCVDD = FLLVDD = CPVDD2 = 1.2 V; MICVDD = 3.1 V (powered from internal LDO); T_A = +25ºC; 1 kHz sinusoid signal; Fs = 48 kHz; PGA gain = 0 dB, 24-bit audio data.

Parameter			Min	Typ	Max	Units
Analog input paths (IN1xx, IN2xx) to ADC (Differential Input, Mid Power Mode)	SNR, defined in Table 3-1	A-weighted	—	88	—	dB
	THD, defined in Table 3-1	–7 dBV input	—	–81	—	dB
	THD+N, defined in Table 3-1	–7 dBV input	—	–80	—	dB
	Channel separation (L/R), defined in Table 3-1	100 Hz to 10 kHz	—	96	—	dB
	Input-referred noise floor	A-weighted, PGA gain = +20 dB	—	4.79	—	μV_{RMS}
	CMRR, defined in Table 3-1	PGA gain = +30 dB	—	73	—	dB
		PGA gain = 0 dB	—	81	—	dB
	PSRR (DBVDD, CPVDD1, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	93	—	dB
		100 mV (peak-peak) 10 kHz	—	75	—	dB
	PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	97	—	dB
		100 mV (peak-peak) 10 kHz	—	81	—	dB
DAC to line output (HPOUT1x, HPOUT2x; Load = 10 kΩ, 50 pF)	Full-scale output signal level	0 dBFS input	—	1	—	V_{RMS}
			—	0	—	dBV
	SNR, defined in Table 3-1	A-weighted, output signal = 1 V_{RMS}	—	125	—	dB
	Dynamic range, defined in Table 3-1	A-weighted, –60 dBFS input	108	117	—	dB
	THD+N, defined in Table 3-1	0 dBFS input	—	–100	–90	dB
	Channel separation (L/R), defined in Table 3-1	100 Hz to 10 kHz	—	95	—	dB
	Output noise floor	A-weighted	—	0.7	—	μV_{RMS}
	PSRR (DBVDD, CPVDD1, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	105	—	dB
		100 mV (peak-peak) 10 kHz	—	81	—	dB
	PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	108	—	dB
		100 mV (peak-peak) 10 kHz	—	81	—	dB
DAC to headphone output (HPOUT1x, HPOUT2x; R_L = 32 Ω)	Maximum output power	0.1% THD+N	—	33	—	mW
	SNR, defined in Table 3-1	A-weighted, output signal = 1 V_{RMS}	—	125	—	dB
	Dynamic range, defined in Table 3-1	A-weighted, –60 dBFS input	108	117	—	dB
	THD+N, defined in Table 3-1	P_O = 20 mW	—	–100	–90	dB
	THD+N, defined in Table 3-1	P_O = 2 mW	—	–96	—	dB
	Channel separation (L/R), defined in Table 3-1	100 Hz to 10 kHz	—	105	—	dB
	Output noise floor	A-weighted	—	0.6	—	μV_{RMS}
	PSRR (DBVDD, CPVDD1, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	126	—	dB
		100 mV (peak-peak) 10 kHz	—	103	—	dB
	PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	128	—	dB
		100 mV (peak-peak) 10 kHz	—	105	—	dB
DAC to headphone output (HPOUT1x, HPOUT2x; R_L = 16 Ω)	Maximum output power	0.1% THD+N	—	46	—	mW
	SNR, defined in Table 3-1	A-weighted, output signal = 1 V_{RMS}	—	125	—	dB
	Dynamic range, defined in Table 3-1	A-weighted, –60 dBFS input	108	117	—	dB
	THD+N, defined in Table 3-1	P_O = 20 mW	—	–97	–90	dB
	THD+N, defined in Table 3-1	P_O = 2 mW	—	–95	—	dB
	Channel separation (L/R), defined in Table 3-1	100 Hz to 10 kHz	—	97	—	dB
	Output noise floor	A-weighted	—	0.6	—	μV_{RMS}
	PSRR (DBVDD, CPVDD1, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	127	—	dB
		100 mV (peak-peak) 10 kHz	—	107	—	dB
	PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	127	—	dB
		100 mV (peak-peak) 10 kHz	—	108	—	dB
DAC to headphone output (HPOUT1L+HPOUT1R, HPOUT2L+HPOUT2R; Stereo differential output, R_L = 32 Ω BTL)	Maximum output power	0.1% THD+N	—	109	—	mW
	SNR, defined in Table 3-1	A-weighted, output signal = 2 V_{RMS}	—	127	—	dB
	Dynamic range, defined in Table 3-1	A-weighted, –60 dBFS input	—	115	—	dB
	THD+N, defined in Table 3-1	P_O = 75 mW	—	–100	—	dB
	THD+N, defined in Table 3-1	P_O = 5 mW	—	–97	—	dB
	Output noise floor	A-weighted	—	0.36	—	μV_{RMS}
	PSRR (DBVDD, CPVDD1, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	120	—	dB
		100 mV (peak-peak) 10 kHz	—	90	—	dB
	PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	120	—	dB
		100 mV (peak-peak) 10 kHz	—	90	—	dB

Table 3-9. Input/Output Path Characteristics *(Cont.)*

Test conditions (unless specified otherwise): DBVDD = CPVDD1 = AVDD = 1.8 V, DCVDD = FLLVDD = CPVDD2 = 1.2 V; MICVDD = 3.1 V (powered from internal LDO); T_A = +25ºC; 1 kHz sinusoid signal; Fs = 48 kHz; PGA gain = 0 dB, 24-bit audio data.

Parameter			Min	Typ	Max	Units
DAC to line output (HPOUT3*x*, HPOUT4*x*; Load = 10 kΩ, 50 pF)	Full-scale output signal level	0 dBFS input	—	1	—	V_{RMS}
			—	0	—	dBV
	SNR, defined in Table 3-1	A-weighted, output signal = 1 V_{RMS}	115	125	—	dB
	Dynamic range, defined in Table 3-1	A-weighted, –60 dBFS input	107	115	—	dB
	THD, defined in Table 3-1	0 dBFS input	—	–92	—	dB
	THD+N, defined in Table 3-1	0 dBFS input	—	–91	–85	dB
	Channel separation (L/R), defined in Table 3-1	100 Hz to 10 kHz	—	90	—	dB
	Output noise floor	A-weighted	—	0.63	—	μV_{RMS}
	PSRR (DBVDD, CPVDD1, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	110	—	dB
		100 mV (peak-peak) 10 kHz	—	78	—	dB
	PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	99	—	dB
		100 mV (peak-peak) 10 kHz	—	69	—	dB
DAC to headphone output (HPOUT3*x*, HPOUT4*x*; R_L = 32 Ω)	Maximum output power	0.1% THD+N	—	33	—	mW
	SNR, defined in Table 3-1	A-weighted, output signal = 1 V_{RMS}	—	124	—	dB
	Dynamic range, defined in Table 3-1	A-weighted, –60 dBFS input	107	115	—	dB
	THD, defined in Table 3-1	P_O = 20 mW	—	–93	—	dB
	THD+N, defined in Table 3-1	P_O = 20 mW	—	–90	–85	dB
	THD, defined in Table 3-1	P_O = 2 mW	—	–94	—	dB
	THD+N, defined in Table 3-1	P_O = 2 mW	—	–92	—	dB
	Channel separation (L/R), defined in Table 3-1	100 Hz to 10 kHz	—	102	—	dB
	Output noise floor	A-weighted	—	0.63	—	μV_{RMS}
	PSRR (DBVDD, CPVDD1, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	127	—	dB
		100 mV (peak-peak) 10 kHz	—	100	—	dB
	PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	120	—	dB
		100 mV (peak-peak) 10 kHz	—	95	—	dB
DAC to headphone output (HPOUT3*x*, HPOUT4*x*; R_L = 16 Ω)	Maximum output power	0.1% THD+N	—	46	—	mW
	SNR, defined in Table 3-1	A-weighted, output signal = 1 V_{RMS}	—	124	—	dB
	Dynamic range, defined in Table 3-1	A-weighted, –60 dBFS input	107	115	—	dB
	THD, defined in Table 3-1	P_O = 20 mW	—	–94	—	dB
	THD+N, defined in Table 3-1	P_O = 20 mW	—	–89	–80	dB
	THD, defined in Table 3-1	P_O = 2 mW	—	–91	—	dB
	THD+N, defined in Table 3-1	P_O = 2 mW	—	–89	—	dB
	Channel separation (L/R), defined in Table 3-1	100 Hz to 10 kHz	—	100	—	dB
	Output noise floor	A-weighted	—	0.63	—	μV_{RMS}
	PSRR (DBVDD, CPVDD1, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	128	—	dB
		100 mV (peak-peak) 10 kHz	—	104	—	dB
	PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	125	—	dB
		100 mV (peak-peak) 10 kHz	—	97	—	dB
DAC to earpiece output (HPOUT3L+HPOUT3R, HPOUT4L+HPOUT4R, Mono Mode, R_L = 32 Ω BTL)	Maximum output power	0.1% THD+N	—	115	—	mW
	SNR, defined in Table 3-1	A-weighted, output signal = 2 V_{RMS}	—	129	—	dB
	Dynamic range, defined in Table 3-1	A-weighted, –60 dBFS input	110	120	—	dB
	THD, defined in Table 3-1	P_O = 75 mW	—	–99	—	dB
	THD+N, defined in Table 3-1	P_O = 75 mW	—	–97	—	dB
	THD, defined in Table 3-1	P_O = 5 mW	—	–98	—	dB
	THD+N, defined in Table 3-1	P_O = 5 mW	—	–94	—	dB
	Output noise floor	A-weighted	—	0.36	—	μV_{RMS}
	PSRR (DBVDD, CPVDD1, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	127	—	dB
		100 mV (peak-peak) 10 kHz	—	106	—	dB
	PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	125	—	dB
		100 mV (peak-peak) 10 kHz	—	101	—	dB

Table 3-9. Input/Output Path Characteristics *(Cont.)*

Test conditions (unless specified otherwise): DBVDD = CPVDD1 = AVDD = 1.8 V, DCVDD = FLLVDD = CPVDD2 = 1.2 V; MICVDD = 3.1 V (powered from internal LDO); T_A = +25ºC; 1 kHz sinusoid signal; Fs = 48 kHz; PGA gain = 0 dB, 24-bit audio data.

Parameter			Min	Typ	Max	Units
DAC to earpiece output (HPOUT3L+HPOUT3R, HPOUT4L+HPOUT4R, Mono Mode, R_L = 16 Ω BTL)	Maximum output power	0.1% THD+N	—	138	—	mW
	SNR, defined in Table 3-1	A-weighted, output signal = 2 V_{RMS}	—	128	—	dB
	Dynamic range, defined in Table 3-1	A-weighted, –60 dBFS input	110	120	—	dB
	THD, defined in Table 3-1	P_O = 75 mW	—	–97	—	dB
	THD+N, defined in Table 3-1	P_O = 75 mW	—	–95	—	dB
	THD, defined in Table 3-1	P_O = 5 mW	—	–96	—	dB
	THD+N, defined in Table 3-1	P_O = 5 mW	—	–94	—	dB
	Output noise floor	A-weighted	—	0.4	—	μV_{RMS}
	PSRR (DBVDD, CPVDD1, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	125	—	dB
		100 mV (peak-peak) 10 kHz	—	106	—	dB
	PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	125	—	dB
		100 mV (peak-peak) 10 kHz	—	101	—	dB

Table 3-10. Digital Input/Output

The following electrical characteristics are valid across the full range of recommended operating conditions.

Parameter			Minimum	Typical	Maximum	Units
Digital I/O (except DMICDAT*n* and DMICCLK*n*) [1,2]	Input HIGH level	V_{DBVDD} = 1.71–1.98 V	0.75 × DBVDD	—	—	V
		V_{DBVDD} = 2.5 V ±10%	0.8 × DBVDD	—	—	V
		V_{DBVDD} = 3.3 V ±10%	0.7 × DBVDD	—	—	V
	Input LOW level	V_{DBVDD} = 1.71–1.98 V	—	—	0.3 × DBVDD	V
		V_{DBVDD} = 2.5 V ±10%	—	—	0.25 × DBVDD	V
		V_{DBVDD} = 3.3 V ±10%	—	—	0.2 × DBVDD	V
	Output HIGH level (I_{OH} = 1 mA)	V_{DBVDD} = 1.71–1.98 V	0.75 × DBVDD	—	—	V
		V_{DBVDD} = 2.5 V ±10%	0.65 × DBVDD	—	—	V
		V_{DBVDD} = 3.3 V ±10%	0.7 × DBVDD	—	—	V
	Output LOW level (I_{OL} = 1mA)	V_{DBVDDn} = 1.71–1.98 V	—	—	0.25 × DBVDD	V
		V_{DBVDDn} = 2.5 V ±10%	—	—	0.3 × DBVDD	V
		V_{DBVDDn} = 3.3 V ±10%	—	—	0.15 × DBVDD	V
	Input capacitance		—	—	5	pF
	Input leakage		–10	—	10	μA
	Pull-up/pull-down resistance (where applicable)		35	—	55	kΩ
DMIC I/O (DMICDAT*n* and DMICCLK*n*) [2,3]	DMICDAT*n* input HIGH level		0.65 × V_{SUP}	—	—	V
	DMICDAT*n* input LOW level		—	—	0.35 × V_{SUP}	V
	DMICCLK*n* output HIGH level	I_{OH} = 1 mA	0.8 × V_{SUP}	—	—	V
	DMICCLK*n* output LOW level	I_{OL} = –1 mA	—	—	0.2 × V_{SUP}	V
	Input capacitance		—	25		pF
	Input leakage		–1	—	1	μA
GPIO*n*	Clock output frequency	GPIO pin as OPCLK or FLL output	—	—	50	MHz

1. Digital I/O is referenced to DBVDD.
2. Note that digital input pins should not be left unconnected or floating.
3. DMICDAT*n* and DMICCLK*n* are referenced to a selectable supply, V_{SUP}, according to the IN*n*_DMIC_SUP fields.

Table 3-11. Miscellaneous Characteristics

Test conditions (unless specified otherwise): DBVDD = CPVDD1 = AVDD = 1.8 V, DCVDD = FLLVDD = CPVDD2 = 1.2 V; MICVDD = 3.1 V (powered from internal LDO); T_A = +25ºC; 1 kHz sinusoid signal; Fs = 48 kHz; PGA gain = 0 dB, 24-bit audio data.

Parameter		Min	Typ	Max	Units
Microphone bias (MICBIAS*nx*) [1]	Minimum bias voltage [2]	—	1.5	—	V
	Maximum bias voltage	—	2.8	—	V
	Bias voltage output step size	—	0.1	—	V
	Bias voltage accuracy	–5%	—	+5%	V
	Bias current [3] Regulator Mode (MICB*n*_BYPASS = 0), $V_{MICVDD} - V_{MICBIAS}$ >200 mV	—	—	2.4	mA
	Bypass Mode (MICB*n*_BYPASS = 1)	—	—	5.0	mA
	Output noise density Regulator Mode (MICB*n*_BYPASS = 0), MICB*n*_LVL = 0x4, Load current = 1 mA, Measured at 1 kHz	—	50	—	nV/√Hz
	Integrated noise voltage Regulator Mode (MICB*n*_BYPASS = 0), MICB*n*_LVL = 0x4, Load current = 1 mA, 100 Hz to 7 kHz, A-weighted	—	4	—	μV_{RMS}
	PSRR (DBVDD, CPVDD1, AVDD), defined in Table 3-1 100 mV (peak-peak) 217 Hz	—	105	—	dB
	100 mV (peak-peak) 10 kHz	—	95	—	dB
	PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1 100 mV (peak-peak) 217 Hz	—	99	—	dB
	100 mV (peak-peak) 10 kHz	—	92	—	dB
	Load capacitance [3] Regulator Mode (MICB*n*_BYPASS = 0), MICB*n*_EXT_CAP = 0	—	—	50	pF
	Regulator Mode (MICB*n*_BYPASS = 0), MICB*n*_EXT_CAP = 1	0.1	1.0	10	µF
	Output discharge resistance MICB*nx*_ENA = 0, MICB*nx*_DISCH = 1	—	2	—	kΩ
General-purpose switch [4]	Switch resistance Switch closed, I = 1 mA	—	40	—	Ω
	Switch open	—	100	—	MΩ
External Accessory Detect	Headphone detection load impedance range: Detection via HPDET1 (HPD_SENSE_SEL = 0100) or HPDET2 (HPD_SENSE_SEL = 0101) HPD_IMPEDANCE_RANGE = 00	4	—	30	Ω
	HPD_IMPEDANCE_RANGE = 01	8	—	100	Ω
	HPD_IMPEDANCE_RANGE = 10	100	—	1000	Ω
	HPD_IMPEDANCE_RANGE = 11	1000	—	10000	Ω
	Headphone detection load impedance range: Detection via MICDET*n* or JACKDET*n* pins	400	—	6000	Ω
	Headphone detection accuracy: (HPD_DACVAL, HPDET*n* pin) HPD_IMPEDANCE_RANGE = 01 or 10	–5	—	+5	%
	HPD_IMPEDANCE_RANGE = 00 or 11	–10	—	+10	%
	Headphone detection accuracy (HPD_LVL, MICDET*n* or JACKDET*n* pin)	–20	—	+20	%
	Microphone impedance detection range: (MICD*n*_ADC_MODE = 0, 2.2 kΩ ±2% MICBIAS resistor. [5]) for MICD*n*_LVL[0] = 1	0	—	70	Ω
	for MICD*n*_LVL[1] = 1	110	—	180	Ω
	for MICD*n*_LVL[2] = 1	210	—	290	Ω
	for MICD*n*_LVL[3] = 1	360	—	680	Ω
	for MICD*n*_LVL[8] = 1	1000	—	30000	Ω
	Jack-detection input threshold voltage (JACKDET*n*) Detection on JACKDET1, Jack insertion	—	0.9	—	V
	Detection on JACKDET1, Jack removal	—	1.65	—	V
	Detection on JACKDET2/3, Jack insertion	—	0.27	—	V
	Detection on JACKDET2/3, Jack removal	—	0.9	—	V
MICVDD Charge Pump and Regulator (CP2 and LDO2)	Output voltage	0.9	2.7	3.3	V
	Programmable output voltage step size LDO2_VSEL = 0x00–0x14 (0.9–1.4V)	—	25	—	mV
	LDO2_VSEL = 0x14 to 0x27 (1.4 V–3.3 V)	—	100	—	mV
	Maximum output current	—	8	—	mA
	Start-up time 4.7 µF on MICVDD	—	1.0	2.5	ms
Frequency-Locked Loop (FLL1, FLL2)	Output frequency	45	—	50	MHz
	Lock Time F_{REF} = 32 kHz, F_{FLL} = 49.152 MHz	—	5	—	ms
	F_{REF} = 12 MHz, F_{FLL} = 49.152 MHz	—	1	—	ms
RESET pin input	RESET input pulse width [6]	1	—	—	µs

1. No capacitor on MICBIAS*nx*. In Regulator Mode, it is required that $V_{MICVDD} - V_{MICBIAS}$ > 200 mV.
2. Regulator Mode (MICB*n*_BYPASS = 0), Load current ≤ 1.0 mA.
3. Bias current and load capacitance specifications are per MICBIAS generator (MICBIAS1 or MICBIAS2).
4. The GPSW*n*N pin voltage must not exceed GPSW*n*P + 0.3 V. See Table 3-2 for voltage limits applicable to the GPSW*n*P and GPSW*n*N pins.
5. These characteristics assume no other component is connected to MICDET*n*.
6. To trigger a hardware reset, the RESET input must be asserted for longer than this duration.

Table 3-12. Device Reset Thresholds

The following electrical characteristics are valid across the full range of recommended operating conditions.

Parameter		Symbol	Minimum	Typical	Maximum	Units
AVDD reset threshold	V_{AVDD} rising	V_{AVDD}	—	—	1.66	V
	V_{AVDD} falling		1.06	—	1.44	V
DCVDD reset threshold	V_{DCVDD} rising	V_{DCVDD}	—	—	1.04	V
	V_{DCVDD} falling		0.49	—	0.70	V
DBVDD Reset threshold	V_{DBVDD} rising	V_{DBVDD}	—	—	1.66	V
	V_{DBVDD} falling		1.06	—	1.44	V

Note: The reset thresholds are derived from simulations only, across all operational and process corners. Device performance is not assured outside the voltage ranges defined in Table 3-3.

Table 3-13. System Clock and Frequency-Locked Loop (FLL)

The following timing information is valid across the full range of recommended operating conditions.

Parameter			Minimum	Typical	Maximum	Units
Master clock timing (MCLK1, MCLK2, MCLK3) [1]	MCLK cycle time	MCLK as input to FLL, FLLn_REFCLK_DIV = 00	74	—	—	ns
		MCLK as input to FLL, FLLn_REFCLK_DIV = 01	37	—	—	ns
		MCLK as input to FLL, FLLn_REFCLK_DIV = 10	18	—	—	ns
		MCLK as input to FLL, FLLn_REFCLK_DIV = 11	12.5	—	—	ns
		MCLK as direct SYSCLK or ASYNCCLK source	40	—	—	ns
	MCLK duty cycle	MCLK as input to FLL	80:20	—	20:80	%
		MCLK as direct SYSCLK or ASYNCCLK source	60:40	—	40:60	%
Frequency-locked loop (FLL1, FLL2)	FLL input frequency	FLLn_REFCLK_DIV = 00	0.032	—	13	MHz
		FLLn_REFCLK_DIV = 01	0.064	—	26	MHz
		FLLn_REFCLK_DIV = 11	0.128	—	52	MHz
		FLLn_REFCLK_DIV = 11	0.256	—	80	MHz
Internal clocking	SYSCLK frequency	SYSCLK_FREQ = 000, SYSCLK_FRAC = 0	−1%	6.144	+1%	MHz
		SYSCLK_FREQ = 000, SYSCLK_FRAC = 1	−1%	5.6448	+1%	MHz
		SYSCLK_FREQ = 001, SYSCLK_FRAC = 0	−1%	12.288	+1%	MHz
		SYSCLK_FREQ = 001, SYSCLK_FRAC = 1	−1%	11.2896	+1%	MHz
		SYSCLK_FREQ = 010, SYSCLK_FRAC = 0	−1%	24.576	+1%	MHz
		SYSCLK_FREQ = 010, SYSCLK_FRAC = 1	−1%	22.5792	+1%	MHz
		SYSCLK_FREQ = 011, SYSCLK_FRAC = 0	−1%	49.152	+1%	MHz
		SYSCLK_FREQ = 011, SYSCLK_FRAC = 1	−1%	45.1584	+1%	MHz
		SYSCLK_FREQ = 100, SYSCLK_FRAC = 0	−1%	98.304	+1%	MHz
		SYSCLK_FREQ = 100, SYSCLK_FRAC = 1	−1%	90.3168	+1%	MHz
	ASYNCCLK frequency	ASYNC_CLK_FREQ = 000	−1%	6.144	+1%	MHz
			−1%	5.6448	+1%	MHz
		ASYNC_CLK_FREQ = 001	−1%	12.288	+1%	MHz
			−1%	11.2896	+1%	MHz
		ASYNC_CLK_FREQ = 010	−1%	24.576	+1%	MHz
			−1%	22.5792	+1%	MHz
		ASYNC_CLK_FREQ = 011	−1%	49.152	+1%	MHz
			−1%	45.1584	+1%	MHz
		ASYNC_CLK_FREQ = 100	−1%	98.304	+1%	MHz
			−1%	90.3168	+1%	MHz
	DSPCLK frequency		5	—	150	MHz

1. If MCLK1, MCLK2, or MCLK3 is selected as a source for SYSCLK or ASYNCCLK (either directly or via one of the FLLs), the frequency must be within 1% of the applicable SYSCLK_FREQ or ASYNC_CLK_FREQ setting.
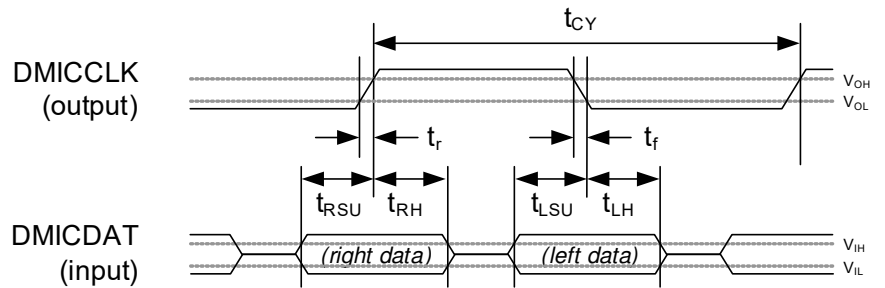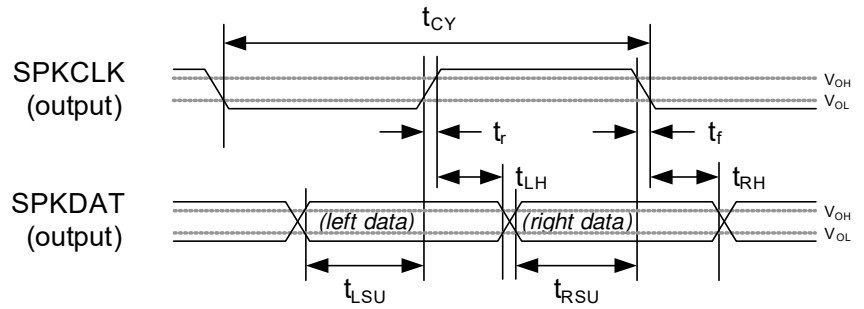
Table 3-14. Digital Microphone (DMIC) Interface Timing

The following timing information is valid across the full range of recommended operating conditions.

Parameter [1]	Symbol	Minimum	Typical	Maximum	Units
DMICCLK*n* cycle time	t_{CY}	160	163	1432	ns
DMICCLK*n* duty cycle	—	45	—	55	%
DMICCLK*n* rise/fall time (25-pF load, 1.8-V supply)	t_r, t_f	5	—	30	ns
DMICDAT*n* (left) setup time to falling DMICCLK edge	t_{LSU}	15	—	—	ns
DMICDAT*n* (left) hold time from falling DMICCLK edge	t_{LH}	0	—	—	ns
DMICDAT*n* (right) setup time to rising DMICCLK edge	t_{RSU}	15	—	—	ns
DMICDAT*n* (right) hold time from rising DMICCLK edge	t_{RH}	0	—	—	ns

Note: The voltage reference for the DMIC interfaces is selectable, using the IN*n*_DMIC_SUP fields—each interface may be referenced to MICVDD, MICBIAS1, or MICBIAS2.

1. DMIC interface timing

Table 3-15. Digital Speaker (PDM) Interface Timing

The following timing information is valid across the full range of recommended operating conditions.

	Parameter	Symbol	Minimum	Typical	Maximum	Units
Mode A [1]	SPKCLK cycle time	t_{CY}	160	163	358	ns
	SPKCLK duty cycle	—	45	—	55	%
	SPKCLK rise/fall time (25-pF load)	t_r, t_f	2	—	8	ns
	SPKDAT set-up time to SPKCLK rising edge (left channel)	t_{LSU}	30	—	—	ns
	SPKDAT hold time from SPKCLK rising edge (left channel)	t_{LH}	30	—	—	ns
	SPKDAT set-up time to SPKCLK falling edge (right channel)	t_{RSU}	30	—	—	ns
	SPKDAT hold time from SPKCLK falling edge (right channel)	t_{RH}	30	—	—	ns
Mode B [2]	SPKCLK cycle time	t_{CY}	160	163	358	ns
	SPKCLK duty cycle	—	45	—	55	%
	SPKCLK rise/fall time (25-pF load)	t_r, t_f	2	—	8	ns
	SPKDAT enable from SPKCLK rising edge (right channel)	t_{REN}	—	—	15	ns
	SPKDAT disable to SPKCLK falling edge (right channel)	t_{RDIS}	—	—	5	ns
	SPKDAT enable from SPKCLK falling edge (left channel)	t_{LEN}	—	—	15	ns
	SPKDAT disable to SPKCLK rising edge (left channel)	t_{LDIS}	—	—	5	ns

1. Digital speaker (PDM) interface timing—Mode A
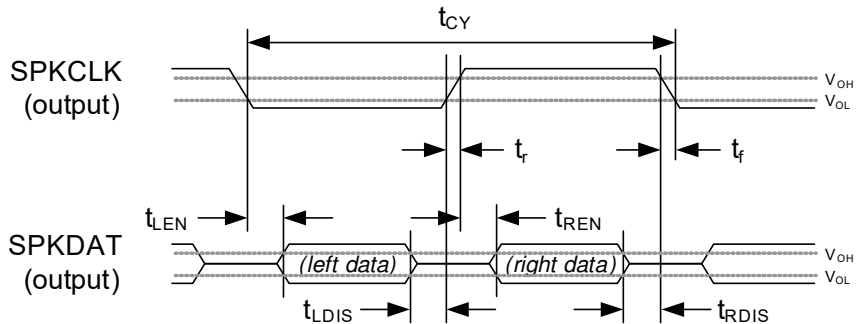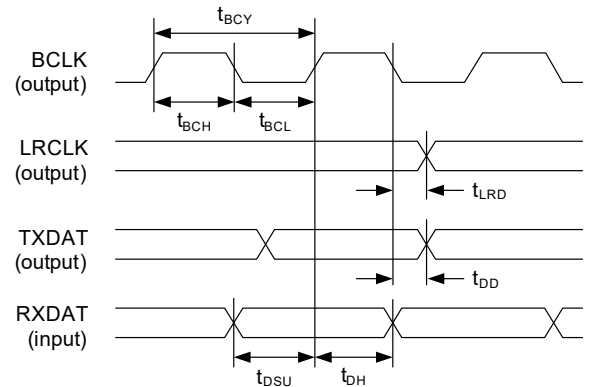

2. Digital speaker (PDM) interface timing—Mode B

Table 3-16. Digital Audio Interface—Master Mode

Test conditions (unless specified otherwise): C_{LOAD} = 25 pF (output pins); BCLK slew (10% to 90%) = 3.7–5.6 ns; with the exception of the conditions noted, the following electrical characteristics are valid across the full range of recommended operating conditions.

Parameter [1]		Symbol	Minimum	Typical	Maximum	Units
Master Mode	AIF*n*BCLK cycle time	t_{BCY}	40	—	—	ns
	AIF*n*BCLK pulse width high	t_{BCH}	18	—	—	ns
	AIF*n*BCLK pulse width low	t_{BCL}	18	—	—	ns
	AIF*n*LRCLK propagation delay from BCLK falling edge [2]	t_{LRD}	0	—	8.3	ns
	AIF*n*TXDAT propagation delay from BCLK falling edge	t_{DD}	0	—	5	ns
	AIF*n*RXDAT setup time to BCLK rising edge	t_{DSU}	11	—	—	ns
	AIF*n*RXDAT hold time from BCLK rising edge	t_{DH}	0	—	—	ns
Master Mode, Slave LRCLK	AIF*n*LRCLK setup time to BCLK rising edge	t_{LRSU}	14	—	—	ns
	AIF*n*LRCLK hold time from BCLK rising edge	t_{LRH}	0	—	—	ns

Notes: The descriptions above assume noninverted polarity of AIF*n*BCLK.

1. Digital audio interface timing—Master Mode. Note that BCLK and LRCLK outputs can be inverted if required; the figure shows the default, noninverted polarity.

2. The timing of the AIF*n*LRCLK signal is selectable. If the LRCLK advance option is enabled, the LRCLK transition is timed relative to the preceding BCLK edge. Under the required condition that BCLK is inverted in this case, the LRCLK transition is still timed relative to the falling BCLK edge.
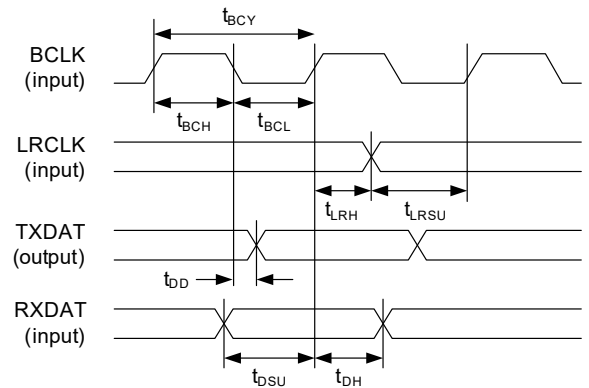
Table 3-17. Digital Audio Interface—Slave Mode

The following timing information is valid across the full range of recommended operating conditions, unless otherwise noted.

Parameter [1,2]		Symbol	Min	Typ	Max	Units
AIF*n*BCLK cycle time		t_{BCY}	40	—	—	ns
AIF*n*BCLK pulse width high	BCLK as direct SYSCLK or ASYNCCLK source	t_{BCH}	16	—	—	ns
	All other conditions	t_{BCH}	14	—	—	ns
AIF*n*BCLK pulse width low	BCLK as direct SYSCLK or ASYNCCLK source	t_{BCL}	16	—	—	ns
	All other conditions	t_{BCL}	14	—	—	ns
C_{LOAD} = 15 pF (output pins), BCLK slew (10%–90%) = 3 ns	AIF*n*LRCLK set-up time to BCLK rising edge	t_{LRSU}	7	—	—	ns
	AIF*n*LRCLK hold time from BCLK rising edge	t_{LRH}	0	—	—	ns
	AIF*n*TXDAT propagation delay from BCLK falling edge	t_{DD}	0	—	12.2	ns
	AIF*n*RXDAT set-up time to BCLK rising edge	t_{DSU}	2	—		ns
	AIF*n*RXDAT hold time from BCLK rising edge	t_{DH}	0	—		ns
	Master LRCLK, AIF*n*LRCLK propagation delay from BCLK falling edge	t_{LRD}	—	—	14.8	ns
C_{LOAD} = 25 pF (output pins), BCLK slew (10%–90%) = 6 ns	AIF*n*LRCLK set-up time to BCLK rising edge	t_{LRSU}	7	—		ns
	AIF*n*LRCLK hold time from BCLK rising edge	t_{LRH}	0	—		ns
	AIF*n*TXDAT propagation delay from BCLK falling edge	t_{DD}	0	—	14.2	ns
	AIF*n*RXDAT set-up time to BCLK rising edge	t_{DSU}	2	—		ns
	AIF*n*RXDAT hold time from BCLK rising edge	t_{DH}	0	—		ns
	Master LRCLK, AIF*n*LRCLK propagation delay from BCLK falling edge	t_{LRD}	—	—	15.9	ns

Note: The descriptions above assume noninverted polarity of AIF*n*BCLK.

1. Digital audio interface timing—Slave Mode. Note that BCLK and LRCLK inputs can be inverted if required; the figure shows the default, noninverted polarity.

2. If AIF*n*BCLK or AIF*n*LRCLK is selected as a source for SYSCLK or ASYNCCLK (either directly or via one of the FLLs), the frequency must be within 1% of the applicable SYSCLK_FREQ or ASYNC_CLK_FREQ setting.

Table 3-18. Digital Audio Interface Timing—TDM Mode

The following timing information is valid across the full range of recommended operating conditions, unless otherwise noted.

Parameter [1]		Min	Typ	Max	Units
Master Mode—C_{LOAD} (AIF*n*TXDAT) = 15 to 25 pF. BCLK slew (10%–90%) = 3.7ns to 5.6 ns.	AIF*n*TXDAT enable time from BCLK falling edge	0	—	—	ns
	AIF*n*TXDAT disable time from BCLK falling edge	—	—	6	ns
Slave Mode—C_{LOAD} (AIF*n*TXDAT) = 15 pF). BCLK slew (10%–90%) = 3 ns	AIF*n*TXDAT enable time from BCLK falling edge	2	—	—	ns
	AIF*n*TXDAT disable time from BCLK falling edge	—	—	12.2	ns
Slave Mode—C_{LOAD} (AIF*n*TXDAT) = 25 pF). BCLK slew (10%–90%) = 6 ns	AIF*n*TXDAT enable time from BCLK falling edge	2	—	—	ns
	AIF*n*TXDAT disable time from BCLK falling edge	—	—	14.2	ns

Note: If TDM operation is used on the AIF*n*TXDAT pins, it is important that two devices do not attempt to drive the AIF*n*TXDAT pin simultaneously. To support this requirement, the AIF*n*TXDAT pins can be configured to be tristated when not outputting data.

1. Digital audio interface timing—TDM Mode. The timing of the AIF*n*TXDAT tristating at the start and end of the data transmission is shown.
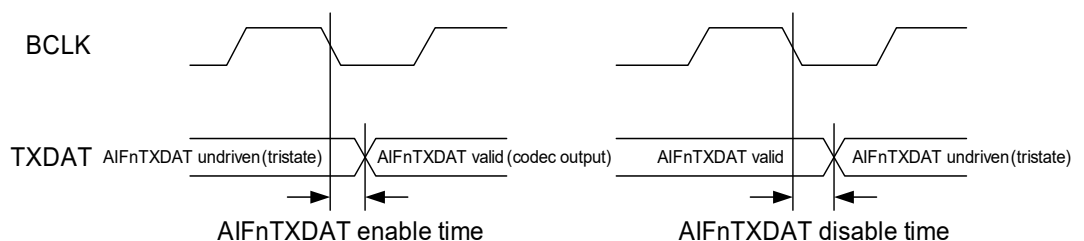
Table 3-19. Control Interface Timing—Two-Wire (I2C) Mode

The following timing information is valid across the full range of recommended operating conditions.

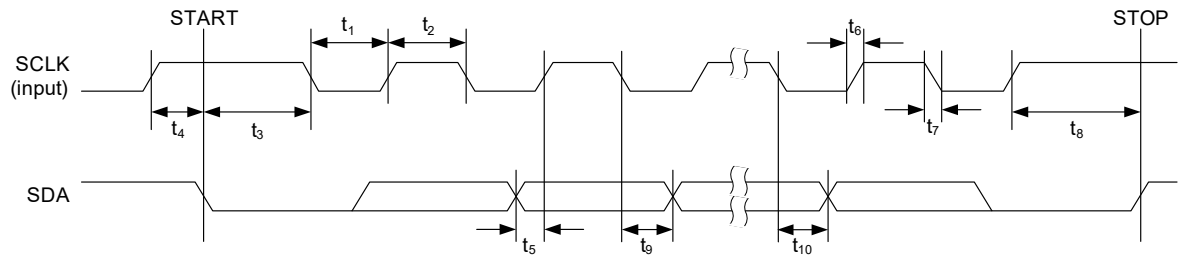| Parameter [1]		Symbol	Min	Typ	Max	Units
SCLK frequency		—	—	—	3400	kHz
SCLK pulse-width low		t_1	160	—	—	ns
SCLK pulse-width high		t_2	100	—	—	ns
Hold time (start condition)		t_3	160	—	—	ns
Setup time (start condition)		t_4	160	—	—	ns
SDA, SCLK rise time (10%–90%)	SCLK frequency > 1.7 MHz	t_6	—	—	80	ns
	SCLK frequency > 1 MHz	t_6	—	—	160	ns
	SCLK frequency $\leq$ 1 MHz	t_6	—	—	2000	ns
SDA, SCLK fall time (90%–10%)	SCLK frequency > 1.7 MHz	t_7	—	—	60	ns
	SCLK frequency > 1 MHz	t_7	—	—	160	ns
	SCLK frequency $\leq$ 1 MHz	t_7	—	—	200	ns
Setup time (stop condition)		t_8	160	—	—	ns
SDA setup time (data input)		t_5	40	—	—	ns
SDA hold time (data input)		t_9	0	—	—	ns
SDA valid time (data/ACK output)	SCLK slew (90%–10%) = 20ns, C_{LOAD} (SDA) = 15 pF	t_{10}	—	—	40	ns
	SCLK slew (90%–10%) = 60ns, C_{LOAD} (SDA) = 100 pF	t_{10}	—	—	130	ns
	SCLK slew (90%–10%) = 160ns, C_{LOAD} (SDA) = 400 pF	t_{10}	—	—	190	ns
	SCLK slew (90%–10%) = 200ns, C_{LOAD} (SDA) = 550 pF	t_{10}	—	—	220	ns
Pulse width of spikes that are suppressed		t_{ps}	0	—	25	ns

1. Control interface timing—I2C Mode

Table 3-20. Control Interface Timing—Four-Wire (SPI) Mode

The following timing information is valid across the full range of recommended operating conditions.

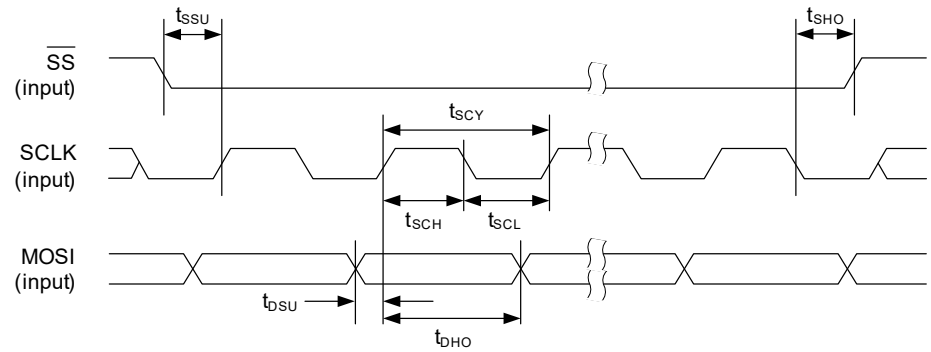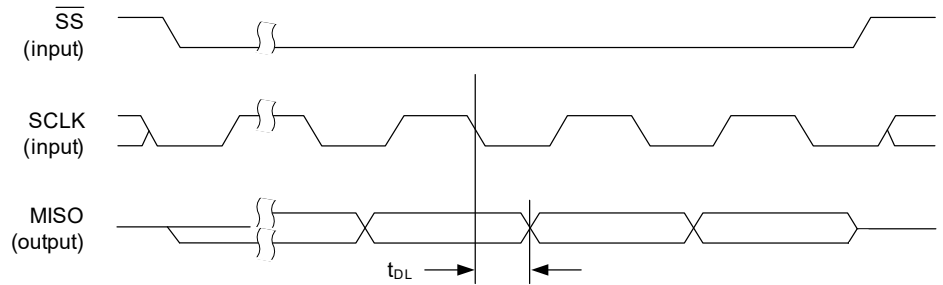| Parameter [1], [2]		Symbol	Min	Typ	Max	Units
$\overline{SS}$ falling edge to SCLK rising edge		t_{SSU}	2.6	—	—	ns
SCLK falling edge to $\overline{SS}$ rising edge		t_{SHO}	0	—	—	ns
SCLK pulse cycle time	SYSCLK disabled (SYSCLK_ENA = 0)	t_{SCY}	38.4	—	—	ns
	SYSCLK_ENA = 1, SYSCLK_FREQ = 000	t_{SCY}	76.8	—	—	ns
	SYSCLK_ENA = 1, SYSCLK_FREQ > 000	t_{SCY}	38.4	—	—	ns
SCLK pulse-width low		t_{SCL}	15.3	—	—	ns
SCLK pulse-width high		t_{SCH}	15.3	—	—	ns
MOSI to SCLK set-up time		t_{DSU}	1.5	—	—	ns
MOSI to SCLK hold time		t_{DHO}	1.7	—	—	ns
SCLK falling edge to MISO transition	SCLK slew (90%–10%) = 5 ns, C_{LOAD} (MISO) = 25 pF	t_{DL}	0	—	12.6	ns

1. Control interface timing—SPI Mode (write cycle)

2. Control interface timing—SPI Mode (read cycle)
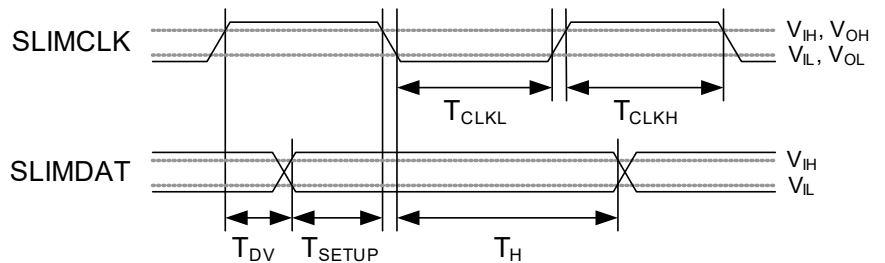
Table 3-21. SLIMbus Interface Timing

The following timing information is valid across the full range of recommended operating conditions.

Parameter [1]		Symbol	Minimum	Typ	Maximum	Units
SLIMCLK input	SLIMCLK cycle time	—	35	—	—	ns
	SLIMCLK pulse width high	T_{CLKH}	12	—	—	ns
	SLIMCLK pulse width low	T_{CLKL}	12	—	—	ns
SLIMCLK output	SLIMCLK cycle time	—	40	—	—	ns
	SLIMCLK pulse width high	T_{CLKH}	12	—	—	ns
	SLIMCLK pulse width low	T_{CLKL}	12	—	—	ns
	SLIMCLK slew rate (20%–80%) C_{LOAD} = 15 pF, SLIMCLK_DRV_STR = 0	SR_{CLK}	0.09 x V_{DBVDD}	—	0.22 x V_{DBVDD}	V/ns
	C_{LOAD} = 70 pF, SLIMCLK_DRV_STR = 0	SR_{CLK}	0.02 x V_{DBVDD}	—	0.05 x V_{DBVDD}	V/ns
	C_{LOAD} = 70 pF, SLIMCLK_DRV_STR = 1	SR_{CLK}	0.04 x V_{DBVDD}	—	0.11 x V_{DBVDD}	V/ns
SLIMDAT input	SLIMDAT setup time to SLIMCLK falling edge	T_{SETUP}	3.5	—	—	ns
	SLIMDAT hold time from SLIMCLK falling edge	T_H	2	—	—	ns
SLIMDAT output	SLIMDAT time for data output valid (relative to SLIMCLK rising edge) — SLIMDAT_DRV_STR = 0, DBVDD = 1.71 V	T_{DV}	—	4.7	8.1	ns
	C_{LOAD} = 15 pF, SLIMDAT_DRV_STR = 1, DBVDD = 1.71 V	T_{DV}	—	4.3	7.3	ns
	C_{LOAD} = 30 pF, SLIMDAT_DRV_STR = 0, DBVDD = 1.71 V	T_{DV}	—	6.8	11.8	ns
	C_{LOAD} = 30 pF, SLIMDAT_DRV_STR = 1, DBVDD = 1.71 V	T_{DV}	—	5.8	10.0	ns
	C_{LOAD} = 50 pF, SLIMDAT_DRV_STR = 0, DBVDD = 1.71 V	T_{DV}	—	9.6	16.6	ns
	C_{LOAD} = 50 pF, SLIMDAT_DRV_STR = 1, DBVDD = 1.71 V	T_{DV}	—	7.9	13.7	ns
	C_{LOAD} = 70 pF, SLIMDAT_DRV_STR = 0, DBVDD = 1.71 V	T_{DV}	—	12.4	21.5	ns
	C_{LOAD} = 70 pF, SLIMDAT_DRV_STR = 1, DBVDD = 1.71 V	T_{DV}	—	10.0	17.4	ns
	SLIMDAT slew rate (20%–80%) C_{LOAD} = 15 pF, SLIMDAT_DRV_STR = 0	SR_{DATA}	—	—	0.64 x V_{DBVDD}	V/ns
	C_{LOAD} = 30 pF, SLIMDAT_DRV_STR = 0	SR_{DATA}	—	—	0.35 x V_{DBVDD}	V/ns
	C_{LOAD} = 30pF, SLIMDAT_DRV_STR = 1	SR_{DATA}	—	—	0.46 x V_{DBVDD}	V/ns
	C_{LOAD} = 70pF, SLIMDAT_DRV_STR = 0	SR_{DATA}	—	—	0.16 x V_{DBVDD}	V/ns
	C_{LOAD} = 70pF, SLIMCLK_DRV_STR = 1	SR_{DATA}	—	—	0.21 x V_{DBVDD}	V/ns
Other parameters	Driver disable time	T_{DD}	—	—	6	ns
	Bus holder output impedance 0.1 x V_{DBVDD} < V < 0.9 x V_{DBVDD}	R_{DATAS}	18	—	50	kΩ

Notes:
- The signal timing information describes the timing requirements of the SLIMbus interface as a whole, not just the CS42L92 device.
- T_{DV} is the propagation delay from the rising SLIMCLK edge (at CS42L92 input) to the SLIMDAT output being achieved at the input to all devices across the bus.
- T_{SETUP} is the set-up time for SLIMDAT input (at CS42L92), relative to the falling SLIMCLK edge (at CS42L92).
- T_H is the hold time for SLIMDAT input (at CS42L92) relative to the falling SLIMCLK edge (at CS42L92).
- For more details of the interface timing, refer to the *MIPI Alliance Specification for Serial Low-Power Inter-Chip Media Bus (SLIMbus)*

1. SLIMbus interface timing.

V_{IL}, V_{IH} are the 35%/65% levels of the respective inputs.
V_{OL}, V_{OH} are the 20%/80% levels of the respective outputs.
The SLIMDAT output delay (T_{DV}) is with respect to the input pads of all receiving devices

Table 3-22. JTAG Interface Timing

Test conditions (unless specified otherwise): C_{LOAD} = 25 pF (output pins); TCK slew (20%–80%) = 5 ns; with the exception of the conditions noted, the following electrical characteristics are valid across the full range of recommended operating conditions.

Parameter [1]	Symbol	Minimum	Typical	Maximum	Units
TCK cycle time	T_{CCY}	50	—	—	ns
TCK pulse width high	T_{CCH}	20	—	—	ns
TCK pulse width low	T_{CCL}	20	—	—	ns
TMS setup time to TCK rising edge	T_{MSU}	1	—	—	ns
TMS hold time from TCK rising edge	T_{MH}	2	—	—	ns
TDI setup time to TCK rising edge	T_{DSU}	1	—	—	ns
TDI hold time from TCK rising edge	T_{DH}	2	—	—	ns
TDO propagation delay from TCK falling edge	T_{DD}	0	—	17	ns
TRST setup time to TCK rising edge	T_{RSU}	3	—	—	ns
TRST hold time from TCK rising edge	T_{RH}	3	—	—	ns
TRST pulse-width low	—	20	—	—	ns

1. JTAG Interface timing