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CS43130

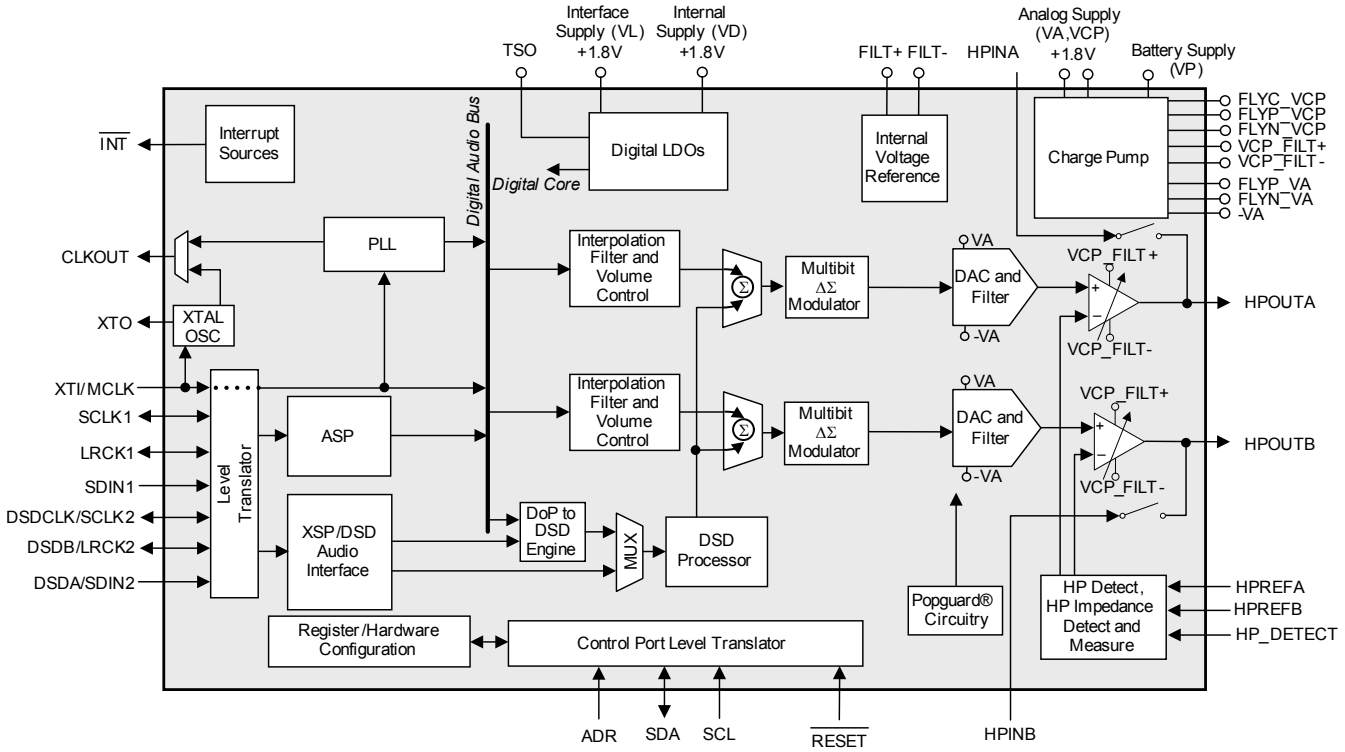
130-dB, 32-Bit High-Performance DAC with Integrated Headphone Driver and Impedance Detection

System Features

- Enhanced ΔΣ oversampling DAC architecture
  - 32-bit resolution
  - Up to 384-kHz sampling rate
  - Low clock jitter sensitivity
  - Auto mute detection
- Integrated high performance, ground-centered stereo headphone outputs
  - 130-dB dynamic range (A-weighted)
  - –108-dB total harmonic distortion + noise (THD+N)
  - 110-dB interchannel isolation
  - Headphone power output
    - 30 mW per channel into 32 Ω
    - 5 mW per channel into 600 Ω
- Headphone detection
  - Headphone DC and AC impedance measurement
  - Headphone plug-in detection
  - Popguard® technology eliminates pop noise
- Integrated PLL
  - Support for 11.2896-/22.5792-, 12.288-/24.576-, 9.6-/19.2-, 12-/24-, and 13-/26-MHz system MCLK rates
  - Reference clock sourced from XTI/MCLK pin
  - System clock output
- Mono mode support
- I²C control—up to 1 MHz
- Direct Stream Digital (DSD®) path
  - Patented DSD processor
    - On-chip 50-kHz filter to meet Scarlet Book Super Audio Compact Disk (SACD) recommendations
    - Matched PCM and DSD analog output levels
    - Nondecimating volume control with 0.5-dB step size and soft ramp
    - DSD and Pulse-code modulation (PCM) mixing for alerts
  - Dedicated DSD and DoP pin interface
- Serial audio input path
  - Five selectable digital filter responses
    - Low-latency mode minimizes pre-echo
    - 110 dB of stopband attenuation
  - Supports sample rates from 32 to 384 kHz
  - I²S, right-justified, left-justified, TDM, and DSD-over-PCM (DoP) interface
  - Master or slave operation
  - Volume control with 0.5-dB step size and soft ramp
  - 44.1 kHz deemphasis and inverting feature
- Alternate headphone input
- 40-pin QFN or 42-ball CSP package option

Applications

- Smart phones, tablets, portable media players, laptops, digital headphones, powered speakers, AVR, home theater systems, Blu-ray/DVD/SACD players and pro audio



General Description

The CS43130 is a high-performance, 32-bit resolution, stereo audio DAC that supports up to 384-kHz sampling frequency with integrated low-noise ground-centered headphone amplifiers. The advanced 32-bit oversampled multibit modulator with mismatch shaping technology eliminates distortion due to on-chip component mismatch. Proprietary digital-interpolation filters support five selectable filter responses with pseudo-linear phase and ultralow latency to minimize pre-echos and ringing artifacts. Other features include volume control with 0.5-dB steps and digital deemphasis for 44.1-kHz sample rate.

The integrated ground-centered stereo headphone amplifiers are capable of delivering more than 30 mW into 32-Ω load or 5 mW into 600-Ω load per channel. Proprietary headphone impedance detection enables wide-band impedance detection for further digital post-processing. An internal stereo audio switch with true bypass supports an alternate analog input path for interfacing with external audio sources to minimize the overall bill-of-materials cost and PCB area.

The patented on-chip DSD processor preserves audio integrity by allowing signal processing such as volume control and 50-kHz Scarlet Book recommended filtering to be applied directly to the DSD stream without an intermediate decimation stage. Additional features like volume matching and channel mixing enable seamless transition between DSD and PCM playback paths.

The CS43130 accepts I²S, right-justified, left-justified, and TDM-format PCM data at sample rates from 32 to 384 kHz. The industry-standard high-speed I²C interface capable of up to 1-MHz operation provides easy configuration control. An integrated PLL allows for maximum clocking flexibility in any system. Popguard® technology eliminates output transients upon power-up or power-down events.

The CS43130 is available in a commercial-grade 42-ball WLCSP or 40-pin QFN package for operation from –10°C to +70°C.

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1 Pin Assignments and Descriptions

1.1 40-Pin QFN (Top-Down, Through-Package View)

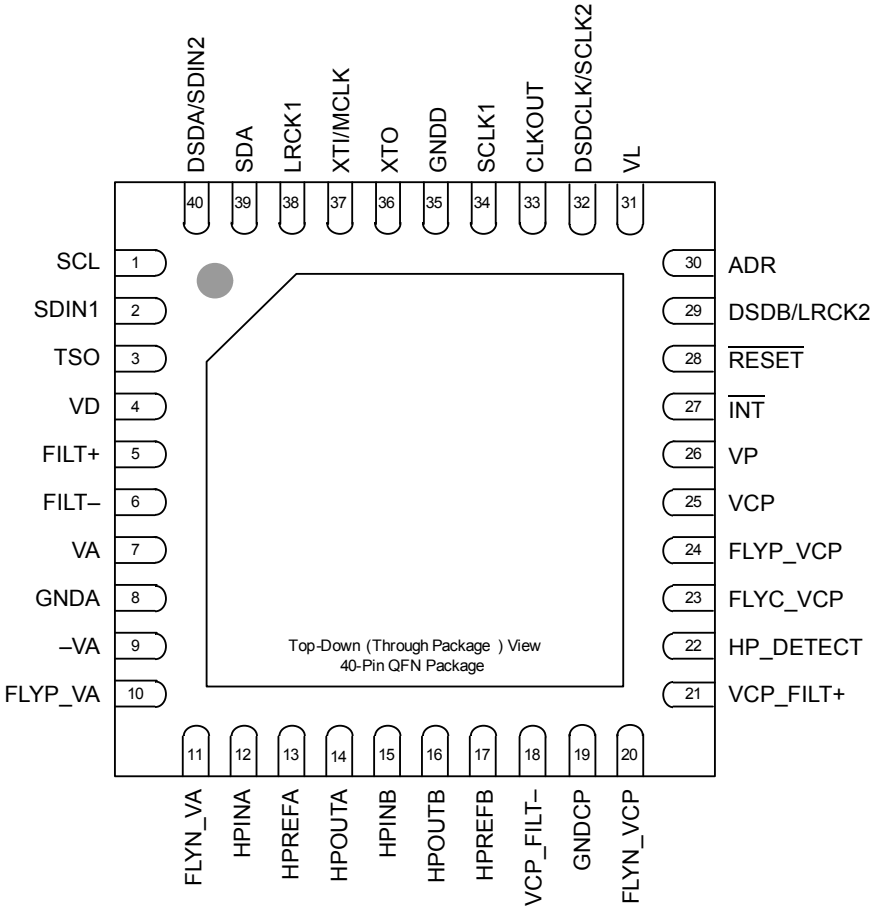


Figure 1-1. Top-Down (Through-Package) View—QFN 40-Pin Diagram

1.2 42-Ball WLCSP (Top-down, Through-Package View)

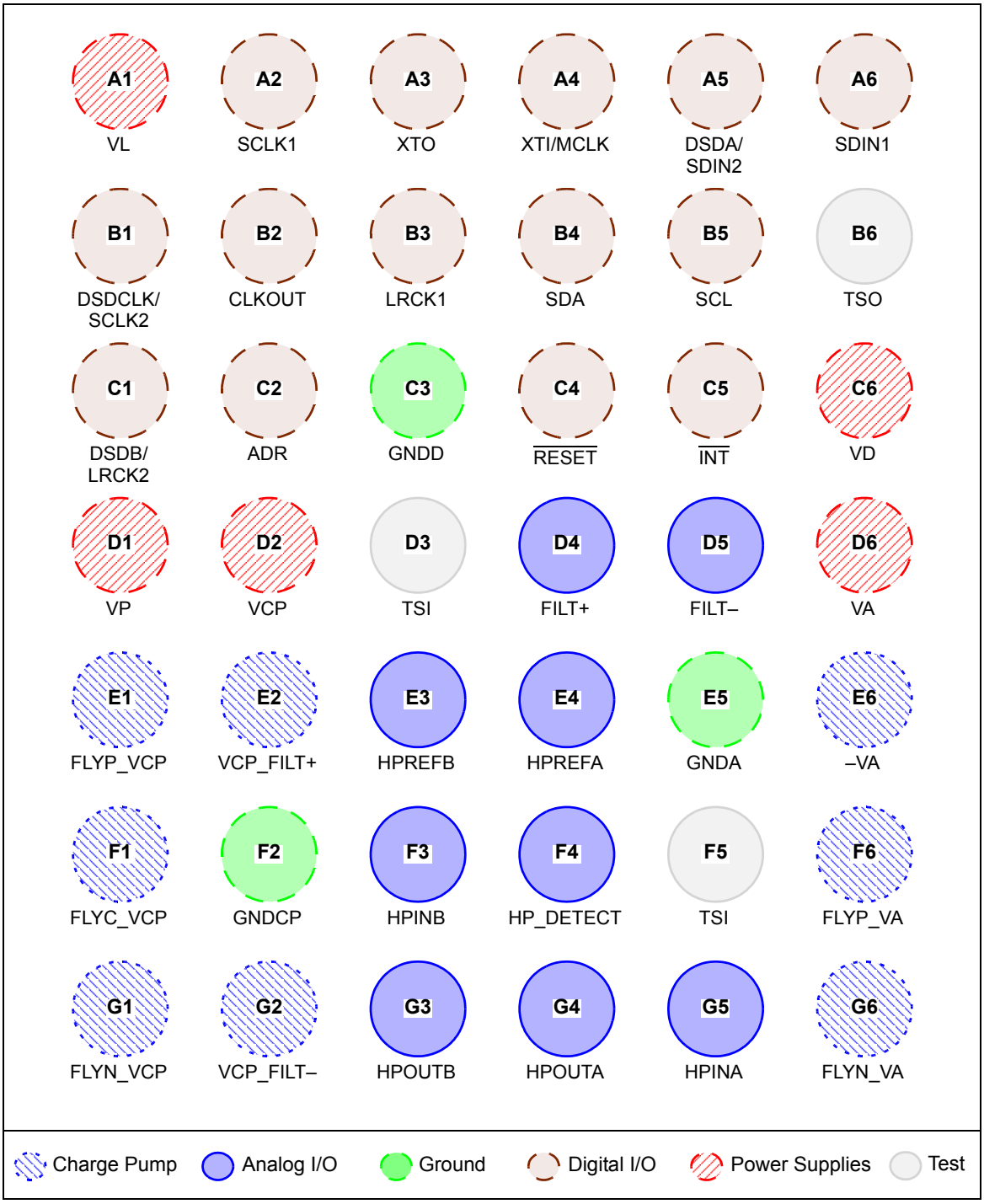


Figure 1-2. Top-Down (Through-Package) View—42-Ball WLCSP Package

1.3 Pin Descriptions

Table 1-1. Pin Descriptions

Pin Name	QFN Pin #	WLCSP Ball	Power Supply	I/O	Pin Description	Internal Connection	Digital I/O Driver	Digital I/O Receiver
					Digital I/O			
ADR	30	C2	VL	I	**Address Bit (I²C).** In I²C Mode, ADR is a chip address pin.	—	—	—
CLKOUT	33	B2	VL	O	**CLK Output.** Single-ended clock output sourced from PLL or buffered crystal.	Weak pull-down	CMOS output	—
SCLK1	34	A2	VL	I/O	**Serial Audio Input Bit Clock 1.** Serial bit clock for audio data on the SDIN pins.	Weak pull-down	CMOS output	Hysteresis on CMOS input
LRCK1	38	B3	VL	I/O	**Serial Audio Input Left/Right Clock.** Word-rate clock for the audio data on the SDIN pins.	Weak pull-down	CMOS output	Hysteresis on CMOS input
SDIN1	2	A6	VL	I	**Serial Audio Input Data Port.** Audio data serial input pin 1.	Weak pull-down	—	Hysteresis on CMOS input
DSDA/ SDIN2	40	A5	VL	I	**DSD Data Input A/Serial Data In 2.** DSD audio or PCM audio data serial input pin 2.	Weak pull-down	—	Hysteresis on CMOS input
DSDB/ LRCK2	29	C1	VL	I/O	**DSD Data Input B/Serial Audio Input Left/Right Clock 2.** DSD audio data serial input pin or word rate clock for the audio data on the SDIN2 pin.	Weak pull-down	CMOS output	Hysteresis on CMOS input
DSDCLK/ SCLK2	32	B1	VL	I/O	**DSD Clock Input/Serial Audio Input Bit Clock 2.** DSD clock input. Serial bit clock for audio data on the SDIN2 pin.	Weak pull-down	CMOS output	Hysteresis on CMOS input
$\overline{\text{INT}}$	27	C5	VP	O	**Interrupt.** When pulled up, works as system interrupt pin. Open drain, active low programmable.	—	CMOS open-drain output	—
$\overline{\text{RESET}}$	28	C4	VP	I	**System Reset.** The device enters system reset when enabled.	—	—	Hysteresis on CMOS input
SDA	39	B4	VL	I/O	**Serial Control Data I/O (I²C).** In I²C Mode, SDA is the control I/O data line.	—	CMOS open-drain output	Hysteresis on CMOS input
SCL	1	B5	VL	I	**Software Clock (I²C).** Serial control interface clock used to clock control data bits into and out of the CS43130.	—	—	Hysteresis on CMOS input
XTI/MCLK	37	A4	VL	I	**Crystal/Oscillator Input/MCLK In.** Crystal or digital clock input for the master clock.	Weak pull-down	—	Hysteresis on CMOS input
XTO	36	A3	VL	O	**Crystal/Oscillator Output.** Crystal output.	Weak pull-down	CMOS output	—
					Analog I/O			
FILT+ FILT–	5 6	D4 D5	VA	O	**Positive/Negative Voltage Reference.** Positive/negative reference voltage for DAC.	—	—	—
HP_ DETECT	22	F4	VP	I	**Headphone Detect.** Can be configured to be debounced on unplugged and plugged events before it is presented as a noninterrupt status bit (HPDETECT).	—	Hi-Z	—
HPINB HPINA	15 12	F3 G5	VCP_ FILT±	I	**Headphone Audio Input.** For interfacing low power audio source, an alternate analog input path for the headphone output. Refer to analog specification table for full-scale input level.	Weak pull-down	—	—
HPOUTB HPOUTA	16 14	G3 G4	VCP_ FILT±	O	**Headphone Audio Output.** Refer to analog specification table for full-scale output level.	—	—	—
HPREFB HPREFA	17 13	E3 E4	VCP_ FILT±	I	**Headphone Output Reference.** Reference for headphone amplifier and detect.	—	—	—
					Power Supplies			
VL	31	A1	N/A	I	**Logic Power.** Input/Output power supply, typically +1.8 V.	—	—	—

Table 1-1. Pin Descriptions *(Cont.)*

Pin Name	QFN Pin #	WLCSP Ball	Power Supply	I/O	Pin Description	Internal Connection	Digital I/O Driver	Digital I/O Receiver
VD	4	C6	N/A	I	**Internal Digital Power.** Internal digital power supply, typically +1.8 V.	—	—	—
VA	7	D6	N/A	I	**Analog Power.** Power supply for the internal analog section.	—	—	—
VCP	25	D2	N/A	I	**Charge Pump Supply**. Provides charge pump voltage to the headphone Class H analog output circuit.	—	—	—
VP	26	D1	N/A	I	**Battery supply**. Provides voltage to the headphone Class H circuit.	—	—	—
					Ground			
GNDD	35	C3	N/A	I	**Digital and I/O Ground.** Ground for the I/O and core logic. GNDA, GNDCP, and GNDD must be connected to a common ground area under the chip.	—	—	—
GNDA	8	E5	N/A	I	**Analog Ground.** Ground reference for the internal analog section. GNDA, GNDCP, and GNDD must be connected to a common ground area under the chip.	—	—	—
GNDCP	19	F2	N/A	I	**Charge Pump Ground.** Ground reference for the charge pump section. GNDA, GNDCP, and GNDD must be connected to a common ground area under the chip.	—	—	—
					Charge Pump			
VCP_FILT+ VCP_FILT–	21 18	E2 G2	VCP/ VP [1]	I/O	**Inverting Charge Pump Filter Connection.** Power supply from the inverting charge pump that provides the positive/negative rail for the analog output. When operating in external VCP_FILT mode, these pins can directly take in supply voltage.	—	—	—
–VA	9	E6	VA	O	**VA Negative Charge Pump Output.** Negative charge pump output for DAC rail. It is derived from VA.	—	—	—
FLYP_VA FLYN_VA	10 11	F6 G6	VA	O	**–VA Charge Pump Cap Positive/Negative Node.** Positive/ negative nodes for the DAC negative charge pump's flying capacitor.	—	—	—
FLYP_VCP	24	E1	VCP/ VP [1]	O	**–VCP Charge Pump Cap Positive Node.** Positive node for the analog output negative charge pump's flying capacitor.	—	—	—
FLYC_VCP	23	F1	VCP/ VP [1]	O	**–VCP Charge Pump Cap Center Node.** Center node for the analog output negative charge pump's flying capacitor.	—	—	—
FLYN_VCP	20	G1	VCP_ FILT±	O	**–VCP Charge Pump Cap Negative Node.** Negative node for the analog output negative charge pump's flying capacitor.	—	—	—
					Test			
TSO	3	B6	N/A	I/O	**Test Output.**	—	—	—
TSI	—	D3, F5			**Test Input.**	—	—	—

1. The power supply is determined by ADPT_PWR setting (see Section 4.3.1). VP is used if ADPT_PWR = 001 (VP_LDO Mode) or when necessary for ADPTPWR = 111 (Adapt-to-Signal Mode).

1.4 Electrostatic Discharge (ESD) Protection Circuitry

ESD-sensitive device. The CS43130 is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to current JEDEC ESD standards.

Fig. 1-3 provides a composite view of the ESD domains showing the ESD protection paths between each pad and the substrate (GND), as well as the interrelations between some domains. Note that this figure represents the structure for the internal protection devices and that additional protections can be implemented as part of the integration into the board.

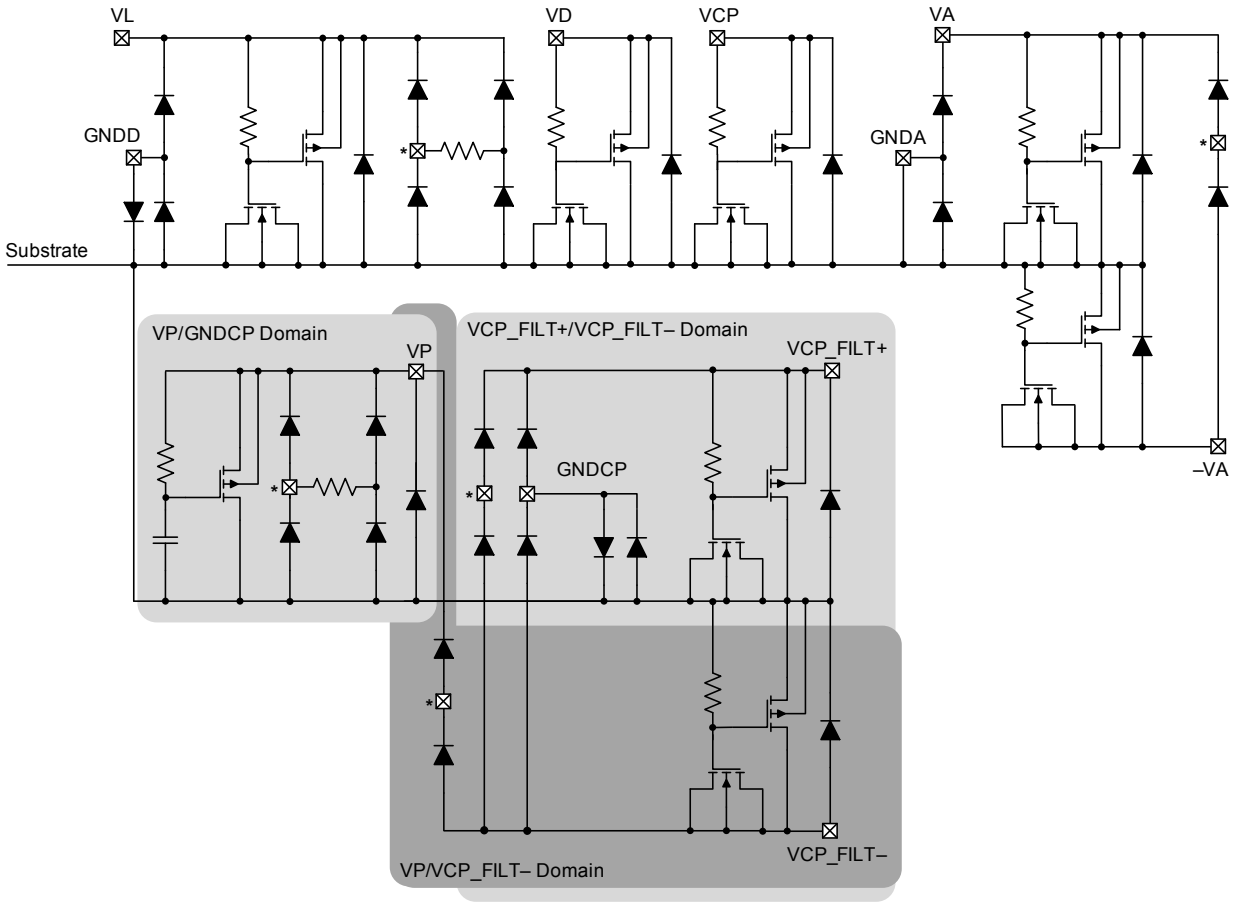


Figure 1-3. Composite ESD Topology

Table 1-2 shows the individual ESD domains and lists the pins associated with each domain.

Table 1-2. ESD Domains

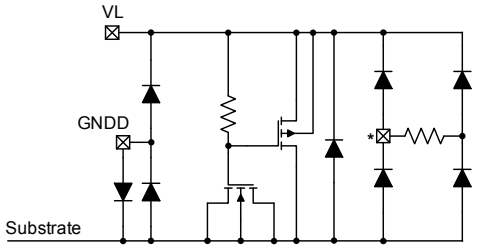
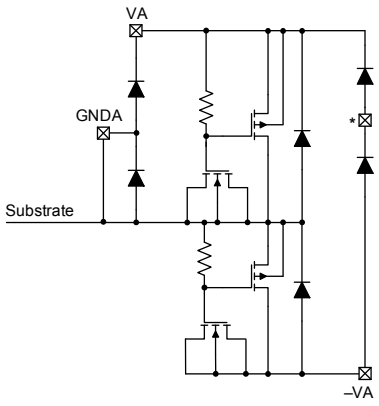
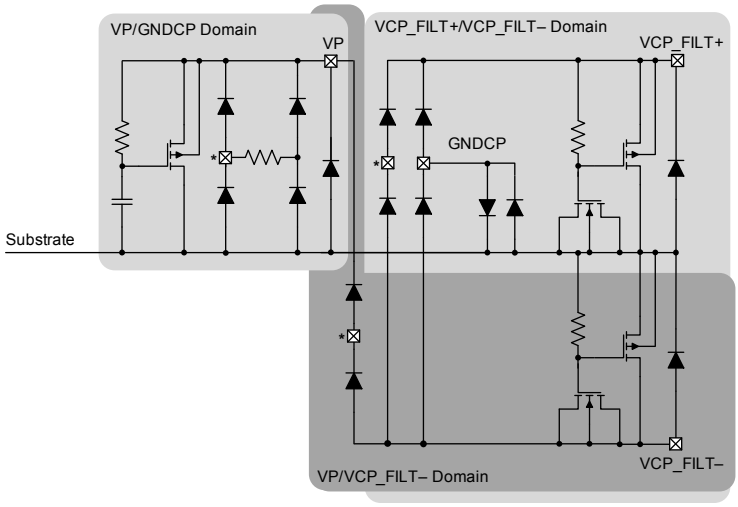
ESD Domain	Signal Name (See * in Topology Figures for Pad)	Topology
VL/GNDD	ADR DSDCLK/SCLK2 SCL SDA DSDB/LRCK2 DSDA/SDIN2 SDIN1 LRCK1 SCLK1 CLKOUT XTI/MCLK XTO	

Table 1-2. ESD Domains *(Cont.)*

ESD Domain	Signal Name (See * in Topology Figures for Pad)	Topology
VA/–VA	FLYN_VA FLYP_VA FILT+ FILT–	
VP/GNDCP	$\overline{\text{RESET}}$ $\overline{\text{INT}}$	
VP/VCP_FILT–	FLYP_VCP FLYC_VCP HP_DETECT	
VCP_FILT+/ VCP_FILT–	FLYN_VCP HPINA HPINB HPOUTA HPOUTB HPREFA HPREFB	

2 Typical Connection Diagram

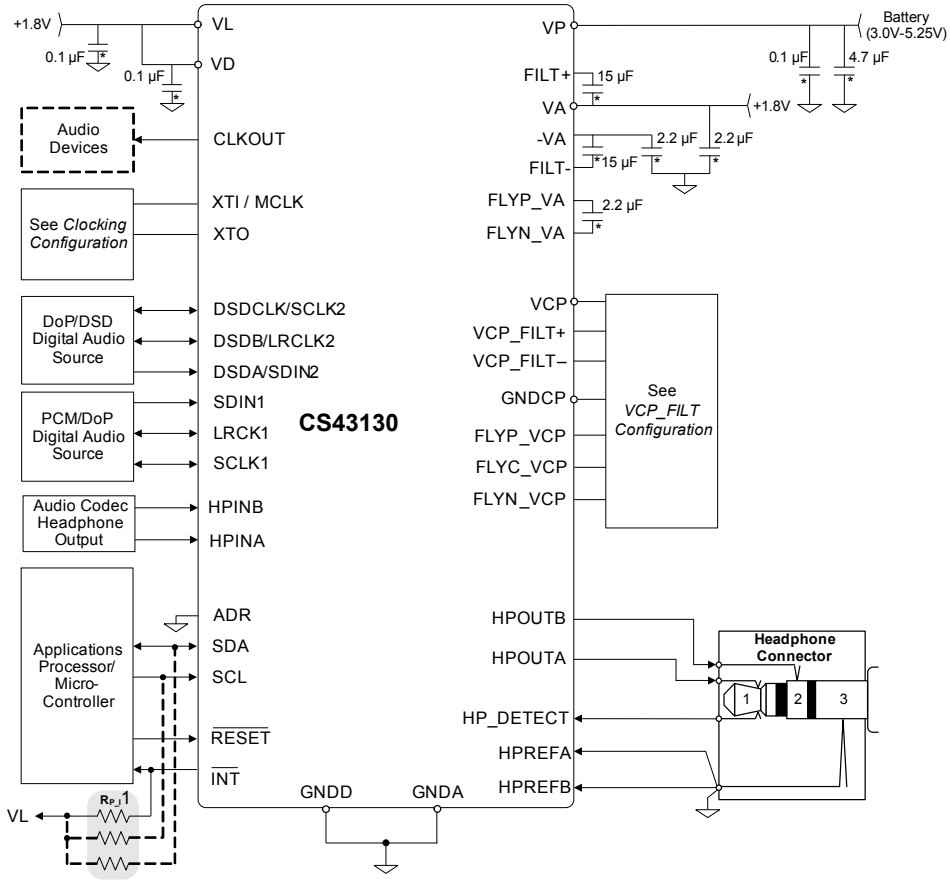


Figure 2-1. Typical Connection Diagram

Note:
1. The value for R_{P_I} can be determined by the interrupt pin specification in Table 3-11.

3 Characteristics and Specifications

Table 3-1 defines parameters as they are characterized in this section.

Table 3-1. Parameter Definitions

Parameter	Definition
Dynamic range	The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. A signal-to-noise ratio measurement over the specified bandwidth made with a –60-dB signal; 60 dB is added to resulting measurement to refer the measurement to full scale. This technique ensures that distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17–1991, and the Electronic Industries Association of Japan, EIAJ CP–307. Dynamic range is expressed in decibel units.
Gain drift	The change in gain value with temperature, expressed in ppm/°C units.
Idle channel noise	The rms value of the signal with no input applied (properly back-terminated analog input, digital zero, or zero modulation input). Measured over the specified bandwidth.
Interchannel gain mismatch	The gain difference between left and right channel pairs. Interchannel gain mismatch is expressed in decibel units.
Interchannel phase mismatch	The phase difference between left and right channel pairs at 997-Hz sine wave input. Interchannel phase mismatch is expressed in degree units (with respect to 997-Hz sine wave input).
Interchannel isolation	A measure of cross talk between the left and right channel pairs. Interchannel isolation is measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Interchannel isolation is expressed in decibel units.
Load resistance and capacitance	The recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. The load capacitance effectively moves the band-limiting pole of the amp in the output stage. Increasing load capacitance beyond the recommended value can cause the internal op-amp to become unstable.
Output offset voltage	The DC offset voltage present at the amplifier's output when its input signal is in a mute state. The offset exists due to CMOS process limitations and is proportional to analog volume settings. When measuring the offset out of the headphone amplifier, the headphone amplifier is ON.
Total harmonic distortion + noise (THD+N)	The ratio of the rms sum of distortion and noise spectral components across the specified bandwidth (typically 20 Hz–20 kHz) relative to the rms value of the signal. THD+N is measured at –1 and –20 dBFS for the analog input and at 0 and –20 dB for the analog output, as suggested in AES17–1991 Annex A. THD+N is expressed in decibel units.
Turn-on time	Turn-on time is measured from when the PDN_HP = 0 ACK signal is received to when the signal appears on the HP output.

Table 3-2. Recommended Operating Conditions

GNDD = GNDA= GNDCP = 0 V, all voltages with respect to ground.

Parameters [1]			Symbol	Minimum	Maximum	Units
DC power supply	Analog		VA	1.66	1.94	V
	Charge pump		VCP	1.66	1.94	V
	Filtered charge pump	EXT_VCPFLT = 1	VCP_FILT+	2.85	3.15	V
			VCP_FILT–	–3.15	–2.85	V
	Battery supply	HV_EN = 0, EXT_VCPFILT = 0 HV_EN = 1, EXT_VCPFILT = 0 EXT_VCPFILT = 1	VP	3.0 3.3 3.3	5.25 5.25 5.25	V V V
	Digital Interface		VL	1.66	1.94	V
	Digital Internal		VD	1.66	1.94	V
External voltage applied to pin[2,3]		HP_DETECT pin VCP_FILT± domain pins [4] VL domain pins VA domain pins VP domain pins	V_{INHI} V_{VCPF} V_{VL} V_{VA} V_{VP}	–0.3 – VCP_FILT– –0.3 – VCP_FILT– –0.3 –0.3 –0.3	VP + 0.3 0.3 + VCP_FILT+ VL + 0.3 VA + 0.3 VP + 0.3	V V V V V
Ambient temperature			T_A	–10	+70	°C

1. Device functional operation is guaranteed within these limits. Functionality is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.
2. The maximum over/undervoltage is limited by the input current.
3. Table 1-1 lists the power supply domain in which each CS43130 pin resides.
4. VCP_FILT± is specified in Table 3-16.

Table 3-3. Absolute Maximum Ratings

GNDD = GNDA= GNDCP = 0 V; all voltages with respect to ground.

Parameters		Symbol	Minimum	Maximum	Units
DC power supply	Analog	VA	–0.3	2.33	V
	Battery	VP	–0.3	6.3	V
	Charge pump	VCP	–0.3	2.33	V
	Filtered charge pump (positive)	VCP_FILT+	–0.3	3.3	V
	Filtered charge pump (negative)	VCP_FILT–	0.3	–3.3	V
	Digital interface	VL	–0.3	2.33	V
	Digital internal	VD	–0.3	2.33	V
Input current [1]		I_{in}	—	±10	mA
Ambient operating temperature (power applied)		T_A	–50	+115	°C
Storage temperature		T_{stg}	–65	+150	°C

Caution: Stresses beyond "Absolute Maximum Ratings" levels may cause permanent damage to the device. These levels are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Table 3-2, "Recommended Operating Conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1.Any pin except supplies and HPINx. Transient currents of up to ±100 mA on the analog input pins do not cause SCR latch-up.

Table 3-4. Analog Output Characteristics (HV_EN = 1) [1]

Test conditions (unless otherwise specified): Fig. 2-1 shows CS43130 connections; input test signal is a 32-bit, full-scale 997-Hz sine wave (unless specified otherwise); GNDA = GNDCP = GNDD = 0 V; voltages are with respect to ground; HV_EN = 1; ASP_M/Sb = 1; typical, min/max performance data taken with VA = VCP = 1.8 V; VL = VD = 1.8 V; VP = 3.6 V; T_A = +25°C; measurement bandwidth is 20 Hz–20 kHz; ASP_SPRATE = 0001 (LRCK = 44.1-kHz mode); PDN_XTAL = 0, MCLK_INT = 1, and MCLK_SRC_SEL = 00 (crystal frequency f_{XTAL} = 22.5792 MHz); Volume = 0 dB; when testing in DSD processor mode, DSD_ZERODB = 1; when testing noise related specifications (dynamic range, THD+N, idle channel noise), no external impedance on HPREFx.

PCM and DSD Processor Mode Parameter [2,3,4]				Minimum	Typical	Maximum	Units
HPOUTx R_L = 10 kΩ C_L = 200 pF OUT_FS = 11 Volume = 0 dB [5], unless otherwise specified	Dynamic range (defined in Table 3-1)	24-bit, 32-bit, DSD	A-weighted	124	130	—	dB
			Unweighted	121	127	—	dB
		16-bit	A-weighted	91	97	—	dB
			Unweighted	88	94	—	dB
	THD+N (defined in Table 3-1)	24-bit, 32-bit, DSD	0 dB	—	–108	–101	dB
			–20 dB	—	–97	—	dB
			–60 dB	—	–67	–61	dB
		16-bit	0 dB	—	–94	–88	dB
			–20 dB	—	–74	—	dB
			–60 dB	—	–34	–28	dB
	Idle channel noise (A-weighted) (defined in Table 3-1)	24-bit, 32-bit, DSD		—	0.55	—	µV
	Full-scale output voltage			4.66	4.90	5.14	Vpp
	Interchannel isolation [6](defined in Table 3-1)		217 Hz	—	110	—	dB
			1 kHz	—	95	—	dB
			20 kHz	—	68	—	dB
HPOUTx R_L = 600 Ω C_L = 200 pF OUT_FS = 11 Volume = 0 dB [5], unless otherwise specified	Dynamic range (defined in Table 3-1)	24-bit, 32-bit, DSD	A-weighted	124	130	—	dB
			Unweighted	121	127	—	dB
		16-bit	A-weighted	91	97	—	dB
			Unweighted	88	94	—	dB
	THD+N (defined in Table 3-1)	24-bit, 32-bit, DSD	0 dB	—	–108	–101	dB
			–20 dB	—	–97	—	dB
			–60 dB	—	–67	–61	dB
		16-bit	0 dB	—	–94	–88	dB
			–20 dB	—	–74	—	dB
			–60 dB	—	–34	–28	dB
	Idle channel noise (A-weighted) (defined in Table 3-1)	24-bit, 32-bit, DSD		—	0.55	—	µV
	Full-scale output voltage			4.66	4.90	5.14	Vpp
	Output power			—	5	—	mW
	Interchannel isolation [6](defined in Table 3-1)		217 Hz	—	110	—	dB
			1 kHz	—	95	—	dB
			20 kHz	—	68	—	dB

Table 3-4. Analog Output Characteristics (HV_EN = 1) [1] *(Cont.)*

Test conditions (unless otherwise specified): Fig. 2-1 shows CS43130 connections; input test signal is a 32-bit, full-scale 997-Hz sine wave (unless specified otherwise); GNDA = GNDCP = GNDD = 0 V; voltages are with respect to ground; HV_EN = 1; ASP_M/Sb = 1; typical, min/max performance data taken with VA = VCP = 1.8 V; VL = VD = 1.8 V; VP = 3.6 V; T_A = +25°C; measurement bandwidth is 20 Hz–20 kHz; ASP_SPRATE = 0001 (LRCK = 44.1-kHz mode); PDN_XTAL = 0, MCLK_INT = 1, and MCLK_SRC_SEL = 00 (crystal frequency f_{XTAL} = 22.5792 MHz); Volume = 0 dB; when testing in DSD processor mode, DSD_ZERODB = 1; when testing noise related specifications (dynamic range, THD+N, idle channel noise), no external impedance on HPREFx.

PCM and DSD Processor Mode Parameter [2,3,4]			Minimum	Typical	Maximum	Units
Other characteristics for HPOUTx	Interchannel gain mismatch (defined in Table 3-1)		—	±0.1	—	dB
	Interchannel phase mismatch (defined in Table 3-1)		—	±0.05	—	°
	Output offset voltage: Mute (defined in Table 3-1)		—	±0.5	±1	mV
	Gain drift (defined in Table 3-1)		—	±100	—	ppm/°C
	Load resistance (R_L)		600	—	—	Ω
	Load capacitance (C_L)		—	—	1	nF
	Turn-on time (defined in Table 3-1)		—	—	10	ms
	Click/pop during PDN_HP enable or disable	A-weighted	—	—	–60	dBV

1. This table also applies to external VCP_FILT supply mode: CS43130 power up procedure is per description in Section 5.10.1; EXT_VCPFILT = 1; VCP_FILT+ and VCP_FILT– comply to Table 3-2 when EXT_VCPFILT = 1; in this mode, HV_EN setting becomes don't care.
2. One LSB of triangular PDF dither is added to PCM data.
3. Referred to the typical full-scale voltage. Applies to all THD+N and dynamic range values in the table.
4. DSD performance may be limited by the source recording. 0 dB-SACD = 50% modulation index.
5. The volume must be configured as indicated to achieve specified output characteristics.
6. Output test configuration. Symbolized component values are specified in the test conditions.

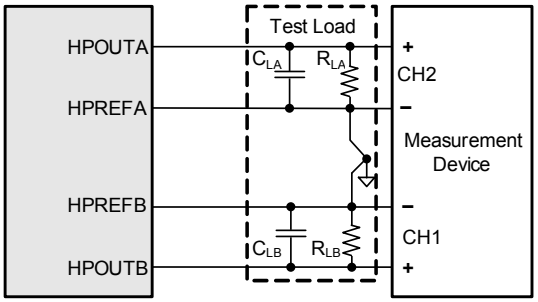


Table 3-5. Analog Output Characteristics (HV_EN = 0) [1]

Test conditions (unless otherwise specified): Fig. 2-1 shows CS43130 connections; input test signal is a 32-bit, full-scale 997-Hz sine wave (unless specified otherwise); GNDA = GNDCP = GNDD = 0 V; voltages are with respect to ground; HV_EN = 0; ASP_M/Sb = 1; typical, min/max performance data taken with VA = VCP = 1.8 V; VL = VD = 1.8 V; VP = 3.6 V; T_A = +25°C; measurement bandwidth is 20 Hz–20 kHz; ASP_SPRATE = 0001 (LRCK = 44.1-kHz mode); PDN_XTAL = 0, MCLK_INT = 1, and MCLK_SRC_SEL = 00 (crystal frequency f_{XTAL} = 22.5792 MHz); Volume = 0 dB; when testing in DSD processor mode, DSD_ZERODB = 1; when testing noise related specifications (dynamic range, THD+N, idle channel noise), no external impedance on HPREFx.

PCM and DSD Processor Mode Parameter [2,3,4]				Minimum	Typical	Maximum	Units
HPOUTx; R_L = 10 kΩ C_L = 200 pF OUT_FS = 10 Volume = 0 dB,[5] unless otherwise specified	Dynamic range (defined in Table 3-1)	24-bit, 32-bit, DSD	A-weighted	122	128	—	dB
			Unweighted	119	125	—	dB
		16-bit	A-weighted	91	97	—	dB
			Unweighted	88	94	—	dB
	THD+N (defined in Table 3-1)	24-bit, 32-bit, DSD	0 dB	—	–109	–103	dB
			–20 dB	—	–95	—	dB
			–60 dB	—	–65	–59	dB
		16-bit	0 dB	—	–94	–88	dB
			–20 dB	—	–74	—	dB
			–60 dB	—	–34	–28	dB
	Idle channel noise (A-weighted) (defined in Table 3-1)	24-bit, 32-bit, DSD		—	0.55	—	µV
	Full-scale output voltage			3.76	3.96	4.16	Vpp
	Interchannel isolation [6] (defined in Table 3-1)		217 Hz	—	110	—	dB
			1 kHz	—	94	—	dB
			20 kHz	—	68	—	dB

Table 3-5. Analog Output Characteristics (HV_EN = 0) [1] *(Cont.)*

Test conditions (unless otherwise specified): Fig. 2-1 shows CS43130 connections; input test signal is a 32-bit, full-scale 997-Hz sine wave (unless specified otherwise); GNDA = GNDCP = GNDD = 0 V; voltages are with respect to ground; HV_EN = 0; ASP_M/Sb = 1; typical, min/max performance data taken with VA = VCP = 1.8 V; VL = VD = 1.8 V; VP = 3.6 V; T_A = +25°C; measurement bandwidth is 20 Hz–20 kHz; ASP_SPRATE = 0001 (LRCK = 44.1-kHz mode); PDN_XTAL = 0, MCLK_INT = 1, and MCLK_SRC_SEL = 00 (crystal frequency f_{XTAL} = 22.5792 MHz); Volume = 0 dB; when testing in DSD processor mode, DSD_ZERODB = 1; when testing noise related specifications (dynamic range, THD+N, idle channel noise), no external impedance on HPREFx.

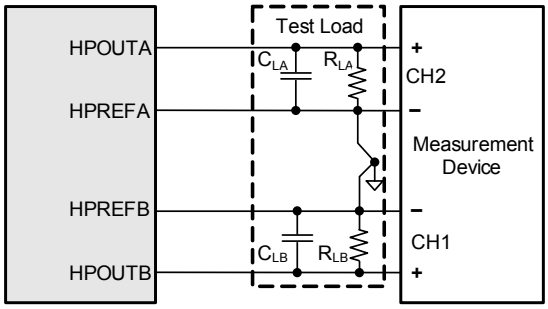
PCM and DSD Processor Mode Parameter [2,3,4]				Minimum	Typical	Maximum	Units
HPOUTx; R_L = 600 Ω C_L = 200 pF OUT_FS = 10 Volume = 0 dB, unless otherwise specified	Dynamic range (defined in Table 3-1)	24-bit, 32-bit, DSD	A-weighted	122	128	—	dB
			Unweighted	119	125	—	dB
		16-bit	A-weighted	91	97	—	dB
			Unweighted	88	94	—	dB
	THD+N (defined in Table 3-1)	24-bit, 32-bit, DSD	0 dB	—	–109	–103	dB
			–20 dB	—	–95	—	dB
			–60 dB	—	–65	–59	dB
		16-bit	0 dB	—	–94	–88	dB
			–20 dB	—	–74	—	dB
			–60 dB	—	–34	–28	dB
	Idle channel noise (A-weighted) (defined in Table 3-1)	24-bit, 32-bit, DSD		—	0.55	—	µV
	Full-scale output voltage			3.76	3.96	4.16	Vpp
	Output power			—	3.3	—	mW
	Interchannel isolation [6] (defined in Table 3-1)		217 Hz	—	110	—	dB
			1 kHz	—	94	—	dB
			20 kHz	—	68	—	dB
HPOUTx; R_L = 32 Ω C_L = 200 pF OUT_FS = 01 Volume = 0 dB, unless otherwise specified	Dynamic range (defined in Table 3-1)	24-bit, 32-bit, DSD	A-weighted	119	125	—	dB
			Unweighted	116	122	—	dB
		16-bit	A-weighted	91	97	—	dB
			Unweighted	88	94	—	dB
	THD+N (defined in Table 3-1)	24-bit, 32-bit, DSD	0 dB	—	–106	–96	dB
			–20 dB	—	–92	—	dB
			–60 dB	—	–62	–56	dB
		16-bit	0 dB	—	–94	–88	dB
			–20 dB	—	–74	—	dB
			–60 dB	—	–34	–28	dB
	Idle channel noise (A-weighted) (defined in Table 3-1)	24-bit, 32-bit, DSD		—	0.55	—	µV
	Full-scale output voltage			2.68	2.81	2.96	Vpp
	Output power			—	30.8	—	mW
	Interchannel isolation [6] (defined in Table 3-1)		217 Hz	—	110	—	dB
			1 kHz	—	90	—	dB
			20 kHz	—	66	—	dB
HPOUTx; R_L = 16 Ω C_L = 200 pF OUT_FS = 00 Volume = 0 dB, unless otherwise specified	Dynamic range (defined in Table 3-1)	24-bit, 32-bit	A-weighted	113	119	—	dB
			Unweighted	110	116	—	dB
		16-bit	A-weighted	89	95	—	dB
			Unweighted	86	92	—	dB
	THD+N (defined in Table 3-1)	24-bit, 32-bit, DSD	0 dB	—	–100	–94	dB
			–20 dB	—	–86	—	dB
			–60 dB	—	–56	–50	dB
		16-bit	0 dB	—	–94	–88	dB
			–20 dB	—	–74	—	dB
			–60 dB	—	–34	–28	dB
	Idle channel noise (A-weighted) (defined in Table 3-1)	24-bit, 32-bit, DSD		—	0.55	—	µV
	Full-scale output voltage			1.34	1.41	1.48	Vpp
	Output power			—	15.6	—	mW
	Interchannel isolation [6] (defined in Table 3-1)		217 Hz	—	110	—	dB
			1 kHz	—	83	—	dB
			20 kHz	—	58	—	dB

Table 3-5. Analog Output Characteristics (HV_EN = 0) [1] *(Cont.)*

Test conditions (unless otherwise specified): Fig. 2-1 shows CS43130 connections; input test signal is a 32-bit, full-scale 997-Hz sine wave (unless specified otherwise); GNDA = GNDCP = GNDD = 0 V; voltages are with respect to ground; HV_EN = 0; ASP_M/Sb = 1; typical, min/max performance data taken with VA = VCP = 1.8 V; VL = VD = 1.8 V; VP = 3.6 V; T_A = +25°C; measurement bandwidth is 20 Hz–20 kHz; ASP_SPRATE = 0001 (LRCK = 44.1-kHz mode); PDN_XTAL = 0, MCLK_INT = 1, and MCLK_SRC_SEL = 00 (crystal frequency f_{XTAL} = 22.5792 MHz); Volume = 0 dB; when testing in DSD processor mode, DSD_ZERODB = 1; when testing noise related specifications (dynamic range, THD+N, idle channel noise), no external impedance on HPREFx.

PCM and DSD Processor Mode Parameter [2,3,4]		Minimum	Typical	Maximum	Units
Other characteristics for HPOUTx	Interchannel gain mismatch (defined in Table 3-1)	—	±0.1	—	dB
	Interchannel phase mismatch (defined in Table 3-1)	—	±0.05	—	degree
	Output offset voltage: Mute (defined in Table 3-1)	—	±0.5	±1	mV
	Gain drift (defined in Table 3-1)	—	±100	—	ppm/°C
	Load resistance (R_L)	16	—	—	Ω
	Load capacitance (C_L)	—	—	1	nF
	Turn-on time (defined in Table 3-1)	—	—	8	ms
	Audio latency after $\overline{\text{RESET}}$ released [7]	—	—	20	ms
	Click/pop during PDN_HP enable or disable A-weighted	—	—	–60	dBV

1. This table also applies to external VCP_FILT supply mode: CS43130 power up procedure as described in Section 4.3.5; EXT_VCPFILT=1; VCP_FILT+ and VCP_FILT– comply to Table 3-2 when EXT_VCPFILT = 1; in this mode, HV_EN setting becomes don't care.
2. One LSB of triangular PDF dither is added to PCM data.
3. Referred to the typical full-scale voltage. Applies to all THD+N and dynamic range values in the table.
4. DSD performance may be limited by the source recording. 0 dB-SACD = 50% modulation index.
5. The volume must be configured as indicated to achieve specified output characteristics.
6. HP output test configuration. Symbolized component values are specified in the test conditions.



7. With I²C normal speed mode and 22.5792-MHz XTAL used as MCLK source, this specification is measured from reset released to when the audio signal appears on the output per power-up sequence listed in Section 5.10.1. PCM_SZC should be set to Immediate (PCM_SZC = 00) to hear audio at 20 ms after startup.

Table 3-6. Headphone Load Measurement

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43130 connections; GNDD = GNDCP = GNDA = 0 V; voltages are with respect to ground; typical performance data taken with VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; min/max performance data taken with VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; T_A = +25°C. MCLK_INT = 1, PDN_XTAL = 0, and MCLK_SRC_SEL = 00 (crystal frequency f_{XTAL} = 22.5792 MHz)

Parameters		Symbol	Minimum	Typical	Maximum	Units
Frequency range		—	20	—	20k	Hz
Frequency resolution		—	—	5.94	—	Hz
Low frequency impedance range		—	8	—	1200	Ω
Relative impedance measurement capability [1]		—	–12 [2]	—	+12	dB
Impedance measurement accuracy [3]	Gain error	—	–5	—	+5	%
	Offset	—	–1	—	1	Ω

1. Impedance measurement range is relative to low-frequency HP load impedance measured.
2. Or 4 Ω, whichever is greater.
3. Accuracy is referred to reported impedance.

Table 3-7. Alternate Headphone Path

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43130 connections; GNDD = GNDCP = GNDA = 0 V; voltages are with respect to ground; typical performance data taken with VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; min/max performance data taken with VP = 3.6 V, VCP = 1.8 V, VA = 0 V, VL = VD = 1.8 V; R_L = 32 Ω; TA = +25°C; measurement bandwidth is 20 Hz–20 kHz; MCLK_SRC_SEL = 10, PDN_XTAL = 1.

Parameters			Symbol	Minimum	Typical	Maximum	Units
Switch on characteristics (PDN_HP = 1 HP_IN_EN = 1)	Signal range when switch on [1]		V_{INAI}	—	—	3.00	Vpp
	THD+N with 32 Ω @ 2.82 Vpp		—	—	–99	—	dB
	Interchannel isolation	217 Hz	—	104	110	—	dB
		1 kHz		—	110	—	dB
		20 kHz		—	90	—	dB
	HPINx turn-on time [2]		t_{HPIN_ON}	—	—	80	µs
Switch off characteristics (PDN_HP = 1, HP_IN_EN = 0)	Analog signal range when switched off [3,4]		V_{INOFF}	—	—	0.3	Vp
	Turn-off time [5]		t_{HPIN_OFF}	—	—	20	µs
	Off isolation [6]	217 Hz		—	120	—	dB
		1 kHz		—	120	—	dB
		20 kHz		—	100	—	dB

1. When switch is on, maximally allowable voltage applied to HPINx pins.
2. HPINx turn-on time is measured when setting HP_IN_EN = 1 I²C ACK signal is received to when the signal appears on the HP out. MCLK_SRC_SEL = 00, PDN_XTAL = 0, MCLK_INT = 1, and VCP_FILT± has been properly charged to expected nominal values.
3. When switch is off, maximally allowable voltage applied to HPINx pins.
4. Before switch off event, it is required HPINx signal is within this range before the switch is turned off. When the switch is in off state, HPINx signal cannot exceed this specified range.
5. HPINx turn-off time is measured when HP_IN_EN = 0 ACK signal is received to when the signal disappears from the HP out. This spec also applies when register settings are: MCLK_SRC_SEL = 00, PDN_XTAL = 0, MCLK_INT = 1.
6. Off isolation specification is measured with V_{INOFF} = 0.1 Vp input.

Table 3-8. Combined DAC Digital, On-Chip Analog and HPOUTx Filter Characteristics

Test conditions (unless specified otherwise): The filter characteristics have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs. Single-Speed Mode refers to 32-, 44.1-, and 48-kHz sample rates. Double-Speed Mode refers to 88.2- and 96-kHz sample rates. Quad-Speed Mode refers to 176.4- and 192-kHz sample rates. Octuple-Speed Mode refers to 352.8- and 384-kHz sample rates. MCLK_INT is an integer multiple of Fs; HPF disabled; no DC offset applied; group delay does not include serial port delay.

Parameter			Minimum	Typical	Maximum	Units
Fast Roll-Off (FILTER_SLOW_FASTB = 0) Single-Speed Mode [1]	Passband [2]	to –0.01-dB corner	0	—	0.4535 [4]	Fs
		to –3-dB corner	0	—	0.49	Fs
		attenuation @ Fs/2	8.44 [3]	—	—	dB
	Passband ripple 10 Hz to –0.01-dB corner [5]		–0.01	—	+0.01	dB
	Stopband		0.547	—	—	Fs
	Stopband attenuation [6]	PHCOMP_LOWLATB = 0	110 [7]	—	—	dB
		PHCOMB_LOWLATB = 1	105	—	—	dB
	Group delay (linear phase)	PHCOMB_LOWLATB = 1	—	39.5/Fs [8]	—	s
	Group delay (minimum phase)	PHCOMB_LOWLATB = 0	—	6.3/Fs [9]	—	s
	Deemphasis error [10] (Relative to 1 kHz)	Fs = 44.1 kHz	—	—	±0.14	dB
Fast Roll-Off (FILTER_SLOW_FASTB = 0) Double-Speed Mode [1]	Passband [2]	to –0.01-dB corner	0	—	0.227	Fs
		to –3-dB corner	0	—	0.48	Fs
		attenuation @ Fs/2	7.77	—	—	dB
	Passband ripple 10 Hz to –0.01-dB corner		–0.01	—	0.01	dB
	Stopband		0.583	—	—	Fs
	Stopband attenuation [6]		80	—	—	dB
	Group delay (linear phase)	PHCOMB_LOWLATB = 1	—	22.3/Fs	—	s
	Group delay (minimum phase)	PHCOMB_LOWLATB = 0	—	7.5/Fs	—	s
Fast Roll-Off (FILTER_SLOW_FASTB = 0) Quad-Speed Mode [1]	Passband [2]	to –0.01-dB corner	0	—	0.114	Fs
		to –3-dB corner	0	—	0.46	Fs
		attenuation @ Fs/2	9.44	—	—	dB
	Passband ripple 10 Hz to –0.01-dB corner		–0.01	—	0.01	dB
	Stopband		0.583	—	—	Fs
	Stopband attenuation [6]		80	—	—	dB
	Group delay (linear phase)	PHCOMB_LOWLATB = 1	—	20.7/Fs	—	s
	Group delay (minimum phase)	PHCOMB_LOWLATB = 0	—	11.3/Fs	—	s

Table 3-8. Combined DAC Digital, On-Chip Analog and HPOUTx Filter Characteristics *(Cont.)*

Test conditions (unless specified otherwise): The filter characteristics have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs. Single-Speed Mode refers to 32-, 44.1-, and 48-kHz sample rates. Double-Speed Mode refers to 88.2- and 96-kHz sample rates. Quad-Speed Mode refers to 176.4- and 192-kHz sample rates. Octuple-Speed Mode refers to 352.8- and 384-kHz sample rates. MCLK_INT is an integer multiple of Fs; HPF disabled; no DC offset applied; group delay does not include serial port delay.

Parameter			Minimum	Typical	Maximum	Units
Slow Roll-Off (FILTER_SLOW_FASTB = 1) Single-Speed Mode [1]	Passband [2]	to –0.01-dB corner to –3-dB corner attenuation @ Fs/2	0 0 6.45 [11]	— — —	0.417 0.49 —	Fs Fs dB
	Passband ripple 10 Hz to –0.01-dB corner [5]		–0.01	—	+0.01	dB
	Stopband		0.583	—	—	Fs
	Stopband attenuation [6]		64	—	—	dB
	Group delay (linear phase)	PHCOMB_LOWLATB = 1	—	34.5/Fs [12]	—	s
	Group delay (minimum phase)	PHCOMB_LOWLATB = 0	—	5.6/Fs [13]	—	s
	Deemphasis error [10] (Relative to 1 kHz)	Fs = 44.1 kHz	—	—	±0.14	dB
Slow Roll-Off (FILTER_SLOW_FASTB = 1) Double-Speed Mode [1]	Passband [2]	to –0.01-dB corner to –3-dB corner attenuation @ Fs/2	0 0 7	— — —	0.208 0.458 —	Fs Fs dB
	Passband ripple 10 Hz to –0.01-dB corner		–0.01	—	0.01	dB
	Stopband		0.792	—	—	Fs
	Stopband attenuation [6]		70	—	—	dB
	Group delay (linear phase)	PHCOMB_LOWLATB = 1	—	22.3/Fs	—	s
	Group delay (minimum phase)	PHCOMB_LOWLATB = 0	—	6.7/Fs	—	s
Slow Roll-Off (FILTER_SLOW_FASTB = 1) Quad-Speed Mode [1]	Passband [2]	to –0.01-dB corner to –3-dB corner attenuation @ Fs/2	0 0 7.00	— — —	0.104 0.43 —	Fs Fs dB
	Passband ripple 10 Hz to –0.01-dB corner		–0.01	—	0.01	dB
	Stopband		0.792	—	—	Fs
	Stopband attenuation [6]		75	—	—	dB
	Group delay (linear phase)	PHCOMB_LOWLATB = 1	—	20.7/Fs	—	s
	Group delay (minimum phase)	PHCOMB_LOWLATB = 0	—	10.6/Fs	—	s
Nonoversampling (NOS) (NOS = 1) Single-Speed Mode [1]	Passband [2]	to –0.01-dB corner to –3-dB corner	0 0	— —	0.026 0.444	Fs Fs
	Passband droop 10 Hz to 20 kHz		—	—	3.2 [14]	dB
	Group delay		—	2.7/Fs	—	s
Nonoversampling (NOS) (NOS = 1) Double-Speed Mode [1]	Passband [2]	to –0.01-dB corner to –3-dB corner	0 0	— —	0.0246 0.446	Fs Fs
	Passband droop 10 Hz to 20 kHz		—	—	0.73	dB
	Group delay		—	4.5/Fs	—	s
Nonoversampling (NOS) (NOS = 1) Quad-Speed Mode [1]	Passband [2]	to –0.01-dB corner to –3-dB corner	0 0	— —	0.026 0.405	Fs Fs
	Passband droop 10 Hz to 20 kHz		—	—	0.167	dB
	Group delay		—	8.4/Fs	—	s
Octuple-Speed Mode [1]	Passband [2]	to –0.01-dB corner to –3-dB corner	0 0	— —	0.0299 0.302	Fs Fs
	Passband droop 10 Hz to 20 kHz		—	—	0.037	dB
	Group delay		—	17/Fs	—	s

1. Filter response is by design.
2. Response is clock-dependent and scales with Fs.
3. 8.5 dB for 32-kHz sample rate.
4. 0.454 Fs for 32-kHz sample rate.
5. Filter ripple specification is invalid with deemphasis enabled.
6. For Single-Speed Mode, the measurement bandwidth is from stopband to 3 Fs.
   For Double-Speed Mode, the measurement bandwidth is from stopband to 3 Fs.
   For Quad-Speed Mode, the measurement bandwidth is from stopband to 1.34 Fs.
7. 105 dB for 32-kHz sample rate.
8. 39/Fs for 32-kHz sample rate.
9. 5.9/Fs for 32-kHz sample rate.
10. Deemphasis is available only in 44.1 kHz.
11. 6.5 dB for 32-kHz sample rate.
12. 34/Fs for 32-kHz sample rate.

13. 5.2/Fs for 32-kHz sample rate.
14. 3.9 dB for 32-kHz sample rate (passband droop 10 Hz to 15 kHz).

Table 3-9. DAC High-Pass Filter (HPF) Characteristics

Test conditions (unless specified otherwise): Gains are all set to 0 dB; T_A = +25°C.

Parameter [1]	Minimum	Typical	Maximum	Units
Passband [2] –0.05-dB corner	—	0.18×10^{-3}/N	—	Fs
–3.0-dB corner	—	19.5×10^{-6}/N	—	Fs
Passband ripple (0.417×10^{-3}/N Fs to 0.417/N Fs; normalized to 0.417/N Fs) [2]	—	—	0.01	dB
Phase deviation @ 0.453×10^{-3}/N Fs [2]	—	2.45	—	°
Filter settling time [3]	—	0.56 [4]	—	s

1. Response scales with Fs in PCM Mode. Specifications are normalized to Fs and are denormalized by multiplying by Fs. For DSD Mode, Fs is 44.1 kHz.
2. For PCM Single-Speed Mode, N = 1.
   For PCM Double-Speed Mode, N = 2.
   For PCM Quad-Speed Mode, N = 4.
   For PCM Octuple-Speed Mode, N = 8.
   For DSD 64 x Fs Mode, N = 1.
   For DSD 128 x Fs Mode, N = 1.
3. Required time for the magnitude of the DC component present at the output of the HPF to reach 5% of the applied DC signal.
4. Filter settling time is 0.775 seconds at Fs = 32 kHz.

Table 3-10. DSD Combined Digital and On-Chip Analog Filter Response [1]

Test conditions (unless specified otherwise): Digital gains are all set to 0 dB; T_A = +25°C; PDN_XTAL = 0, MCLK_INT = 1, and MCLK_SRC_SEL = 00 (crystal frequency f_{XTAL} = 22.5792 MHz).

	Parameter	Minimum	Typical	Maximum	Units
DSD Mode	Passband to –3-dB corner	—	50	—	kHz
	Frequency response 20 Hz to 20 kHz	–0.05	—	0.05	dB
	Roll-off	27	—	—	dB/Oct

1. Filter response is by design.

Table 3-11. Digital Interface Specifications and Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43130 connections; GNDD = GNDCP = GNDA = 0 V; voltages are with respect to ground; parameters can vary with VL and VP; typical performance data taken with VP = 3.6 V, VCP = VA = 1.8 V, VD = 1.8V and VL = 1.8 V; min/max performance data taken with VP = 3.6 V, VCP = VA = 1.8 V, VD = 1.8V and VL = 1.8 V; T_A = +25°C; C_L = 60 pF.

Parameters [1]		Symbol	Minimum	Maximum	Units
Input leakage current [2,3]	LRCK1, DSDB/LRCK2	I_{in}	—	±4	µA
	SDIN1, SCLK1, DSDA/SDIN2, DSDCLK/SCLK2		—	±3	µA
	HP_DETECT		—	±100	nA
	$\overline{\text{SDA}}$, SCL		—	±100	nA
	$\overline{\text{INT}}$, RESET		—	±100	nA
Internal weak pull-down		—	550	2450	kΩ
Input capacitance		—	—	10	pF
$\overline{\text{INT}}$ current sink (V_{OL} = 0.3 V maximum)		—	825	—	µA
VL Logic (non-I²C)	High-level output voltage (I_{OH} = –100 µA)	V_{OH}	0.9•VL	—	V
	Low-level output voltage	V_{OL}	—	0.1•VL	V
	High-level input voltage	V_{IH}	0.7•VL	—	V
	Low-level input voltage	V_{IL}	—	0.3•VL	V
VL Logic (I²C only)	Hysteresis voltage (Fast Mode and Fast Mode Plus)	V_{HYS}	0.05•VL	—	V
	Low-level output voltage	V_{OL}	—	0.2•VL	V
	High-level input voltage	V_{IH}	0.7•VL	—	V
	Low-level input voltage	V_{IL}	—	0.3•VL	V
HP_DETECT [4]	High-level input voltage	V_{IH}	0.93•VP	—	V
	Low-level input voltage	V_{IL}	—	2.0	V
HP_DETECT current to VCP_FILT– [4]		I_{HP_DETECT}	1.00	2.91	µA

1. See Table 1-1 for serial and control-port power rails.
2. Specification is per pin.
3. Includes current through internal pull-up or pull-down resistors on pin.
4. The HP_DETECT input circuit allows the HP_DETECT signal to be as low of a voltage as VCP_FILT– and as high as VP. Section 4.5.1 provides configuration details.

Table 3-12. CLKOUT Characteristics

Test conditions (unless specified otherwise): GNDD = GNDCP = GNDA = 0 V; voltages are with respect to ground; VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; C_L = 60 pF; PLL reference input must meet the phase-noise mask specified in Fig. 4-15; TA = +25°C; Output jitter is measured from 100 Hz to half of the output frequency.

Parameters		Symbol	Minimum	Typical	Maximum	Units
CLKOUT output frequency		f_{CLKOUT}	2.8224	3	3.072	MHz
			5.6448	6	6.144	MHz
			7.5264	8	8.192	MHz
			11.2896	12	12.288	MHz
CLKOUT output duty cycle		—	40	50	60	%
CLKOUT output TIE jitter (RMS)	CLKOUT_SRC_SEL = 01	t_{JIT}	—	500	—	ps

Table 3-13. PLL Characteristics

Test conditions (unless specified otherwise): GNDD = GNDCP = GNDA = 0 V; voltages are with respect to ground; VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; PLL reference input must meet the phase-noise mask specified in Fig. 4-15; TA = +25°C.

Parameters	Symbol	Minimum	Typical	Maximum	Units
PLL output frequency	f_{out}	22.5792	24	24.576	MHz
PLL lock time	t_{Lock}	—	620	1000	µs
PLL reference clock input	—	—	11.2896	—	MHz
		—	22.5792	—	MHz
		—	12.2880	—	MHz
		—	24.5760	—	MHz
		—	9.6000	—	MHz
		—	19.2000	—	MHz
		—	12.0000	—	MHz
		—	24.0000	—	MHz
		—	13.0000	—	MHz
		—	26.000	—	MHz
PLL reference clock input jitter	—	—	—	50	ps

Table 3-14. Crystal Characteristics

Test conditions (unless specified otherwise): GNDD = GNDCP = GNDA = 0 V; voltages are with respect to ground; VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; T_A = +25°C

Parameters [1]	Symbol	Minimum	Typical	Maximum	Units
Crystal oscillator frequency	f_{XTAL}	22.57	22.5792/ 24.576	24.58	MHz
Crystal load capacitance	C_{L_XTAL}	5	—	8	pF
Equivalent series resistance	esr_{XTAL}	—	—	100	Ω
Startup time	t_{XTAL_pup}	—	—	8	ms
Shunt capacitance	C_O	—	—	0.8	pF
Maximum drive level	—	200	—	—	µW

1. Refer to Section 5.3 for supported crystal options.

Table 3-15. Power-Supply Rejection Ratio (PSRR) Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43130 connections; input test signal held low (all zero data); GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground; VL = VA = VD = 1.8 V, VP = 3.6 V; When testing PSRR, PCM input test signal held low (all zero data); T_A = +25°C; PCM_AMUTE = 0.

Parameter [1]		Minimum	Typical	Maximum	Units
HPOUTx PSRR with 100-mVpp signal AC coupled to VA supply PDN_HP = 0, HP_IN_EN = 0	217 Hz 1 kHz 20 kHz	— — —	75 75 70	— — —	dB dB dB
HPOUTx PSRR with 100-mVpp signal AC coupled to VCP supply PDN_HP = 0, HP_IN_EN = 0	217 Hz 1 kHz 20 kHz	— — —	80 80 60	— — —	dB dB dB
HPOUTx PSRR with 100-mVpp signal AC coupled to VP supply PDN_HP = 0, HP_IN_EN = 0	217 Hz 1 kHz 20 kHz	— — —	100 100 80	— — —	dB dB dB
HPOUTx (0-dB analog gain) PSRR with 100-mVpp signal AC coupled to VCP supply PDN_HP = 1, HP_IN_EN = 1, R_L = 32 Ω	217 Hz 1 kHz 20 kHz	— — —	80 80 60	— — —	dB dB dB
HPOUTx (0-dB analog gain) PSRR with 100-mVpp signal AC coupled to VP supply PDN_HP = 1, HP_IN_EN = 1, R_L = 32 Ω	217 Hz 1 kHz 20 kHz	— — —	100 100 80	— — —	dB dB dB

1. PSRR test configuration: Typical PSRR can vary by approximately 6 dB below the indicated values.

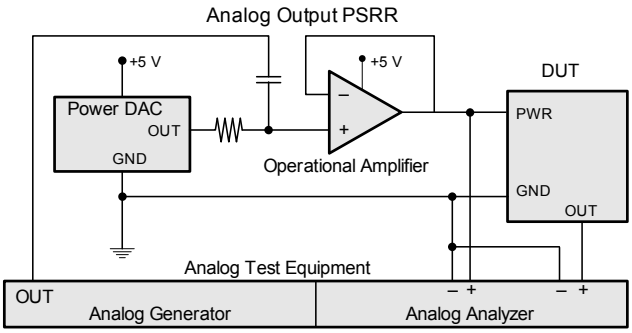


Table 3-16. DC Characteristics

Test conditions (unless otherwise specified): Fig. 2-1 shows CS43130 connections; GNDD = GNDA = GNDCP = 0 V; all voltages with respect to ground.

Parameters			Minimum	Typical	Maximum	Units
VCP_FILT (No load connected to HPOUTx) EXT_VCPFILT = 0	VP_LDO Mode	VCP_FILT+ pin (HV_EN = 1) VCP_FILT+ pin (HV_EN = 0) VCP_FILT– pin (HV_EN = 1) VCP_FILT– pin (HV_EN = 0)	— — — —	3.0 2.6 –3.0 –2.6	— — — —	V V V V
	VCP Mode	VCP_FILT+ pin VCP_FILT– pin	— —	VCP –VCP	— —	V V
–VA		–VA pin	—	– VA	—	V
Alternate headphone path switch-on characteristics PDN_HP = 1, HP_IN_EN = 1	On-resistance		—	1	—	Ω
	r_{ON} matching between channels		—	0.05	—	Ω

Table 3-16. DC Characteristics *(Cont.)*

Test conditions (unless otherwise specified): Fig. 2-1 shows CS43130 connections; GNDD = GNDA = GNDCP = 0 V; all voltages with respect to ground.

Parameters			Minimum	Typical	Maximum	Units
Other DC filter characteristics	FILT+ voltage		—	–0.35	—	V
	FILT– voltage		—	0.35	—	V
	HP output current limiter on threshold.		—	120	160	mA
	VD power-on reset threshold (V_{POR})	Up	—	1.15	—	V
		Down	—	0.950	—	V

Table 3-17. Power Consumption

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43130 connections; GNDA = GNDCP = GNDD = 0 V; voltages are with respect to ground; performance data taken with VA = VCP = VD = VL = 1.8 V; VP = 3.6 V; T_A = +25°C; ASP_SPRATE = 0001(44.1-kHz mode); MCLK_INT= 1 (22.5792 MHz); MCLK_SRC_SEL = 00; all other fields are set to defaults; no signal on any input; control port inactive; all serial ports are set to Slave or Master Mode as indicated, input clock/data are held low unless active; test load is R_L = 32 Ω and C_L = 1 nF for HPOUTx; measured values include currents consumed by the DAC and do not include current delivered to external loads unless specified otherwise (e.g., from HPOUTx outputs); see Fig. 2-1.

Use Cases			Typical Current (µA)						Total Power (µW)
			P_{OUT}	i_{VCP}	i_{VA}	i_{VD}	i_{VL}	i_{VP}	
1		Off [1]	—	0	0	0	0	6	22
2		Standby [2] HPDETECT enabled	—	0	0	256	0	32	576
3	A	Playback External MCLK = 22.5792 MHz, I²S/DoP	Quiescent [3]	4021	7302	1444	40	32	23167
	B	Stereo HPOUT	0.1mW	12363	7862	2004	40	32	40199
4		Alternate HP path stereo HPIN enabled [4]	Quiescent	209	110	393	3	66	1524

1. Off configuration: Clock/data lines held low; $\overline{\text{RESET}}$ = LOW; VA = VD = VL = 0 V, VCP = 0 V, VP = 3.6 V.
2. Standby configuration: Clock/data lines held low; $\overline{\text{RESET}}$ = HIGH; VA = VD = VL = 1.8 V, VCP = 1.8 V, VP = 3.6 V; HP_DETECT_CTRL = 11 (enabled); HPDETECT_PLUG_INT_MASK=0 (unmasked); PDN_XTAL = 1, MCLK_SRC_SEL = 10 (RCO selected as MCLK source).
3. Quiescent configuration: data lines held low; $\overline{\text{RESET}}$ = HIGH; VA = 1.8 V, VD = VL = VCP = 1.8 V, VP = 3.6 V. Serial port, I²S/DoP Mode (ASP and SDIN, ASP_M/Sb = 0); PDN_XTAL = 1.
4. Quiescent configuration: PDN_XTAL = 1; MCLK_SRC_SEL = 10 (RCO selected as MCLK source); alternate headphone path (PDN_HP = 1, HPOUT_CLAMP = 1, HP_IN_EN = 1); data lines held low; $\overline{\text{RESET}}$ = HIGH; VA = 1.8 V, VD = VL = VCP = 1.8 V, VP = 3.6 V.

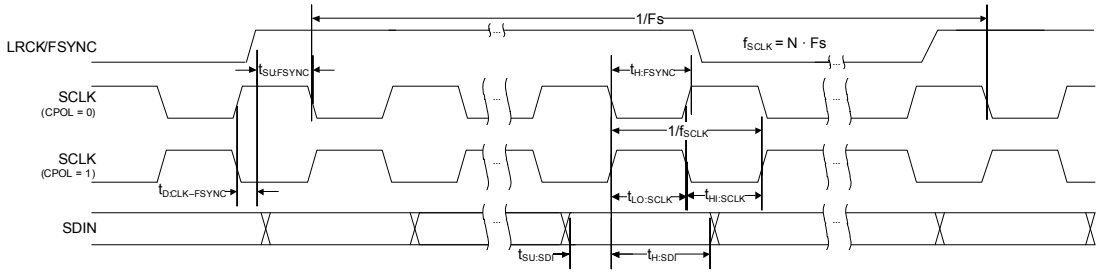
Table 3-18. Serial-Port Interface Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43130 connections; GNDA = GNDCP = GNDD = 0 V; voltages are with respect to ground; parameters can vary with VL; typical performance data taken with VL = VD = VA = VCP = 1.8 V, VP = 3.6 V; min/max performance data taken with VL = 1.8 V; VD = VA = VCP = 1.8 V, VP = 3.6 V; T_A = +25°C; C_L = 60 pF; Logic 0 = ground, Logic 1 = VL; output timings are measured at V_{OL} and V_{OH} thresholds (see Table 3-11).

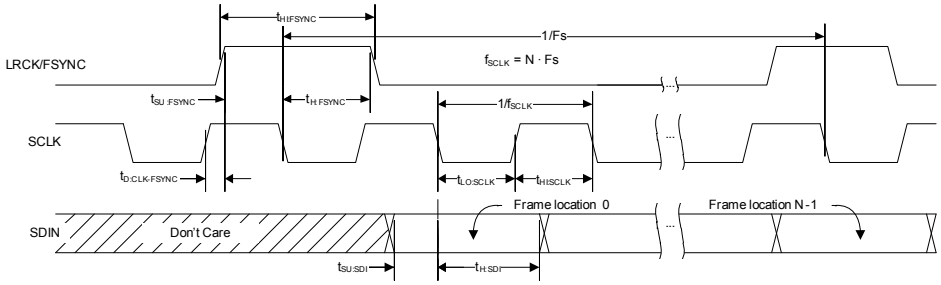
Parameters [1,2,3,4,5]			Symbol	Minimum	Typical	Maximum	Units
FSYNC frame rate			Fs	(See Section 4.9.5)			kHz
FSYNC high period [6]			$t_{HI:FSYNC}$	$1/f_{SCLK}$	—	$(n–1)/f_{SCLK}$	s
Master Mode	FSYNC duty cycle	xSP_5050 = 1	—	45	—	55	%
	FSYNC delay time after SCLK launching edge [7]		$t_{D:CLK–FSYNC}$	—	—	20	ns
	SCLK frequency		f_{SCLK}	—	—	f_{MCLK_INT}	MHz
	SCLK high period [8]		$t_{HI:SCLK}$	$1/(2•f_{SCLK}) – 1/f_{MCLK\_INT}$	—	$1/(2•f_{SCLK}) + 1/f_{MCLK\_INT}$	ns
	SDIN setup time before SCLK latching edge [7]		$t_{SU:SDI}$	10	—	—	ns
	SDIN hold time after SCLK latching edge [7]		$t_{H:SDI}$	5	—	—	ns
Slave Mode	FSYNC setup time before SCLK latching edge [7]		$t_{SU:FSYNC}$	10	—	—	ns
	FSYNC hold time after SCLK latching edge [7]		$t_{H:FSYNC}$	5	—	—	ns
	SCLK frequency		f_{SCLK}	—	—	24.58	MHz
	SCLK high period		$t_{HI:SCLK}$	16	—	—	ns
	SCLK low period		$t_{LO:SCLK}$	16	—	—	ns
	SDIN setup time before SCLK latching edge [9]		$t_{SU:SDI}$	10	—	—	ns
	SDIN hold time after SCLK latching edge [7]		$t_{H:SDI}$	5	—	—	ns

1. MCLK in this table refers to the external clock supplied to the MCLK pin ($MCLK_{EXT}$).
2. Output clock frequencies follow the master clock ($MCLK_{EXT}$) frequency proportionally. Any deviation of the clock source from the nominal supported rates are directly imparted to the output clock rate by the same factor (e.g., +100-ppm offset in the frequency of $MCLK_{EXT}$ becomes a +100-ppm offset in LRCK/FSYNC and SCLK).

3. I²S interface timing



4. TDM interface timing
(shown with xSP_FSD = 010, xSP_LCHI = 1)



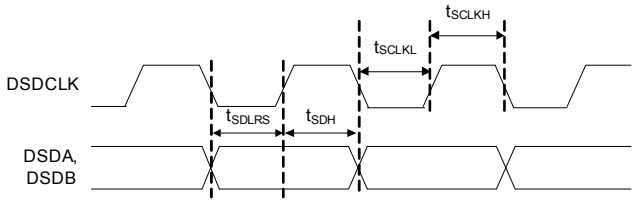
5. Applies to Master and Slave Modes, unless specified otherwise.
6. Maximum LRCK duty cycle is equal to frame length, in SCLK periods, minus 1. Maximum duty cycle occurs when LRCK high (xSP_LCHI) is set to 768 SCLK periods and LRCK period (xSP_LCPR) is set to 769 SCLK periods.
7. Data may be latched/launched on either the rising or falling edge of SCLK.
8. SCLK duty cycle in Master Mode depends on Master Mode clock configuration, and can vary by up to 1 $MCLK_{EXT}$ period.
9. Data is latched/launched on the rising or falling edge of SCLK as determined by xSP_SCPOL_OUT, xSP_SCPOL_IN, and xSP_FSD bits. See the SCLK launching specs in Table 3-18.

Table 3-19. DSD Switching Characteristic

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43130 connections; GNDA = GNDCP = GNDD = 0 V; voltages are with respect to ground; parameters can vary with VL; typical performance data taken with VL = VD = VA = VCP = 1.8 V, VP = 3.6 V; min/max performance data taken with VL = 1.8 V; VD = VA = VCP = 1.8 V, VP = 3.6 V; T_A = +25°C; C_L = 60 pF; Logic 0 = ground, Logic 1 = VL; output timings are measured at V_{OL} and V_{OH} thresholds (see Table 3-11).

Parameter [1,2]	Symbol	Minimum	Typical	Maximum	Units
DSDCLK duty cycle	—	40	—	60	%
DSDCLK pulse width low	t_{SCLKL}	80	—	—	ns
DSDCLK pulse width high	t_{SCLKH}	80	—	—	ns
DSDCLK frequency (64× oversampled) (128× oversampled)	—	1.024 2.048	2.8224 5.6448	$f_{MCLK\_INT}/8$ $f_{MCLK\_INT}/4$	MHz MHz
DSDA/DSDB valid to DSDCLK rising setup time	t_{SDLRS}	20	—	—	ns
DSDCLK rising to DSDA or DSDB hold time	t_{SDH}	20	—	—	ns
DSD clock to data transition (Phase Modulation Mode)	t_{DPM}	–20	—	20	ns

1. Serial audio input interface timing



2. Phase modulation mode serial audio input interface timing

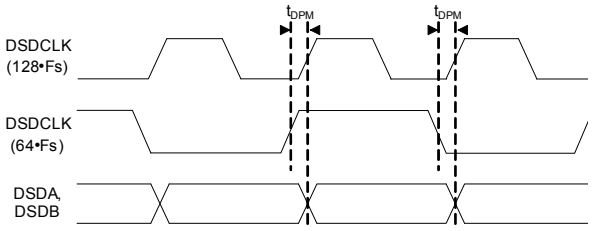
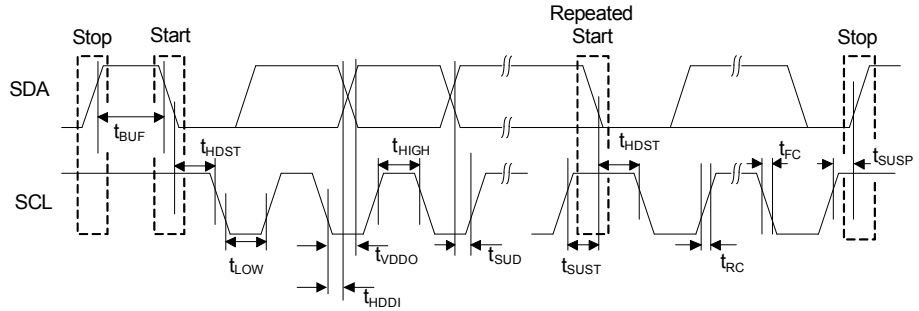


Table 3-20. I²C Slave Port Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows typical connections; Inputs: GNDA = GNDL = GNDCP = 0 V; all voltages with respect to ground; VL = 1.8 V; inputs: Logic 0 = GNDA = 0 V, Logic 1 = VL; T_A = +25°C; SDA load capacitance equal to maximum value of C_B = 400 pF; minimum SDA pull-up resistance, $R_{P(min)}$.[1] Table 3-1 describes some parameters in detail. All specifications are valid for the signals at the pins of the CS43130 with the specified load capacitance.

Parameter [2]		Symbol [3]	Minimum	Maximum	Units
SCL clock frequency		f_{SCL}	—	1000	kHz
Clock low time		t_{LOW}	500	—	ns
Clock high time		t_{HIGH}	260	—	ns
Start condition hold time (before first clock pulse)		t_{HDST}	260	—	ns
Setup time for repeated start		t_{SUST}	260	—	ns
Rise time of SCL and SDA	Standard Mode Fast Mode Fast Mode Plus	t_{RC}	— — —	1000 300 120	ns ns ns
Fall time of SCL and SDA	Standard Mode Fast Mode Fast Mode Plus	t_{FC}	— — —	300 300 120	ns ns ns
Setup time for stop condition		t_{SUSP}	260	—	ns
SDA setup time to SCL rising		t_{SUD}	50	—	ns
SDA input hold time from SCL falling [4]		t_{HDDI}	0	—	ns
Output data valid (Data/Ack) [5]	Standard Mode Fast Mode Fast Mode Plus	t_{VDDO}	— — —	3450 900 450	ns ns ns
Bus free time between transmissions		t_{BUF}	500	—	ns
SDA bus capacitance	SCL frequency = 1 MHz, V_L = 1.8 V SCL frequency ≤ 400 kHz	C_B	— —	400 400	pF pF
SCL/SDA pull-up resistance [1]	V_L = 1.8 V	R_P	350	—	Ω
Pulse width of spikes to be suppressed		t_{PS}	—	50	ns
Switching time between RCO and MCLK_INT [6]		—	150	—	µs
Power-up delay (delay before I²C can communicate after $\overline{\text{RESET}}$ released)		t_{PUD}	1500	—	µs

1. The minimum R_P value (resistor shown in Fig. 2-1) is determined by using the maximum level of VL, the minimum sink current strength of its respective output, and the maximum low-level output voltage V_{OL}. The maximum R_P value may be determined by how fast its associated signal must transition (e.g., the lower the value of R_P, the faster the I²C bus is able to operate for a given bus load capacitance). See I²C bus specification referenced in Section 13.
2. All timing is relative to thresholds specified in Table 3-11, V_{IL} and V_{IH} for input signals, and V_{OL} and V_{OH} for output signals.
3. I²C control-port timing



4. Data must be held long enough to bridge the transition time, t_F, of SCL.
5. Time from falling edge of SCL until data output is valid.
6. Upon setting MCLK_SRC_SEL and sending the I²C stop condition, the switching of RCO and other MCLK_INT sources occurs. A least wait time as specified is required after changing MCLK_SRC_SEL and sending the I²C stop condition before the next I²C transaction is initiated.

4 Functional Description

This section describes the general theory of operation of the CS43130, tracing the signal and control flow through the various blocks within the device. It comprises the following sections:

4.1 Overview

4.1.1 Analog Outputs

The analog output block includes separate pseudodifferential headphone Class H amplifiers output. An on-chip inverting charge pump creates a positive and negative voltage equal to the input, allowing an adaptable, full-scale output swing centered around ground. The resulting internal amplifier supply can be ±VCP, or ±VP_LDO (either ±3.0 V with HV_EN = 1 or ±2.6 V with HV_EN = 0).

The inverting architecture eliminates the need for large DC-blocking capacitors and allows the amplifier to deliver more power to HP loads at lower supply voltages. This adaptive power supply scheme converts traditional Class AB amplifiers into more power-efficient Class H amplifiers.

4.1.2 Alternate Headphone Inputs

The alternate headphone inputs provide an integrated selectable path to interface between the system codec output and the headphone connector, which allows for lower-power operation in applications such as voice or compressed music playback. These inputs eliminate the need for an external audio switch and prevent the high-fidelity headphone outputs of CS43130 from degradation by the external audio switch.

4.1.3 Headphone Detection

The CS43130 detects the presence of a headphone and notifies the application processor to wake up through an interrupt event.

4.1.4 Headphone Impedance Measurement

The CS43130 detects headphone impedance information at low frequencies, which can be used to adjust the system properly to accommodate different load conditions. One example is to adjust signal chain gain to avoid distortion.

The CS43130 also provides impedance measurement functions to evaluate the headphone load within 20 Hz to 20 kHz. A specific frequency is selected and the impedance measurement process is initiated by setting the register. Through a series of interrupt events, the CS43130 notifies application processor to retrieve the impedance information after completion.

4.1.5 Audio Interfaces and Supported Formats

There are two serial input ports on the CS43130, the audio serial port (ASP) and the auxiliary serial port (XSP). The ASP on the CS43130 supports I²S, TDM, and DoP (DSD over PCM) formats up to a 384-kHz sample rate. The XSP on the CS43130 supports the DoP format up to a 352.8-kHz sample rate.

The CS43130 also has a dedicated DSD interface to support up to 128•Fs. The DSD interface shares pins with the XSP.

4.1.6 System Clocking

The CS43130 internal MCLK can be sourced from three options:

- Direct MCLK/crystal mode. The internal MCLK is provided through XTI/MCLK pin directly or generated by crystal oscillator.
- PLL mode. A PLL reference CLK is provided externally through XTI/MCLK. The PLL is configured, and output is used as the internal MCLK.
- RCO mode. An internal RCO is used as the internal MCLK. Note that HPIN input path is the only supported audio playback feature in this mode for optimized power consumption. This mode can also support HP detection and I²C communication. DAC playback and headphone impedance measurement function s are not supported.

The clock output is provided for audio applications that require high quality audio rate system clock. This clock output can be sourced from the following two options:

- The clock generated by the CS43130 crystal oscillator.
- Output of the internal Fractional-N PLL that refers to MCLK input. See Section 4.7.1 for supported frequencies.

The internal MCLK is used to generate serial port clocks. See Table 4-6 for supported LRCK combinations.

4.1.7 System Interrupts

The CS43130 includes an open-drain interrupt output ($\overline{\text{INT}}$ pin). Interrupt mask registers control whether an event associated with an interrupt status/mask bit pair triggers the assertion of $\overline{\text{INT}}$. All types of interrupts are described in Section 4.11.

4.1.8 System Reset

The CS43130 offers two types of reset options:

- Asserting $\overline{\text{RESET}}$. If $\overline{\text{RESET}}$ is asserted, all registers and all state machines are immediately set to their default values/states. No operation can begin until $\overline{\text{RESET}}$ is deasserted. Before normal operation can begin, $\overline{\text{RESET}}$ must be asserted at least once after the VP supply is first brought up.
- Power-on reset (POR). If the VD supply is lower than the POR threshold specified in Table 3-16, the VD register fields and the state machines are held in reset, setting them to their default values/states. The POR releases the reset when the VD supply goes above the POR threshold. When the VD supply is turned on, the VL and VA supplies must also be turned on at the same time.

4.1.9 Power Down

The CS43130 has a register byte to power down individual components on the chip. Before any change can be applied to an individual component (except PLL), the block must be powered down first. For the PLL, changes can be applied after PLL_START is cleared.

The PDN_HP bit is responsible for enabling or disabling the playback signal chain operation. All the necessary components for playback operation need to be powered up and configured properly before PDN_HP is cleared. To disable the playback signal chain, PDN_HP is set. PDN_HP needs to be set before making any changes to the playback signal chain setup, except the following functions:

- Volume and mute related functions
- PCM filter settings (see Section 7.5.2)