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CS4341

24-Bit, 96 kHz Stereo DAC with Volume Control

Features

- 101 dB Dynamic Range
- -91 dB THD+N
- +3.0 V or +5.0 V Power Supply
- Low Clock-Jitter Sensitivity
- Filtered Line-Level Outputs
- On-Chip Digital De-Emphasis for 32, 44.1 and 48 kHz
- ATAPI Mixing
- Digital Volume Control with Soft Ramp
  - 94 dB Attenuation
  - 1 dB Step Size
  - Zero Crossing Click-Free Transitions
- Popguard® Technology for Control of Clicks and Pops
- 33 mW with 3.0 V Supply

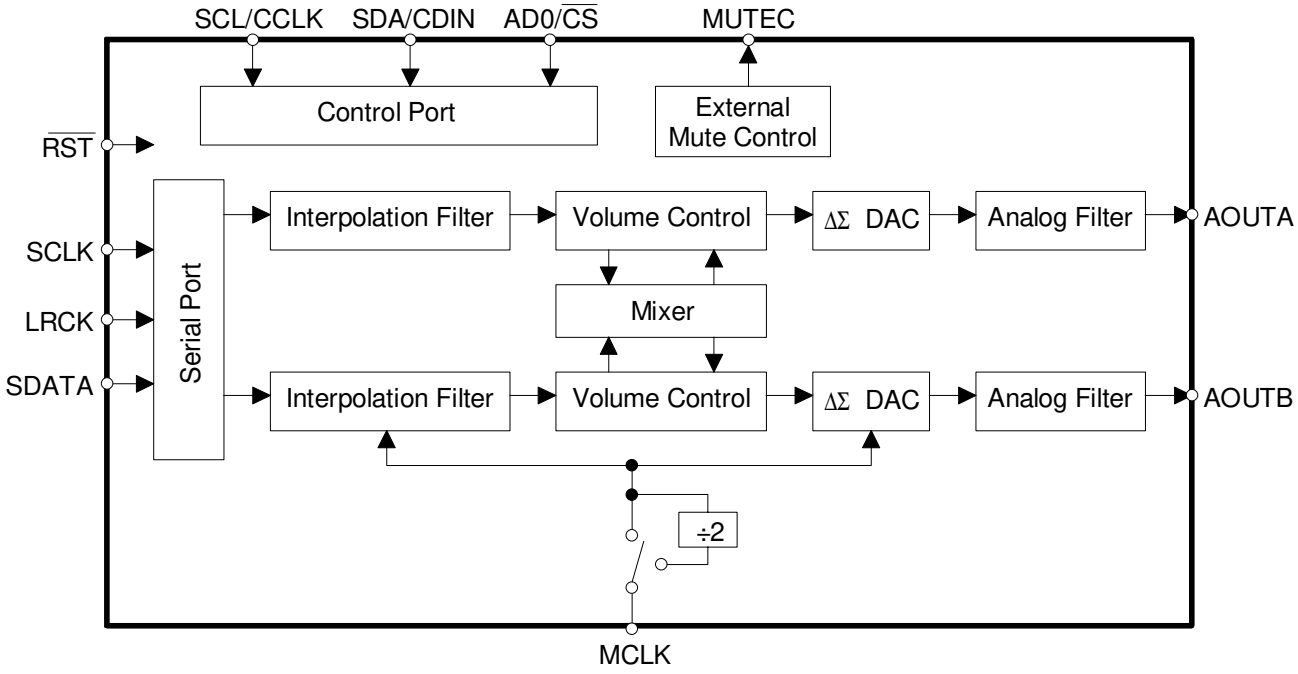
Description

The CS4341 is a complete stereo digital-to-analog system including digital interpolation, fourth-order Delta-Sigma digital-to-analog conversion, digital de-emphasis and switched capacitor analog filtering. The advantages of this architecture include: ideal differential linearity, no distortion mechanisms due to resistor matching errors, no linearity drift over time and temperature and a high tolerance to clock jitter.

The CS4341 accepts data at audio sample rates from 4 kHz to 100 kHz, consumes very little power, and operates over a wide power supply range. The features of the CS4341 are ideal for DVD players, CD players, set-top box and automotive systems.

ORDERING INFORMATION

CS4341-KS	16-pin SOIC, -10 to 70 °C
CS4341-CZZ, Lead Free	16-pin TSSOP, -10 to 70 °C
CDB4341	Evaluation Board



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LIST OF TABLES

1. CHARACTERISTICS AND SPECIFICATIONS

(Min/Max performance characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics are derived from measurements taken at T_A = 25°C.)

SPECIFIED OPERATING CONDITIONS (All voltages with respect to AGND = 0 V.)

Parameters		Symbol	Min	Nom	Max	Units
DC Power Supply						
	Nominal 3.3 V	VA	2.7	3.3	3.6	V
	Nominal 5.0 V	VA	4.75	5.0	5.5	V
Specified Operating Temperature (Power Applied)	-KS/CZZ	T_A	-10	-	+70	°C

ABSOLUTE MAXIMUM RATINGS (AGND = 0 V; all voltages with respect to AGND. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.)

Parameters		Symbol	Min	Max	Units
DC Power Supply		VA	-0.3	6.0	V
Input Current	(Note 1)	I_{in}	-	±10	mA
Digital Input Voltage		V_{IND}	-0.3	VA+0.4	V
Ambient Operating Temperature (power applied)		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Notes: 1. Any pin except supplies.

ANALOG CHARACTERISTICS (CS4341-KS/CZZ) (Test conditions (unless otherwise specified): Input test signal is a 997 Hz sine wave at 0 dBFS; measurement bandwidth is 10 Hz to 20 kHz; test load R_L = 10 kΩ, C_L = 10 pF (see Figure 1).)

Parameter		VA = 5.0 V			VA = 3.0 V			Unit
		Min	Typ	Max	Min	Typ	Max	
Single-Speed Mode	**Fs = 48 kHz**							
Dynamic Range	(Note 2)							
18 to 24-Bit	unweighted	93	98	-	89	94	-	dB
	A-Weighted	96	101	-	92	97	-	dB
16-Bit	unweighted	-	92	-	-	92	-	dB
	A-Weighted	-	95	-	-	95	-	dB
Total Harmonic Distortion + Noise	(Note 2)							
18 to 24-Bit	0 dB	-	-91	-86	-	-94	-89	dB
	-20 dB	-	-78	-	-	-74	-	dB
	-60 dB	-	-38	-	-	-34	-	dB
16-Bit	0 dB	-	-90	-	-	-91	-	dB
	-20 dB	-	-72	-	-	-72	-	dB
	-60 dB	-	-32	-	-	-32	-	dB
Double-Speed Mode	**Fs = 96 kHz**							
Dynamic Range	(Note 2)							
18 to 24-Bit	unweighted	93	98	-	89	94	-	dB
	A-Weighted	96	101	-	92	97	-	dB
16-Bit	unweighted	-	92	-	-	92	-	dB
	A-Weighted	-	95	-	-	95	-	dB
Total Harmonic Distortion + Noise	(Note 2)							
18 to 24-Bit	0 dB	-	-91	-86	-	-94	-89	dB
	-20 dB	-	-78	-	-	-74	-	dB
	-60 dB	-	-38	-	-	-34	-	dB
16-Bit	0 dB	-	-90	-	-	-91	-	dB
	-20 dB	-	-72	-	-	-72	-	dB
	-60 dB	-	-32	-	-	-32	-	dB

ANALOG CHARACTERISTICS (CS4341-KS/CZZ) (Continued)

Parameters		Symbol	Min	Typ	Max	Units
Dynamic Performance for All Modes						
Interchannel Isolation (1 kHz)			-	100	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	-	dB
Gain Drift			-	±100	-	ppm/°C
Analog Output Characteristics and Specifications						
Full-Scale Output Voltage			0.6•VA	0.7•VA	0.8•VA	Vpp
Output Impedance			-	100	-	Ω
Minimum AC-Load Resistance	(Note 3)	R_L	-	3	-	kΩ
Maximum Load Capacitance	(Note 3)	C_L	-	100	-	pF

Notes: 2. One-half LSB of triangular PDF dither is added to data.

3. Refer to Figure 2.

.

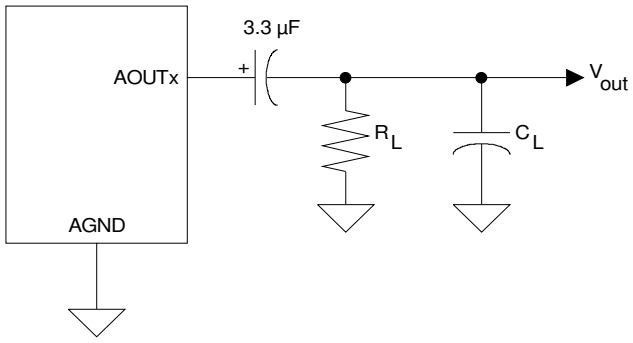


Figure 1. Output Test Load

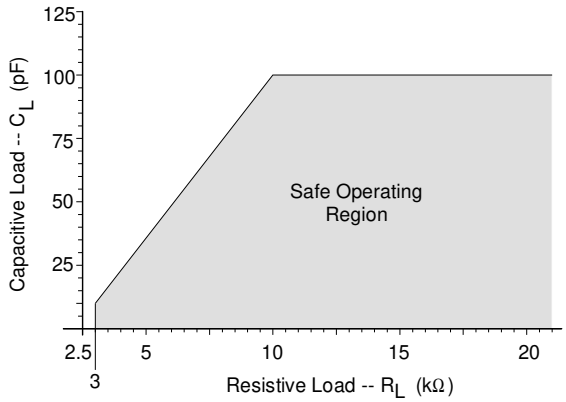


Figure 2. Maximum Loading

COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE (The filter characteristics and the X-axis of the response plots have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs.)

Parameter		Min	Typ	Max	Unit
Single-Speed Mode - (4 kHz to 50 kHz sample rates)					
Passband					
	to -0.05 dB corner	0	-	0.4535	Fs
	to -3 dB corner	0	-	0.4998	Fs
Frequency Response 10 Hz to 20 kHz		-0.02	-	+0.08	dB
StopBand		0.5465	-	-	Fs
StopBand Attenuation	(Note 4)	50	-	-	dB
Group Delay		-	9/Fs	-	s
Passband Group Delay Deviation	0 - 20 kHz	-	±0.36/Fs	-	s
De-emphasis Error (Relative to 1 kHz)	Fs = 32 kHz	-	-	+0.2/-0.1	dB
(Note 5)	Fs = 44.1 kHz	-	-	+0.05/-0.14	dB
	Fs = 48 kHz	-	-	+0/-0.22	dB
Double-Speed Mode - (50 kHz to 100 kHz sample rates)					
Passband					
	to -0.1 dB corner	0	-	0.4621	Fs
	to -3 dB corner	0	-	0.4982	Fs
Frequency Response 10 Hz to 20 kHz		-0.06	-	+0.2	dB
StopBand		0.577	-	-	Fs
StopBand Attenuation	(Note 4)	55	-	-	dB
Group Delay		-	4/Fs	-	s
Passband Group Delay Deviation	0 - 40 kHz	-	±1.39/Fs	-	s
	0 - 20 kHz	-	±0.23/Fs	-	s

Notes: 4. For Single-Speed Mode, the measurement bandwidth is 0.5465 Fs to 3 Fs.
For Double-Speed Mode, the measurement bandwidth is 0.577 Fs to 1.4 Fs.

5. De-emphasis is only available in Single-Speed Mode.

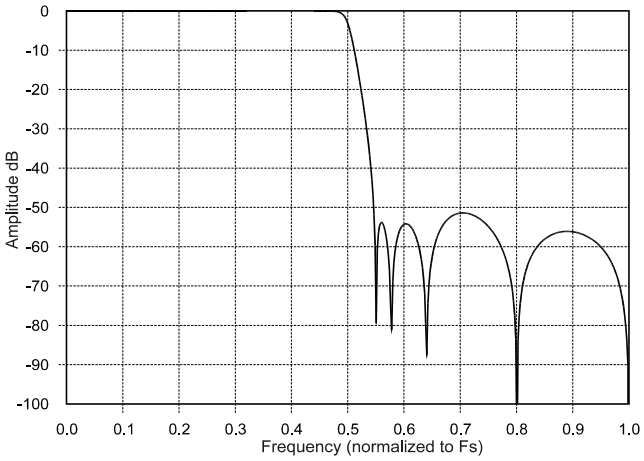


Figure 3. Single-Speed Stopband Rejection

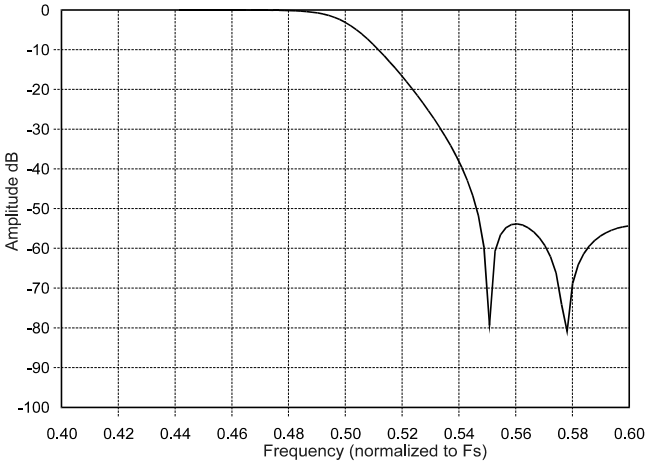


Figure 4. Single-Speed Transition Band

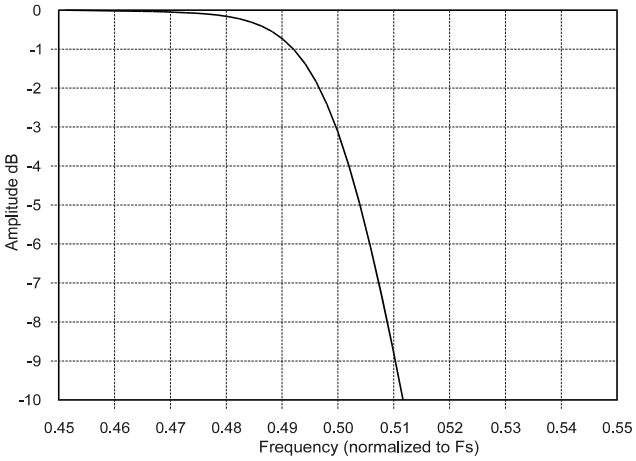


Figure 5. Single-Speed Transition Band (Detail)

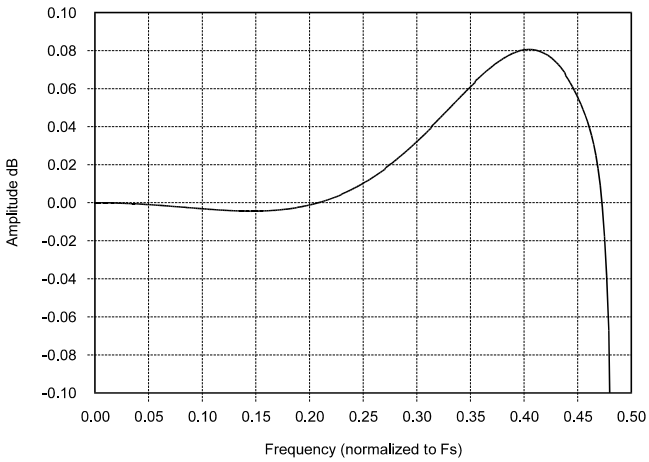


Figure 6. Single-Speed Passband Ripple

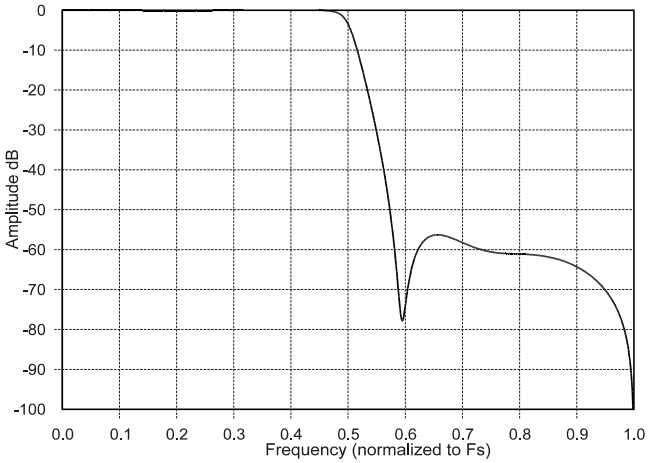


Figure 7. Double-Speed Stopband Rejection

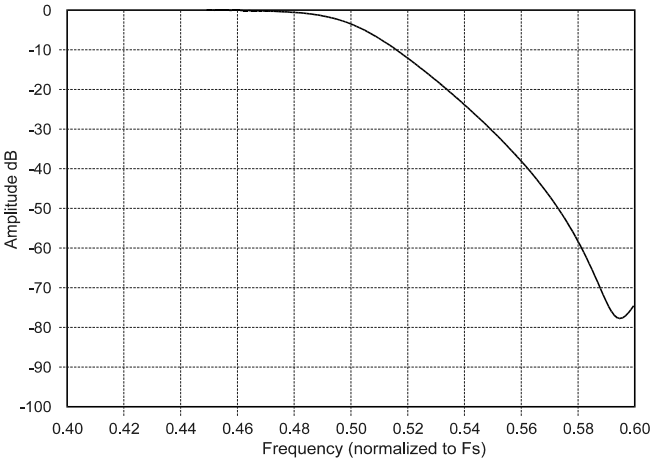


Figure 8. Double-Speed Transition Band

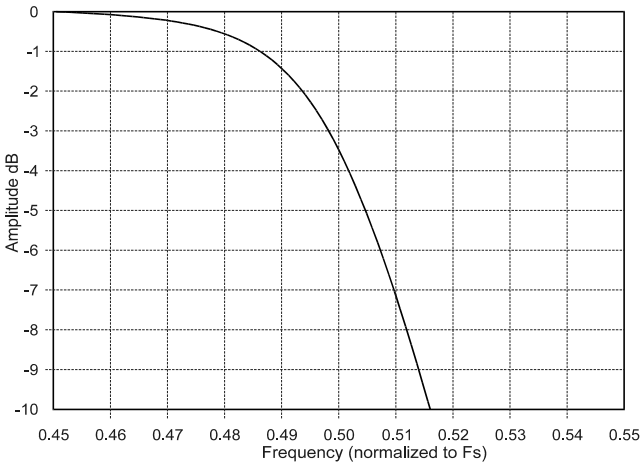


Figure 9. Double-Speed Transition Band (Detail)

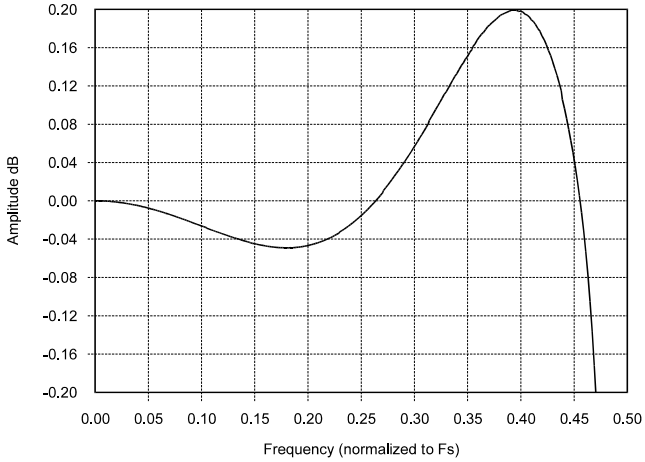


Figure 10. Double-Speed Passband Ripple

SWITCHING SPECIFICATIONS - SERIAL AUDIO INTERFACE

Parameters		Symbol	Min	Max	Units
MCLK Frequency			1.024	51.2	MHz
MCLK Duty Cycle			45	55	%
Input Sample Rate	Single-Speed Mode Double-Speed Mode	Fs Fs	4 50	50 100	kHz kHz
LRCK Duty Cycle			40	60	%
SCLK Pulse Width Low		t_{sclkl}	20	-	ns
SCLK Pulse Width High		t_{sclkh}	20	-	ns
SCLK Frequency	Single-Speed Mode Double-Speed Mode		- -	128xFs 64xFs	Hz Hz
SCLK rising to LRCK edge delay		t_{slrd}	20	-	ns
SCLK rising to LRCK edge setup time		t_{slrs}	20	-	ns
SDIN valid to SCLK rising setup time		t_{sdlrs}	20	-	ns
SCLK rising to SDIN hold time		t_{sdh}	20	-	ns

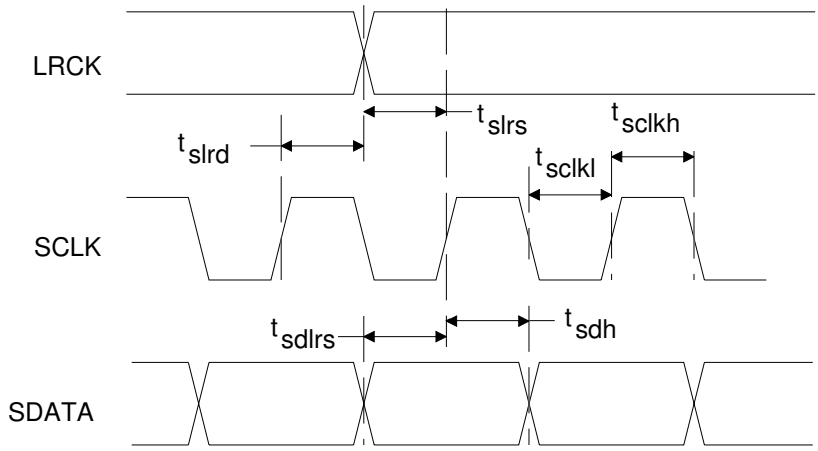


Figure 11. Serial Input Timing (External SCLK)

SWITCHING CHARACTERISTICS - INTERNAL SERIAL CLOCK

Parameters	Symbol	Min	Typ	Max	Units
MCLK Frequency		1.024	-	51.2	MHz
MCLK Duty Cycle		45	-	55	%
Input Sample Rate Single-Speed Mode Double-Speed Mode	Fs Fs	4 50	- -	50 100	kHz kHz
LRCK Duty Cycle			(Note 6)		%
SCLK Period (Note 7)	t_{sclkw}	$\frac{1}{SCLK}$	-	-	s
SCLK rising to LRCK edge	t_{sclkr}	-	$\frac{t_{sclkw}}{2}$	-	s
SDATA valid to SCLK rising setup time	t_{sdlrs}	$\frac{1}{(512)Fs} + 10$	-	-	ns
SCLK rising to SDATA hold time MCLK / LRCK = 512, 256 or 128	t_{sdh}	$\frac{1}{(512)Fs} + 15$	-	-	ns
SCLK rising to SDATA hold time MCLK / LRCK = 384 or 192	t_{sdh}	$\frac{1}{(384)Fs} + 15$	-	-	ns

Notes: 6. The Duty Cycle must be 50% +/– 1/2 MCLK Period.

7. See section 4.2.1 for derived internal frequencies.

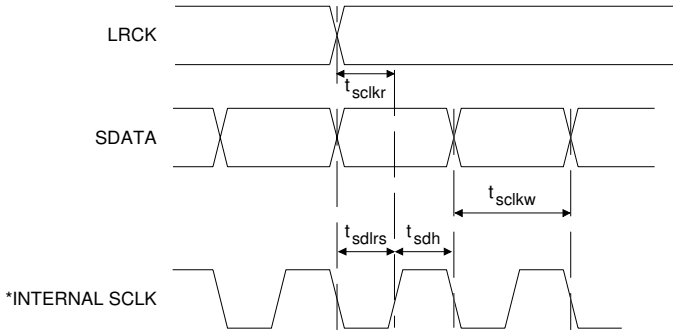


Figure 12. Internal Serial Mode Input Timing

*The SCLK pulses shown are internal to the CS4341.

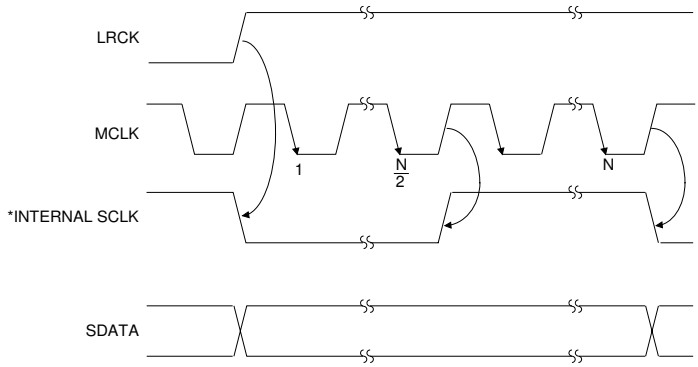


Figure 13. Internal Serial Clock Generation

* The SCLK pulses shown are internal to the CS4341. N equals MCLK divided by SCLK

SWITCHING CHARACTERISTICS - CONTROL PORT INTERFACE (I²C®)

Parameter		Symbol	Min	Max	Unit
I²C Mode					
SCL Clock Frequency		f_{scl}	-	100	kHz
$\overline{RST}$ Rising Edge to Start		t_{irs}	500	-	ns
Bus Free Time Between Transmissions		t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)		t_{hdst}	4.0	-	µs
Clock Low time		t_{low}	4.7	-	µs
Clock High Time		t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition		t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling	(Note 8)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising		t_{sud}	250	-	ns
Rise Time of SCL	(Note 9)	t_{rc}	-	25	ns
Fall Time of SCL		t_{fc}	-	25	ns
Rise Time SDA		t_{rd}	-	1	µs
Fall Time of SDA		t_{fd}	-	300	ns
Setup Time for Stop Condition		t_{susp}	4.7	-	µs

Notes: 8. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

9. See “Rise Time for Control Port Clock” on page 21 for a recommended circuit to meet rise time specification.

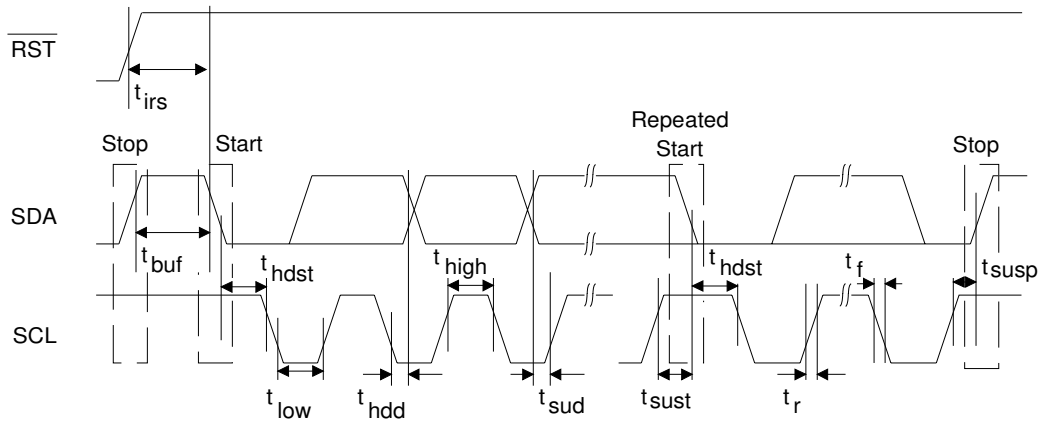


Figure 14. Control Port Timing - I²C Mode

SWITCHING CHARACTERISTICS - CONTROL PORT INTERFACE (SPI™)

Parameter		Symbol	Min	Max	Unit
SPI Mode					
CCLK Clock Frequency		f_{sclk}	-	6	MHz
$\overline{RST}$ Rising Edge to $\overline{CS}$ Falling		t_{srs}	500	-	ns
CCLK Edge to $\overline{CS}$ Falling	(Note 10)	t_{spi}	500	-	ns
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	$\frac{1}{MCLK}$	-	ns
CCLK High Time		t_{sch}	$\frac{1}{MCLK}$	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 11)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN	(Note 12)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 12)	t_{f2}	-	100	ns

Notes: 10. t_{spi} only needed before first falling edge of $\overline{CS}$ after $\overline{RST}$ rising edge. t_{spi} = 0 at all other times.

11. Data must be held for sufficient time to bridge the transition time of CCLK.

12. For f_{sclk} < 1 MHz.

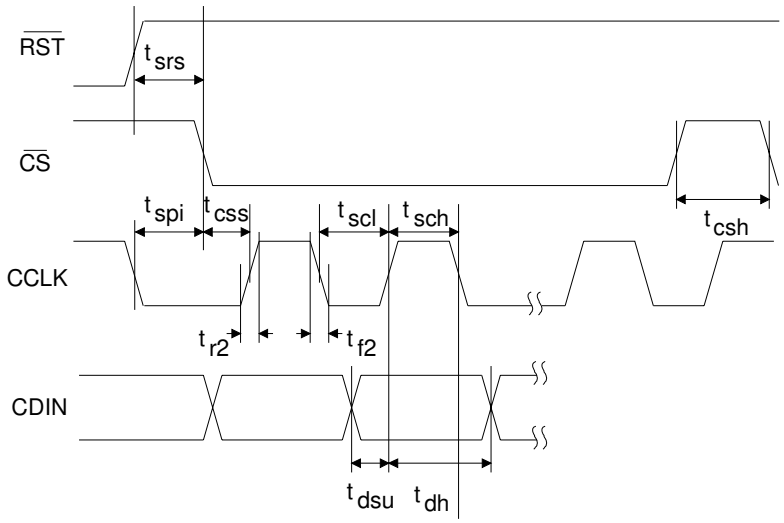


Figure 15. Control Port Timing - SPI Mode

DC ELECTRICAL CHARACTERISTICS (AGND = 0 V; all voltages with respect to AGND.)

Parameters		Symbol	Min	Typ	Max	Units
Normal Operation (Note 13)						
Power Supply Current	VA = 5.0 V	I_A	-	15	18	mA
	VA = 3.0 V	I_A	-	11	14	mA
Power Dissipation	VA = 5.0 V		-	75	90	mW
	VA = 3.0 V		-	33	42	mW
Power-down Mode (Note 14)						
Power Supply Current	VA = 5.0 V	I_A	-	60	-	µA
	VA = 3.0 V		-	30	-	µA
Power Dissipation	VA = 5.0 V		-	0.3	-	mW
	VA = 3.0 V		-	0.09	-	mW
All Modes of Operation						
Power Supply Rejection Ratio (Note 15)	1 kHz	PSRR	-	60	-	dB
	60 Hz		-	40	-	dB
V_Q Nominal Voltage			-	0.45•VA	-	V
Output Impedance			-	250	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA
Filt+ Nominal Voltage			-	VA	-	V
Output Impedance			-	250	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA
MUTEC Low-Level Output Voltage			-	0	-	V
MUTEC High-Level Output Voltage			-	VA	-	V
Maximum MUTEC Drive Current			-	3	-	mA

Notes: 13. Normal operation is defined as $\overline{RST}$ = HI with a 997 Hz, 0 dBFS input sampled at the highest Fs for each speed mode, and open outputs, unless otherwise specified.

14. Power Down Mode is defined as $\overline{RST}$ = LO with all clocks and data lines held static.

15. Valid with the recommended capacitor values on FILT+ and VQ as shown in Figure 16. Increasing the capacitance will also increase the PSRR.

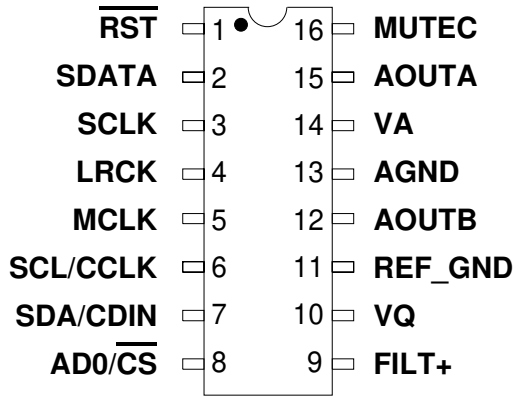
DIGITAL INPUT CHARACTERISTICS (AGND = 0 V; all voltages with respect to AGND.)

Parameters	Symbol	Min	Typ	Max	Units
Input Leakage Current	I_{in}	-	-	±10	µA
Input Capacitance		-	8	-	pF

DIGITAL INTERFACE SPECIFICATIONS (AGND = 0 V; all voltages with respect to AGND.)

Parameters	Symbol	Min	Max	Units
3.3 V Logic *(3.0 V to 3.6 V DC Supply)*				
High-Level Input Voltage	V_{IH}	2.0	-	V
Low-Level Input Voltage	V_{IL}	-	0.8	V
5.0 V Logic *(4.75 V to 5.25 V DC Supply)*				
High-Level Input Voltage	V_{IH}	2.0	-	V
Low-Level Input Voltage	V_{IL}	-	0.8	V

2. PIN DESCRIPTION



Pin Name	#	Pin Description
RST	1	**Reset** (*Input*) - Powers down device and resets registers to their default settings.
SDATA	2	**Serial Audio Data** (*Input*) - Input for two's complement serial audio data.
SCLK	3	**Serial Clock** (*Input*) -Serial clock for the serial audio interface.
LRCK	4	**Left Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	5	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
SCL/CCLK	6	**Serial Control Port Clock** (*Input*) - Serial clock for the control port interface.
SDA/CDIN	7	**Serial Control Data I/O** (*Input/Output*) - Input/Output for I²C data. Input for SPI data.
AD0/CS	8	**Address Bit** / **Chip Select** (*Input*) - Chip address bit in I²C Mode. Control signal used to select the chip in SPI mode.
FILT+	9	**Positive Voltage Reference** (*Output*) **-** Positive voltage reference for the internal sampling circuits.
VQ	10	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent reference voltage.
REF_GND	11	**Reference Ground** (*Input*) - Ground reference for the internal sampling circuits.
AOUTB AOUTA	12 15	**Analog Outputs** (*Output*) - The full-scale analog output level is specified in the *Analog Characteristics* table.
AGND	13	**Analog Ground** (*Input*)
VA	14	**Power** (*Input*) **-** Positive power for the analog, digital, and serial audio interface sections.
MUTEC	16	**Mute Control** (*Output*) - Control signal for an optional mute circuit.

3. TYPICAL CONNECTION DIAGRAM

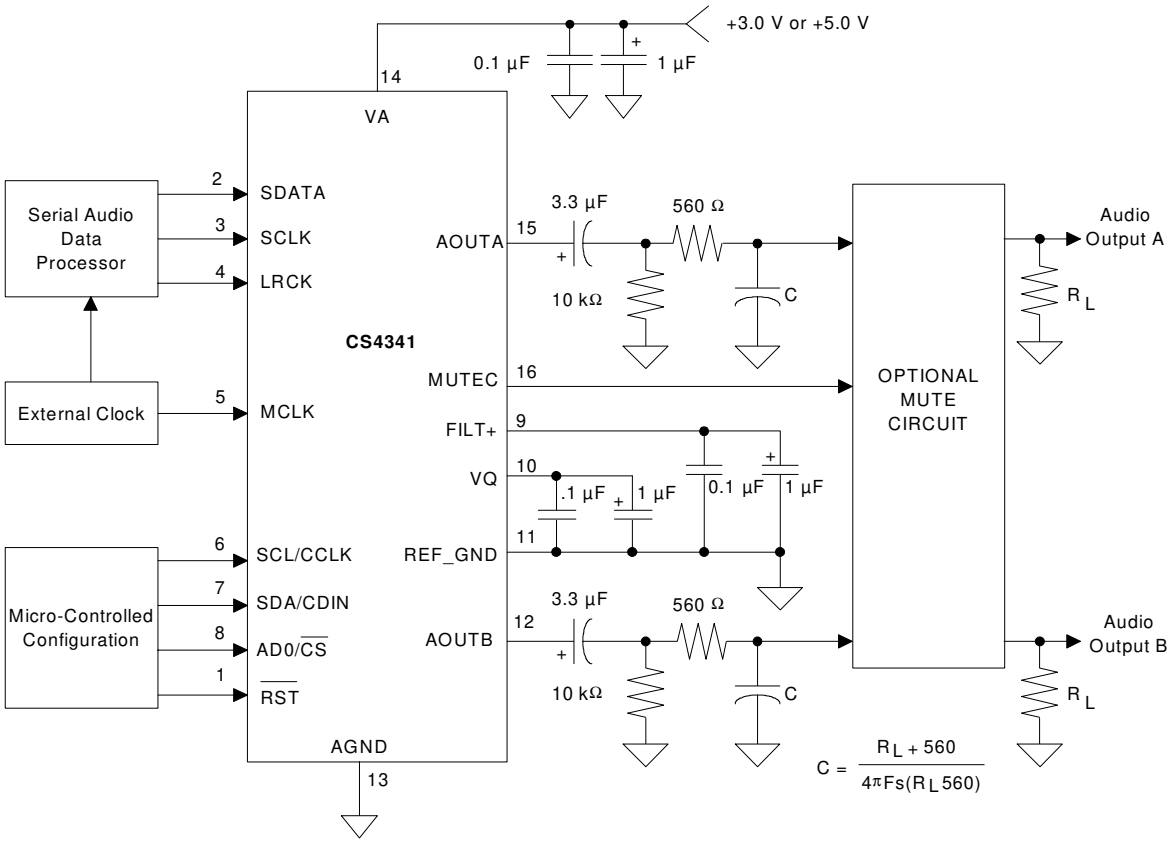


Figure 16. Typical Connection Diagram

4. APPLICATIONS

4.1 Sample Rate Range/Operational Mode

The device operates in one of two operational modes determined by the Master Clock to Left/Right Clock ratio (see section 4.2). Sample rates outside the specified range for each mode are not supported.

Input Sample Rate (Fs)	MODE
4 kHz - 50 kHz	Single-Speed Mode
50 kHz - 100 kHz	Double-Speed Mode

Table 1. CS4341 Speed Modes

4.2 System Clocking

The device requires external generation of the master (MCLK) and left/right (LRCK) clocks. The device also requires external generation of the serial clock (SCLK) if the internal serial clock is not used. The LRCK, defined also as the input sample rate Fs, must be synchronously derived from MCLK according to specified ratios. The specified ratios of MCLK to LRCK, along with several standard audio sample rates and the required MCLK frequency, are illustrated in Tables 2 and 3.

Sample Rate (kHz)	MCLK (MHz)				
	256x	384x	512x	768x*	1024x*
32	8.1920	12.2880	16.3840	24.5760	32.768
44.1	11.2896	16.9344	22.5792	33.8688	45.1584
48	12.2880	18.4320	24.5760	36.8640	49.1520

Table 2. Single-Speed Mode Standard Frequencies

Sample Rate (kHz)	MCLK (MHz)			
	128x	192x	256x*	384x*
64	8.1920	12.2880	16.3840	24.5760
88.2	11.2896	16.9344	22.5792	33.8688
96	12.2880	18.4320	24.5760	36.8640

Table 3. Double-Speed Mode Standard Frequencies

*Requires MCLKDIV bit = 1 in the MCLK Control (address 00h) register.

4.2.1 Internal Serial Clock Mode

The device will enter the Internal Serial Clock Mode if no low to high transitions are detected on the SCLK pin for 2 consecutive periods of LRCK. In this mode, the SCLK is internally derived and synchronous with MCLK and LRCK. The SCLK/LRCK ratio is either 32, 48, or 64 depending upon the MCLK/LRCK ratio and the Digital Interface Format selection (see Table 4).

Operation in the Internal Serial Clock mode is identical to operation with an external SCLK synchronized with LRCK; however, External SCLK mode is recommended for system clocking applications.

Input MCLK/LRCK Ratio	Digital Interface Format Selection				Internal SCLK/LRCK Ratio
	I²S up to 16 or 24 Bits	*Left Justified 24 Bits*	*Right Justified 18, 20 or 24 Bits*	*Right Justified 16 Bits*	
512, 256, 128	(Format 1)	-	-	X	32
384, 192	X	X	X	X	48
512, 256, 128	(Format 0)	X	X	-	64

Table 4. Internal SCLK/LRCK Ratio

4.2.2 External Serial Clock Mode

The device will enter the External Serial Clock Mode whenever 16 low to high transitions are detected on the SCLK pin during any phase of the LRCK period. The device will revert to Internal Serial Clock Mode if no low to high transitions are detected on the SCLK pin for 2 consecutive periods of LRCK.

4.3 Digital Interface Format

The device will accept audio samples in several digital interface formats. The desired format is selected via the DIF0, DIF1 and DIF2 bits in the Mode Control register (see section 6.2.2). For an illustration of the required relationship between LRCK, SCLK and SDATA, see Figures 17 through 19.

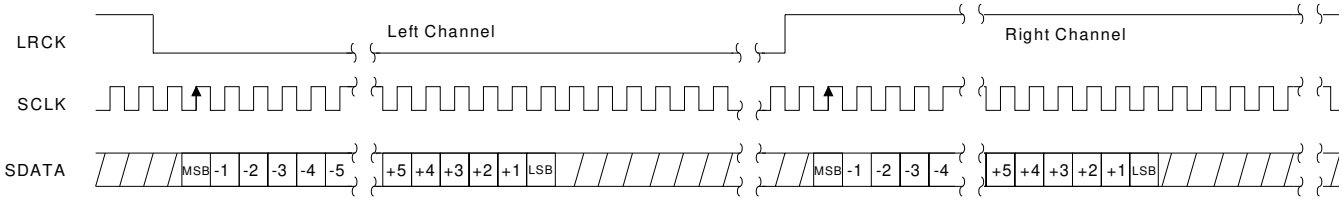


Figure 17. CS4341 Formats 0-1 - I²S up to 24-Bit Data

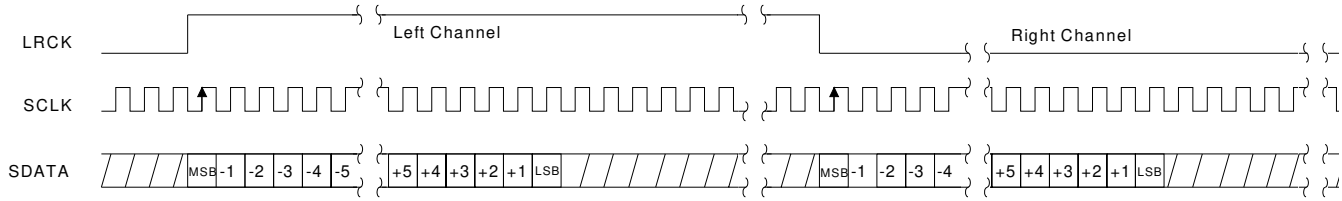


Figure 18. CS4341 Format 2 - Left Justified up to 24-Bit Data

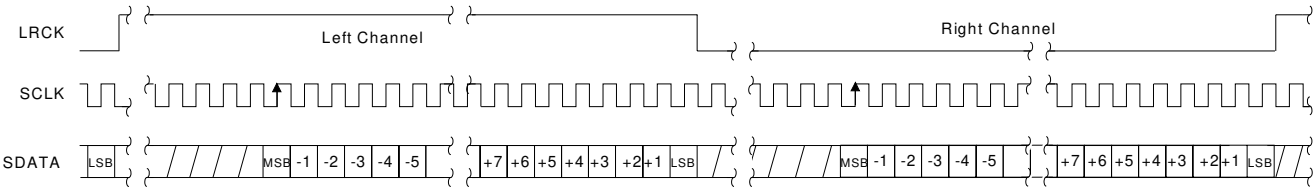


Figure 19. CS4341 Formats 3-6 - Right Justified

4.4 De-Emphasis

The device includes on-chip digital de-emphasis. The Mode Control (address 01h) bits select either the 32, 44.1 or 48 kHz de-emphasis filter. Figure 20 shows the de-emphasis curve for F_s equal to 44.1 kHz. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, Fs. Please see section 6.2.3 for the desired de-emphasis control.

De-emphasis is only available in Single-Speed Mode.

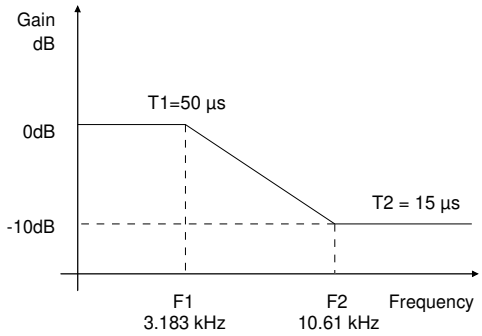


Figure 20. De-Emphasis Curve

4.5 Power-Up Sequence

1) Hold $\overline{\text{RST}}$ low until the power supply is stable, and the master and left/right clocks are locked to the appropriate frequencies, as discussed in section 4.2. In this state, the control port is reset to its default settings and VQ will remain low.
2) Bring $\overline{\text{RST}}$ high. The device will remain in a low power state with VQ low.
3) Load the desired register settings while keeping the PDN bit set to 1.
4) Set the PDN bit to 0. This will initiate the power-up sequence, which lasts approximately 50 µS when the POR bit is set to 0. If the POR bit is set to 1, see section 4.6 for a complete description of power-up timing.

4.6 Popguard® Transient Control

The CS4341 uses Popguard® technology to minimize the effects of output transients during power-up and power-down. This technology, when used with external DC-blocking capacitors in series with the audio outputs, minimizes the audio transients commonly produced by single-ended single-supply converters. It is activated inside the DAC when $\overline{\text{RST}}$ is enabled/disabled and requires no other external control, aside from choosing the appropriate DC-blocking capacitors.

4.6.1 Power-Up

When the device is initially powered-up, the audio outputs, AOUTL and AOUTR, are clamped to AGND. Following a delay of approximately 1000 sample periods, each output begins to ramp toward the quiescent voltage. Approximately 10,000 LRCK cycles later, the outputs reach V_Q and audio output begins. This gradual voltage ramping allows time for the external DC-blocking capacitors to charge to the quiescent voltage, minimizing the power-up transient.

4.6.2 Power-Down

To prevent transients at power-down, the device must first enter its power-down state by enabling $\overline{RST}$ or setting the PDN bit. When this occurs, audio output ceases and the internal output buffers are disconnected from AOUTL and AOUTR. In their place, a soft-start current sink is substituted which allows the DC-blocking capacitors to slowly discharge. Once this charge is dissipated, the power to the device may be turned off and the system is ready for the next power-on.

4.6.3 Discharge Time

To prevent an audio transient at the next power-on, it is necessary to ensure that the DC-blocking capacitors have fully discharged before turning on the power or exiting the power-down state. If not, a transient will occur when the audio outputs are initially clamped to AGND. The time that the device must remain in the power-down state is related to the value of the DC-blocking capacitance. For example, with a 3.3 µF capacitor, the minimum power-down time will be approximately 0.4 seconds.

4.7 Mute Control

The Mute Control pin goes high during power-up initialization, reset, muting (see section 6.2.1 and 6.5.1) or if the MCLK to LRCK ratio is incorrect. This pin is intended to be used as a control for an external mute circuit to prevent the clicks and pops that can occur in any single-ended single supply system.

Use of the Mute Control function is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the Mute Control function can enable the system designer to achieve idle channel noise/signal-to-noise ratios which are only limited by the external mute circuit. See the CDB4341 data sheet for a suggested mute circuit.

4.8 Grounding and Power Supply Arrangements

As with any high resolution converter, the CS4341 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 16 shows the recommended power arrangements, with VA connected to a clean supply. If the ground planes are split between digital ground and analog ground, REF_GND & AGND should be connected to the analog ground plane.

Decoupling capacitors should be as close to the DAC as possible, with the low value ceramic capacitor being the closest. To further minimize impedance, these capacitors should be located on the same layer as the DAC.

All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The FILT+ and VQ decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from FILT+ and REF_GND (as well as VQ and REF_GND), and should also be located on the same layer as the DAC. The CDB4341 evaluation board demonstrates the optimum layout and power supply arrangements.

4.9 Control Port Interface

The control port is used to load all the internal register settings (see section 6). The operation of the control port may be completely asynchronous with the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port operates in one of two modes: I²C or SPI.

Notes: MCLK must be applied during all I²C communication.

4.9.1 Rise Time for Control Port Clock

When excess capacitive loading is present on the I²C clock line, pin 6 (SCL/CCLK) may not have sufficient hysteresis to meet the standard I²C rise time specification. This prevents the use of common I²C configurations with a resistor pull-up. A workaround is achieved by placing a Schmitt Trigger buffer, a 74HC14 for example, on the SCL line just prior to the CS4341. This will not affect the operation of the I²C bus as pin 6 is an input only.

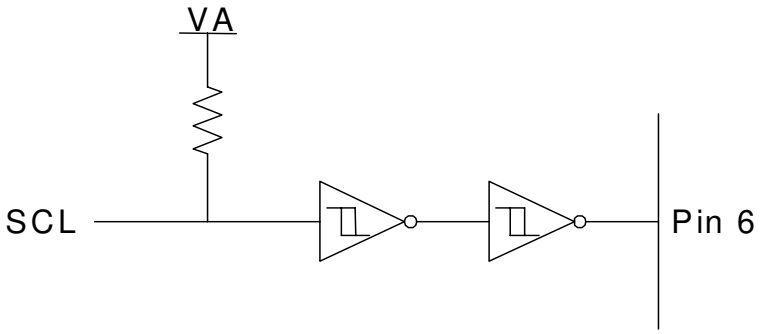


Figure 21. I²C Buffer Example

4.9.2 Memory Address Pointer (MAP)

The MAP byte precedes the control port register byte during a write operation and is not available again until after a start condition is initiated. During a read operation the byte transmitted after the ACK will contain the data of the register pointed to by the MAP (see section 4.9.3 for write/read details).

7	6	5	4	3	2	1	0
INCR	Reserved	Reserved	Reserved	MAP3	MAP2	MAP1	MAP0
0	0	0	0	0	0	0	0

4.9.2a INCR (Auto Map Increment)

The device has a MAP auto increment capability enabled by the INCR bit (the MSB) of the MAP. If INCR is set to 0, MAP will stay constant for successive I²C writes or reads and SPI writes. If INCR is set to 1, MAP will auto increment after each byte is written, allowing block reads or writes of successive registers.

Default = '0'
0 - Disabled
1 - Enabled

4.9.2b MAP0-3 (Memory Address Pointer)

Default = '0000'

4.9.3 I²C Mode

In the I²C Mode, data is clocked into and out of the bi-directional serial control data line, SDA, by the serial control port clock, SCL. There is no CS pin. Pin AD0 enables the user to alter the chip address (001000[AD0][R/W]) and should be tied to VA or AGND as required, before powering up the device. If the device ever detects a high to low transition on the AD0/CS pin after power-up, SPI mode will be selected.

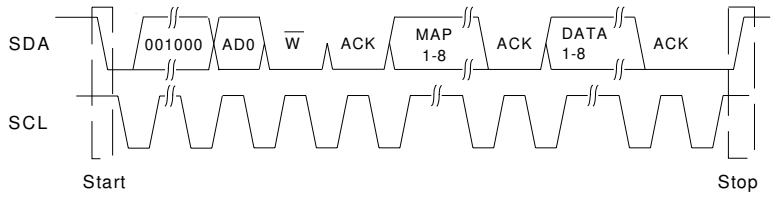


Figure 22. I²C Write

4.9.3a I²C Write

To write to the device, follow the procedure below while adhering to the control port Switching Specifications in section 6.

1) Initiate a START condition to the I²C bus followed by the address byte. The upper 6 bits must be 001000. The seventh bit must match the setting of the AD0 pin, and the eighth must be 0. The eighth bit of the address byte is the R/$\overline{W}$ bit.
2) Wait for an acknowledge (ACK) from the part, then write to the memory address pointer, MAP. This byte points to the register to be written.
3) Wait for an acknowledge (ACK) from the part, then write the desired data to the register pointed to by the MAP.
4) If the INCR bit (see section 4.9.2a) is set to 1, repeat the previous step until all the desired registers are written, then initiate a STOP condition to the bus.
5) If the INCR bit is set to 0 and further I²C writes to other registers are desired, it is necessary to repeat the procedure detailed from step 1. If no further writes to other registers are desired, initiate a STOP condition to the bus.

4.9.3b I²C Read

To read from the device, follow the procedure below while adhering to the control port Switching Specifications. During this operation it is first necessary to write to the device, specifying the appropriate register through the MAP.

1) After writing to the MAP (see section 4.9.3a), initiate a repeated START condition to the I²C bus followed by the address byte. The upper 6 bits must be 001000. The seventh bit must match the setting of the AD0 pin, and the eighth must be 1. The eighth bit of the address byte is the R/$\overline{W}$ bit.
2) Signal the end of the address byte by *not* issuing an acknowledge. The device will then transmit the contents of the register pointed to by the MAP. The MAP will contain the address of the last register written to the MAP.
3) If the INCR bit is set to 1, the device will continue to transmit the contents of successive registers. Continue providing a clock but do not issue an ACK on the bytes clocked out of the device. After all the desired registers are read, initiate a STOP condition to the bus.
4) If the INCR bit is set to 0 and further I²C reads from other registers are desired, it is necessary to repeat the procedure detailed from step 1. If no further reads from other registers are desired, initiate a STOP condition to the bus.

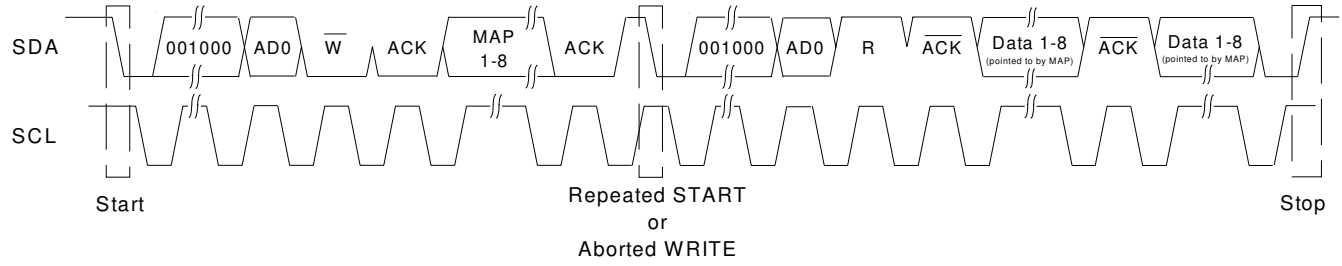


Figure 23. I²C Read

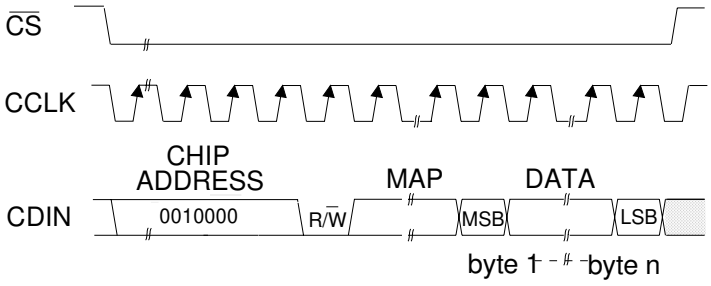
4.9.4 SPI Mode

In SPI mode, data is clocked into the serial control data line, CDIN, by the serial control port clock, CCLK (see Figure 24 for the clock to data relationship). There is no AD0 pin. Pin $\overline{CS}$ is the chip select signal and is used to control SPI writes to the control port. When the device detects a high to low transition on the AD0/$\overline{CS}$ pin after power-up, SPI mode will be selected. All signals are inputs and data is clocked in on the rising edge of CCLK.

4.9.4a SPI Write

To write to the device, follow the procedure below while adhering to the control port Switching Specifications in section 1.

1) Bring $\overline{CS}$ low.
2) The address byte on the CDIN pin must then be 00100000.
3) Write to the memory address pointer, MAP. This byte points to the register to be written.
4) Write the desired data to the register pointed to by the MAP.
5) If the INCR bit (see section 4.9.2a) is set to 1, repeat the previous step until all the desired registers are written, then bring $\overline{CS}$ high.
6) If the INCR bit is set to 0 and further SPI writes to other registers are desired, it is necessary to bring $\overline{CS}$ high, and repeat the procedure detailed from step 1. If no further writes to other registers are desired, bring $\overline{CS}$ high.



MAP = Memory Address Pointer

Figure 24. Control Port Timing, SPI Mode

5. REGISTER QUICK REFERENCE

Addr	Function	7	6	5	4	3	2	1	0
0h	MCLK Control	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MCLKDIV	Reserved
	DEFAULT	0	0	0	0	0	0	0	0
1h	Mode Control 2	AMUTE	DIF2	DIF1	DIF0	DEM1	DEM1	POR	PDN
	DEFAULT	1	0	0	0	0	0	1	1
2h	Transition and Mixing Control	A = B	SCZ1	SCZ0	ATAPI4	ATAPI3	ATAPI2	ATAPI1	ATAPI0
	DEFAULT	0	0	0	0	0	0	0	0
3h	Channel A Volume Control	MUTEA	VOLA6	VOLA5	VOLA4	VOLA3	VOLA2	VOLA1	VOLA0
	DEFAULT	0	0	0	0	0	0	0	0
4h	Channel B Volume Control	MUTEB	VOLB6	VOLB5	VOLB4	VOLB3	VOLB2	VOLB1	VOLB0
	DEFAULT	0	0	0	0	0	0	0	0

6. REGISTER DESCRIPTION

NOTE: All registers are read/write in I²C Mode and write only in SPI mode, unless otherwise stated.

6.1 MCLK CONTROL (ADDRESS 00H)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MCLKDIV	Reserved
0	0	0	0	0	0	0	0

6.1.1 MCLK DIVIDE-BY-2 (MCLKDIV) BIT 1

Default = 0

0 - Disabled

1 - Enabled

Function:

The MCLKDIV bit enables a circuit which divides the externally applied MCLK signal by 2.

6.2 MODE CONTROL (ADDRESS 01H)

7	6	5	4	3	2	1	0
AMUTE	DIF2	DIF1	DIF0	DEM1	DEM0	POR	PDN
1	0	0	0	0	0	1	1

6.2.1 AUTO-MUTE (AMUTE) BIT 7

Default = 1

0 - Disabled

1 - Enabled

Function:

The Digital-to-Analog converter output will mute following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-zero data will release the mute. Detection and muting is done independently for each channel. The quiescent voltage on the output will be retained and the Mute Control pin will go active during the mute period. The muting function is affected, similar to volume control changes, by the Soft and Zero Cross bits in the Transition and Mixing Control (address 02h) register.