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CS4341A

24-Bit, 192 kHz Stereo DAC with Volume Control

Features

- 101 dB Dynamic Range
- -91 dB THD+N
- +3.3 V or +5 V Power Supply
- 50 mW with 3.3 V supply
- Low Clock Jitter Sensitivity
- Filtered Line-level Outputs
- On-Chip Digital De-emphasis for 32, 44.1, and 48 kHz
- ATAPI Mixing
- Digital Volume Control with Soft Ramp
  - 94 dB Attenuation
  - 1 dB Step Size
  - Zero Crossing Click-Free Transitions
- Up to 200-kHz Sample Rates
- Automatic Mode Detection for Sample Rates between 4 and 200 kHz
- Pin Compatible with the CS4341

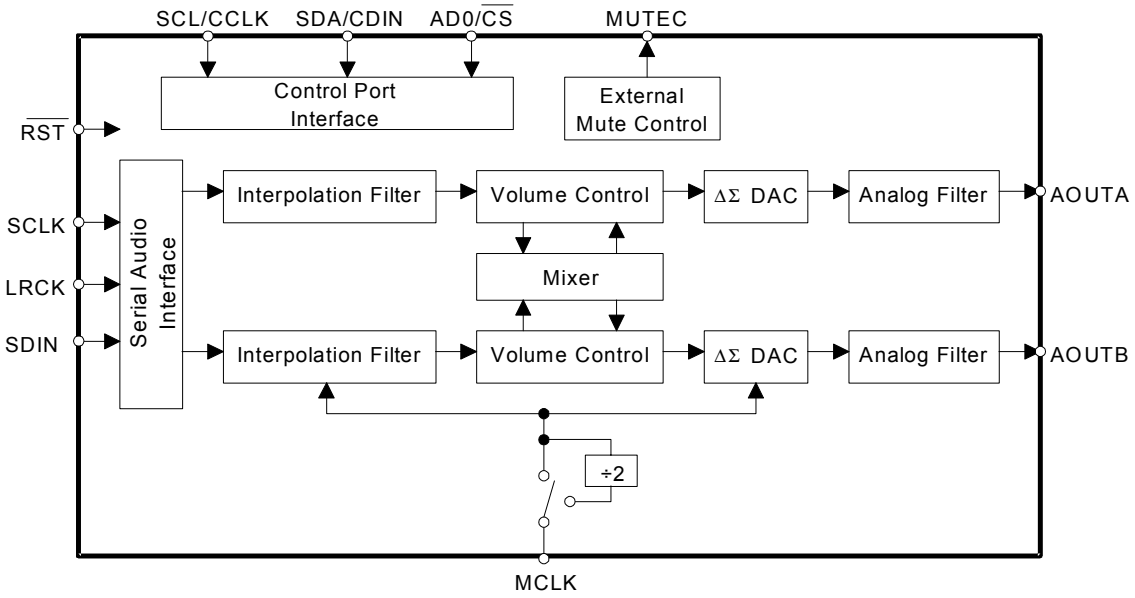
Description

The CS4341A is a complete stereo digital-to-analog system including digital interpolation, fourth-order delta-sigma digital-to-analog conversion, digital de-emphasis, volume control, channel mixing and analog filtering. The advantages of this architecture include: ideal differential linearity, no distortion mechanisms due to resistor matching errors, no linearity drift over time and temperature and a high tolerance to clock jitter.

The CS4341A accepts data at all standard audio sample rates up to 192 kHz, consumes very little power, operates over a wide power supply range and is pin compatible with the CS4341, as described in section 3.1. These features are ideal for DVD audio players.

ORDERING INFORMATION

CS4341A-KS	16-pin SOIC, -10 to 70 °C
CS4341A-KSZ, Lead Free	16-pin SOIC, -10 to 70 °C
CDB4341A	Evaluation Board



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Contacting Cirrus Logic Support

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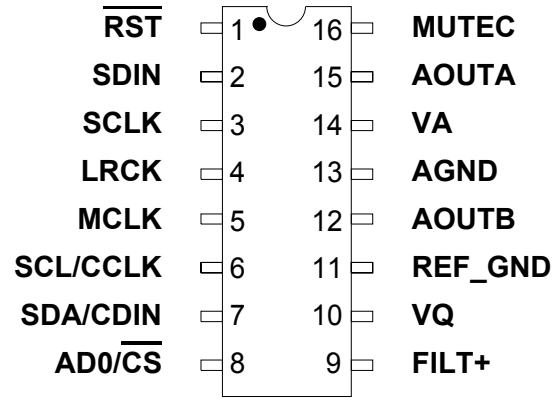
1. PIN DESCRIPTION



Pin Name	#	Pin Description
RST	1	**Reset** (*Input*) - Powers down device when enabled.
SDIN	2	**Serial Audio Data** (*Input*) - Input for two's complement serial audio data.
SCLK	3	**Serial Clock** (*Input*) -Serial clock for the serial audio interface.
LRCK	4	**Left Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	5	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
SCL/CCLK	6	**Serial Control Port Clock** (*Input*) - Serial clock for the control port interface.
SDA/CDIN	7	**Serial Control Data I/O** (*Input*/*Output*) - Input/Output for I^2C data. Input for SPI data.
AD0/CS	8	**Address Bit / Chip Select** (*Input*) - Chip address bit in I^2C Mode. Control signal used to select the chip in SPI mode.
FILT+	9	**Positive Voltage Reference** (*Output*) **-** Positive voltage reference for the internal sampling circuits.
VQ	10	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent reference voltage.
REF_GND	11	**Reference Ground** (*Input*) - Ground reference for the internal sampling circuits.
AOUTR **AOUTL**	12 15	**Analog Outputs** (*Output*) - The full scale analog output level is specified in the *Analog Characteristics* table.
AGND	13	**Analog Ground** (*Input*) - Ground reference.
VA	14	**Power** (*Input*) **-** Positive power for the analog, digital, control port interface, and serial audio interface sections.
MUTEC	16	**Mute Control** (*Output*) - Control signal for optional mute circuit.

2. TYPICAL CONNECTION DIAGRAM

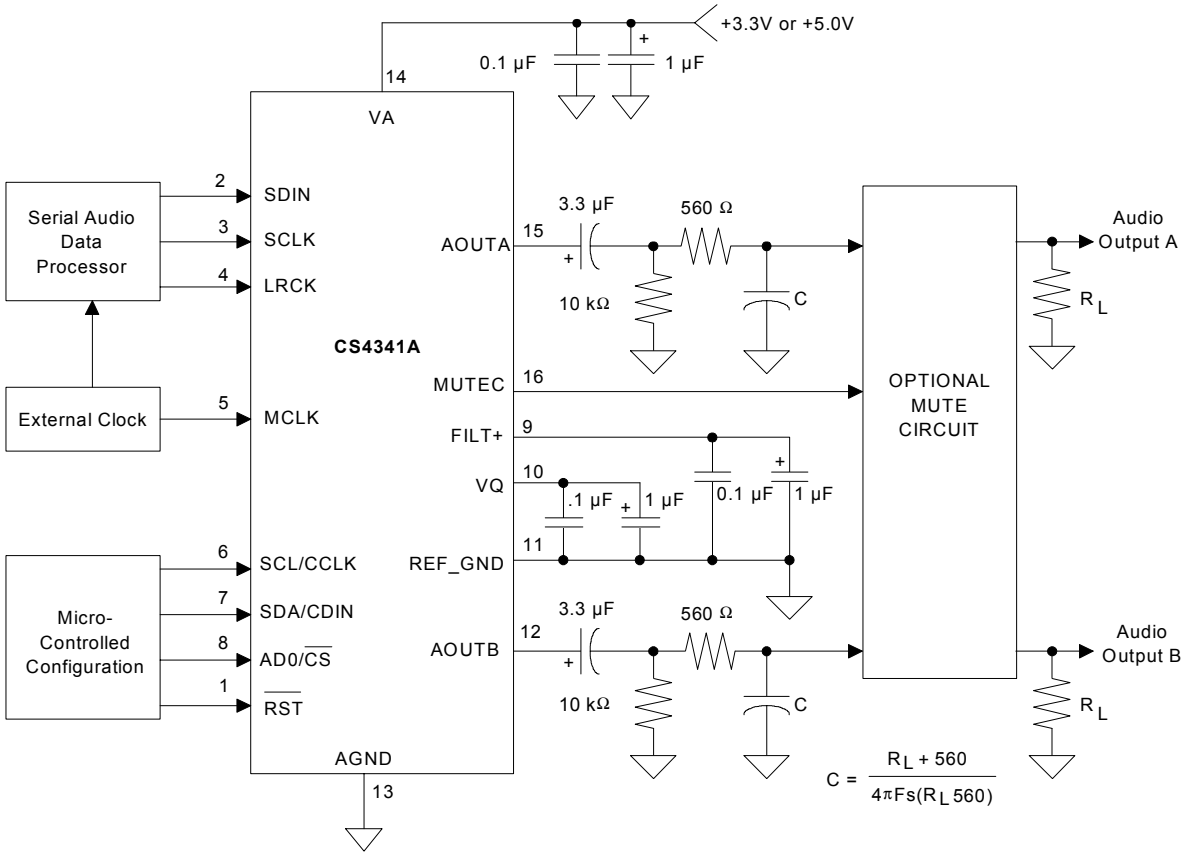


Figure 1. Typical Connection Diagram

3. APPLICATIONS

3.1 Upgrading from the CS4341 to the CS4341A

The CS4341A is pin and functionally compatible with all CS4341 designs, operating at the standard audio sample rates, that use pin 3 as a serial clock input. In addition to the features of the CS4341, the CS4341A supports standard sample rates up to 192 kHz, as well as automatic mode detection for sample rates between 4 and 200 kHz. The automatic speed mode detection feature allows sample rate changes between single, double and quad-speed modes without external intervention.

The CS4341A does not support an internal serial clock mode, sample rates between 50 kHz and 84 kHz (unless otherwise stated), or 2.7 V operation as does the CS4341.

3.2 Sample Rate Range/Operational Mode Detect

The device operates in one of three operational modes. The allowed sample rate range in each mode will depend on whether the Auto-Detect Defeat bit is enabled/disabled.

3.2.1 Auto-Detect Enabled

The Auto-Detect feature is enabled by default in the control port register 5.1. In this state, the CS4341A will auto-detect the correct mode when the input sample rate (F_S), defined by the LRCK frequency, falls within one of the ranges illustrated in Table 1. Sample rates outside the specified range for each mode are not supported.

Input Sample Rate (F_S)	MODE
4 kHz - 50 kHz	Single Speed Mode
84 kHz - 100 kHz	Double Speed Mode
170 kHz - 200 kHz	Quad Speed Mode

Table 1. CS4341A Auto-Detect

3.2.2 Auto-Detect Disabled

The Auto-Detect feature can be defeated via the control port register 5.1. In this state, the CS4341A will not auto-detect the correct mode based on the input sample rate (F_S). The operational mode must be set appropriately if F_S falls within one of the ranges illustrated in Table 2. Please refer to section 5.1.1 for implementation details. Sample rates outside the specified range for each mode are not supported.

MC1	MC0	Input Sample Rate (F_S)	MODE
0	0	4 kHz - 50 kHz	Single Speed Mode
0	1	50 kHz - 100 kHz	Double Speed Mode
1	0	100 kHz - 200 kHz	Quad Speed Mode

Table 2. CS4341A Mode Select

3.3 System Clocking

The device requires external generation of the master (MCLK), left/right (LRCK) and serial (SCLK) clocks. The LRCK, defined also as the input sample rate (F_S), must be synchronously derived from the MCLK according to specified ratios. The specified ratios of MCLK to LRCK for each Speed Mode, along with several standard audio sample rates and the required MCLK frequency, are illustrated in Tables 3-5.

Sample Rate (kHz)	MCLK (MHz)				
	256x	384x	512x	768x	1024x*
32	8.1920	12.2880	16.3840	24.5760	32.7680
44.1	11.2896	16.9344	22.5792	33.8688	45.1584
48	12.2880	18.4320	24.5760	36.8640	49.1520

Table 3. Single-Speed Mode Standard Frequencies

Sample Rate (kHz)	MCLK (MHz)				
	128x	192x	256x	384x	512x*
64	8.1920	12.2880	16.3840	24.5760	32.7680
88.2	11.2896	16.9344	22.5792	33.8688	45.1584
96	12.2880	18.4320	24.5760	36.8640	49.1520

Table 4. Double-Speed Mode Standard Frequencies

Sample Rate (kHz)	MCLK (MHz)		
	128x	192x	256x*
176.4	22.5792	33.8688	45.1584
192	24.5760	36.8640	49.1520

Table 5. Quad-Speed Mode Standard Frequencies

* Requires MCLKDIV bit = 1 in the Mode Control 1 register (address 00h).

3.4 Digital Interface Format

The device will accept audio samples in several digital interface formats. The desired format is selected via the DIF0, DIF1 and DIF2 bits in the Mode Control 2 register (see section 5.2.2) . For an illustration of the required relationship between LRCK, SCLK and SDIN, see Figures 2-4.

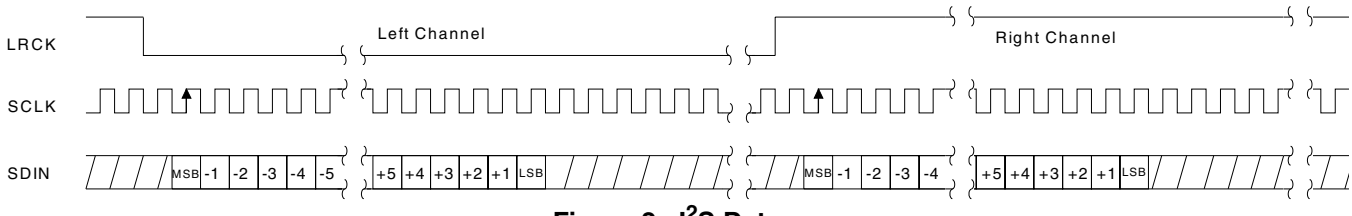


Figure 2. I^2S Data

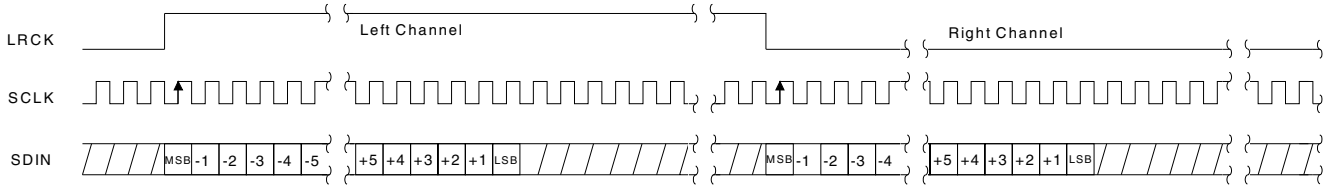


Figure 3. Left Justified up to 24-Bit Data

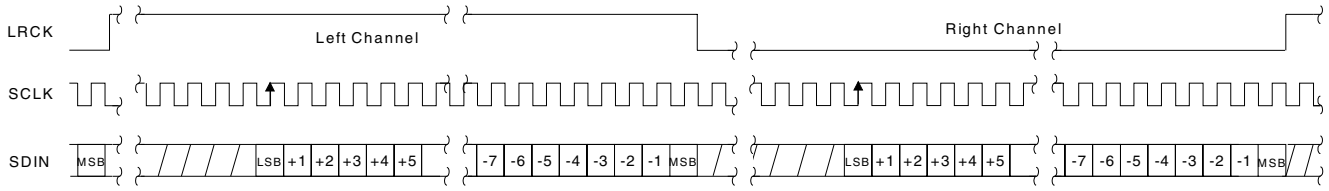


Figure 4. Right Justified Data

3.5 De-Emphasis Control

The device includes on-chip digital de-emphasis. The Mode Control 2 bits select either the 32, 44.1, or 48 kHz de-emphasis filter. Figure 5 shows the de-emphasis curve for F_s equal to 44.1 kHz. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, Fs. Please see section 5.2.3 for the desired de-emphasis control.

NOTE: De-emphasis is only available in Single-Speed Mode.

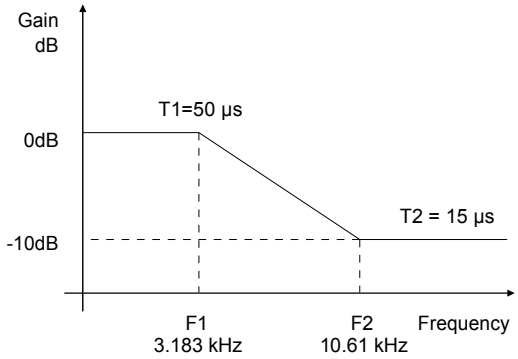


Figure 5. De-Emphasis Curve

3.6 Recommended Power-up Sequence

1. Hold $\overline{\text{RST}}$ low until the power supply is stable, and the master and left/right clocks are locked to the appropriate frequences, as discussed in section 3.3. In this state, the control port is reset to its default settings and VQ will remain low.

2. Bring $\overline{\text{RST}}$ high. The device will remain in a low power state with VQ low.

3. Load the desired register settings while keeping the PDN bit set to 1.

4. Set the PDN bit to 0. This will initiate the power-up sequence, which lasts approximately 50 µS when the POR bit is set to 0. If the POR bit is set to 1, see section 3.7 for a complete description of power-up timing.

3.7 Popguard® Transient Control

The CS4341A uses Popguard® technology to minimize the effects of output transients during power-up and power-down. This technology, when used with external DC-blocking capacitors in series with the audio outputs, minimizes the audio transients commonly produced by single-ended single-supply converters. It is activated inside the DAC when the PDN bit or the $\overline{\text{RST}}$ pin is enabled/disabled and requires no other external control, aside from choosing the appropriate DC-blocking capacitors.

3.7.1 Power-up

When the device is initially powered-up, the audio outputs, AOUTL and AOUTR, are clamped to AGND. Following a delay of approximately 1000 sample periods, each output begins to ramp toward the quiescent voltage. Approximately 10,000 LRCK cycles later, the outputs reach V_Q and audio output begins. This gradual voltage ramping allows time for the external DC-blocking capacitors to charge to the quiescent voltage, minimizing the power-up transient.

3.7.2 Power-down

To prevent transients at power-down, the device must first enter its power-down state by enabling $\overline{\text{RST}}$ or PDN. When this occurs, audio output ceases and the internal output buffers are disconnected from AOUTL and AOUTR. In their place, a soft-start current sink is substituted which allows the DC-blocking capacitors to slowly discharge. Once this charge is dissipated, the power to the device may be turned off and the system is ready for the next power-on.

3.7.3 Discharge Time

To prevent an audio transient at the next power-on, it is necessary to ensure that the DC-blocking capacitors have fully discharged before turning on the power or exiting the power-down state. If not, a transient will occur when the audio outputs are initially clamped to AGND. The time that the device must remain in the power-down state is related to the value of the DC-blocking capacitance. For example, with a 3.3 µF capacitor, the minimum power-down time will be approximately 0.4 seconds.

3.8 Grounding and Power Supply Arrangements

As with any high resolution converter, the CS4341A requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements, with VA connected to a clean supply. If the ground planes are split between digital ground and analog ground, REF_GND & AGND should be connected to the analog ground plane.

Decoupling capacitors should be as close to the DAC as possible, with the low value ceramic capacitor being the closest. To further minimze impedance, these capacitors should be located on the same layer as the DAC.

All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The FILT+ and VQ decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from FILT+ to REF_GND (and VQ to REF_GND), and should also be located on the same layer as the DAC. The CDB4341A evaluation board demonstrates the optimum layout and power supply arrangements.

3.9 Control Port Interface

The control port is used to load all the internal register settings (see section 5). The operation of the control port may be completely asynchronous with the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port operates in one of two modes: I^2C or SPI.

Notes: MCLK must be applied during all I^2C communication.

3.9.1 Rise Time for Control Port Clock

When excess capacitive loading is present on the I^2C clock line, pin 6 (SCL/CCLK) may not have sufficient hysteresis to meet the standard I^2C rise time specification. This prevents the use of common I^2C configurations with a resistor pull-up. A workaround is achieved by placing a Schmitt Trigger buffer, a 74HC14 for example, on the SCL line just prior to the CS4341A. This will not affect the operation of the I^2C bus as pin 6 is an input only.

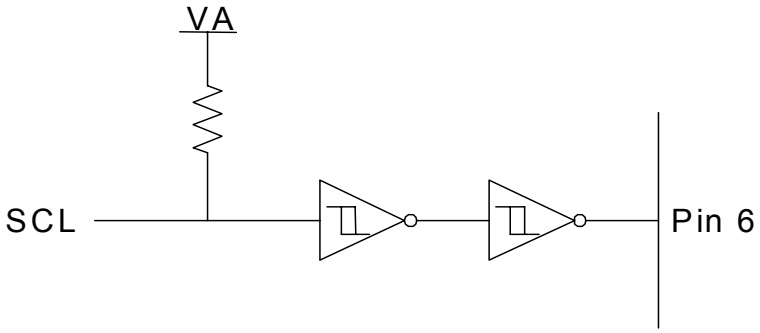


Figure 6. I^2C Buffer Example

3.9.2 MAP Auto Increment

The device has MAP (memory address pointer) auto increment capability enabled by the INCR bit (also the MSB) of the MAP. If INCR is set to 0, MAP will stay constant for successive I^2C writes or reads, and SPI writes. If INCR is set to 1, MAP will auto increment after each byte is written, allowing block reads or writes of successive registers.

3.9.3 I²C Mode

In the I²C mode, data is clocked into and out of the bi-directional serial control data line, SDA, by the serial control port clock, SCL (see Figure 7 for the clock to data relationship). There is no $\overline{CS}$ pin. Pin AD0 enables the user to alter the chip address (001000[AD0][R/$\overline{W}$]) and should be tied to VA or GND as required, before powering up the device. If the device ever detects a high to low transition on the AD0/$\overline{CS}$ pin after power-up, SPI mode will be selected.

3.9.3a I²C Write

To write to the device, follow the procedure below while adhering to the control port Switching Specifications in section 7.

1) Initiate a START condition to the I²C bus followed by the address byte. The upper 6 bits must be 001000. The seventh bit must match the setting of the AD0 pin, and the eighth must be 0. The eighth bit of the address byte is the R/$\overline{W}$ bit.

2) Wait for an acknowledge (ACK) from the part, then write to the memory address pointer, MAP. This byte points to the register to be written.

3) Wait for an acknowledge (ACK) from the part, then write the desired data to the register pointed to by the MAP.

4) If the INCR bit (see section 3.9.2) is set to 1, repeat the previous step until all the desired registers are written, then initiate a STOP condition to the bus.

5) If the INCR bit is set to 0 and further I²C writes to other registers are desired, it is necessary to initiate a repeated START condition and follow the procedure detailed from step 1. If no further writes to other registers are desired, initiate a STOP condition to the bus.

3.9.3b I²C Read

To read from the device, follow the procedure below while adhering to the control port *Switching Specifications*.

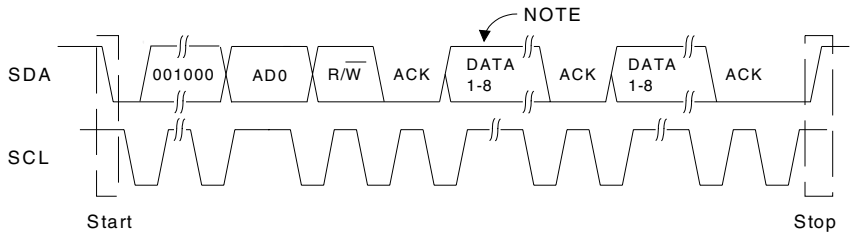
1) Initiate a START condition to the I²C bus followed by the address byte. The upper 6 bits must be 001000. The seventh bit must match the setting of the AD0 pin, and the eighth must be 1. The eighth bit of the address byte is the R/$\overline{W}$ bit.

2) After transmitting an acknowledge (ACK), the device will then transmit the contents of the register pointed to by the MAP. The MAP register will contain the address of the last register written to the MAP, or the default address (see section 3.9.2) if an I²C read is the first operation performed on the device.

3) Once the device has transmitted the contents of the register pointed to by the MAP, issue an ACK.

4) If the INCR bit is set to 1, the device will continue to transmit the contents of successive registers. Continue providing a clock and issue an ACK after each byte until all the desired registers are read, then initiate a STOP condition to the bus.

5) If the INCR bit is set to 0 and further I²C reads from other registers are desired, it is necessary to initiate a repeated START condition and follow the procedure detailed from step 1. If no further reads from other registers are desired, initiate a STOP condition to the bus.



NOTE: If operation is a write, this byte contains the Memory Address Pointer, MAP. If operation is a read, this byte contains the data of the register pointed to by the MAP.

Figure 7. Control Port Timing, I²C Mode

3.9.4 SPI Mode

In SPI mode, data is clocked into the serial control data line, CDIN, by the serial control port clock, CCLK (see Figure 7 for the clock to data relationship). There is no AD0 pin. Pin $\overline{CS}$ is the chip select signal and is used to control SPI writes to the control port. When the device detects a high to low transition on the AD0/$\overline{CS}$ pin after power-up, SPI mode will be selected. All signals are inputs and data is clocked in on the rising edge of CCLK.

3.9.4a SPI Write

To write to the device, follow the procedure below while adhering to the control port Switching Specifications in section 6.

1) Bring $\overline{CS}$ low.

2) The address byte on the CDIN pin must then be 00100000.

3) Write to the memory address pointer, MAP. This byte points to the register to be written.

4) Write the desired data to the register pointed to by the MAP.

5) If the INCR bit (see section 3.9.2) is set to 1, repeat the previous step until all the desired registers are written, then bring $\overline{CS}$ high.

6) If the INCR bit is set to 0 and further SPI writes to other registers are desired, it is necessary to bring $\overline{CS}$ high, and follow the procedure detailed from step 1. If no further writes to other registers are desired, bring $\overline{CS}$ high.

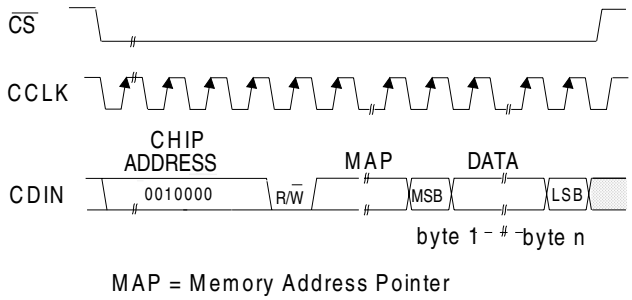


Figure 7. Control Port Timing, SPI mode

3.10 Memory Address Pointer (MAP)

7	6	5	4	3	2	1	0
INCR	Reserved	Reserved	Reserved	Reserved	MAP2	MAP1	MAP0
0	0	0	0	0	0	0	0

3.10.1 INCR (AUTO MAP INCREMENT ENABLE)

Default = '0'

0 - Disabled

1 - Enabled

3.10.2 MAP (MEMORY ADDRESS POINTER)

Default = '000'

4. REGISTER QUICK REFERENCE

Addr	Function	7	6	5	4	3	2	1	0
0h	Mode Control 1	Reserved	MC1	MC0	Reserved	Reserved	AUTOD	MCLKDIV	Reserved
	DEFAULT	0	0	0	0	0	0	0	0
1h	Mode Control 2	AMUTE	DIF2	DIF1	DIF0	DEM1	DEM0	POR	PDN
	DEFAULT	1	0	0	0	0	0	1	1
2h	Transition and Mixing Control	A = B	SOFT	ZERO CROSS	ATAPI4	ATAPI3	ATAPI2	ATAPI1	ATAPI0
	DEFAULT	0	0	0	0	0	0	0	0
3h	Channel A Volume Control	MUTEA	VOLA6	VOLA5	VOLA4	VOLA3	VOLA2	VOLA1	VOLA0
	DEFAULT	0	0	0	0	0	0	0	0
4h	Channel B Volume Control	MUTEB	VOLB6	VOLB5	VOLB4	VOLB3	VOLB2	VOLB1	VOLB0
	DEFAULT	0	0	0	0	0	0	0	0

5. REGISTER DESCRIPTION

NOTE: All registers are read/write in I^2C mode and write only in SPI mode, unless otherwise stated.

5.1 MODE CONTROL 1 (ADDRESS 00H)

7	6	5	4	3	2	1	0
Reserved	MC1	MC0	Reserved	Reserved	AUTOD	MCLKDIV	Reserved
0	0	0	0	0	0	0	0

5.1.1 SPEED MODE CONTROL (MC) BIT 5-6

Default = 00
00 - Single-Speed Mode
01 - Double-Speed Mode
10 - Quad-Speed Mode

The operational speed mode must be set if the auto-detect defeat bit is enabled (AUTOD = 1). These bits are ignored if the auto-detect defeat is disabled (AUTOD = 0).

5.1.2 AUTO-DETECT DEFEAT (AUTOD) BIT 2

Default = 0
0 - Disabled
1 - Enabled

The Auto-Detect function can be defeated to allow sample rate changes from 50 to 84 kHz, and from 100 to 170 kHz. The operational speed mode must be set via the speed mode control bits (see section 5.1.1) if the auto-detect feature is defeated.

5.1.3 MCLK DIVIDE-BY-2 (MCLKDIV) BIT 1

Default = 0
0 - Disabled
1 - Enabled

Function:

The MCLKDIV bit enables a circuit which divides the externally applied MCLK signal by 2.

5.2 MODE CONTROL 2 (ADDRESS 01H)

7	6	5	4	3	2	1	0
AMUTE	DIF2	DIF1	DIF0	DEM1	DEM0	POR	PDN
1	0	0	0	0	0	1	1

5.2.1 AUTO-MUTE (AMUTE) BIT 7

Default = 1
0 - Disabled
1 - Enabled

Function:

The Digital-to-Analog converter output will mute following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-zero data will release the mute. Detection and muting is done independently for each channel. The quiescent voltage on the output will be retained and the Mute Control pin will go active during the mute period. The muting function is affected, similiar to volume control changes, by the Soft and Zero Cross bits in the Transition and Mixing Control (address 02h) register.

5.2.2 DIGITAL INTERFACE FORMAT (DIF) BIT 4-6

Default = 000 - Format 0 (I^2S, up to 24-bit data)

Function:

The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in Figures 2-4.

DIF2	DIF1	DIF0	DESCRIPTION	Format	FIGURE
0	0	0	I^2S, up to 24-bit data	1	2
0	0	1	Identical to Format 1	1	2
0	1	0	Left Justified, up to 24-bit data,	2	3
0	1	1	Right Justified, 24-bit data	3	4
1	0	0	Right Justified, 20-bit data	4	4
1	0	1	Right Justified, 16-bit data	5	4
1	1	0	Right Justified, 18-bit data	6	4
1	1	1	Identical to Format 1	1	2

Table 6. Digital Interface Format

5.2.3 DE-EMPHASIS CONTROL (DEM[1:0]) BIT 2-3

Default = 00
00 - Disabled
01 - 44.1 kHz
10 - 48 kHz
11 - 32 kHz

Function:

Implementation of the standard 15µs/50µs digital de-emphasis filter response, Figure 5, requires reconfiguration of the digital filter to maintain the proper filter response for 32, 44.1 or 48 kHz sample rates.

NOTE: De-emphasis is only available in Single-Speed Mode.

5.2.4 POPGUARD® TRANSIENT CONTROL (POR) BIT 1

Default = 1
0 - Disabled
1 - Enabled

Function:

The PopGuard® Transient Control allows the quiescent voltage to slowly ramp to and from 0 volts to the quiescent voltage during power-on or power-down. Please refer to section 3.7 for implementation details.

5.2.5 POWER DOWN (PDN) BIT 0

Default = 1
0 - Disabled
1 - Enabled

Function:

The device will enter a low-power state when this function is enabled. The power-down bit defaults to 'enabled' on power-up and must be disabled before normal operation can occur. The contents of the control registers are retained in this mode.

5.3 TRANSITION AND MIXING CONTROL (ADDRESS 02H)

7	6	5	4	3	2	1	0
A = B	SZC1	SZC0	ATAPI4	ATAPI3	ATAPI2	ATAPI1	ATAPI0
0	1	0	0	1	0	0	1

5.3.1 CHANNEL A VOLUME = CHANNEL B VOLUME (A = B) BIT 7

Default = 0
0 - Disabled
1 - Enabled

Fucntion:

The AOUTA and AOUTB volume levels are independently controlled by the A and the B Channel Volume Control Bytes when this function is disabled. The volume on both AOUTA and AOUTB are determined by the A Channel Volume Control Byte and the B Channel Byte is ignored when this function is enabled.

5.3.2 SOFT RAMP AND ZERO CROSS CONTROL (SZC) BIT 5-6

Default = 10
00 - Immediate Changes
01 - Changes On Zero Crossings
10 - Soft Ramped Changes
11 - Soft Ramped Changes On Zero Crossings

Fucntion:

Immediate Changes

When *Immediate Changes* is selected all level changes will take effect immediately in one step.

Changes On Zero Crossings

Changes on Zero Crossings dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independenttly monitored and implemented for each channel.

Soft Ramped Changes

Soft Ramped Changes allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1dB per 8 left/right clock periods.

Soft Ramped Changes on Zero Crossings

Soft Ramped Changes On Zero Crossings dictates that signal level changes, either by attenuation changes or muting, will occur in 1/8 dB steps implemented on a signal zero crossing. The 1/8 dB level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is indepently monitored and implemented for each channel.

5.3.3 ATAPI CHANNEL MIXING AND MUTING (ATAPI) BIT 0-4

Default = 01001 - AOUTA = Left Channel, AOUTB = Right Channel (Stereo)

Fucntion:

The CS4341A implements the channel mixing functions of the ATAPI CD-ROM specification. Refer to Table 7 and Figure 8 for additional information.

ATAPI4	ATAPI3	ATAPI2	ATAPI1	ATAPI0	AOUTA	AOUTB
0	0	0	0	0	MUTE	MUTE
0	0	0	0	1	MUTE	bR
0	0	0	1	0	MUTE	bL
0	0	0	1	1	MUTE	b[(L+R)/2]
0	0	1	0	0	aR	MUTE
0	0	1	0	1	aR	bR
0	0	1	1	0	aR	bL
0	0	1	1	1	aR	b[(L+R)/2]
0	1	0	0	0	aL	MUTE
0	1	0	0	1	aL	bR

Table 7. ATAPI Decode

ATAPI4	ATAPI3	ATAPI2	ATAPI1	ATAPI0	AOUTA	AOUTB
0	1	0	1	0	aL	bL
0	1	0	1	1	aL	b[(L+R)/2]
0	1	1	0	0	a[(L+R)/2]	MUTE
0	1	1	0	1	a[(L+R)/2]	bR
0	1	1	1	0	a[(L+R)/2]	bL
0	1	1	1	1	a[(L+R)/2]	b[(L+R)/2]
1	0	0	0	0	MUTE	MUTE
1	0	0	0	1	MUTE	bR
1	0	0	1	0	MUTE	bL
1	0	0	1	1	MUTE	[(aL+bR)/2]
1	0	1	0	0	aR	MUTE
1	0	1	0	1	aR	bR
1	0	1	1	0	aR	bL
1	0	1	1	1	aR	[(bL+aR)/2]
1	1	0	0	0	aL	MUTE
1	1	0	0	1	aL	bR
1	1	0	1	0	aL	bL
1	1	0	1	1	aL	[(aL+bR)/2]
1	1	1	0	0	[(aL+bR)/2]	MUTE
1	1	1	0	1	[(aL+bR)/2]	bR
1	1	1	1	0	[(bL+aR)/2]	bL
1	1	1	1	1	[(aL+bR)/2]	[(aL+bR)/2]

Table 7. ATAPI Decode (Continued)

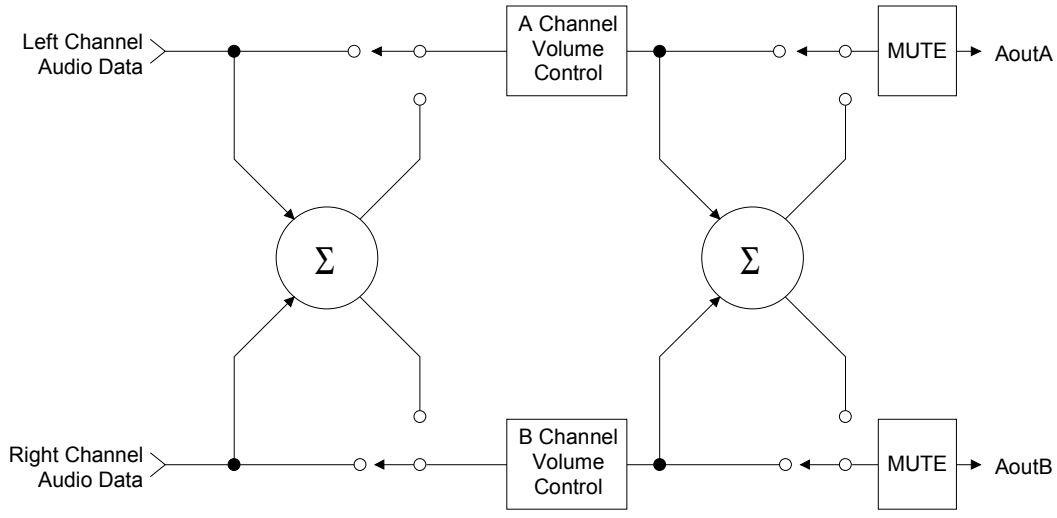


Figure 8. ATAPI Block Diagram

5.4 CHANNEL A VOLUME CONTROL (ADDRESS 03H)

5.5 CHANNEL B VOLUME CONTROL (ADDRESS 04H)

7	6	5	4	3	2	1	0
MUTEx	VOLx6	VOLx5	VOLx4	VOLx3	VOLx2	VOLx1	VOLx0
0	0	0	0	0	0	0	0

5.5.1 MUTE (MUTE) BIT 7

Default = 0
0 - Disabled
1 - Enabled

Fucntion:

The Digital-to-Analog converter output will mute when enabled. The quiescent voltage on the output will be retained. The muting function is affected, similiar to attenuation changes, by the Soft and Zero Cross bits in the Transition and Mixing Control (address 02h) register. The MUTEC will go active during the mute period if the Mute function is enabled for both channels.

5.5.2 VOLUME (VOLx) BIT 0-6

Default = 0 dB (No Attenuation)

Function:

The digital volume control allows the user to attenuate the signal in 1 dB increments from 0 to -90 dB. Volume settings are decoded as shown in Table 8. The volume changes are implemented as dictated by the Soft and Zero Cross bits in the Transition and Mixing Control (address 02h) register. All volume settings less than - 94 dB are equivalent to enabling the Mute bit.

Binary Code	Decimal Value	Volume Setting
0000000	0	0 dB
0010100	20	-20 dB
0101000	40	-40 dB
0111100	60	-60 dB
1011010	90	-90 dB

Table 8. Example Digital Volume Settings

6. CHARACTERISTICS AND SPECIFICATIONS

(Min/Max performance characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics are derived from measurements taken at T_A = 25°C.)

SPECIFIED OPERATING CONDITIONS

Parameters	Symbol	Min	Typ	Max	Units
DC Power Supply					
Analog	VA	3.0 4.5	3.3 5	3.6 5.5	V V
Ambient Operating Temperature (Power Applied)	T_A	-10	-	+70	°C

ABSOLUTE MAXIMUM RATINGS (AGND = 0 V; all voltages with respect to AGND. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.)

Parameters	Symbol	Min	Max	Units
DC Power Supply	VA	-0.3	6.0	V
Input Current (Note 1)	I_{in}	-	±10	mA
Digital Input Voltage	V_{IND}	-0.3	VA+0.4	V
Ambient Operating Temperature (power applied)	T_A	-55	125	°C
Storage Temperature	T_{stg}	-65	150	°C

Notes: 1. Any pin except supplies.

ANALOG CHARACTERISTICS (CS4341A-KS) (Test conditions (unless otherwise specified): Input test signal is a 997 Hz sine wave at 0 dBFS; measurement bandwidth is 10 Hz to 20 kHz; test load R_L = 10 kΩ, C_L = 10 pF (see Figure 9))

Parameter		VA = 5.0 V			VA = 3.3 V			Unit
		Min	Typ	Max	Min	Typ	Max	
Single-Speed Mode	**Fs = 48 kHz**							
Dynamic Range	(Note 2)							
18 to 24-Bit	unweighted	92	98	-	88	94	-	dB
	A-Weighted	95	101	-	91	97	-	dB
16-Bit	unweighted	-	92	-	-	92	-	dB
	A-Weighted	-	95	-	-	95	-	dB
Total Harmonic Distortion + Noise	(Note 2)							
18 to 24-Bit	0 dB	-	-91	-85	-	-94	-88	dB
	-20 dB	-	-78	-	-	-74	-	dB
	-60 dB	-	-38	-	-	-34	-	dB
16-Bit	0 dB	-	-90	-	-	-91	-	dB
	-20 dB	-	-72	-	-	-72	-	dB
	-60 dB	-	-32	-	-	-32	-	dB
Double-Speed Mode	**Fs = 96 kHz**							
Dynamic Range	(Note 2)							
18 to 24-Bit	unweighted	92	98	-	88	94	-	dB
	A-Weighted	95	101	-	91	97	-	dB
16-Bit	unweighted	-	92	-	-	92	-	dB
	A-Weighted	-	95	-	-	95	-	dB
Total Harmonic Distortion + Noise	(Note 2)							
18 to 24-Bit	0 dB	-	-91	-85	-	-94	-88	dB
	-20 dB	-	-78	-	-	-74	-	dB
	-60 dB	-	-38	-	-	-34	-	dB
16-Bit	0 dB	-	-90	-	-	-91	-	dB
	-20 dB	-	-72	-	-	-72	-	dB
	-60 dB	-	-32	-	-	-32	-	dB
Quad-Speed Mode	**Fs = 192 kHz**							
Dynamic Range	(Note 2)							
18 to 24-Bit	unweighted	92	98	-	88	94	-	dB
	A-Weighted	95	101	-	91	97	-	dB
16-Bit	unweighted	-	92	-	-	92	-	dB
	A-Weighted	-	95	-	-	95	-	dB
Total Harmonic Distortion + Noise	(Note 2)							
18 to 24-Bit	0 dB	-	-91	-85	-	-94	-88	dB
	-20 dB	-	-78	-	-	-74	-	dB
	-60 dB	-	-38	-	-	-34	-	dB
16-Bit	0 dB	-	-90	-	-	-91	-	dB
	-20 dB	-	-72	-	-	-72	-	dB
	-60 dB	-	-32	-	-	-32	-	dB

ANALOG CHARACTERISTICS (CS4341A-KS) (Continued)

Parameters	Symbol	Min	Typ	Max	Units
Dynamic Performance for All Modes					
Interchannel Isolation (1 kHz)		-	102	-	dB
DC Accuracy					
Interchannel Gain Mismatch		-	0.1	-	dB
Gain Drift		-	±100	-	ppm/°C
Analog Output Characteristics and Specifications					
Full Scale Output Voltage		0.6•VA	0.7•VA	0.8•VA	Vpp
Output Impedance		-	100	-	Ω
Minimum AC-Load Resistance (Note 3)	R_L	-	3	-	kΩ
Maximum Load Capacitance (Note 3)	C_L	-	100	-	pF

Notes: 2. One-half LSB of triangular PDF dither is added to data.

3. Refer to Figure 10.

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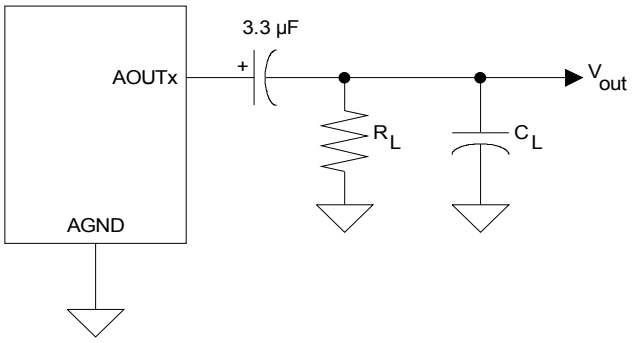

Figure 9. Output Test Load

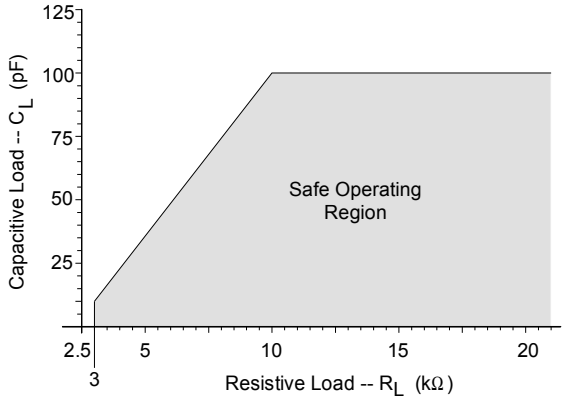

Figure 10. Maximum Loading