



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



## 192 kHz Stereo DAC with 2 Vrms Line Out

### Features

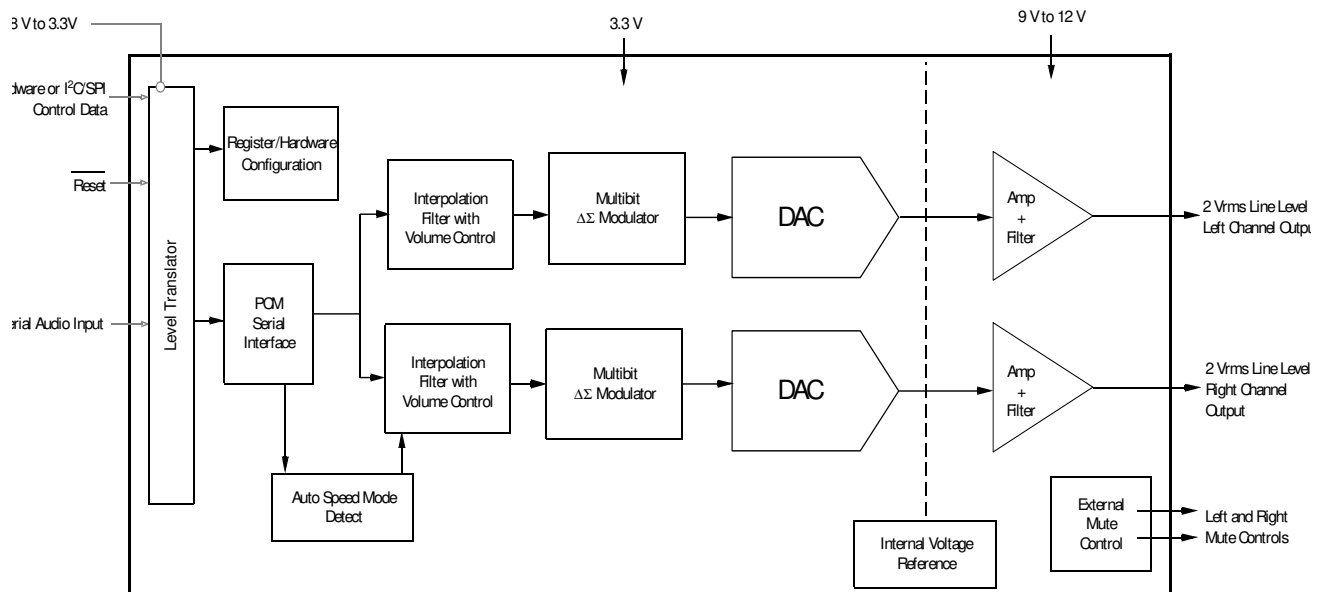
- ◆ Multi-Bit Delta-Sigma Modulator
- ◆ 24-Bit Conversion
- ◆ Up to 192 kHz Sample Rates
- ◆ 112 dB Dynamic Range
- ◆ -100 dB THD+N
- ◆ +3.3 V, +9 to 12 V, and VL Power Supplies
- ◆ 2 Vrms Output into 5 kΩ AC Load
- ◆ Digital Volume Control with Soft Ramp
  - 119 dB Attenuation
  - 1/2 dB Step Size
  - Zero Crossing Click-Free Transitions
- ◆ ATAPI Mixing
- ◆ Low Clock Jitter Sensitivity
- ◆ Popguard® Technology for Control of Clicks and Pops

### Description

The CS4351 is a complete stereo digital-to-analog system including digital interpolation, fifth-order multi-bit delta-sigma digital-to-analog conversion, digital de-emphasis, volume control, channel mixing, analog filtering, and on-chip 2 Vrms line-level driver. The advantages of this architecture include ideal differential linearity, no distortion mechanisms due to resistor matching errors, no linearity drift over time and temperature, high tolerance to clock jitter, and a minimal set of external components.

The CS4351 is available in a 20-pin TSSOP package in both Commercial (-10°C - +70°C) and Automotive grades (-40°C to +85°C). The CDB4351 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please see [“Ordering Information” on page 37](#) for complete details.

These features are ideal for cost-sensitive, 2-channel audio systems including DVD players, A/V receivers, set-top boxes, digital TVs and VCRs, mini-component systems, and mixing consoles.



---

**TABLE OF CONTENTS**

<b>1. PIN DESCRIPTION .....</b>	<b>5</b>
<b>2. CHARACTERISTICS AND SPECIFICATIONS .....</b>	<b>6</b>
SPECIFIED OPERATING CONDITIONS .....	6
ABSOLUTE MAXIMUM RATINGS .....	6
DAC ANALOG CHARACTERISTICS .....	7
COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE .....	8
COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE .....	9
SWITCHING SPECIFICATIONS - SERIAL AUDIO INTERFACE .....	10
SWITCHING CHARACTERISTICS - CONTROL PORT - I <sup>2</sup> C <sup>®</sup> FORMAT .....	11
SWITCHING CHARACTERISTICS - CONTROL PORT - SPI <sup>™</sup> FORMAT .....	12
DIGITAL CHARACTERISTICS .....	13
POWER AND THERMAL CHARACTERISTICS .....	13
<b>3. TYPICAL CONNECTION DIAGRAM .....</b>	<b>14</b>
<b>4. APPLICATIONS .....</b>	<b>15</b>
4.1 Sample Rate Range/Operational Mode Detect .....	15
4.1.1 Auto-Detect Enabled .....	15
4.1.2 Auto-Detect Disabled .....	15
4.2 System Clocking .....	15
4.3 Digital Interface Format .....	16
4.3.1 Stand-Alone Mode .....	16
4.3.2 Control Port Mode .....	16
4.4 De-Emphasis Control .....	17
4.4.1 Stand-Alone Mode .....	18
4.4.2 Control Port Mode .....	18
4.5 Recommended Power-Up Sequence .....	18
4.5.1 Stand-Alone Mode .....	18
4.5.2 Control Port Mode .....	18
4.6 Popguard <sup>®</sup> Transient Control .....	18
4.6.1 Power-Up .....	18
4.6.2 Power-Down .....	19
4.6.3 Discharge Time .....	19
4.7 Mute Control .....	19
4.8 Grounding and Power Supply Arrangements .....	19
4.8.1 Capacitor Placement .....	19
4.9 Control Port Interface .....	20
4.9.1 MAP Auto Increment .....	20
4.9.2 I <sup>2</sup> C Mode .....	20
4.9.3 SPI Mode .....	21
4.10 Memory Address Pointer (MAP) .....	22
4.10.1 INCR (Auto Map Increment Enable) .....	22
4.10.2 MAP (Memory Address Pointer) .....	22
<b>5. REGISTER QUICK REFERENCE .....</b>	<b>23</b>
<b>6. REGISTER DESCRIPTION .....</b>	<b>24</b>
6.1 Chip ID - Register 01h .....	24
6.2 Mode Control 1 - Register 02h .....	24
6.2.1 Digital Interface Format (DIF2:0) Bits 6-4 .....	24
6.2.2 De-Emphasis Control (DEM1:0) Bits 3-2 .....	24
6.2.3 Functional Mode (FM) Bits 1-0 .....	25
6.3 Volume Mixing and Inversion Control - Register 03h .....	25
6.3.1 Channel A Volume = Channel B Volume (VOLB=A) Bit 7 .....	25
6.3.2 Invert Signal Polarity (Invert_A) Bit 6 .....	25
6.3.3 Invert Signal Polarity (Invert_B) Bit 5 .....	25



6.3.4 ATAPI Channel Mixing and Muting (ATAPI3:0) Bits 3-0 .....	26
6.4 Mute Control - Register 04h .....	27
6.4.1 Auto-Mute (AMUTE) Bit 7 .....	27
6.4.2 AMUTE <sub>C</sub> = BMUTE <sub>C</sub> (MUTE <sub>C</sub> A=B) Bit 5 .....	27
6.4.3 A Channel Mute (MUTE_A) Bit 4 B Channel Mute (MUTE_B) Bit 3 .....	27
6.5 Channel A Volume Control - Register 05h Channel B Volume Control - Register 06h .....	27
6.5.1 Digital Volume Control (VOL7:0) Bits 7-0 .....	28
6.6 Ramp and Filter Control - Register 07h .....	28
6.6.1 Soft Ramp and Zero Cross Control (SZC1:0) Bits 7-6 .....	28
6.6.2 Soft Volume Ramp-Up After Error (RMP_UP) Bit 5 .....	29
6.6.3 Soft Ramp-Down Before Filter Mode Change (RMP_DN) Bit 4 .....	29
6.6.4 Interpolation Filter Select (FILT_SEL) Bit 2 .....	29
6.7 Misc Control - Register 08h .....	29
6.7.1 Power Down (PDN) Bit 7 .....	30
6.7.2 Control Port Enable (CPEN) Bit 6 .....	30
6.7.3 Freeze Controls (Freeze) Bit 5 .....	30
<b>7. DIGITAL FILTER RESPONSE PLOTS .....</b>	<b>31</b>
<b>8. PARAMETER DEFINITIONS .....</b>	<b>35</b>
<b>9. PACKAGE DIMENSIONS .....</b>	<b>36</b>
<b>10. ORDERING INFORMATION .....</b>	<b>37</b>
<b>11. REVISION HISTORY .....</b>	<b>37</b>

## LIST OF FIGURES

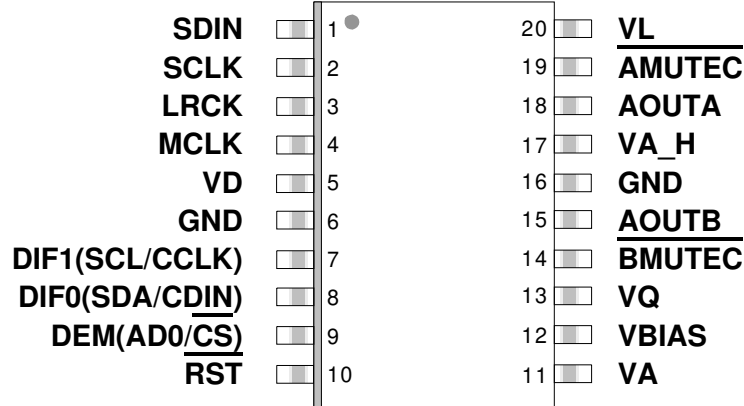
Figure 1. Serial Input Timing .....	10
Figure 2. Control Port Timing - I <sup>2</sup> C Format .....	11
Figure 3. Control Port Timing - SPI Format (Write) .....	12
Figure 4. Typical Connection Diagram .....	14
Figure 5. Left-Justified up to 24-Bit Data .....	17
Figure 6. I <sup>2</sup> S, up to 24-Bit Data .....	17
Figure 7. Right-Justified Data .....	17
Figure 8. De-Emphasis Curve .....	17
Figure 9. Control Port Timing, I <sup>2</sup> C Mode .....	21
Figure 10. Control Port Timing, SPI mode .....	22
Figure 11. De-Emphasis Curve .....	24
Figure 12. ATAPI Block Diagram .....	26
Figure 13. Single-Speed (fast) Stopband Rejection .....	31
Figure 14. Single-Speed (fast) Transition Band .....	31
Figure 15. Single-Speed (fast) Transition Band (detail) .....	31
Figure 16. Single-Speed (fast) Passband Ripple .....	31
Figure 17. Single-Speed (slow) Stopband Rejection .....	31
Figure 18. Single-Speed (slow) Transition Band .....	31
Figure 19. Single-Speed (slow) Transition Band (detail) .....	32
Figure 20. Single-Speed (slow) Passband Ripple .....	32
Figure 21. Double-Speed (fast) Stopband Rejection .....	32
Figure 22. Double-Speed (fast) Transition Band .....	32
Figure 23. Double-Speed (fast) Transition Band (detail) .....	32
Figure 24. Double-Speed (fast) Passband Ripple .....	32
Figure 25. Double-Speed (slow) Stopband Rejection .....	33
Figure 26. Double-Speed (slow) Transition Band .....	33
Figure 27. Double-Speed (slow) Transition Band (detail) .....	33
Figure 28. Double-Speed (slow) Passband Ripple .....	33

Figure 29. Quad-Speed (fast) Stopband Rejection .....	33
Figure 30. Quad-Speed (fast) Transition Band .....	33
Figure 31. Quad-Speed (fast) Transition Band (detail) .....	34
Figure 32. Quad-Speed (fast) Passband Ripple .....	34
Figure 33. Quad-Speed (slow) Stopband Rejection.....	34
Figure 34. Quad-Speed (slow) Transition Band.....	34
Figure 35. Quad-Speed (slow) Transition Band (detail).....	34
Figure 36. Quad-Speed (slow) Passband Ripple.....	34

## LIST OF TABLES

Table 1. CS4351 Auto-Detect .....	15
Table 2. CS4351 Mode Select .....	15
Table 3. Single-Speed Mode Standard Frequencies .....	16
Table 4. Double-Speed Mode Standard Frequencies.....	16
Table 5. Quad-Speed Mode Standard Frequencies .....	16
Table 6. Digital Interface Format - Stand-Alone Mode.....	16
Table 7. Digital Interface Formats .....	24
Table 8. ATAPI Decode .....	26
Table 9. Example Digital Volume Settings .....	28
Table 10. Revision History .....	37

## 1. PIN DESCRIPTION



Pin Name	#	Pin Description
SDIN	1	<b>Serial Audio Data Input</b> ( <i>Input</i> ) - Input for two's complement serial audio data.
SCLK	2	<b>Serial Clock</b> ( <i>Input</i> ) - Serial clock for the serial audio interface.
LRCK	3	<b>Left / Right Clock</b> ( <i>Input</i> ) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	4	<b>Master Clock</b> ( <i>Input</i> ) - Clock source for the delta-sigma modulator and digital filters.
VD	5	<b>Digital Power</b> ( <i>Input</i> ) - Positive power supply for the digital section.
GND	6 16	<b>Ground</b> ( <i>Input</i> ) - Ground reference.
$\overline{RST}$	10	<b>Reset</b> ( <i>Input</i> ) - Powers down device and resets all internal registers to their default settings when enabled.
VA	11	<b>Low Voltage Analog Power</b> ( <i>Input</i> ) - Positive power supply for the analog section.
VBIAS	12	<b>Positive Voltage Reference</b> ( <i>Output</i> ) - Positive reference voltage for the internal DAC.
VQ	13	<b>Quiescent Voltage</b> ( <i>Output</i> ) - Filter connection for internal quiescent voltage.
VA_H	17	<b>High Voltage Analog Power</b> ( <i>Input</i> ) - Positive power supply for the analog section.
VL	20	<b>Serial Audio Interface Power</b> ( <i>Input</i> ) - Positive power for the serial audio interface
$\overline{BMUTE}$	14	<b>Mute Control</b> ( <i>Output</i> ) - Control signal for optional mute circuit.
$\overline{AMUTE}$	19	
AOUTB	15	<b>Analog Outputs</b> ( <i>Output</i> ) - The full scale analog line output level is specified in the <i>Analog Characteristics</i> table.
AOUTA	18	
<b>Control Port Definitions</b>		
SCL/CCLK	7	<b>Serial Control Port Clock</b> ( <i>Input</i> ) - Serial clock for the control port interface.
SDA/CDIN	8	<b>Serial Control Data</b> ( <i>Input/Output</i> ) - Input/Output for I <sup>2</sup> C data. Input for SPI data.
AD0/ $\overline{CS}$	9	<b>Address Bit 0 / Chip Select</b> ( <i>Input</i> ) - Chip address bit in I <sup>2</sup> C Mode. Control Port enable in SPI Mode.
<b>Stand-Alone Definitions</b>		
DIF0	8	<b>Digital Interface Format</b> ( <i>Input</i> ) - Defines the required relationship between the Left Right Clock, Serial Clock, and Serial Audio Data.
DIF1	7	
DEM	9	<b>De-emphasis</b> ( <i>Input</i> ) - Selects the standard 15 $\mu$ s/50 $\mu$ s digital de-emphasis filter response for 44.1 kHz sample rates

## 2. CHARACTERISTICS AND SPECIFICATIONS

(Min/Max performance characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical specifications are derived from performance measurements at  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{A\_H} = 12\text{ V}$ ,  $V_A = 3.3\text{ V}$ ,  $V_D = 3.3\text{ V}$ .)

### SPECIFIED OPERATING CONDITIONS

(GND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Typ	Max	Units
DC Power Supply	High Voltage Analog power	$V_{A\_H}$	8.55	12	12.6	V
	Low Voltage Analog power	$V_A$	3.13	3.3	3.47	V
	Digital power	$V_D$	3.13	3.3	3.47	V
	Interface power	$V_L$	1.7	3.3	3.47	V
Specified Temperature Range	-CZZ	$T_A$	-10	-	70	$^\circ\text{C}$
	-DZZ	$T_A$	-40	-	85	$^\circ\text{C}$

### ABSOLUTE MAXIMUM RATINGS

(GND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Max	Units
DC Power Supply	High Voltage Analog power	$V_{A\_H}$	-0.3	14	V
	Low Voltage Analog power	$V_A$	-0.3	3.63	V
	Digital power	$V_D$	-0.3	3.63	V
	Interface power	$V_L$	-0.3	3.63	V
Input Current, Any Pin Except Supplies		$I_{in}$	-	$\pm 10$	mA
Digital Input Voltage	Digital Interface	$V_{IN-L}$	-0.3	$V_L + 0.4$	V
Ambient Operating Temperature (power applied)		$T_A$	-55	125	$^\circ\text{C}$
Storage Temperature		$T_{stg}$	-65	150	$^\circ\text{C}$

Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

## DAC ANALOG CHARACTERISTICS

(Test conditions (unless otherwise specified): input test signal is a 997 Hz sine wave at 0 dBFS; measurement bandwidth 10 Hz to 20 kHz)

Parameter	Symbol	Min	Typ	Max	Unit	
<b>All Speed Modes</b> <i>F<sub>s</sub> = 48, 96, and 192 kHz</i>						
Dynamic Range (Note 1)	24-bit unweighted	99	109	-	dB	
		102	112	-	dB	
	16-bit unweighted	-	95	-	dB	
		-	98	-	dB	
Total Harmonic Distortion + Noise (Note 1)	24-bit	0 dB	-100	-90	dB	
		-20 dB	-89	-79	dB	
		-60 dB	-49	-39	dB	
	16-bit	0 dB	-	-92	-	dB
		-20 dB	-	-75	-	dB
		-60 dB	-	-35	-	dB
All Speed Modes						
Idle Channel Noise / Signal-to-noise ratio		-	109	-	dB	
Interchannel Isolation (1 kHz)		-	100	-	dB	
<b>Analog Output - All Modes</b>						
Full Scale Output Voltage		1.85	2.00	2.15	V <sub>rms</sub>	
Common Mode Voltage	V <sub>Q</sub>	-	4	-	V <sub>dc</sub>	
Max DC Current draw from an AOUT pin	I <sub>OUTmax</sub>	-	10	-	μA	
Max Current draw from V <sub>Q</sub>	I <sub>Qmax</sub>	-	1	-	μA	
Interchannel Gain Mismatch		-	0.1	-	dB	
Gain Drift		-	-100	-	ppm/°C	
Output Impedance	Z <sub>OUT</sub>	-	50	-	Ω	
AC-Load Resistance	R <sub>L</sub>	5	-	-	kΩ	
Load Capacitance	C <sub>L</sub>	-	-	100	pF	

### Notes:

1. One-half LSB of triangular PDF dither is added to data.



## COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

(The filter characteristics have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs. See (Note 6))

Parameter	Fast Roll-Off			Unit	
	Min	Typ	Max		
<b>Combined Digital and On-Chip Analog Filter Response - Single-Speed Mode - 48 kHz</b>					
Passband (Note 3)	to -0.01 dB corner	0	-	.454	Fs
	to -3 dB corner	0	-	.499	Fs
Frequency Response 10 Hz to 20 kHz	-0.01	-	+0.01		dB
StopBand	0.547	-	-		Fs
StopBand Attenuation (Note 4)	102	-	-		dB
Total Group Delay (Fs = Output Sample Rate)	-	9.4/Fs	-		s
Intra-channel Phase Deviation	-	-	±0.56/Fs		s
Inter-channel Phase Deviation	-	-	0		s
De-emphasis Error (Note 5) (Relative to 1 kHz)	Fs = 32 kHz	-	-	±0.23	dB
	Fs = 44.1 kHz	-	-	±0.14	dB
	Fs = 48 kHz	-	-	±0.09	dB
<b>Combined Digital and On-Chip Analog Filter Response - Double-Speed Mode - 96 kHz</b>					
Passband (Note 3)	to -0.01 dB corner	0	-	.430	Fs
	to -3 dB corner	0	-	.499	Fs
Frequency Response 10 Hz to 20 kHz	-0.01	-	0.01		dB
StopBand	.583	-	-		Fs
StopBand Attenuation (Note 4)	80	-	-		dB
Total Group Delay (Fs = Output Sample Rate)	-	4.6/Fs	-		s
Intra-channel Phase Deviation	-	-	±0.03/Fs		s
Inter-channel Phase Deviation	-	-	0		s
<b>Combined Digital and On-Chip Analog Filter Response - Quad-Speed Mode - 192 kHz</b>					
Passband (Note 3)	to -0.01 dB corner	0	-	.105	Fs
	to -3 dB corner	0	-	.490	Fs
Frequency Response 10 Hz to 20 kHz	-0.01	-	0.01		dB
StopBand	.635	-	-		Fs
StopBand Attenuation (Note 4)	90	-	-		dB
Total Group Delay (Fs = Output Sample Rate)	-	4.7/Fs	-		s
Intra-channel Phase Deviation	-	-	±0.01/Fs		s
Inter-channel Phase Deviation	-	-	0		s

**COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE**

(Continued)

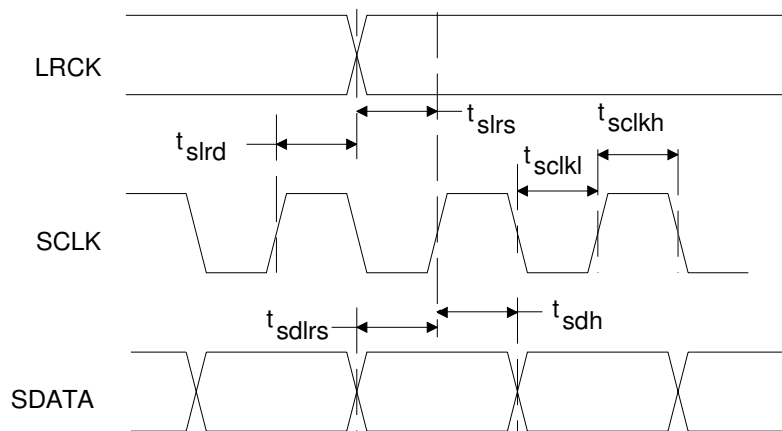
Parameter	Slow Roll-Off (Note 2)			Unit	
	Min	Typ	Max		
<b>Single-Speed Mode - 48 kHz</b>					
Passband (Note 3)	to -0.01 dB corner	0	-	0.417	Fs
	to -3 dB corner	0	-	0.499	Fs
Frequency Response 10 Hz to 20 kHz	-0.01	-	+0.01	dB	
StopBand	.583	-	-	Fs	
StopBand Attenuation (Note 4)	64	-	-	dB	
Total Group Delay (Fs = Output Sample Rate)	-	6.5/Fs	-	s	
Intra-channel Phase Deviation	-	-	±0.14/Fs	s	
Inter-channel Phase Deviation	-	-	0	s	
De-emphasis Error (Note 5) (Relative to 1 kHz)	Fs = 32 kHz	-	-	±0.23	dB
	Fs = 44.1 kHz	-	-	±0.14	dB
	Fs = 48 kHz	-	-	±0.09	dB
<b>Double-Speed Mode - 96 kHz</b>					
Passband (Note 3)	to -0.01 dB corner	0	-	.296	Fs
	to -3 dB corner	0	-	.499	Fs
Frequency Response 10 Hz to 20 kHz	-0.01	-	0.01	dB	
StopBand	.792	-	-	Fs	
StopBand Attenuation (Note 4)	70	-	-	dB	
Total Group Delay (Fs = Output Sample Rate)	-	3.9/Fs	-	s	
Intra-channel Phase Deviation	-	-	±0.01/Fs	s	
Inter-channel Phase Deviation	-	-	0	s	
<b>Quad-Speed Mode - 192 kHz</b>					
Passband (Note 3)	to -0.01 dB corner	0	-	.104	Fs
	to -3 dB corner	0	-	.481	Fs
Frequency Response 10 Hz to 20 kHz	-0.01	-	0.01	dB	
StopBand	.868	-	-	Fs	
StopBand Attenuation (Note 4)	75	-	-	dB	
Group Delay	-	4.2/Fs	-	s	
Intra-channel Phase Deviation	-	-	±0.01/Fs	s	
Inter-channel Phase Deviation	-	-	0	s	

**Notes:**

2. Slow Roll-off interpolation filter is only available in Control Port mode.
3. Response is clock dependent and will scale with Fs.
4. For Single-Speed Mode, the Measurement Bandwidth is from stopband to 3 Fs.  
For Double-Speed Mode, the Measurement Bandwidth is from stopband to 3 Fs.  
For Quad-Speed Mode, the Measurement Bandwidth is from stopband to 1.34 Fs.
5. De-emphasis is available only in Single-Speed Mode; Only 44.1 kHz De-emphasis is available in Stand-Alone Mode.
6. Amplitude vs. Frequency plots of this data are available in the [“Digital Filter Response Plots”](#) on page 31.

**SWITCHING SPECIFICATIONS - SERIAL AUDIO INTERFACE**

Parameters	Symbol	Min	Max	Units	
MCLK Frequency		1.024	51.2	MHz	
MCLK Duty Cycle		45	55	%	
Input Sample Rate (Manual selection)	Single-Speed Mode	Fs	4	50	kHz
	Double-Speed Mode	Fs	50	100	kHz
	Quad-Speed Mode	Fs	100	200	kHz
Input Sample Rate (Auto selection)	Single-Speed Mode	Fs	4	50	kHz
	Double-Speed Mode	Fs	84	100	kHz
	Quad-Speed Mode	Fs	170	200	kHz
LRCK Duty Cycle		40	60	%	
SCLK Pulse Width Low	t <sub>sckl</sub>	20	-	ns	
SCLK Pulse Width High	t <sub>sckh</sub>	20	-	ns	
SCLK Period	Single-Speed Mode	t <sub>sckw</sub>	$\frac{1}{(128)Fs}$	-	-
	Double-Speed Mode	t <sub>sckw</sub>	$\frac{1}{(64)Fs}$	-	-
	Quad-Speed Mode	t <sub>sckw</sub>	$\frac{2}{MCLK}$	-	-
SCLK rising to LRCK edge delay	t <sub>slrd</sub>	23	-	ns	
SCLK rising to LRCK edge setup time	t <sub>slrs</sub>	20	-	ns	
SDIN valid to SCLK rising setup time	t <sub>sdls</sub>	20	-	ns	
SCLK rising to SDIN hold time	t <sub>sdh</sub>	20	-	ns	


**Figure 1. Serial Input Timing**

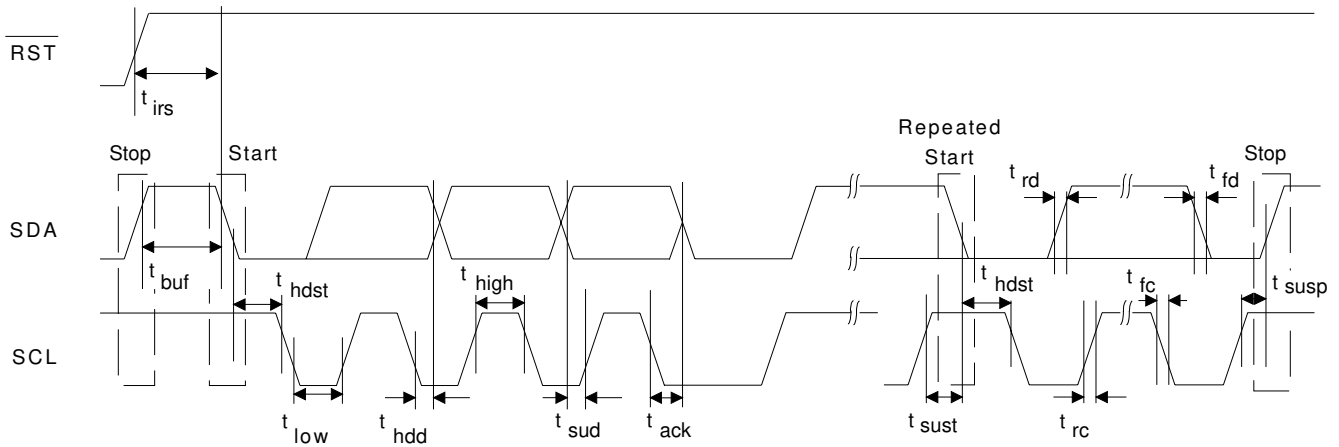
## Switching Characteristics - Control Port - I<sup>2</sup>C® Format

(Inputs: Logic 0 = GND, Logic 1 = VL, C<sub>L</sub> = 20 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	$f_{scl}$	-	100	kHz
RST Rising Edge to Start	$t_{irs}$	500	-	ns
Bus Free Time Between Transmissions	$t_{buf}$	4.7	-	$\mu$ s
Start Condition Hold Time (prior to first clock pulse)	$t_{hdst}$	4.0	-	$\mu$ s
Clock Low time	$t_{low}$	4.7	-	$\mu$ s
Clock High Time	$t_{high}$	4.0	-	$\mu$ s
Setup Time for Repeated Start Condition	$t_{sust}$	4.7	-	$\mu$ s
SDA Hold Time from SCL Falling (Note 7)	$t_{hdd}$	0	-	$\mu$ s
SDA Setup time to SCL Rising	$t_{sud}$	250	-	ns
Rise Time of SCL and SDA	$t_{rc}, t_{rc}$	-	1	$\mu$ s
Fall Time SCL and SDA	$t_{fc}, t_{fc}$	-	300	ns
Setup Time for Stop Condition	$t_{susp}$	4.7	-	$\mu$ s
Acknowledge Delay from SCL Falling	$t_{ack}$	300	1000	ns

### Notes:

- Data must be held for sufficient time to bridge the transition time,  $t_{fc}$ , of SCL.



**Figure 2. Control Port Timing - I<sup>2</sup>C Format**

## SWITCHING CHARACTERISTICS - CONTROL PORT - SPI™ FORMAT

(Inputs: Logic 0 = GND, Logic 1 = VL, C<sub>L</sub> = 20 pF)

Parameter	Symbol	Min	Max	Unit
CCLK Clock Frequency	f <sub>sclk</sub>	-	6	MHz
RST Rising Edge to CS Falling	t <sub>srs</sub>	500	-	ns
CCLK Edge to CS Falling (Note 8)	t <sub>spi</sub>	500	-	ns
CS High Time Between Transmissions	t <sub>csh</sub>	1.0	-	μs
CS Falling to CCLK Edge	t <sub>css</sub>	20	-	ns
CCLK Low Time	t <sub>scl</sub>	66	-	ns
CCLK High Time	t <sub>sch</sub>	66	-	ns
CDIN to CCLK Rising Setup Time	t <sub>dsu</sub>	40	-	ns
CCLK Rising to DATA Hold Time (Note 9)	t <sub>dh</sub>	17	-	ns
Rise Time of CCLK and CDIN (Note 10)	t <sub>r2</sub>	-	100	ns
Fall Time of CCLK and CDIN (Note 10)	t <sub>f2</sub>	-	100	ns

### Notes:

8. t<sub>spi</sub> only needed before first falling edge of CS after RST rising edge. t<sub>spi</sub> = 0 at all other times.
9. Data must be held for sufficient time to bridge the transition time of CCLK.
10. For F<sub>SCK</sub> < 1 MHz.

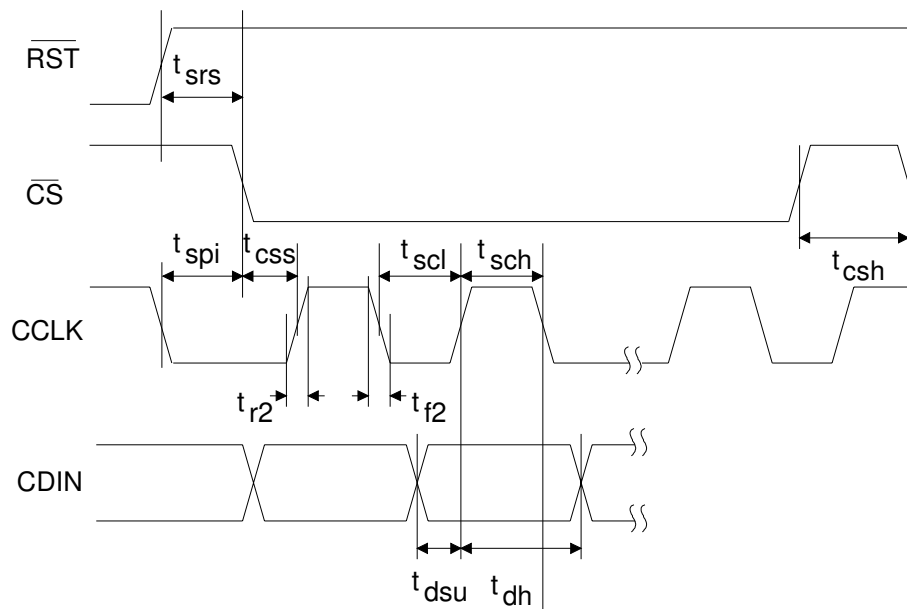


Figure 3. Control Port Timing - SPI Format (Write)



## DIGITAL CHARACTERISTICS

Parameters	Symbol	Min	Typ	Max	Units	
High-Level Input Voltage	VL = 3.3 V	V <sub>IH</sub>	2.0	-	-	V
	VL = 2.5 V	V <sub>IH</sub>	1.7	-	-	V
	VL = 1.8 V	V <sub>IH</sub>	0.65•V <sub>L</sub>	-	-	V
Low-Level Input Voltage	VL = 3.3 V	V <sub>IL</sub>	-	-	0.8	V
	VL = 2.5 V	V <sub>IL</sub>	-	-	0.7	V
	VL = 1.8 V	V <sub>IL</sub>	-	-	0.33•V <sub>L</sub>	V
Input Leakage Current	I <sub>in</sub>	-	-	±10	μA	
Input Capacitance		-	8	-	pF	
Maximum MUTE C Drive Current		-	2	-	mA	
MUTE C High-Level Output Voltage	V <sub>OH</sub>	-	VA_H	-	V	
MUTE C Low-Level Output Voltage	V <sub>OL</sub>	-	0	-	V	

## POWER AND THERMAL CHARACTERISTICS

Parameters	Symbol	Min	Typ	Max	Units	
<b>Power Supplies</b>						
Power Supply Current (Note 11)	normal operation, VA_H = 12 V	I <sub>A_H</sub>	-	15	20	mA
	VA_H = 9 V	I <sub>A_H</sub>	-	14	19	mA
	VA = 3.3 V	I <sub>A</sub>	-	6	8	mA
	VD = 3.3 V	I <sub>D</sub>	-	21	26	mA
	Interface current (Note 12) VL = 3.3 V	I <sub>L</sub>	-	100	400	μA
power-down state, all supplies (Note 13)	I <sub>pd</sub>	-	200	-	μA	
Power Dissipation (all supplies) VA_H = 12 V	(Note 11)		-	270	354	mW
	normal operation		-	1	-	mW
	power-down (Note 13)		-	216	285	mW
VA_H = 9 V			-	1	-	mW
	normal operation		-	1	-	mW
	power-down (Note 13)		-	1	-	mW
Power Supply Rejection Ratio (Note 14)	(1 kHz)	PSRR	-	60	-	dB
	(60 Hz)		-	60	-	dB

### Notes:

- Current consumption increases with increasing FS and increasing MCLK. Typ and Max values are based on highest FS and highest MCLK. Variance between speed modes is small.
- I<sub>L</sub> measured with no external loading on pin 8 (SDA).
- Power-Down Mode is defined as  $\overline{\text{RES}}$  pin = Low with all clock and data lines held static.
- Valid with the recommended capacitor values on VQ and V<sub>BIAS</sub> as shown in the typical connection diagram in Section 3.

### 3. TYPICAL CONNECTION DIAGRAM

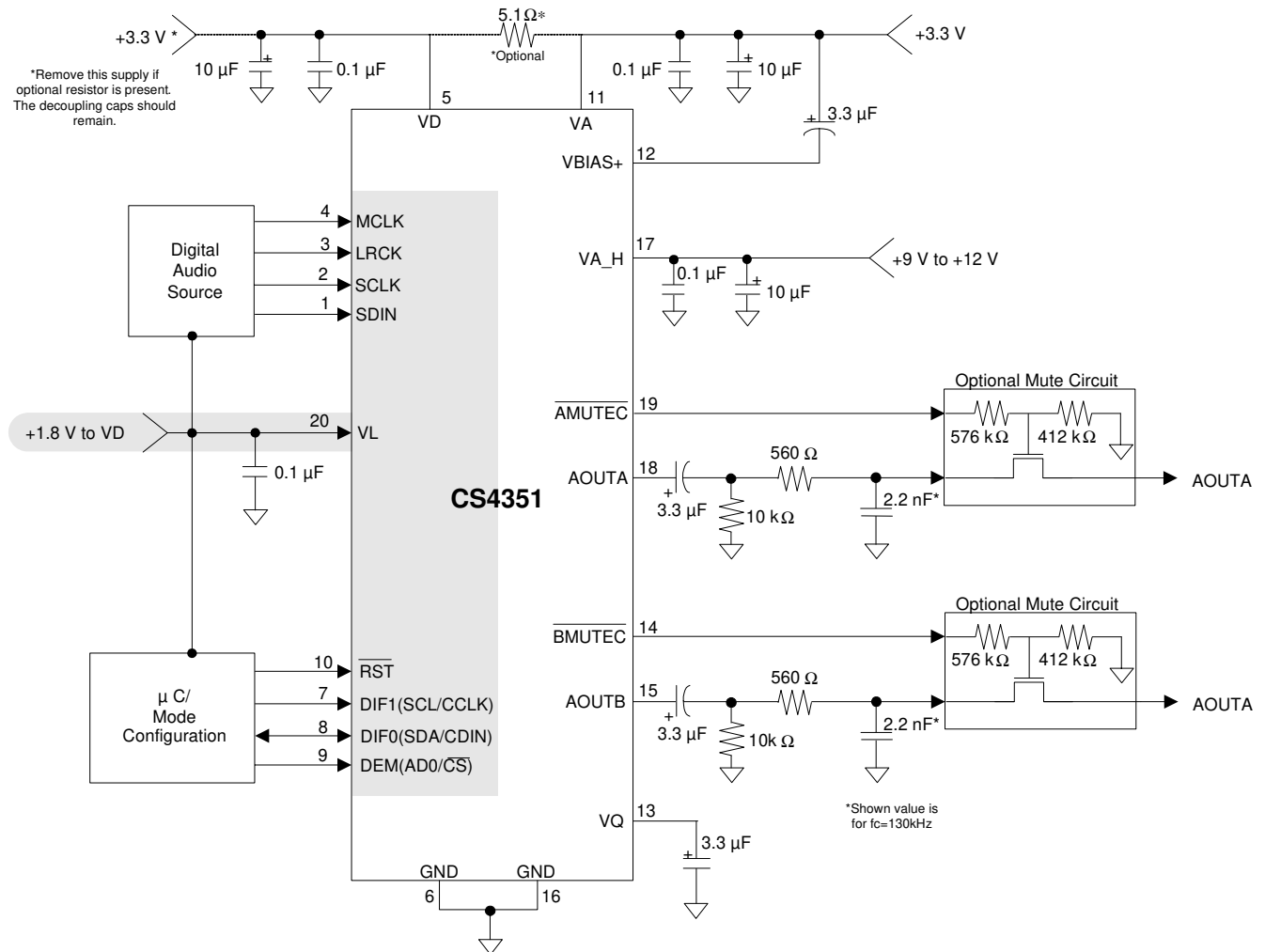


Figure 4. Typical Connection Diagram

## 4. APPLICATIONS

### 4.1 Sample Rate Range/Operational Mode Detect

The device operates in one of three operational modes. The allowed sample rate range in each mode will depend on whether the Auto-Detect Defeat bit is enabled/disabled.

#### 4.1.1 *Auto-Detect Enabled*

The Auto-Detect feature is enabled by default. In this state, the CS4351 will auto-detect the correct mode when the input sample rate ( $F_s$ ), defined by the LRCK frequency, falls within one of the ranges illustrated in [Table 1](#). Sample rates outside the specified range for each mode are not supported.

Input Sample Rate ( $F_s$ )	MODE
4 kHz - 50 kHz	Single-Speed Mode
84 kHz - 100 kHz	Double-Speed Mode
170 kHz - 200 kHz	Quad-Speed Mode

**Table 1. CS4351 Auto-Detect**

#### 4.1.2 *Auto-Detect Disabled*

The Auto-Detect feature can be defeated only by the format bits in the control port register 02h. In this state, the CS4351 will not auto-detect the correct mode based on the input sample rate ( $F_s$ ). The operational mode must then be set manually according to one of the ranges illustrated in [Table 2](#). Please refer to [Section 6.2.3](#) for implementation details. Sample rates outside the specified range for each mode are not supported. In stand-alone mode it is not possible to disable auto-detect of sample rates.

FM1	FM0	Input Sample Rate ( $F_s$ )	MODE
0	0	Auto speed mode detect	Auto
0	1	4 kHz - 50 kHz	Single-Speed Mode
1	0	50 kHz - 100 kHz	Double-Speed Mode
1	1	100 kHz - 200 kHz	Quad-Speed Mode

**Table 2. CS4351 Mode Select**

### 4.2 System Clocking

The device requires external generation of the master (MCLK), left/right (LRCK) and serial (SCLK) clocks. The left/right clock, defined also as the input sample rate ( $F_s$ ), must be synchronously derived from the MCLK according to specified ratios. The specified ratios of MCLK to LRCK, along with several standard audio sample rates and the required MCLK frequency, are illustrated in [Tables 3](#) through [5](#).

Refer to [Section 4.3](#) for the required SCLK timing associated with the selected Digital Interface Format and to the [“Switching Specifications - Serial Audio Interface”](#) section on [page 10](#) for the maximum allowed clock frequencies.

Sample Rate (kHz)	MCLK (MHz)					
	256x	384x	512x	768x	1024x	1152x
32	8.1920	12.2880	16.3840	24.5760	32.7680	36.8640
44.1	11.2896	16.9344	22.5792	33.8688	45.1584	
48	12.2880	18.4320	24.5760	36.8640	49.1520	

**Table 3. Single-Speed Mode Standard Frequencies**

Sample Rate (kHz)	MCLK (MHz)				
	128x	192x	256x	384x	512x
64	8.1920	12.2880	16.3840	24.5760	32.7680
88.2	11.2896	16.9344	22.5792	33.8688	45.1584
96	12.2880	18.4320	24.5760	36.8640	49.1520

**Table 4. Double-Speed Mode Standard Frequencies**

Sample Rate (kHz)	MCLK (MHz)				
	64x	96x	128x	192x	256x
176.4	11.2896	16.9344	22.5792	33.8688	45.1584
192	12.2880	18.4320	24.5760	36.8640	49.1520

**Table 5. Quad-Speed Mode Standard Frequencies**

= Denotes clock modes which are NOT auto detected

### 4.3 Digital Interface Format

The device will accept audio samples in 1 of 4 digital interface formats in Stand-Alone mode, as illustrated in [Table 6](#), and 1 of 6 formats in Control Port mode, as illustrated in [Table 7](#).

#### 4.3.1 Stand-Alone Mode

The desired format is selected via the DIF1 and DIF0 pins. For an illustration of the required relationship between the LRCK, SCLK and SDIN, see [Figures 5](#) through [7](#). For all formats, SDIN is valid on the rising edge of SCLK. Also, SCLK must have at least 32 cycles per LRCK period in format 2, and 48 cycles per LRCK period in format 3.

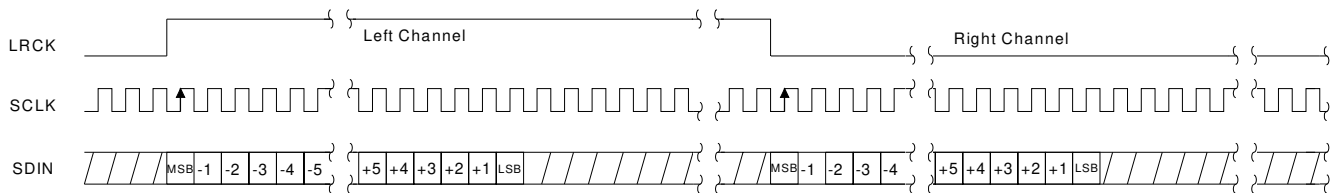
DIF0	DIF1	DESCRIPTION	FORMAT	FIGURE
0	0	I <sup>2</sup> S, up to 24-bit Data	0	<a href="#">6</a>
0	1	Left Justified, up to 24-bit Data	1	<a href="#">5</a>
1	0	Right Justified, 24-bit Data	2	<a href="#">7</a>
1	1	Right Justified, 16-bit Data	3	<a href="#">7</a>

**Table 6. Digital Interface Format - Stand-Alone Mode**

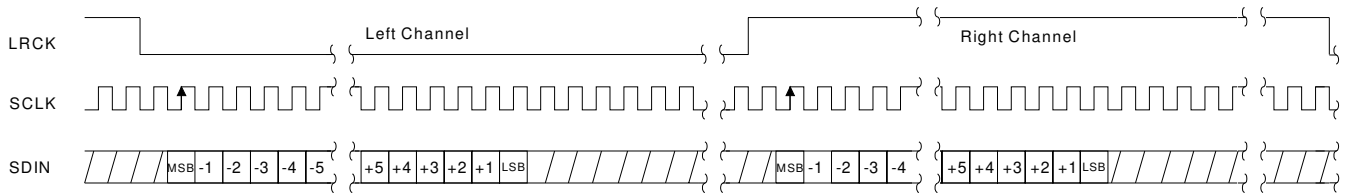
#### 4.3.2 Control Port Mode

The desired format is selected via the DIF2, DIF1 and DIF0 bits in the Mode Control 2 register (see section [Section 6.2.1](#)). For an illustration of the required relationship between LRCK, SCLK and SDIN, see [Figures 5](#) through [7](#). For all formats, SDIN is valid on the rising edge of SCLK. Also, SCLK must have at

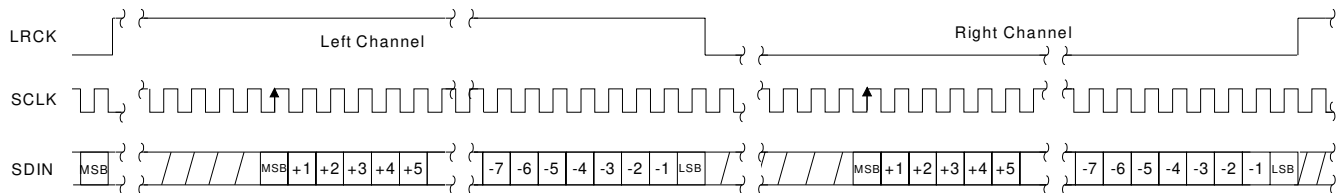
least 32 cycles per LRCK period in format 2, 48 cycles in format 3, 40 cycles in format 4, and 36 cycles in format 5.



**Figure 5. Left-Justified up to 24-Bit Data**



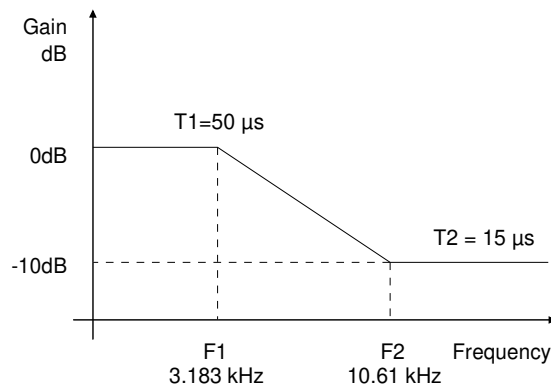
**Figure 6. I²S, up to 24-Bit Data**



**Figure 7. Right-Justified Data**

#### 4.4 De-Emphasis Control

The device includes on-chip digital de-emphasis. [Figure 8](#) shows the de-emphasis curve for  $F_s$  equal to 44.1 kHz. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate,  $F_s$ .



**Figure 8. De-Emphasis Curve**

**Note:** De-emphasis is only available in Single-Speed Mode.



#### 4.4.1 Stand-Alone Mode

When pulled to VL the DEM pin activates the 44.1 kHz de-emphasis filter. When pulled to GND the DEM pin turns off the de-emphasis filter.

#### 4.4.2 Control Port Mode

The Mode Control bits selects either the 32, 44.1, or 48 kHz de-emphasis filter. Please see [Section 6.2.2](#) for the desired de-emphasis control.

### 4.5 Recommended Power-Up Sequence

#### 4.5.1 Stand-Alone Mode

1. Hold  $\overline{\text{RST}}$  low until the power supplies and configuration pins are stable, and the master and left/right clocks are locked to the appropriate frequencies, as discussed in [Section 4.2](#). In this state, the control port is reset to its default settings, VQ will remain low, and VBIAS will be connected to VA.
2. Bring  $\overline{\text{RST}}$  high. The device will remain in a low power state with VQ low and will initiate the Stand-Alone power-up sequence after approximately 512 LRCK cycles in Single-Speed Mode (1024 LRCK cycles in Double-Speed Mode, and 2048 LRCK cycles in Quad-Speed Mode).

#### 4.5.2 Control Port Mode

1. Hold  $\overline{\text{RST}}$  low until the power supply is stable, and the master and left/right clocks are locked to the appropriate frequencies, as discussed in [Section 4.2](#). In this state, the control port is reset to its default settings, VQ will remain low, and VBIAS will be connected to VA.
2. Bring  $\overline{\text{RST}}$  high. The device will remain in a low power state with VQ low.
3. Perform a control port write to the CP\_EN bit prior to the completion of approximately 512 LRCK cycles in Single-Speed Mode (1024 LRCK cycles in Double-Speed Mode, and 2048 LRCK cycles in Quad-Speed Mode). The desired register settings can be loaded while keeping the PDN bit set to 1.
4. Set the PDN bit to 0. This will initiate the power-up sequence, which lasts approximately 50  $\mu\text{s}$  when the POPG bit is set to 0. If the POPG bit is set to 1, see [Section 4.6](#) for a complete description of power-up timing.

### 4.6 Popguard® Transient Control

The CS4351 uses a novel technique to minimize the effects of output transients during power-up and power-down. This technology, when used with external DC-blocking capacitors in series with the audio outputs, minimizes the audio transients commonly produced by single-ended single-supply converters. It is activated inside the DAC when the  $\overline{\text{RST}}$  pin is toggled and requires no other external control, aside from choosing the appropriate DC-blocking capacitors.

#### 4.6.1 Power-Up

When the device is initially powered-up, the audio outputs, AOUTA and AOUTB, are clamped to GND. Following a delay of approximately 1000 sample periods, each output begins to ramp toward the quiescent voltage. Approximately 10,000 LRCK cycles later, the outputs reach  $V_Q$  and audio output begins. This gradual voltage ramping allows time for the external DC-blocking capacitors to charge to the quiescent voltage, minimizing audible power-up transients.

### 4.6.2 Power-Down

To prevent audible transients at power-down, the device must first enter its power-down state. When this occurs, audio output ceases and the internal output buffers are disconnected from AOUTA and AOUTB. In their place, a soft-start current sink is substituted which allows the DC-blocking capacitors to slowly discharge. Once this charge is dissipated, the power to the device may be turned off and the system is ready for the next power-on.

### 4.6.3 Discharge Time

To prevent an audio transient at the next power-on, the DC-blocking capacitors must fully discharge before turning on the power or exiting the power-down state. If full discharge does not occur, a transient will occur when the audio outputs are initially clamped to GND. The time that the device must remain in the power-down state is related to the value of the DC-blocking capacitance and the output load. For example, with a 3.3  $\mu\text{F}$  capacitor, the minimum power-down time will be approximately 0.4 seconds.

## 4.7 Mute Control

The Mute Control pins go active during power-up initialization, reset, muting (see [Section 6.4.3](#)), or if the MCLK to LRCK ratio is incorrect. These pins are intended to be used as control for external mute circuits to prevent the clicks and pops that can occur in any single-ended single supply system.

Use of the Mute Control function is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the Mute Control function can enable the system designer to achieve idle channel noise/signal-to-noise ratios which are only limited by the external mute circuit. Please see the [“Typical Connection Diagram”](#) on page 14 for a suggested mute circuit for single supply systems. This FET circuit must be placed in series after the RC filter, otherwise noise may occur during muting conditions. Further ESD protection will need to be taken into consideration for the FET used. If dual supplies are available, the BJT mute circuit from Figure 12 in the CS4398 datasheet (active Low) may be used.

## 4.8 Grounding and Power Supply Arrangements

As with any high resolution converter, the CS4351 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. [Figure 4](#) shows the recommended power arrangements, with VA\_H, VA, VD, and VL connected to clean supplies. If the ground planes are split between digital ground and analog ground, the GND pins of the CS4351 should be connected to the analog ground plane.

All signals, especially clocks, should be kept away from the VBIAS and VQ pins in order to avoid unwanted coupling into the DAC.

### 4.8.1 Capacitor Placement

Decoupling capacitors should be placed as close to the DAC as possible, with the low value ceramic capacitor being the closest. To further minimize impedance, these capacitors should be located on the same layer as the DAC. If desired, all supply pins may be connected to the same supply, but a decoupling capacitor should still be placed on each supply pin.

**Note:** All decoupling capacitors should be referenced to analog ground.

The CDB4351 evaluation board demonstrates the optimum layout and power supply arrangements.

## 4.9 Control Port Interface

The control port is used to load all the internal register settings (see [Section 6](#)). The operation of the control port may be completely asynchronous with the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port operates in one of two modes: I<sup>2</sup>C or SPI.

### 4.9.1 MAP Auto Increment

The device has MAP (memory address pointer) auto increment capability enabled by the INCR bit (also the MSB) of the MAP. If INCR is set to 0, MAP will stay constant for successive I<sup>2</sup>C writes or reads and SPI writes. If INCR is set to 1, MAP will auto increment after each byte is written, allowing block reads or writes of successive registers.

### 4.9.2 I<sup>2</sup>C Mode

In the I<sup>2</sup>C mode, data is clocked into and out of the bi-directional serial control data line, SDA, by the serial control port clock, SCL (see [Figure 9](#) for the clock to data relationship). There is no  $\overline{\text{CS}}$  pin. Pin AD0 enables the user to alter the chip address (100110[AD0][R/W]) and should be tied to VL or GND as required, before powering up the device. If the device ever detects a high to low transition on the AD0/ $\overline{\text{CS}}$  pin after power-up, SPI mode will be selected.

#### 4.9.2.1 I<sup>2</sup>C Write

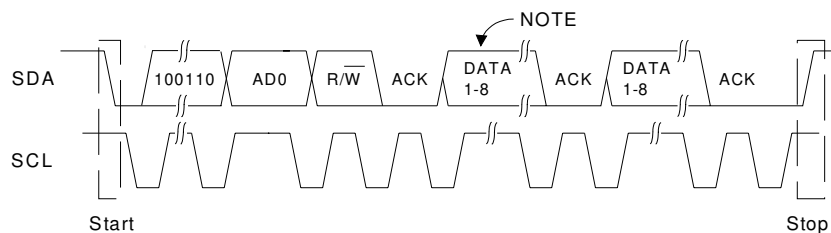
To write to the device, follow the procedure below while adhering to the control port Switching Specifications in [Section 8](#).

1. Initiate a START condition to the I<sup>2</sup>C bus followed by the address byte. The upper 6 bits must be 100110. The seventh bit must match the setting of the AD0 pin, and the eighth must be 0. The eighth bit of the address byte is the R/W bit.
2. Wait for an acknowledge (ACK) from the part, then write to the memory address pointer, MAP. This byte points to the register to be written.
3. Wait for an acknowledge (ACK) from the part, then write the desired data to the register pointed to by the MAP.
4. If the INCR bit (see [Section 4.9.1](#)) is set to 1, repeat the previous step until all the desired registers are written, then initiate a STOP condition to the bus.
5. If the INCR bit is set to 0 and further I<sup>2</sup>C writes to other registers are desired, it is necessary to initiate a repeated START condition and follow the procedure detailed from step 1. If no further writes to other registers are desired, initiate a STOP condition to the bus.

### 4.9.2.2 I<sup>2</sup>C Read

To read from the device, follow the procedure below while adhering to the control port Switching Specifications.

1. Initiate a START condition to the I<sup>2</sup>C bus followed by the address byte. The upper 6 bits must be 100110. The seventh bit must match the setting of the AD0 pin, and the eighth must be 1. The eighth bit of the address byte is the R/W bit.
2. After transmitting an acknowledge (ACK), the device will then transmit the contents of the register pointed to by the MAP. The MAP register will contain the address of the last register written to the MAP, or the default address (see Section 4.10.2) if an I<sup>2</sup>C read is the first operation performed on the device.
3. Once the device has transmitted the contents of the register pointed to by the MAP, issue an ACK.
4. If the INCR bit is set to 1, the device will continue to transmit the contents of successive registers. Continue providing a clock and issue an ACK after each byte until all the desired registers are read, then initiate a STOP condition to the bus.
5. If the INCR bit is set to 0 and further I<sup>2</sup>C reads from other registers are desired, it is necessary to initiate a repeated START condition and follow the procedure detailed from steps 1 and 2 from the I<sup>2</sup>C Write instructions followed by step 1 of the I<sup>2</sup>C Read section. If no further reads from other registers are desired, initiate a STOP condition to the bus.



NOTE: If operation is a write, this byte contains the Memory Address Pointer, MAP. If operation is a read, this byte contains the data of the register pointed to by the MAP.

**Figure 9. Control Port Timing, I<sup>2</sup>C Mode**

### 4.9.3 SPI Mode

In SPI mode, data is clocked into the serial control data line, CDIN, by the serial control port clock, CCLK (see Figure 10 for the clock to data relationship). There is no AD0 pin. Pin  $\overline{CS}$  is the chip select signal and is used to control SPI writes to the control port. When the device detects a high to low transition on the AD0/ $\overline{CS}$  pin after power-up, SPI mode will be selected. All signals are inputs and data is clocked in on the rising edge of CCLK.

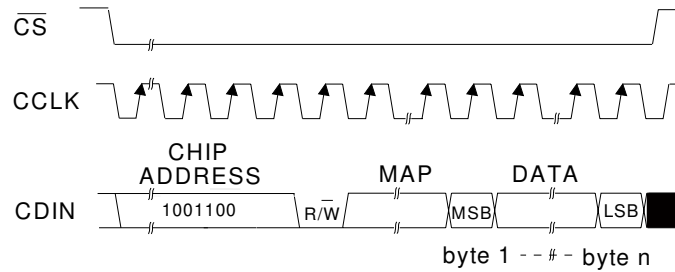
#### 4.9.3.1 SPI Write

To write to the device, follow the procedure below while adhering to the control port Switching Specifications in Section 8.

1. Bring  $\overline{CS}$  low.
2. The address byte on the CDIN pin must then be 10011000.
3. Write to the memory address pointer, MAP. This byte points to the register to be written.

4. Write the desired data to the register pointed to by the MAP.
5. If the INCR bit (see [Section 4.9.1](#)) is set to 1, repeat the previous step until all the desired registers are written, then bring CS high.
6. If the INCR bit is set to 0 and further SPI writes to other registers are desired, it is necessary to bring CS high, and follow the procedure detailed from step 1. If no further writes to other registers are desired, bring CS high.

)



MAP = Memory Address Pointer

**Figure 10. Control Port Timing, SPI mode**

## 4.10 Memory Address Pointer (MAP)

7	6	5	4	3	2	1	0
INCR	Reserved	Reserved	Reserved	MAP3	MAP2	MAP1	MAP0
0	0	0	0	0	0	0	0

### 4.10.1 INCR (AUTO MAP INCREMENT ENABLE)

*Default = '0'*

0 - Disabled

1 - Enabled

### 4.10.2 MAP (MEMORY ADDRESS POINTER)

*Default = '0000'*



**5. REGISTER QUICK REFERENCE**

Addr	Function	7	6	5	4	3	2	1	0
1h	Chip ID default	PART4 1	PART3 1	PART2 1	PART1 1	PART0 1	REV2 -	REV1 -	REV0 -
2h	Mode Control default	Reserved 0	DIF2 0	DIF1 0	DIF0 0	DEM1 0	DEM0 0	FM1 0	FM0 0
3h	Volume, Mixing, and Inversion Control default	VOLB=A 0	INVERTA 0	INVERTB 0	Reserved 0	ATAPI3 1	ATAPI2 0	ATAPI1 0	ATAPI0 1
4h	Mute Control default	AMUTE 1	Reserved 0	MUTE_C A=B 0	MUTE_A 0	MUTE_B 0	Reserved 0	Reserved 0	Reserved 0
5h	Channel A Volume Control default	VOL7 0	VOL6 0	VOL5 0	VOL4 0	VOL3 0	VOL2 0	VOL1 0	VOL0 0
6h	Channel B Volume Control default	VOL7 0	VOL6 0	VOL5 0	VOL4 0	VOL3 0	VOL2 0	VOL1 0	VOL0 0
7h	Ramp and Filter Control default	SZC1 1	SZC0 0	RMP_UP 1	RMP_DN 1	Reserved 0	FILT_SEL 0	Reserved 0	Reserved 1
8h	Misc. Control default	PDN 1	CPEN 0	FREEZE 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0

## 6. REGISTER DESCRIPTION

\*\* All register access is R/W unless specified otherwise\*\*

### 6.1 Chip ID - Register 01h

7	6	5	4	3	2	1	0
PART4	PART3	PART2	PART1	PART0	REV2	REV1	REV0
1	1	1	1	1	-	-	-

Function:

This register is Read-Only. Bits 7 through 3 are the part number ID which is 11111b and the remaining Bits (2 through 0) are for the chip revision (Rev. A = 000, Rev. B = 001, ...)

### 6.2 Mode Control 1 - Register 02h

7	6	5	4	3	2	1	0
Reserved	DIF2	DIF1	DIF0	DEM1	DEM0	FM1	FM0
0	0	0	0	0	0	0	0

#### 6.2.1 Digital Interface Format (DIF2:0) Bits 6-4

Function:

These bits select the interface format for the serial audio input.

The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in [Figures 5 through 7](#).

DIF2	DIF1	DIF0	DESCRIPTION	Format	FIGURE
0	0	0	Left Justified, up to 24-bit data	0 (Default)	5
0	0	1	I <sup>2</sup> S, up to 24-bit data	1	6
0	1	0	Right Justified, 16-bit data	2	7
0	1	1	Right Justified, 24-bit data	3	7
1	0	0	Right Justified, 20-bit data	4	7
1	0	1	Right Justified, 18-bit data	5	7
1	1	0	Reserved		
1	1	1	Reserved		

Table 7. Digital Interface Formats

#### 6.2.2 De-Emphasis Control (DEM1:0) Bits 3-2.

Default = 0

- 00 - No De-emphasis
- 01 - 44.1 kHz De-emphasis
- 10 - 48 kHz De-emphasis
- 11 - 32 kHz De-emphasis

Function:

Selects the appropriate digital filter to maintain the standard 15  $\mu$ s/50  $\mu$ s digital de-emphasis filter response at 32, 44.1 or 48 kHz sample rates. (See [Figure 11](#).)

**Note:** De-emphasis is only available in Single-Speed Mode

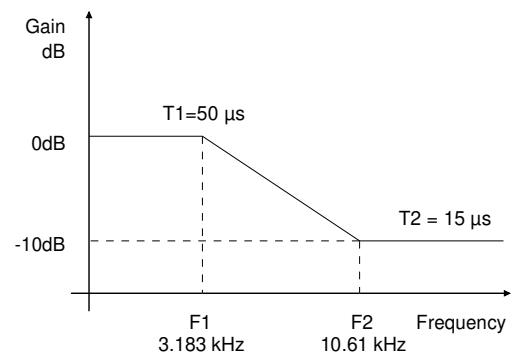


Figure 11. De-Emphasis Curve

### 6.2.3 Functional Mode (FM) Bits 1-0

Default = 00

00 - Auto speed mode detect

01 - Single-Speed Mode (4 to 50 kHz sample rates)

10 - Double-Speed Mode (50 to 100 kHz sample rates)

11 - Quad-Speed Mode (100 to 200 kHz sample rates)

Function:

Selects the required range of input sample rates or DSD Mode.

## 6.3 Volume Mixing and Inversion Control - Register 03h

B7	B6	B5	B4	B3	B2	B1	B0
VOLB=A	INVERT A	INVERT B	Reserved	ATAPI3	ATAPI2	ATAPI1	ATAPI0
0	0	0	0	1	0	0	1

### 6.3.1 Channel A Volume = Channel B Volume (VOLB=A) Bit 7

Function:

When set to 0 (default) the AOUTA and AOUTB volume levels are independently controlled by the A and the B Channel Volume Control Bytes.

When set to 1 the volume on both AOUTA and AOUTB are determined by the A Channel Attenuation and Volume Control Bytes, and the B Channel Bytes are ignored.

### 6.3.2 Invert Signal Polarity (Invert\_A) Bit 6

Function:

When set to 1, this bit inverts the signal polarity of channel A.

When set to 0 (default), this function is disabled.

### 6.3.3 Invert Signal Polarity (Invert\_B) Bit 5

Function:

When set to 1, this bit inverts the signal polarity of channel B.

When set to 0 (default), this function is disabled.