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CS4360

24-Bit, 192 kHz 6-channel D/A Converter

Features

- 24-bit Conversion
- 102 dB Dynamic Range
- -91 dB THD+N
- Low Clock Jitter Sensitivity
- Digital Volume Control with Soft Ramp
  - 119 dB Attenuation
  - 1-dB Step Size
  - Zero Crossing Click-Free Transitions
- ATAPI Mixing
- Logic Levels Between 5.0 V and 1.8 V
- +3.3 V or +5 V Analog Power Supply
- 116 mW with 3.3 V Supply
- Popguard Technology® for Control of Clicks and Pops

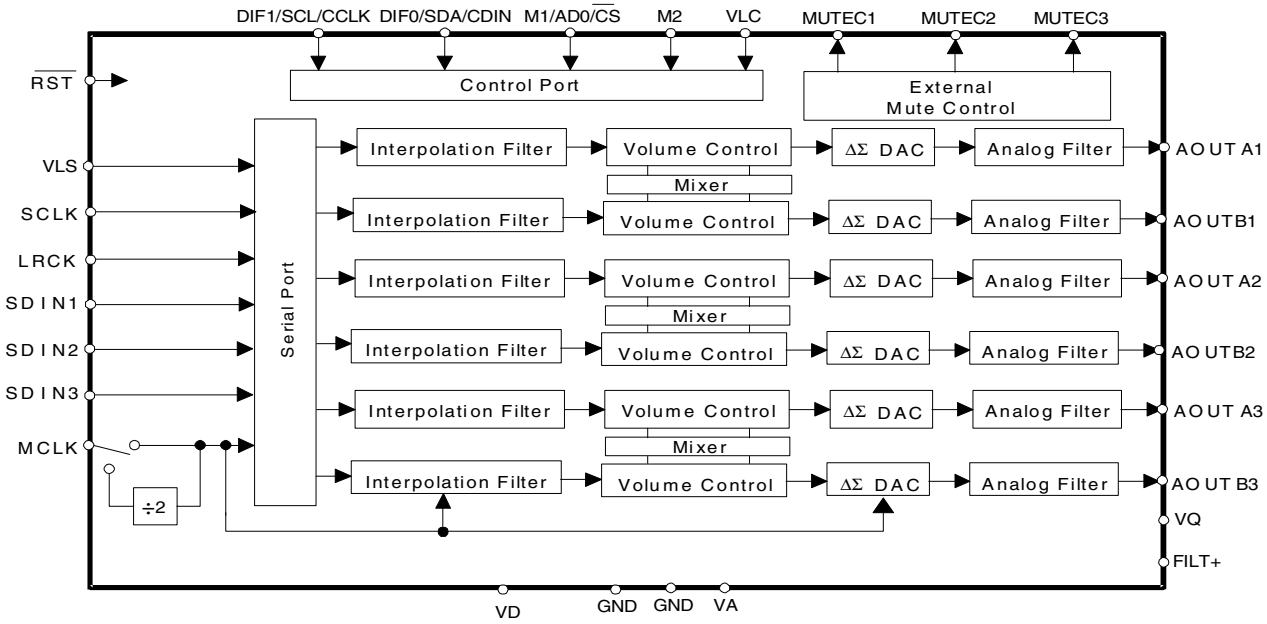
Description

The CS4360 is a complete 6-channel digital-to-analog system including digital interpolation, fourth-order delta-sigma digital-to-analog conversion, digital de-emphasis, volume control, channel mixing and analog filtering. The advantages of this architecture include: ideal differential linearity, no distortion mechanisms due to resistor matching errors, no linearity drift over time and temperature, and a high tolerance to clock jitter.

The CS4360 accepts data at audio sample rates from 4 kHz to 200 kHz, consumes very little power, and operates over a wide power supply range. These features are ideal for cost-sensitive, multi-channel audio systems including DVD players, A/V receivers, set-top boxes, digital TVs and VCRs, mini-component systems, and mixing consoles.

ORDERING INFORMATION

CS4360-KZ	-10 to 70 °C		28-pin TSSOP
CS4360-KZZ	-10 to 70 °C	Lead Free	28-pin TSSOP
CS4360-DZZ	-40 to 85 °C	Lead Free	28-pin TSSOP
CDB4360			Evaluation Board



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Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to **http://www.cirrus.com/**

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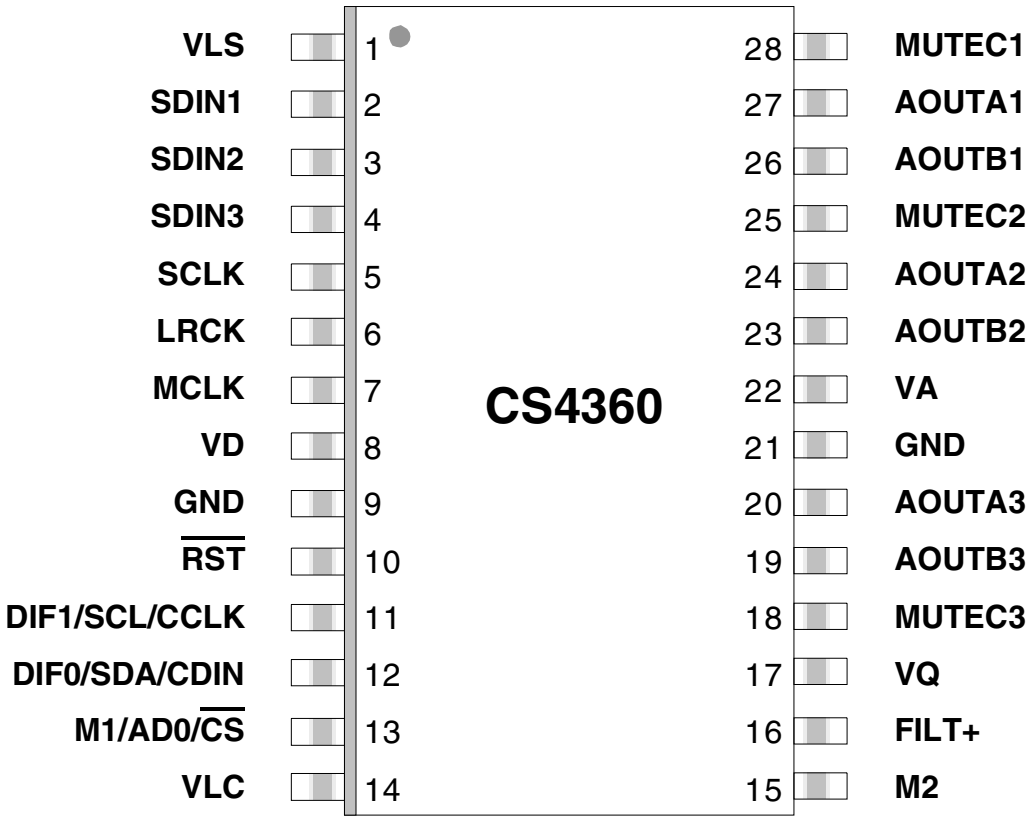
1. PIN DESCRIPTION



Pin Name	#	Pin Description
VLS	1	**Serial Audio Interface Power** (*Input*) **-** Positive power for the serial audio interface.
SDIN1 **SDIN2** **SDIN3**	2 3 4	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
SCLK	5	**Serial Clock** (*Input*) - Serial clock for the serial audio interface.
LRCK	6	**Left Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	7	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
VD	8	**Digital Power** (*Input*) **-** Positive power supply for the digital section.
GND	9 21	**Ground** (*Input*)
$\overline{\text{RST}}$	10	**Reset** (*Input*) - Powers down device and resets all internal resisters to their default settings.
VLC	14	**Control Port Interface Power** (*Input*) **-** Positive power for the control port interface.
FILT+	16	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.
VQ	17	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage.
VA	22	**Analog Power** (*Input*) **-** Positive power supply for the analog section.
AOUTB3 **AOUTA3** **AOUTB2** **AOUTA2** **AOUTB1** **AOUTA1**	19 20 23 24 26 27	**Analog Outputs** (*Output*) - The full scale analog line output level is specified in the *Analog Characteristics and Specifications* table.
MUTEC3 **MUTEC2** **MUTEC1**	18 25 28	**Mute Control** (*Output*) - Control signal for optional mute circuit.
Control Port Definitions		
SCL/CCLK	11	**Serial Control Port Clock** (*Input*) - Serial clock for the control port interface.
SDA/CDIN	12	**Serial Control Data I/O** (*Input/Output*) - Input/Output for I²C data. Input for SPI data.
AD0/$\overline{\text{CS}}$	13	**Address Bit / Chip Select** (*Input*) - Chip address bit in I²C Mode. Control signal used to select the chip in SPI mode.
Stand-Alone Definitions		
DIF1 **DIF0**	11 12	**Digital Interface Format** (*Input*) - Defines the required relationship between the Left Right Clock, Serial Clock and Serial Audio Data.
M1 **M2**	13 15	**Mode Selection** (*Input*) - Determines the operational mode of the device.

2. TYPICAL CONNECTION DIAGRAM

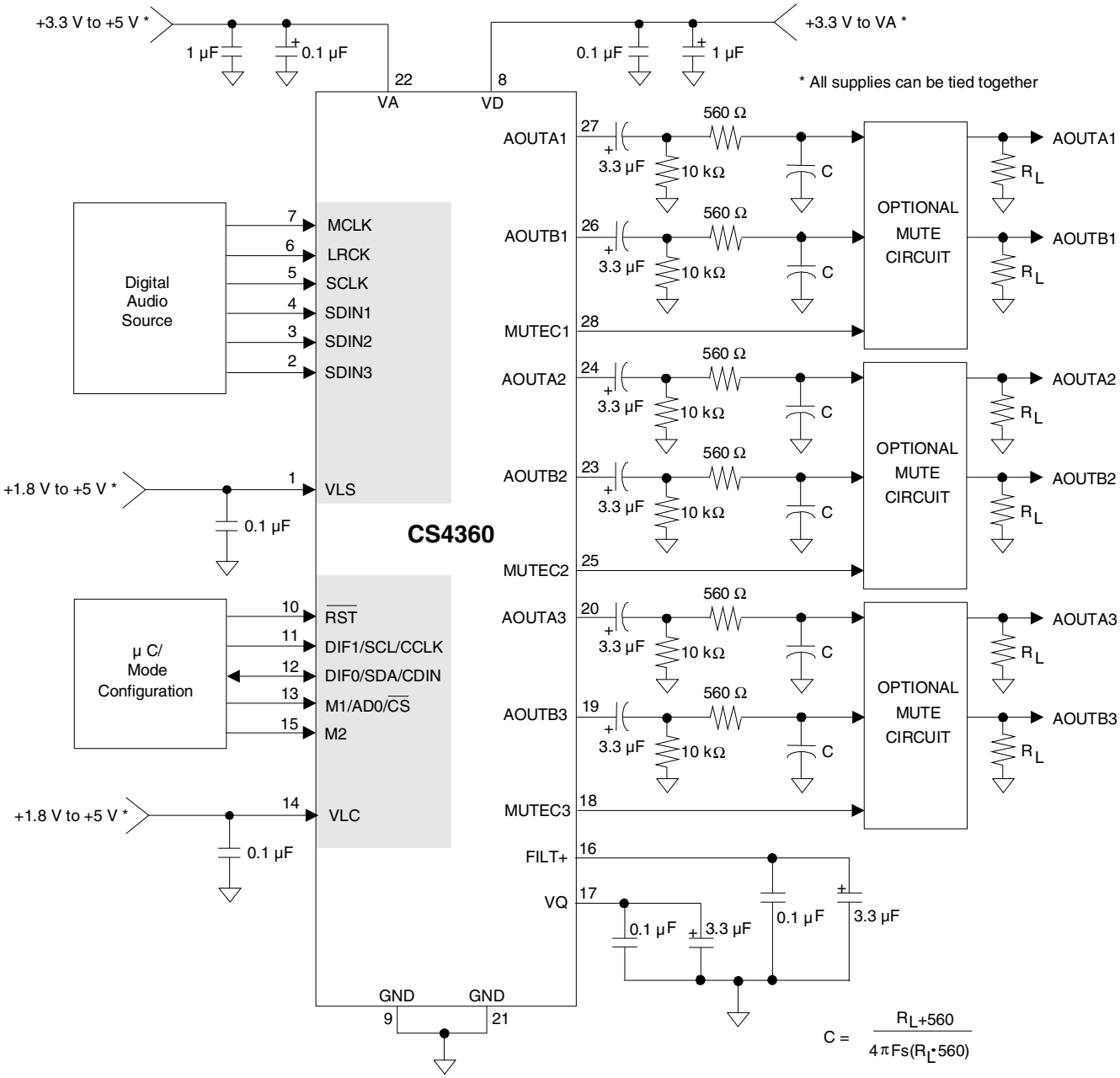


Figure 1. Typical Connection Diagram

3. CHARACTERISTICS AND SPECIFICATIONS

Typical performance characteristics are derived from measurements taken at T_A = 25°C. Min/Max performance characteristics and specifications are guaranteed over the operating temperature and voltages.

SPECIFIED OPERATING CONDITIONS

GND = 0 V; all voltages with respect to GND.

Parameters		Symbol	Min	Typ	Max	Units
DC Power Supply						
Analog	3.3 V Nominal	VA	3.0	3.3	3.6	V
(Note 1)	5.0 V Nominal		4.5	5	5.5	V
Digital	2.5 V Nominal	VD	2.25	2.5	2.75	V
(Note 1)	3.3 V Nominal		3.0	3.3	3.6	V
	5.0 V Nominal		4.5	5	5.5	V
Serial Audio Interface	1.8 V Nominal	VLS	1.7	1.8	1.9	V
	2.5 V Nominal		2.25	2.5	2.75	V
	3.3 V Nominal		3.0	3.3	3.6	V
	5.0 V Nominal		4.5	5	5.5	V
Control Port Interface	1.8 V Nominal	VLC	1.7	1.8	1.9	V
	2.5 V Nominal		2.25	2.5	2.75	V
	3.3 V Nominal		3.0	3.3	3.6	V
	5.0 V Nominal		4.5	5	5.5	V

ABSOLUTE MAXIMUM RATINGS

GND = 0 V; all voltages with respect to GND. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Parameters		Symbol	Min	Max	Units
DC Power Supply	Analog	VA	-0.3	6.0	V
	Digital	VD	-0.3	6.0	V
	Serial Audio Interface	VLS	-0.3	6.0	V
	Control Port Interface	VLC	-0.3	6.0	V
Input Current	(Note 2)	I_{in}	-	±10	mA
Digital Input Voltage	Serial Audio Interface	V_{IND_S}	-0.3	VLS+0.4	V
	Control Port Interface	V_{IND_C}	-0.3	VLC+0.4	V
Ambient Operating Temperature (power applied)		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Notes: 1. Nominal VD supply must be less than or equal to the nominal VA supply.

2. Any pin except supplies.

ANALOG CHARACTERISTICS (CS4360-KZ/KZZ)

Test conditions (unless otherwise specified): Input test signal is a 997 Hz sine wave at 0 dBFS; measurement bandwidth is 10 Hz to 20 kHz; test load R_L = 10 kΩ, C_L = 10 pF (see Figure 2). All supplies = VA = 5.0 V or 3.3 V.

Parameter		5.0 V Min	5.0 V Typ	5.0 V Max	3.3 V Min	3.3 V Typ	3.3 V Max	Unit
Single-Speed Mode	**Fs = 48 kHz**							
Dynamic Range	(Note 3)							
	unweighted	94	99	-	89	94	-	dB
	A-Weighted	97	102	-	92	97	-	dB
	A-Weighted	-	100	-	-	97	-	dB
Total Harmonic Distortion + Noise	(Note 3)							
	0 dB	-	-91	-86	-	-91	-86	dB
	-20 dB	-	-79	-	-	-74	-	dB
	-60 dB	-	-39	-	-	-34	-	dB
Double-Speed Mode	**Fs = 96 kHz**							
Dynamic Range	(Note 3)							
	unweighted	94	99	-	89	94	-	dB
	A-Weighted	97	102	-	92	97	-	dB
40 kHz Bandwidth	A-Weighted	-	100	-	-	97	-	dB
Total Harmonic Distortion + Noise	(Note 3)							
	0 dB	-	-91	-86	-	-91	-86	dB
	-20 dB	-	-79	-	-	-74	-	dB
	-60 dB	-	-39	-	-	-34	-	dB
Quad-Speed Mode	**Fs = 192 kHz**							
Dynamic Range	(Note 3)							
	unweighted	94	99	-	89	94	-	dB
	A-Weighted	97	102	-	92	97	-	dB
40 kHz Bandwidth	A-Weighted	-	100	-	-	97	-	dB
Total Harmonic Distortion + Noise	(Note 3)							
	0 dB	-	-91	-86	-	-91	-86	dB
	-20 dB	-	-79	-	-	-74	-	dB
	-60 dB	-	-39	-	-	-34	-	dB

Notes: 3. One-half LSB of triangular PDF dither is added to data.

ANALOG CHARACTERISTICS (CS4360-KZ/KZZ) (Continued)

Parameters		Symbol	Min	Typ	Max	Units
Dynamic Performance for All Modes						
Interchannel Isolation	(1 kHz)		-	102	-	dB
DC Accuracy						
Interchannel Gain Mismatch		ICGM	-	0.1	-	dB
Gain Drift			-	±100	-	ppm/°C
Analog Output Characteristics and Specifications						
Full Scale Output Voltage			0.60•VA	0.66•VA	0.72•VA	Vpp
Output Impedance		Z_{out}	-	100	-	Ω
Minimum AC-Load Resistance	(Note 4)	R_L	-	3	-	kΩ
Maximum Load Capacitance	(Note 4)	C_L	-	100	-	pF

4. Refer to Figure 3.

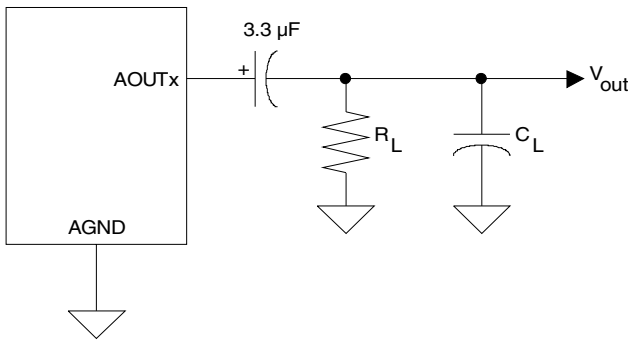


Figure 2. Output Test Load

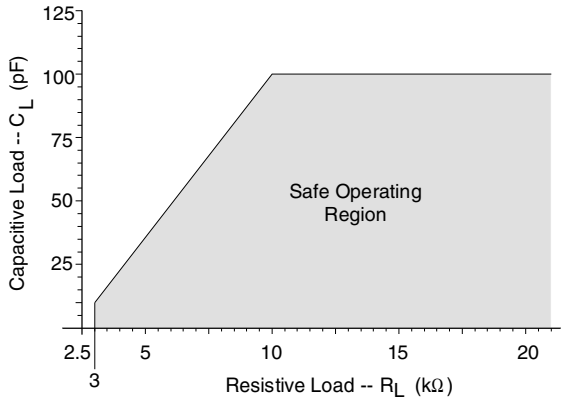


Figure 3. Maximum Loading

ANALOG CHARACTERISTICS (CS4360-DZZ)

Test conditions (unless otherwise specified): Input test signal is a 997 Hz sine wave at 0 dBFS; measurement bandwidth is 10 Hz to 20 kHz; test load R_L = 10 kΩ, C_L = 10 pF (see Figure 2). All supplies = VA = 5.0 V and 3.3 V.

Parameter		VA = 5.0 V			VA = 3.3 V			Unit
		Min	Typ	Max	Min	Typ	Max	
Single-speed Mode	**Fs = 48 kHz**							
Dynamic Range	(Note 3)							
	unweighted	89	99	-	89	94	-	dB
	A-Weighted	92	102	-	92	97	-	dB
	A-Weighted	-	100	-	-	97	-	dB
Total Harmonic Distortion + Noise	(Note 3)							
	0 dB	-	-91	-84	-	-91	-84	dB
	-20 dB	-	-79	-	-	-74	-	dB
	-60 dB	-	-39	-	-	-34	-	dB
Double-speed Mode	**Fs = 96 kHz**							
Dynamic Range	(Note 3)							
	unweighted	89	99	-	89	94	-	dB
	A-Weighted	92	102	-	92	97	-	dB
40 kHz Bandwidth	A-Weighted	-	100	-	-	97	-	dB
Total Harmonic Distortion + Noise	(Note 3)							
	0 dB	-	-91	-84	-	-91	-84	dB
	-20 dB	-	-79	-	-	-74	-	dB
	-60 dB	-	-39	-	-	-34	-	dB
Quad-speed Mode	**Fs = 192 kHz**							
Dynamic Range	(Note 3)							
	unweighted	89	99	-	89	94	-	dB
	A-Weighted	92	102	-	92	97	-	dB
40 kHz Bandwidth	A-Weighted	-	100	-	-	97	-	dB
Total Harmonic Distortion + Noise	(Note 3)							
	0 dB	-	-91	-84	-	-91	-84	dB
	-20 dB	-	-79	-	-	-74	-	dB
	-60 dB	-	-39	-	-	-34	-	dB

ANALOG CHARACTERISTICS (CS4360-DZZ) (Continued)

Parameters		Symbol	Min	Typ	Max	Units
Dynamic Performance for All Modes						
Interchannel Isolation	(1 kHz)		-	102	-	dB
DC Accuracy						
Interchannel Gain Mismatch		ICGM	-	0.1	-	dB
Gain Drift			-	±100	-	ppm/°C
Analog Output Characteristics and Specifications						
Full Scale Output Voltage			0.60•VA	0.66•VA	0.72•VA	Vpp
Output Impedance		Z_{out}	-	100	-	Ω
AC-load Resistance	(Note 4)	R_L	3	-	-	kΩ
Load Capacitance	(Note 4)	C_L	-	-	100	pF

COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

The filter characteristics and the X-axis of the response plots have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs.

Parameter		Min	Typ	Max	Unit
Single-Speed Mode (4 kHz to 50 kHz sample rates)					
Passband					
	to -0.05 dB corner	0	-	0.4535	Fs
	to -3 dB corner	0	-	0.4998	Fs
Frequency Response 10 Hz to 20 kHz		-0.02	-	+0.035	dB
StopBand		0.5465	-	-	Fs
StopBand Attenuation	(Note 5)	50	-	-	dB
Group Delay		-	9/Fs	-	s
De-emphasis Error (Relative to 1 kHz)	(Note 6)				
Control Port Mode	Fs = 32 kHz	-	-	+0.2/-0.1	dB
	Fs = 44.1 kHz	-	-	+0.05/-0.14	dB
	Fs = 48 kHz	-	-	+0/-0.22	dB
Stand-alone Mode	Fs = 32 kHz	-	-	+1.5/-0	dB
	Fs = 44.1 kHz	-	-	+0.05/-0.14	dB
	Fs = 48 kHz	-	-	+0.2/-0.4	dB
Double-Speed Mode (50 kHz to 100 kHz sample rates)					
Passband					
	to -0.1 dB corner	0	-	0.4621	Fs
	to -3 dB corner	0	-	0.4982	Fs
Frequency Response 10 Hz to 20 kHz		-0.1	-	0	dB
StopBand		0.577	-	-	Fs
StopBand Attenuation	(Note 5)	55	-	-	dB
Group Delay		-	4/Fs	-	s
Quad-Speed Mode - (100 kHz to 200 kHz sample rates)					
Passband					
	to -3 dB corner	0	-	0.25	Fs
Frequency Response 10 Hz to 20 kHz		-0.7	-	0	dB
Group Delay		-	1.5/Fs	-	s

Notes: 5. For Single-speed Mode, the measurement bandwidth is 0.5465 Fs to 3 Fs.
For Double-speed Mode, the measurement bandwidth is 0.577 Fs to 1.4 Fs.

6. De-emphasis is only available in Single-speed Mode.

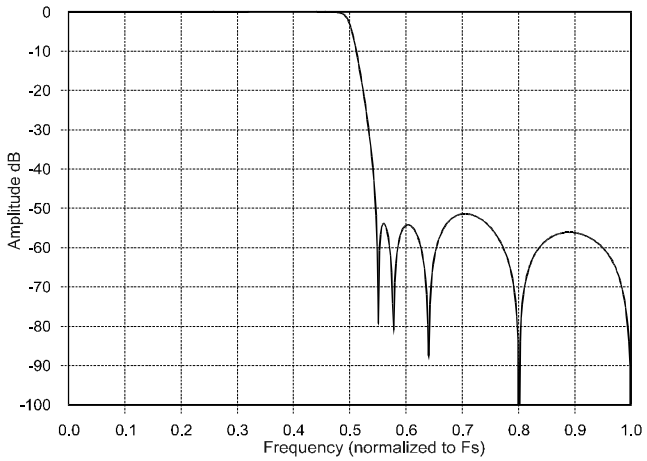


Figure 4. Single-speed Stopband Rejection

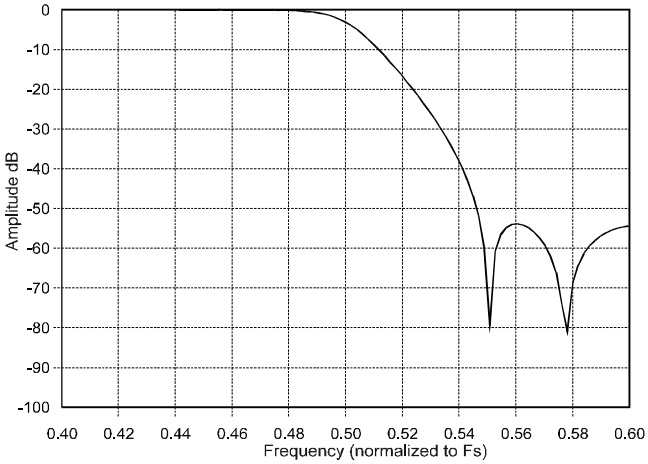


Figure 5. Single-speed Transition Band

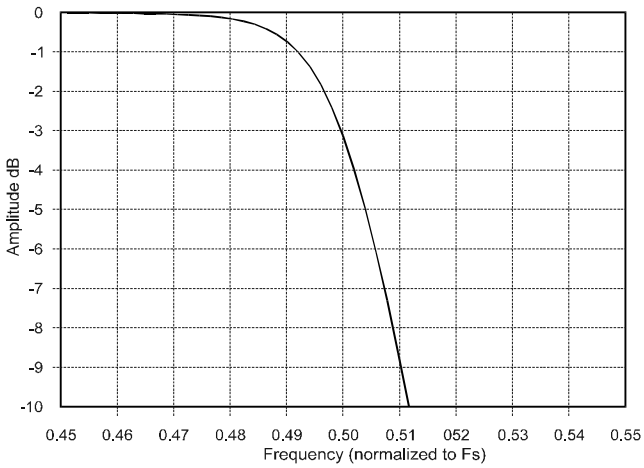


Figure 6. Single-speed Transition Band (Detail)

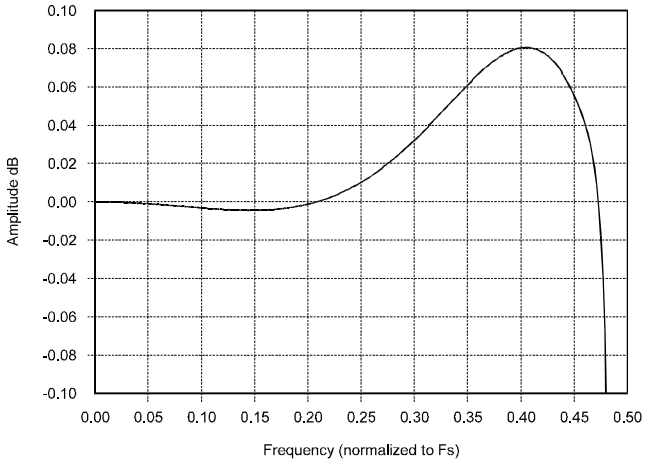


Figure 7. Single-speed Passband Ripple

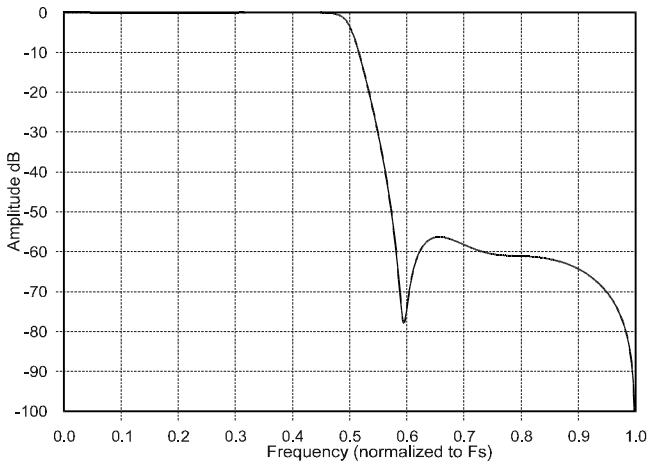


Figure 8. Double-speed Stopband Rejection

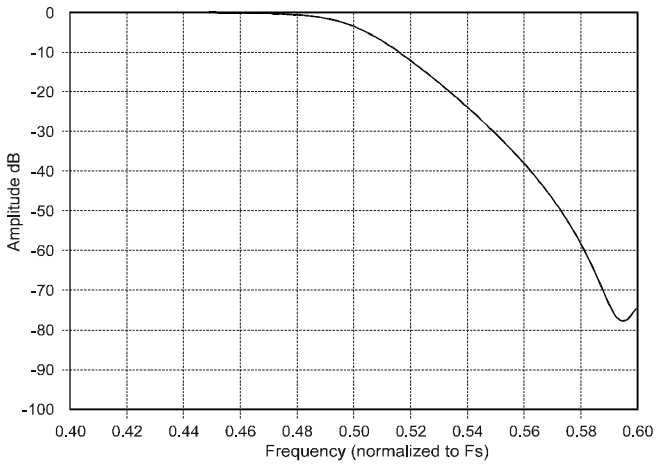


Figure 9. Double-speed Transition Band

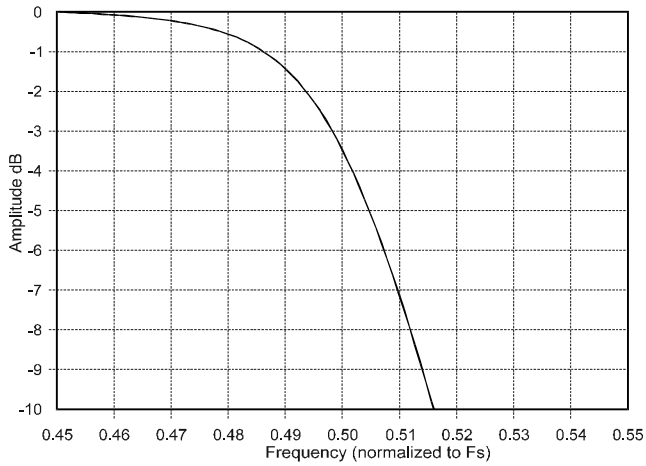


Figure 10. Double-speed Transition Band (Detail)

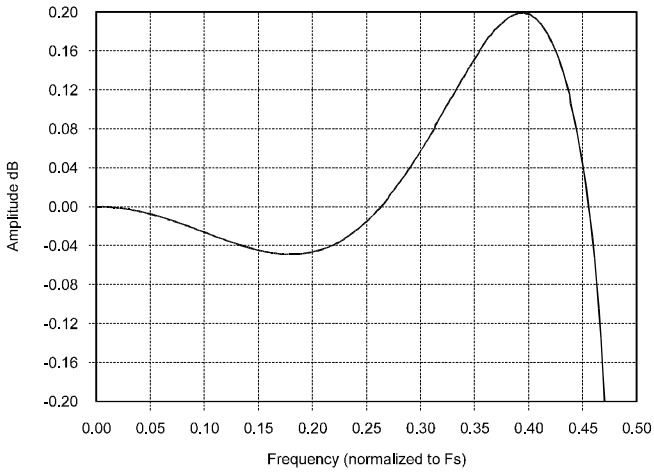


Figure 11. Double-speed Passband Ripple

SWITCHING SPECIFICATIONS - SERIAL AUDIO INTERFACE

Inputs: Logic 0 = GND, Logic 1 = VLS.

Parameters		Symbol	Min	Max	Units
MCLK Frequency			1.024	51.2	MHz
MCLK Duty Cycle			40	60	%
Input Sample Rate	Single-speed Mode	F_s	4	50	kHz
	Double-speed Mode	F_s	50	100	kHz
	Quad-speed Mode	F_s	100	200	kHz
LRCK Duty Cycle			45	55	%
SCLK Pulse Width Low		t_{sclkl}	20	-	ns
SCLK Pulse Width High		t_{sclkh}	20	-	ns
SCLK Frequency	Single-speed Mode		-	128xFs	Hz
	Double-speed Mode		-	64xFs	Hz
	Quad-speed Mode (MCLKDIV = 0)		-	$\frac{MCLK}{2}$	Hz
	Quad-speed Mode (MCLKDIV = 1)		-	$\frac{MCLK}{4}$	Hz
SCLK rising to LRCK edge delay		t_{slrd}	20	-	ns
SCLK rising to LRCK edge setup time		t_{slrs}	20	-	ns
SDINx valid to SCLK rising setup time		t_{sdlrs}	20	-	ns
SCLK rising to SDINx hold time		t_{sdh}	20	-	ns

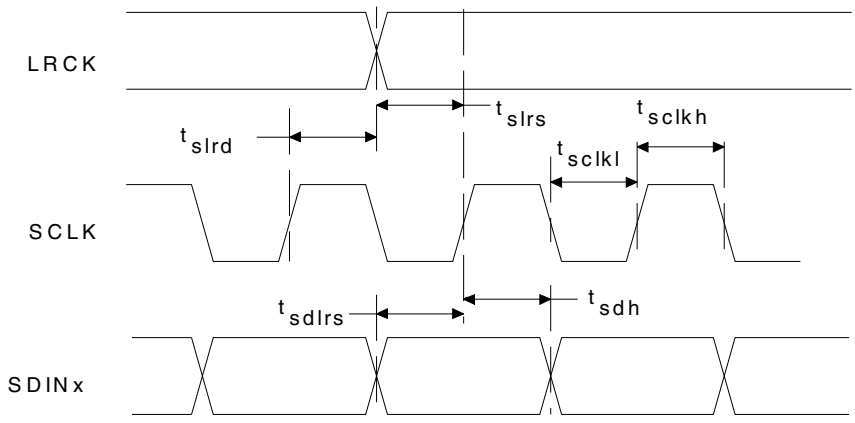


Figure 12. Serial Mode Input Timing

SWITCHING SPECIFICATIONS - CONTROL PORT INTERFACE

Inputs: Logic 0 = GND, Logic 1 = VLC

Parameter		Symbol	Min	Max	Unit
I²C Mode					
SCL Clock Frequency		f_{scl}	-	100	kHz
$\overline{RST}$ Rising Edge to Start		t_{irs}	500	-	ns
Bus Free Time Between Transmissions		t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)		t_{hdst}	4.0	-	µs
Clock Low time		t_{low}	4.7	-	µs
Clock High Time		t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition		t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling	(Note 7)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising		t_{sud}	250	-	ns
Rise Time of SCL and SDA		t_{rc}, t_{rc}	-	1	µs
Fall Time SCL and SDA		t_{fc}, t_{fc}	-	300	ns
Setup Time for Stop Condition		t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	(Note 8)	t_{ack}	-	(Note 9)	ns

Notes: 7. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

8. The acknowledge delay is based on MCLK and can limit the maximum transaction speed.

9. $\frac{5}{256 \times Fs}$ for Single-Speed Mode, $\frac{5}{128 \times Fs}$ for Double-Speed Mode, $\frac{5}{64 \times Fs}$ for Quad-Speed Mode.

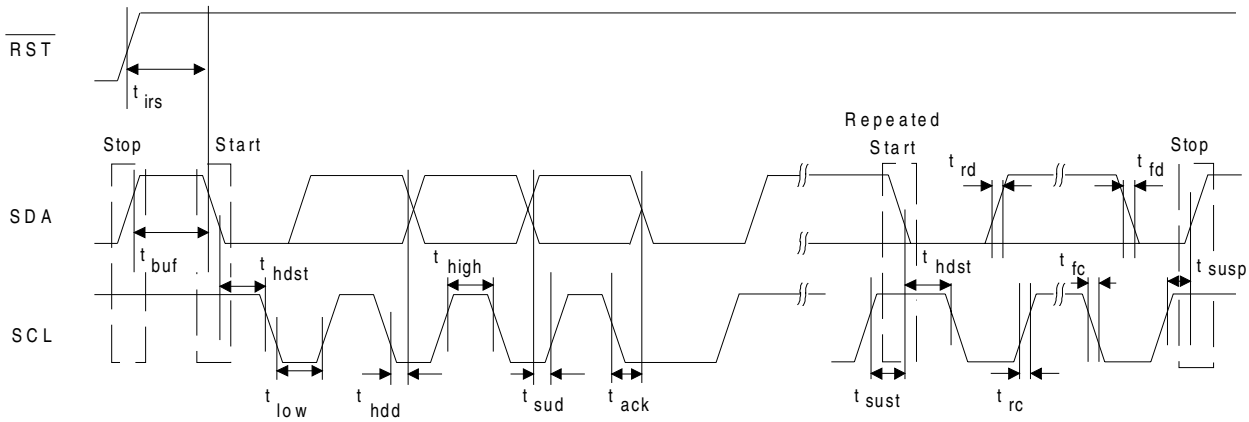


Figure 13. Control Port Timing - I²C Mode

SWITCHING SPECIFICATIONS - CONTROL PORT INTERFACE (Continued)

Parameter		Symbol	Min	Max	Unit
SPI Mode					
CCLK Clock Frequency		f_{sclk}	-	6	MHz
$\overline{RST}$ Rising Edge to $\overline{CS}$ Falling		t_{srs}	500	-	ns
CCLK Edge to $\overline{CS}$ Falling	(Note 10)	t_{spi}	500	-	ns
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	$\frac{1}{MCLK}$	-	ns
CCLK High Time		t_{sch}	$\frac{1}{MCLK}$	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 11)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN	(Note 12)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 12)	t_{f2}	-	100	ns

Notes: 10. t_{spi} only needed before first falling edge of $\overline{CS}$ after $\overline{RST}$ rising edge. t_{spi} = 0 at all other times.

11. Data must be held for sufficient time to bridge the transition time of CCLK.

12. For f_{sclk} < 1 MHz.

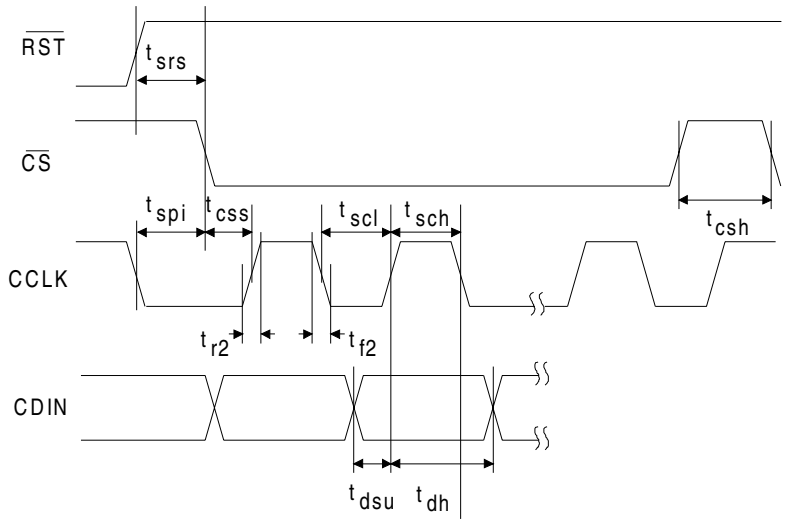


Figure 14. Control Port Timing - SPI Mode

DC ELECTRICAL CHARACTERISTICS GND = 0 V; all voltages with respect to GND.

Parameters		Symbol	Min	Typ	Max	Units
Normal Operation (Note 13)						
Power Supply Current	VA = 5.0 V	I_A	-	22	-	mA
	VD = 5.0 V	I_D	-	25	-	mA
	VA = 3.3 V	I_A	-	21	-	mA
	VD = 3.3 V	I_D	-	14	-	mA
	VLS = 5.0 V	I_{LS}	-	6	-	µA
	VLC = 5.0 V	I_{LC}	-	2	-	µA
	VLS = 3.3 V	I_{LS}	-	2	-	µA
	VLC = 3.3 V (Note 14)	I_{LC}	-	1	-	µA
Power Dissipation	All Supplies = 5.0 V		-	235	265	mW
	All Supplies = 3.3 V		-	116	128	mW
Power-down Mode (Note 15)						
Power Supply Current	All Supplies = 5.0 V		-	16	-	µA
	All Supplies = 3.3 V		-	12	-	µA
Power Dissipation	All Supplies = 5.0 V		-	80	-	µW
	All Supplies = 3.3 V		-	40	-	µW
All Modes of Operation						
Power Supply Rejection Ratio (Note 16)	1 kHz	PSRR	-	60	-	dB
	60 Hz		-	40	-	dB
V_Q Nominal Voltage			-	0.5•VA	-	V
Output Impedance			-	250	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA
Filt+ Nominal Voltage			-	VA	-	V
Output Impedance			-	250	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA
MUTEC Low-level Output Voltage			-	0	-	V
MUTEC High-level Output Voltage			-	VA	-	V
Maximum MUTEC Drive Current			-	3	-	mA

Notes: 13. Normal operation is defined as $\overline{RST}$ = HI with a 997 Hz, 0 dBFS input sampled at the highest F_s for each speed mode, and open outputs, unless otherwise specified.

14. I_{LC} measured with no external loading on pin 12 (SDA).

15. Power Down Mode is defined as $\overline{RST}$ = LO with all clocks and data lines held static.

16. Valid with the recommended capacitor values on FILT+ and VQ as shown in Figure 1. Increasing the capacitance will also increase the PSRR.

DIGITAL INPUT CHARACTERISTICS GND = 0 V; all voltages with respect to GND.

Parameters	Symbol	Min	Typ	Max	Units
Input Leakage Current	I_{in}	-	-	±10	µA
Input Capacitance		-	8	-	pF

DIGITAL INTERFACE SPECIFICATIONS

GND = 0 V; all voltages with respect to GND.

Parameters		Symbol	Min	Max	Units
1.8 V Logic					
High-level Input Voltage	Serial Audio	V_{IH}	80%	-	VLS
	Control Port	V_{IH}	80%	-	VLC
Low-level Input Voltage	Serial Audio	V_{IL}	-	13%	VLS
	Control Port	V_{IL}		13%	VLC
2.5 V Logic					
High-level Input Voltage	Serial Audio	V_{IH}	70%	-	VLS
	Control Port	V_{IH}	70%	-	VLC
Low-level Input Voltage	Serial Audio	V_{IL}	-	13%	VLS
	Control Port	V_{IL}		13%	VLC
3.3 V Logic					
High-level Input Voltage	Serial Audio	V_{IH}	70%	-	VLS
	Control Port	V_{IH}	70%	-	VLC
Low-level Input Voltage	Serial Audio	V_{IL}	-	13%	VLS
	Control Port	V_{IL}		13%	VLC
5.0 V Logic					
High-level Input Voltage	Serial Audio	V_{IH}	70%	-	VLS
	Control Port	V_{IH}	70%	-	VLC
Low-level Input Voltage	Serial Audio	V_{IL}	-	13%	VLS
	Control Port	V_{IL}		13%	VLC

THERMAL CHARACTERISTICS AND SPECIFICATIONS

Parameters		Symbol	Min	Typ	Max	Units
Package Thermal Resistance	TSSOP (-KZ/KZZ & -DZZ)	θ_{JA}	-	40	-	°C/Watt
Ambient Operating Temperature (Power Applied)	-KZ/KZZ	T_A	-10	-	+70	°C
	-DZZ		-40	-	+85	°C

4. APPLICATIONS

4.1 Sample Rate Range/Operational Mode Select

4.1.1 Stand-Alone Mode

The device operates in one of four operational modes determined by the Mode pins in Stand-alone mode. Sample rates outside the specified range for each mode are not supported.

M2	M1	Input Sample Rate (F_S)	MODE
0	0	4 kHz - 50 kHz	Single-Speed (without De-emphasis)
0	1	32 kHz - 48 kHz	Single-Speed (with De-emphasis)
1	0	50 kHz - 100 kHz	Double-Speed
1	1	100 kHz - 200 kHz	Quad-Speed

Table 1. CS4360 Stand-Alone Operational Mode

4.1.2 Control Port Mode

The device operates in one of three operational modes determined by the FM bits (see section 6.1.4) in Control Port mode. Sample rates outside the specified range for each mode are not supported.

FM1	FM0	Input Sample Rate (F_S)	MODE
0	0	4 kHz - 50 kHz	Single-speed
0	1	50 kHz - 100 kHz	Double-speed
1	0	100 kHz - 200 kHz	Quad-speed
1	1	Reserved	Reserved

Table 2. CS4360 Control Port Operational Mode

4.2 System Clocking

The device requires external generation of the master (MCLK), left/right (LRCK) and serial (SCLK) clocks. The LRCK, defined also as the input sample rate (F_s), must be synchronously derived from the MCLK according to specified ratios. The specified ratios of MCLK to LRCK, along with several standard audio sample rates and the required MCLK frequency, are illustrated in Tables 3-5.

Sample Rate (kHz)	MCLK (MHz)				
	256x	384x	512x	768x	1024x*
32	8.1920	12.2880	16.3840	24.5760	32.7680
44.1	11.2896	16.9344	22.5792	33.8688	45.1584
48	12.2880	18.4320	24.5760	36.8640	49.1520

Table 3. Single-speed Mode Standard Frequencies

Sample Rate (kHz)	MCLK (MHz)				
	128x	192x	256x	384x	512x*
64	8.1920	12.2880	16.3840	24.5760	32.7680
88.2	11.2896	16.9344	22.5792	33.8688	45.1584
96	12.2880	18.4320	24.5760	36.8640	49.1520

Table 4. Double-speed Mode Standard Frequencies

Sample Rate (kHz)	MCLK (MHz)				
	64x	96x	128x	192x	256x*
176.4	11.2896	16.9344	22.5792	33.8688	45.1584
192	12.2880	18.4320	24.5760	36.8640	49.1520

Table 5. Quad-speed Mode Standard Frequencies

*Requires MCLKDIV bit = 1 in the Mode Control 2 register (address 0Ch)

4.3 Digital Interface Format

The device will accept audio samples in 1 of 4 digital interface formats in Stand-alone mode, as illustrated in Table 6, and 1 of 6 formats in Control Port mode, as illustrated in Table 8.

4.3.1 Stand-Alone Mode

The desired format is selected via the DIF1 and DIF0 pins. For an illustration of the required relationship between the LRCK, SCLK and SDIN, see Figures 15-17.

DIF1	DIF0	DESCRIPTION	FORMAT	FIGURE
0	0	Left Justified, up to 24-bit Data	0	16
0	1	I^2S, up to 24-bit Data	1	15
1	0	Right Justified, 16-bit Data	2	17
1	1	Right Justified, 24-bit Data	3	17

Table 6. Digital Interface Format - Stand-alone Mode

4.3.2 Control Port Mode

The desired format is selected via the DIF2, DIF1 and DIF0 bits in the Mode Control 2 register (see section 6.1.2). For an illustration of the required relationship between LRCK, SCLK and SDIN, see Figures 15-17.

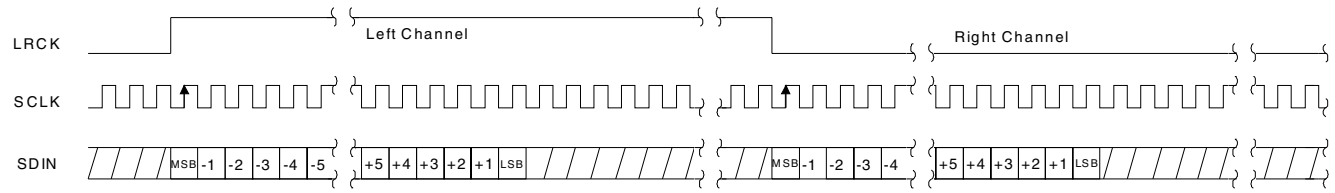


Figure 15. Left Justified up to 24-Bit Data

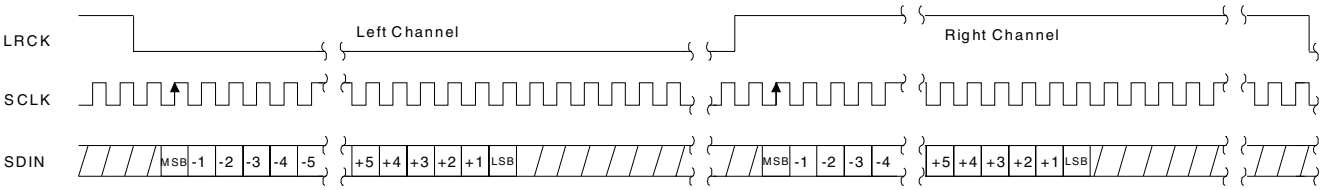


Figure 16. I²S, up to 24-Bit Data

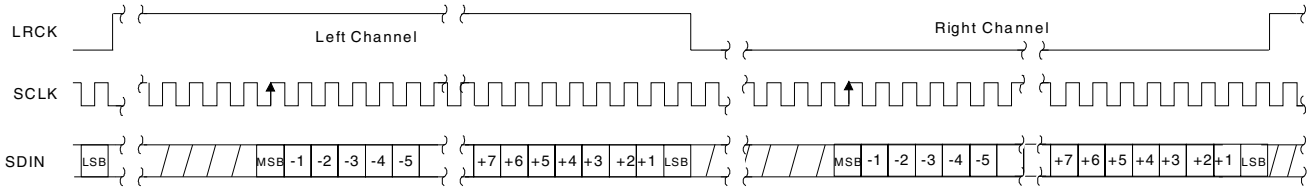


Figure 17. Right Justified Data

4.4 De-Emphasis Control

The device includes on-chip digital de-emphasis. Figure 18 shows the de-emphasis curve for F_s equal to 44.1 kHz. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, Fs.

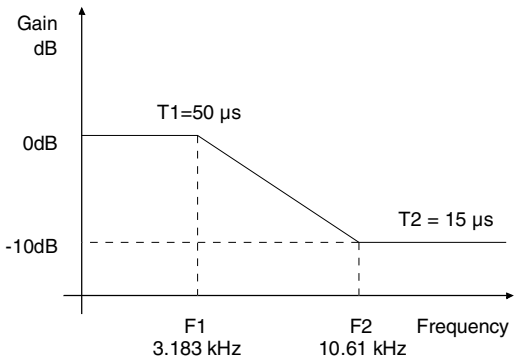


Figure 18. De-emphasis Curve

Notes: De-emphasis is only available in Single-speed Mode.

4.4.1 Stand-Alone Mode

The operational mode pins, M2 and M1, selects the 44.1 kHz de-emphasis filter. Please see section 4.1 for the desired de-emphasis control.

4.4.2 Control Port Mode

The Mode Control bits selects either the 32, 44.1, or 48 kHz de-emphasis filter. Please see section 6.1.3 for the desired de-emphasis control.

4.5 Recommended Power-up Sequence

4.5.1 Stand-Alone Mode

1) Hold $\overline{\text{RST}}$ low until the power supply and configuration pins are stable, and the master and left/right clocks are locked to the appropriate frequencies, as discussed in section 4.2. In this state, the control port is reset to its default settings and VQ will remain low.
2) Bring $\overline{\text{RST}}$ high. The device will remain in a low power state with VQ low and will initiate the Stand-alone power-up sequence after approximately 512 LRCK cycles in Single-Speed Mode (1024 LRCK cycles in Double-Speed Mode, and 2048 LRCK cycles in Quad-Speed Mode).

4.5.2 Control Port Mode

1) Hold $\overline{\text{RST}}$ low until the power supply is stable, and the master and left/right clocks are locked to the appropriate frequencies, as discussed in section 4.2. In this state, the control port is reset to its default settings and VQ will remain low.
2) Bring $\overline{\text{RST}}$ high. The device will remain in a low power state with VQ low.
3) Load the desired register settings while keeping the PDN bit set to 1.
4) Set the PDN bit to 0. This will initiate the power-up sequence, which lasts approximately 50 µS when the POPG bit is set to 0. If the POPG bit is set to 1, see Section 4.6 for a complete description of power-up timing.

4.6 Popguard® Transient Control

The CS4360 uses a novel technique to minimize the effects of output transients during power-up and power-down. This technology, when used with external DC-blocking capacitors in series with the audio outputs, minimizes the audio transients commonly produced by single-ended single-supply converters. It is activated inside the DAC when the $\overline{\text{RST}}$ pin or PDN bit is enabled/disabled and requires no other external control, aside from choosing the appropriate DC-blocking capacitors.

4.6.1 Power-up

When the device is initially powered-up, the audio outputs, AOUTAx and AOUTBx, are clamped to GND. Following a delay of approximately 1000 LRCK cycles, each output begins to ramp toward the quiescent voltage. Approximately 10,000 LRCK cycles later, the outputs reach V_Q and audio output begins. This gradual voltage ramping allows time for the external DC-blocking capacitors to charge to the quiescent voltage, minimizing the power-up transient.

4.6.2 Power-down

To prevent transients at power-down, the device must first enter its power-down state. When this occurs, audio output ceases and the internal output buffers are disconnected from AOUTAx and AOUTBx. In their place, a soft-start current sink is substituted which allows the DC-blocking capacitors to slowly discharge. Once this charge is dissipated, the power to the device may be turned off and the system is ready for the next power-on.

4.6.3 Discharge Time

To prevent an audio transient at the next power-on, the DC-blocking capacitors must fully discharge before turning on the power or exiting the power-down state. If full discharge does not occur, a transient will occur when the audio outputs are initially clamped to GND. The time that the device must remain in the power-down state is related to the value of the DC-blocking capacitance and the output load. For example, with a 3.3 µF capacitor, the minimum power-down time will be approximately 0.4 seconds.

4.7 Mute Control

The Mute Control pins go high during power-up initialization, reset, muting (see section 6.1.1 and 6.4.1), or if the MCLK to LRCK ratio is incorrect. These pins are intended to be used as control for external mute circuits to prevent the clicks and pops that can occur in any single-ended single supply system.

Use of the Mute Control function is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the Mute Control function can enable the system designer to achieve idle channel noise/signal-to-noise ratios which are only limited by the external mute circuit. Please see the CDB4360 data sheet for a suggested mute circuit.

4.8 Grounding and Power Supply Arrangements

As with any high-resolution converter, the CS4360 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements, with VA, VD, VLS and VLC connected to clean supplies. If the ground planes are split between digital ground and analog ground, the GND pins of the CS4360 should be connected to the analog ground plane.

All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The CDB4360 evaluation board demonstrates the optimum layout and power supply arrangements.

4.8.1 Capacitor Placement

Decoupling capacitors should be placed as close to the DAC as possible, with the low-value ceramic capacitor being the closest. To further minimize impedance, these capacitors should be located on the same layer as the DAC. If desired, all supply pins may be connected to the same supply, but a decoupling capacitor should still be placed on each supply pin and referenced to analog ground.

4.8.2 Power Supply Sections

Each power supply pin provides power to specific sections of the CS4360. The logic voltage level for each section must adhere to the corresponding power supply voltage setting. For example: If VLC = 1.8 V; VLS = 3.3 V; VD = VA = 5 V; then the logic level for all mode configuration inputs must equal 1.8 V.

Pin #s	Description	Power Supply Reference
2, 3, 4, 5, 6, 7	Serial Audio Interface Inputs	VLS
10, 11, 12, 13, 15	Mode Configuration Inputs	VLC

Table 7. Power Supply Control Sections

4.9 Control Port Interface

The control port is used to load all the internal register settings (see section 6). The operation of the control port may be completely asynchronous with the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port operates in one of two modes: I²C or SPI.

Notes: MCLK must be applied during all I²C communication.