Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

CS4361

20-Pin, 24-Bit, 192 kHz, 6-Channel D/A Converter

Features

- Multi-Bit Delta-Sigma Modulator
- 24-Bit Conversion
- Automatically Detects Sample Rates Up To 192 kHz
- 103 dB Dynamic Range
- -94 dB THD+N
- Low Clock-Jitter Sensitivity
- +5 V Core Power
- +1.8 V to +5 V Interface Power
- Filtered Line-Level Outputs
- On-Chip Digital De-emphasis
- Popguard® Technology
- Mute Output Control
- Small 20-pin TSSOP Package

Description

The CS4361 is a complete 6-channel digital-to-analog output system including interpolation, multi-bit D/A conversion, and output analog filtering in a small 20-pin package. The CS4361 supports all major audio data interface formats.

The CS4361 is based on a fourth-order, multi-bit, delta-sigma modulator with a linear analog low-pass filter. This device also includes auto-speed mode detection using both sample rate and master clock ratio as a method of auto-selecting sampling rates between 2 kHz and 216 kHz.

The CS4361 contains on-chip digital de-emphasis, operates from a single +5 V power supply with separate built-in level shifter for the digital interface, and requires minimal support circuitry. These features are ideal for DVD players and recorders, digital televisions, home theater and set-top box products, and automotive audio systems.

The CS4361 is available in a 20-pin TSSOP Commercial grade package (-40 to 85° C). The CDB4361 is also available for device evaluation and implementation suggestions. Please refer to "Ordering Information" on page 23 for complete ordering information.

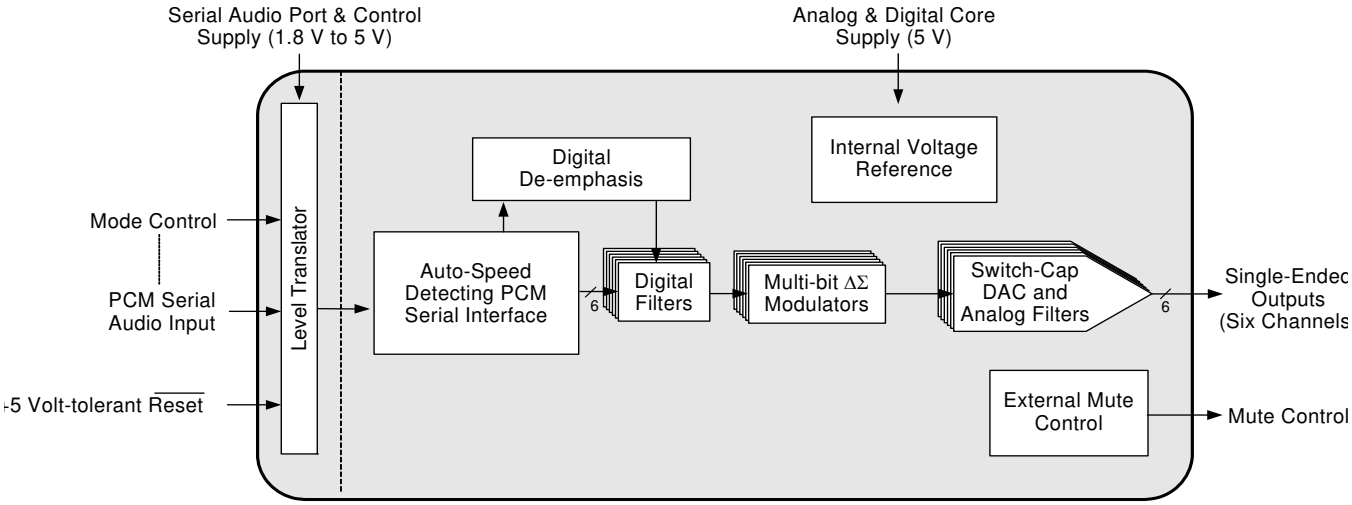


TABLE OF CONTENTS

1. PIN DESCRIPTIONS 4
2. CHARACTERISTICS AND SPECIFICATIONS 5
RECOMMENDED OPERATING CONDITIONS 5
ABSOLUTE MAXIMUM RATINGS 5
DAC ANALOG CHARACTERISTICS - COMMERCIAL (-CZZ) 6
COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE 7
DIGITAL INPUT CHARACTERISTICS 8
POWER & THERMAL CHARACTERISTICS 8
SWITCHING CHARACTERISTICS - SERIAL AUDIO INTERFACE 9
3. TYPICAL CONNECTION DIAGRAM 11
4. APPLICATIONS 12
4.1 Master Clock 12
4.2 Serial Clock 12
4.2.1 External Serial Clock Mode 12
4.2.2 Internal Serial Clock Mode 12
4.3 De-Emphasis 14
4.4 Mode Select 14
4.5 Initialization and Power-Down 15
4.6 Output Transient Control 16
4.6.1 Power-Up 16
4.6.2 Power-Down 16
4.7 Grounding and Power Supply Decoupling 16
4.8 Analog Output and Filtering 16
4.9 Mute Control 17
5. PERFORMANCE PLOTS 18
6. PARAMETER DEFINITIONS 21
7. PACKAGE INFORMATION 22
8. ORDERING INFORMATION 23
9. REVISION HISTORY 24

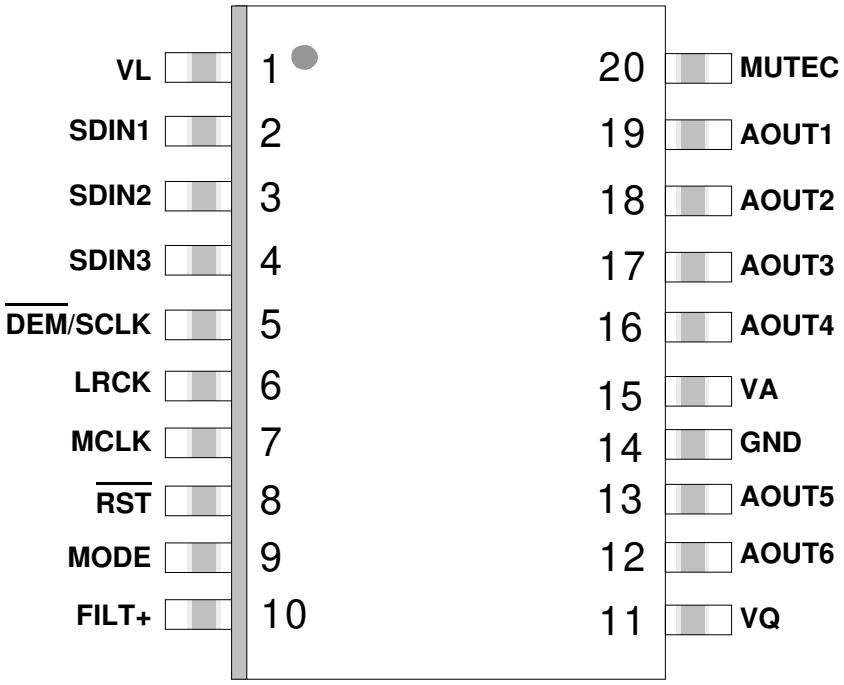
LIST OF FIGURES

Figure 1.Equivalent Output Test Load 8
Figure 2.Maximum Loading 8
Figure 3.External Serial Mode Input Timing 10
Figure 4.Internal Serial Mode Input Timing 10
Figure 5. Internal Serial Clock Generation 10
Figure 6.Recommended Connection Diagram 11
Figure 7.CS4361 Data Format (I²S) 13
Figure 8.CS4361 Data Format (Left-Justified) 13
Figure 9.CS4361 Data Format (Right-Justified 24) 13
Figure 10.CS4361 Data Format (Right-Justified 16) 14
Figure 11.De-Emphasis Curve (Fs = 44.1kHz) 14
Figure 12.CS4361 Initialization and Power-Down Sequence 15
Figure 13.Suggested Active-Low Mute Circuit 17
Figure 14.Single-Speed Stopband Rejection 18
Figure 15.Single-Speed Transition Band 18
Figure 16.Single-Speed Transition Band 18
Figure 17.Single-Speed Passband Ripple 18
Figure 18.Double-Speed Stopband Rejection 19
Figure 19.Double-Speed Transition Band 19
Figure 20.Double-Speed Transition Band 19
Figure 21.Double-Speed Passband Ripple 19
Figure 22.Quad-Speed Stopband Rejection 20
Figure 23.Quad-Speed Transition Band 20
Figure 24.Quad-Speed Transition Band 20
Figure 25.Quad-Speed Passband Ripple 20

LIST OF TABLES

Table 1. Common Clock Frequencies 12
Table 2. Mode Pin Settings 14

1. PIN DESCRIPTIONS



Pin Name	#	Pin Description
SDIN1 SDIN2 SDIN3	2 3 4	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
$\overline{\text{DEM}}$/SCLK	5	**De-emphasis/External Serial Clock Input** (*Input*) - used for de-emphasis filter control or external serial clock input.
LRCK	6	**Left Right Clock** (Input) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	7	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
VQ	11	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage.
FILT+	10	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.
AOUT1 AOUT2 AOUT3 AOUT4 AOUT5 AOUT6	19 18 17 16 13 12	**Analog Output** (Output) - The full scale analog output level is specified in the Analog Characteristics specification table.
GND	14	**Ground** (*Input*) - ground reference.
VA	15	**Analog Power** (*Input*) **-** Positive power for the analog and core digital sections.
VL	1	**Interface Power** (*Input*) **-** Positive power for the digital interface level shifters.
$\overline{\text{RST}}$	8	**$\overline{\text{Reset}}$** (*Input*) **-** Applies reset to the internal circuitry when low.
MUTEC	20	**Mute Control** (*Output*) **-** Control signal for optional external muting circuitry.
MODE	9	**Mode Control** (*Input*) **-** Selects operational modes (see Table 2).

2. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

AGND = 0 V; all voltages with respect to ground.

Parameters	Symbol	Min	Nom	Max	Units
DC Power Supply	VA	4.75	5.0	5.25	V
	VL	1.7	3.3	5.25	V
Specified Temperature Range Commercial	T_A	-40	-	+85	°C

ABSOLUTE MAXIMUM RATINGS

AGND = 0 V; all voltages with respect to ground.

Parameters	Symbol	Min	Max	Units
DC Power Supply	VA	-0.3	6.0	V
	VL	-0.3	VA	V
Input Current, Any Pin Except Supplies	I_{in}	-	±10	mA
Digital Input Voltage (pin 8, $\overline{RST}$)	V_{IND}	-0.3	VA+0.4	V
Digital Input Voltage (all other digital pins)	V_{IND}	-0.3	VL+0.4	V
Ambient Operating Temperature (power applied)	T_{op}	-55	125	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

DAC ANALOG CHARACTERISTICS - COMMERCIAL

Test Conditions (unless otherwise specified). VA = 5.0 V, VL = 3.3 V, and T_A = 25° C. Full-scale input sine wave. Measurement Bandwidth is 10 Hz to 20 kHz. See (Note 1). Specifications apply to all channels unless otherwise indicated.

Parameter			Min	Typ	Max	Unit
Dynamic Performance						
Dynamic Range	18 to 24-Bit	A-weighted	99	103	-	dB
		unweighted	96	100	-	dB
	16-Bit	A-weighted	90	96	-	dB
		unweighted	87	93	-	dB
Total Harmonic Distortion + Noise						
	18 to 24-Bit	Ch. 1-2, 0 dB	-	-93	-86	dB
		Ch. 3-4, 0 dB	-	-90	-83	dB
		Ch. 5-6, 0 dB	-	-94	-87	dB
		-20 dB	-	-80	-76	dB
		-60 dB	-	-40	-36	dB
	16-Bit	Ch. 1-2, 0 dB	-	-92	-85	dB
		Ch. 3-4, 0 dB	-	-89	-82	dB
		Ch. 5-6, 0 dB	-	-93	-86	dB
		-20 dB	-	-73	-67	dB
		-60 dB	-	-33	-27	dB

DAC Analog Characteristics - All Modes					
Parameter	Symbol	Min	Typ	Max	
Interchannel Isolation (1 kHz)		-	100	-	dB
DC Accuracy					
Interchannel Gain Mismatch		-	0.1	0.25	dB
Gain Drift		-	100	-	ppm/°C
Analog Output					
Full Scale Output Voltage		0.60•VA	0.65•VA	0.70•VA	Vpp
Quiescent Voltage	V_Q	-	0.5•VA	-	VDC
Max DC Current draw from an AOUT pin	I_{OUTmax}	-	10	-	µA
Max Current draw from VQ	I_{Qmax}	-	100	-	µA
Min AC-Load Resistance (see Figure 2)	R_L	-	3	-	kΩ
Max Load Capacitance (see Figure 2)	C_L	-	100	-	pF
Output Impedance	Z_{OUT}	-	100	-	Ω

Notes:

1. One LSB of triangular PDF dither added to data.

COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

The filter characteristics have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs. (See Note 5)

Parameter		Symbol	Min	Typ	Max	Unit
Single-Speed Mode						
Passband (Note 2)	to -0.05 dB corner to -3 dB corner		0 0	- -	.4780 .4996	Fs Fs
Frequency Response 10 Hz to 20 kHz			-.01	-	+.08	dB
StopBand			.5465	-	-	Fs
StopBand Attenuation	(Note 3)		50	-	-	dB
Group Delay		tgd	-	10/Fs	-	s
De-emphasis Error (Note 4)	Fs = 44.1 kHz		-	-	+.05/-.25	dB
Double-Speed Mode						
Passband (Note 2)	to -0.1 dB corner to -3 dB corner		0 0	- -	.4650 .4982	Fs Fs
Frequency Response 10 Hz to 20 kHz			-.05	-	+.2	dB
StopBand			.5770	-	-	Fs
StopBand Attenuation	(Note 3)		55	-	-	dB
Group Delay		tgd	-	5/Fs	-	s
Quad-Speed Mode						
Passband (Note 2)	to -0.1 dB corner to -3 dB corner		0 0	- -	0.397 0.476	Fs Fs
Frequency Response 10 Hz to 20 kHz			0	-	+0.00004	dB
StopBand			0.7	-	-	Fs
StopBand Attenuation	(Note 3)		51	-	-	dB
Group Delay		tgd	-	2.5/Fs	-	s

2. Response is clock-dependent and will scale with Fs.
3. For Single-Speed Mode, the measurement bandwidth is 0.5465 Fs to 3 Fs.
   For Double-Speed Mode, the measurement bandwidth is 0.577 Fs to 1.4 Fs.
   For Quad-Speed Mode, the measurement bandwidth is 0.7 Fs to 1 Fs.
4. De-emphasis is available only in Single-Speed Mode.
5. Amplitude vs. Frequency plots of this data are available in “Performance Plots” on page 18.

DIGITAL INPUT CHARACTERISTICS

Parameters	Symbol	Min	Typ	Max	Units
High-Level Input Voltage -all input Pins except RST (% of VL)	V_{IH}	70%	-	-	V
Low-Level Input Voltage -all input Pins except RST (% of VL)	V_{IL}	-	-	30%	V
High-Level Input Voltage -RST pin (Note 6) (% of VL)	V_{IH}	90%	-	-	V
Low-Level Input Voltage -RST pin (% of VL)	V_{IL}	-	-	10%	V
Input Leakage Current (Note 7)	I_{in}	-	-	±10	µA
Input Capacitance		-	8	-	pF

6. RST pin has an input threshold relative to VL, but is VA tolerant.
7. I_{in} for LRCK is ±20 µA max.

POWER & THERMAL CHARACTERISTICS

Parameters		Symbol	5 V Nom Min	5 V Nom Typ	5 V Nom Max	Units
Power Supplies						
Power Supply Current (Note 8)	normal operation	I_A	-	66	90	mA
		I_L	-	0.1	1	mA
	power-down state (Note 9)	I_A	-	300	-	µA
		I_L	-	26	-	µA
Power Dissipation	normal operation		-	331	455	mW
	power-down state (Note 9)		-	1.63	-	mW
Package Thermal Resistance		θ_{JA}	-	72	-	°C/Watt
Power Supply Rejection Ratio (Note 10)	(1 kHz)	PSRR	-	60	-	dB
	(60 Hz)		-	40	-	dB

8. Current consumption increases with increasing FS and increasing MCLK. Typ and Max values are based on highest FS and highest MCLK. Current variance between speed modes is small.
9. Power-Down Mode is defined when all clock and data lines are held static.
10. Valid with the recommended capacitor values on VQ and FILT+ as shown in the typical connection diagram in Section 4.

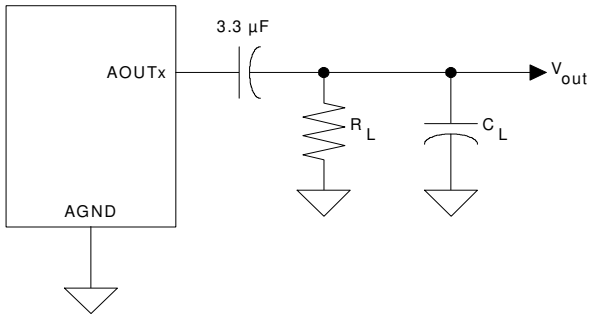


Figure 1. Equivalent Output Test Load

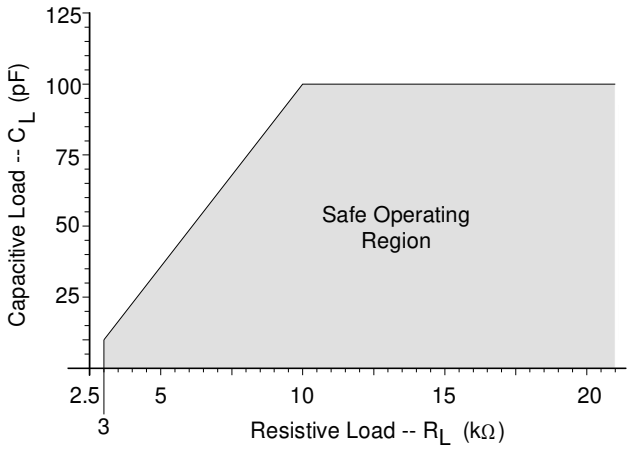


Figure 2. Maximum Loading

SWITCHING CHARACTERISTICS - SERIAL AUDIO INTERFACE

Parameters	Symbol	Min	Typ	Max	Units
MCLK Frequency		0.512	-	50	MHz
MCLK Duty Cycle		45	-	55	%
Input Sample Rate All MCLK/LRCK ratios combined (Note 11)	Fs	2		216	kHz
256x, 384x, 1024x		2		54	kHz
256x, 384x		84		134	kHz
512x, 768x		42		67	kHz
1152x		30		34	kHz
128x, 192x		50		108	kHz
64x, 96x		100		216	kHz
128x, 192x		168		216	kHz
External SCLK Mode					
LRCK Duty Cycle (External SCLK only)		45	50	55	%
SCLK Pulse Width Low	t_{sclkl}	20	-	-	ns
SCLK Pulse Width High	t_{sclkh}	20	-	-	ns
SCLK Duty Cycle		45	50	55	%
SCLK rising to LRCK edge delay	t_{slrd}	20	-	-	ns
SCLK rising to LRCK edge setup time	t_{slrs}	20	-	-	ns
SDIN valid to SCLK rising setup time	t_{sdlrs}	20	-	-	ns
SCLK rising to SDIN hold time	t_{sdh}	20	-	-	ns
Internal SCLK Mode					
LRCK Duty Cycle (Internal SCLK only) (Note 12)		-	50	-	%
SCLK Period (Note 13)	t_{sclkw}	$\frac{10^9}{SCLK}$	-	-	ns
SCLK rising to LRCK edge	t_{sclkr}	-	$\frac{tsclkw}{2}$	-	µs
SDIN valid to SCLK rising setup time	t_{sdlrs}	$\frac{10^9}{(512)Fs} + 10$	-	-	ns
SCLK rising to SDIN hold time MCLK / LRCK =1152, 1024, 512, 256, 128, or 64	t_{sdh}	$\frac{10^9}{(512)Fs} + 15$	-	-	ns
SCLK rising to SDIN hold time MCLK / LRCK = 768, 384, 192, or 96	t_{sdh}	$\frac{10^9}{(384)Fs} + 15$	-	-	ns

11. Not all sample rates are supported for all clock ratios. See table "Common Clock Frequencies" on page 12 for supported ratios and frequencies.
12. In Internal SCLK Mode, the duty cycle must be 50% ± 1/2 MCLK period.
13. The SCLK / LRCK ratio may be either 32, 48, 64, or 72. This ratio depends on data format and MCLK/LRCK ratio. (See Figures 7-10)

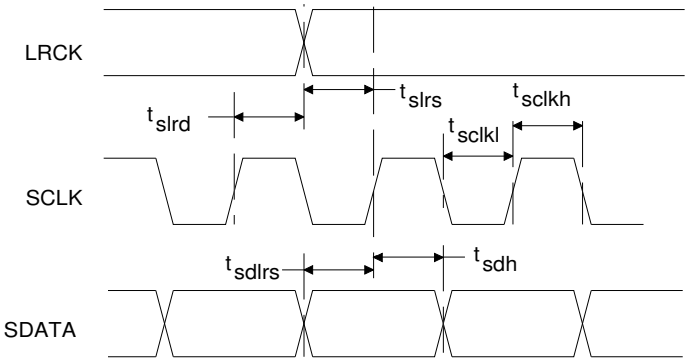


Figure 3. External Serial Mode Input Timing

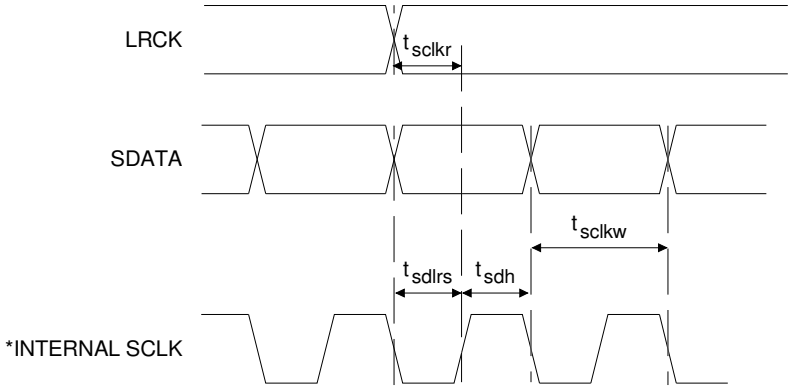


Figure 4. Internal Serial Mode Input Timing

* The SCLK pulses shown are internal to the CS4361.

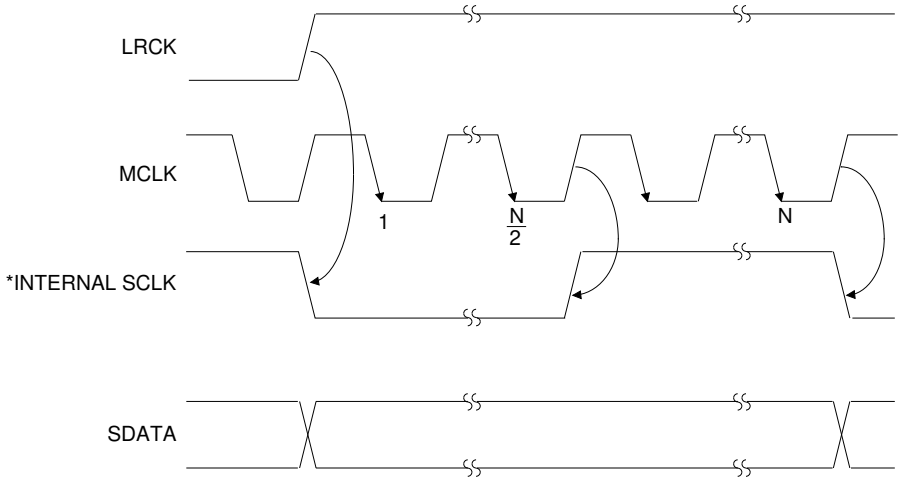


Figure 5. Internal Serial Clock Generation

* The SCLK pulses shown are internal to the CS4361.

N equals MCLK divided by SCLK

3. TYPICAL CONNECTION DIAGRAM

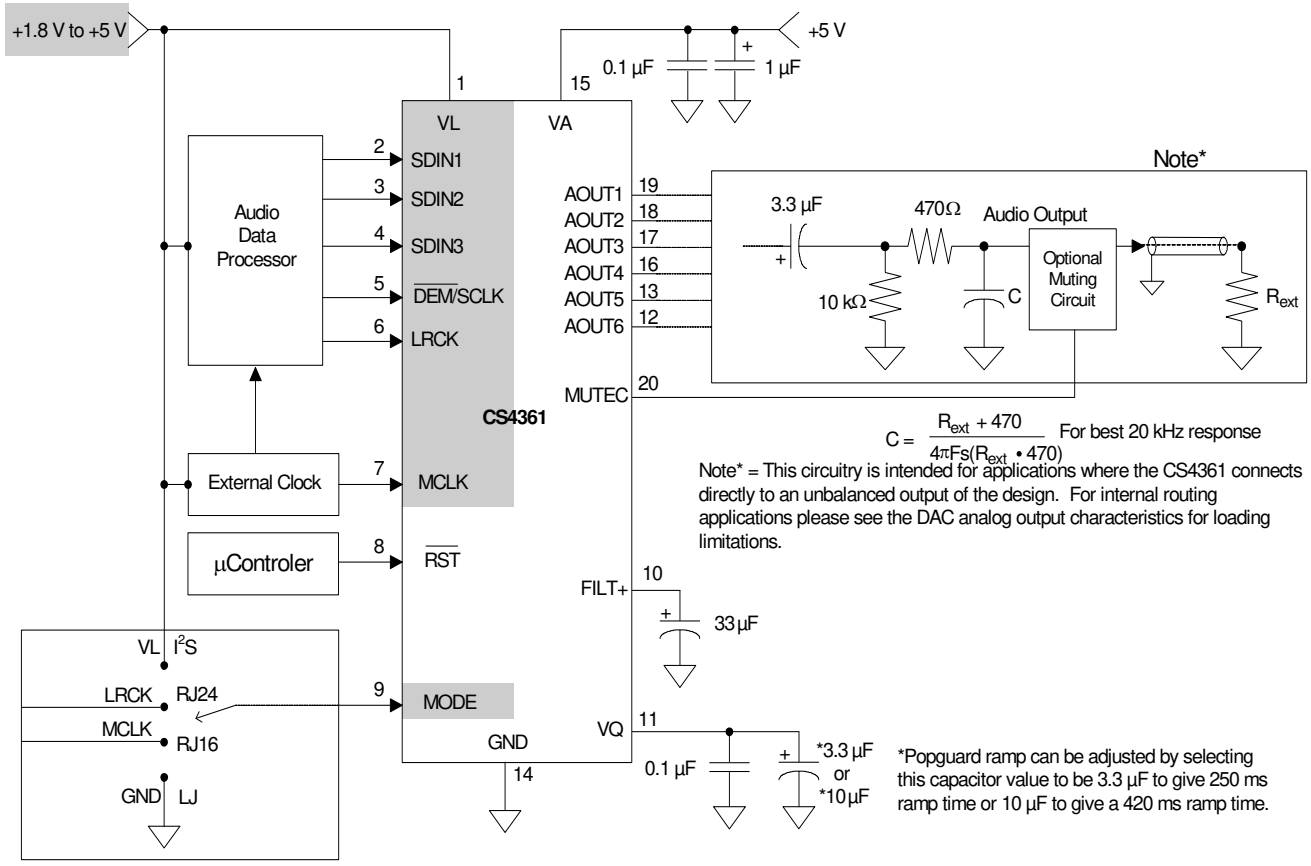


Figure 6. Recommended Connection Diagram

4. APPLICATIONS

The CS4361 accepts data at standard audio sample rates including 48, 44.1 and 32 kHz in SSM, 96, 88.2 and 64 kHz in DSM, and 192, 176.4 and 128 kHz in QSM. Audio data is input via the serial data input pin (SDIN). The Left/Right Clock (LRCK) determines which channel is currently being input on SDIN, and the optional Serial Clock (SCLK) clocks audio data into the input data buffer.

4.1 Master Clock

MCLK/LRCK must be an integer ratio as shown in Table 1. The LRCK frequency is equal to Fs, the frequency at which words for each channel are input to the device. The MCLK-to-LRCK frequency ratio and speed mode is detected automatically during the initialization sequence by counting the number of MCLK transitions during a single LRCK period and by detecting the absolute speed of MCLK. Internal dividers are set to generate the proper clocks. Table 1 illustrates several standard audio sample rates and the required MCLK and LRCK frequencies. Please note there is no required phase relationship, but MCLK, LRCK, and SCLK must be synchronous.

LRCK (kHz)	MCLK (MHz)									
	64x	96x	128x	192x	256x	384x	512x	768x	1024x	1152x
32	-	-	-	-	8.1920	12.2880	-	-	32.7680	36.8640
44.1	-	-	-	-	11.2896	16.9344	22.5792	33.8680	45.1580	-
48	-	-	-	-	12.2880	18.4320	24.5760	36.8640	49.1520	-
64	-	-	8.1920	12.2880	-	-	32.7680	49.1520	-	-
88.2	-	-	11.2896	16.9344	22.5792	33.8680	-	-	-	-
96	-	-	12.2880	18.4320	24.5760	36.8640	-	-	-	-
128	8.1920	12.2880	-	-	32.7680	49.1520	-	-	-	-
176.4	11.2896	16.9344	22.5792	33.8680	-	-	-	-	-	-
192	12.2880	18.4320	24.5760	36.8640	-	-	-	-	-	-
Mode	QSM				DSM		SSM			

Table 1. Common Clock Frequencies

4.2 Serial Clock

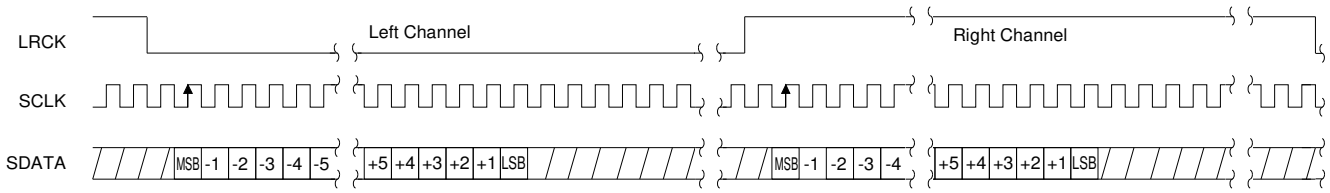
The serial clock controls the shifting of data into the input data buffers. The CS4361 supports both external and internal serial clock generation modes. Refer to Figures 7-10 for data formats.

4.2.1 External Serial Clock Mode

The CS4361 will enter the External Serial Clock Mode when 16 low-to-high transitions are detected on the $\overline{\text{DEM}}$/SCLK pin during any phase of the LRCK period. When this mode is enabled, the Internal Serial Clock Mode and de-emphasis filter cannot be accessed. The CS4361 will switch to Internal Serial Clock Mode if no low-to-high transitions are detected on the $\overline{\text{DEM}}$/SCLK pin for two consecutive frames of LRCK. Refer to Figure 12.

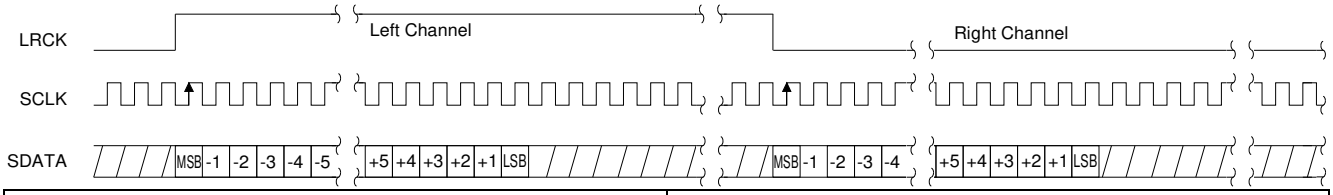
4.2.2 Internal Serial Clock Mode

In the Internal Serial Clock Mode, the serial clock is internally derived and synchronous with MCLK and LRCK. The SCLK/LRCK frequency ratio is either 32, 48, 64, or 72 depending upon data format. Operation in this mode is identical to operation with an external serial clock synchronized with LRCK. This mode allows access to the digital de-emphasis function. Refer to Figures 7 - 12 for details.



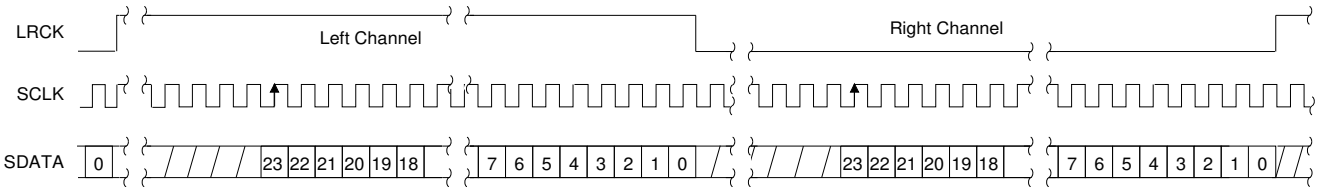
Internal SCLK Mode	External SCLK Mode
I²S, 16-Bit data and INT SCLK = 32 Fs if MCLK/LRCK = 1024, 512, 256, 128, or 64 I²S, Up to 24-Bit data and INT SCLK = 48 Fs if MCLK/LRCK = 768, 384, 192, or 96 I²S, Up to 24-Bit data and INT SCLK = 72 Fs if MCLK/LRCK = 1152	I²S, up to 24-Bit Data Data Valid on Rising Edge of SCLK

Figure 7. CS4361 Data Format (I²S)



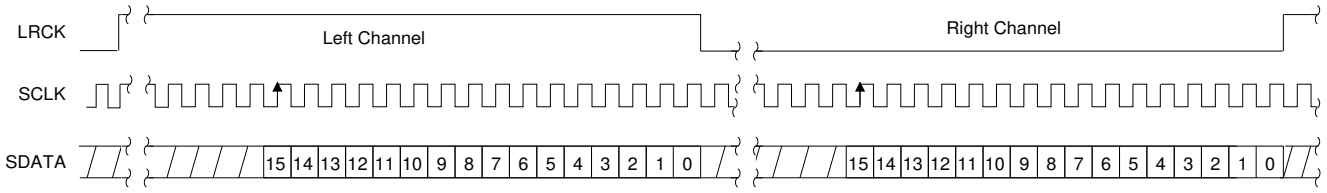
Internal SCLK Mode	External SCLK Mode
Left-Justified, up to 24-Bit Data INT SCLK = 64 Fs if MCLK/LRCK = 1024, 512, 256, 128, or 64 INT SCLK = 48 Fs if MCLK/LRCK = 768, 384, 192, or 96 INT SCLK = 72 Fs if MCLK/LRCK = 1152	Left-Justified, up to 24-Bit Data Data Valid on Rising Edge of SCLK

Figure 8. CS4361 Data Format (Left-Justified)



Internal SCLK Mode	External SCLK Mode
Right-Justified, 24-Bit Data INT SCLK = 64 Fs if MCLK/LRCK = 1024, 512, 256, 128, or 64 INT SCLK = 48 Fs if MCLK/LRCK = 768, 384, 192, or 96 INT SCLK = 72 Fs if MCLK/LRCK = 1152	Right-Justified, 24-Bit Data Data Valid on Rising Edge of SCLK SCLK Must Have at Least 48 Cycles per LRCK Period

Figure 9. CS4361 Data Format (Right-Justified 24)



Internal SCLK Mode	External SCLK Mode
Right-Justified, 16-Bit Data INT SCLK = 32 Fs if MCLK/LRCK = 1024, 512, 256, 128, or 64 INT SCLK = 48 Fs if MCLK/LRCK = 768, 384, 192, or 96 INT SCLK = 72 Fs if MCLK/LRCK = 1152	Right-Justified, 16-Bit Data Data Valid on Rising Edge of SCLK SCLK Must Have at Least 32 Cycles per LRCK Period

Figure 10. CS4361 Data Format (Right-Justified 16)

4.3 De-Emphasis

The CS4361 includes on-chip digital de-emphasis. Figure 11 shows the de-emphasis curve for Fs equal to 44.1 kHz. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, Fs. The de-emphasis filter is active (inactive) if the DEM/SCLK pin is low (high) for five consecutive falling edges of LRCK. This function is available only in the internal Serial Clock Mode when LRCK < 50 kHz.

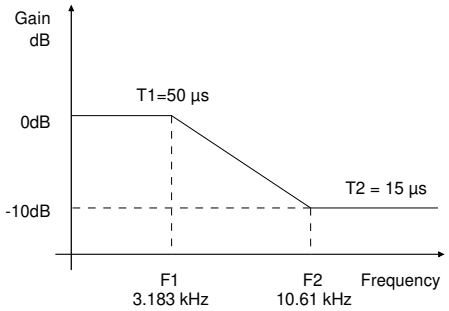


Figure 11. De-Emphasis Curve (Fs = 44.1kHz)

4.4 Mode Select

Mode selection is determined by the Mode Select pin. The value of this pin is locked 1024 LRCK cycles after RST is released. This pin requires a specific connection to supply, ground, MCLK, or LRCK as outlined in Table 2.

Mode pin is:	Mode	Figure
Tied to VL	I²S	7
Tied to GND	Left-Justified	8
Tied to LRCK	Right-Justified - 24 bit	9
Tied to MCLK	Right-Justified - 16bit	10

Table 2. Mode Pin Settings

4.5 Initialization and Power-Down

The initialization and power-down sequence flow chart is shown in Figure 12. The CS4361 enters the power-down state upon initial power-up. The interpolation filters and delta-sigma modulators are reset, and the internal voltage reference, multi-bit digital-to-analog converters, and switched-capacitor low-pass filters are powered down. The device will remain in the Power-Down Mode until $\overline{RST}$ is released and MCLK and LRCK are present. Once MCLK and LRCK are detected, MCLK occurrences are counted over one LRCK period to determine the MCLK/LRCK frequency ratio. Power is then applied to the internal voltage reference. Finally, power is applied to the D/A converters and switched-capacitor filters, and the analog outputs will ramp to the quiescent voltage, VQ.

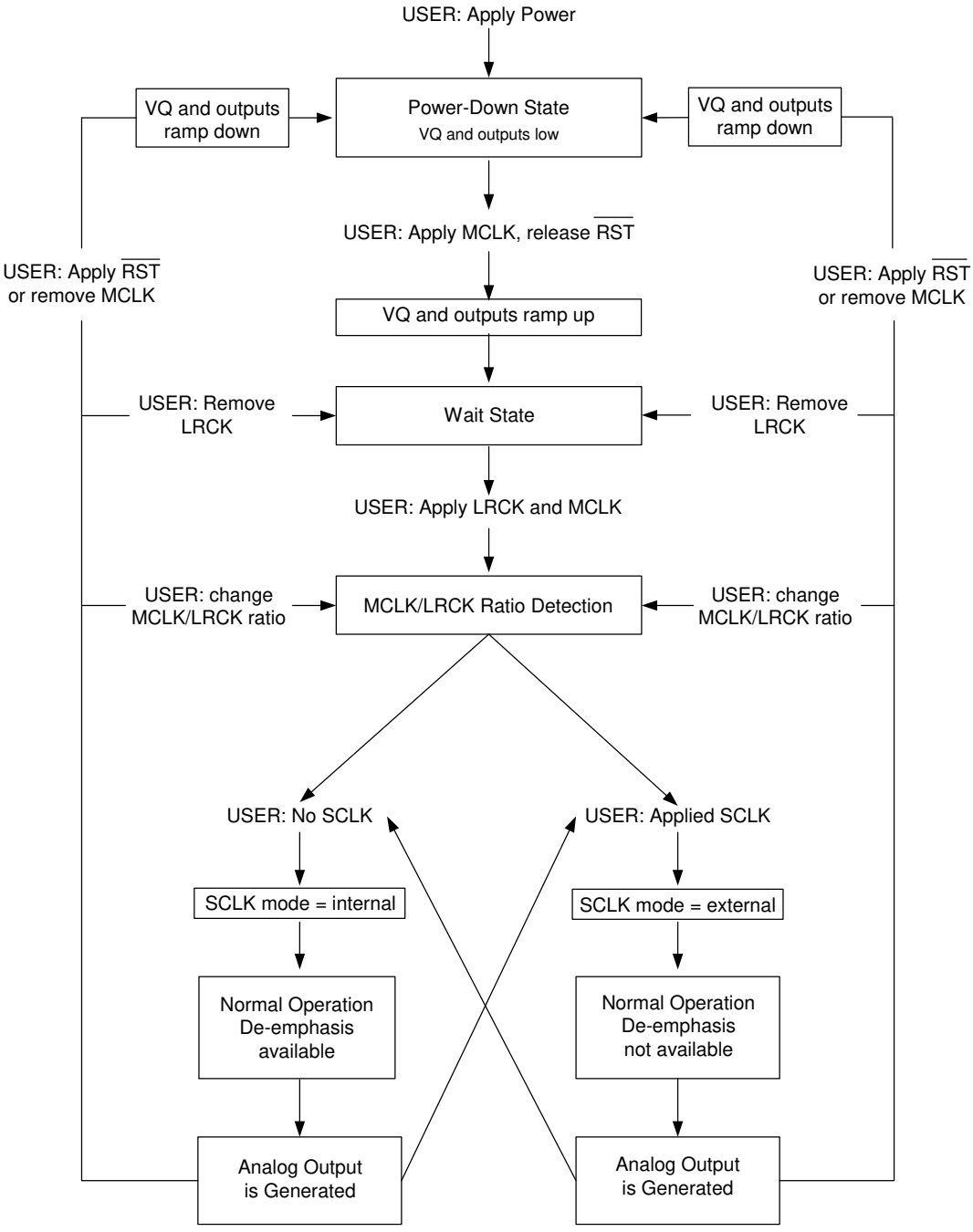


Figure 12. CS4361 Initialization and Power-Down Sequence

4.6 Output Transient Control

The CS4361 uses Popguard technology to minimize the effects of output transients during power-up and power-down. When implemented with external DC-blocking capacitors connected in series with the audio outputs, this feature eliminates the audio transients commonly produced by single-ended, single-supply converters. To make the best use of this feature, it is necessary to understand its operation.

4.6.1 Power-Up

When the device is initially powered up, the audio outputs, AOUT1-6, are clamped to VQ, which is initially low. After RST is released and MCLK is applied, the outputs begin to ramp with VQ towards the nominal quiescent voltage. This ramp takes approximately 200 ms to complete. The gradual voltage ramping allows time for the external DC-blocking capacitors to charge to VQ, effectively blocking the quiescent DC voltage. Audio output begins approximately 2000 sample periods after valid LRCK and SDIN are supplied (and SCLK, if used).

4.6.2 Power-Down

To prevent audio transients at power-down, the DC-blocking capacitors must fully discharge before turning off the power. In order to do this, either stop MCLK or hold RST low for a period of about 250 ms before removing power. During this time, voltage on VQ and the audio outputs discharge gradually to GND. If power is removed before this 250 ms time period has passed, a transient will occur when the VA supply drops below that of VQ. There is no minimum time for a power cycle; power may be reapplied at any time.

When changing clock ratio or sample rate, it is recommended that zero data (or near zero data) be present on SDIN for at least 10 LRCK samples before the change is made. During the clocking change, the DAC outputs will always be in a zero data state. If non-zero audio is present at the time of switching, a slight click or pop may be heard as the DAC output automatically goes to its zero data state.

4.7 Grounding and Power Supply Decoupling

As with any high-resolution converter, the CS4361 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 6 shows the recommended power arrangement, with VA connected to a clean +5 V supply. For best performance, decoupling and filter capacitors should be located as close to the device package as possible, with the smallest capacitors placed closest.

4.8 Analog Output and Filtering

The analog filter present in the CS4361 is a switched-capacitor filter followed by a continuous-time, low-pass filter. Its response, combined with that of the digital interpolator, is given in Figures 14 - 21. The recommended external analog circuitry is shown in the “Typical Connection Diagram” on page 11.

The analog outputs are named AOUT1-6. The SDIN1 feeds AOUT1 as the ‘Left’ marked data and AOUT2 as the ‘Right’ marked data. The SDIN2 feeds AOUT3 as the ‘Left’ marked data and AOUT4 as the ‘Right’ marked data. The SDIN3 feeds AOUT5 as the ‘Left’ marked data and AOUT6 as the ‘Right’ marked data.

4.9 Mute Control

The MUTEC pin is intended to be used as control for an external mute circuit in order to add off-chip mute capability.

This pin becomes active under the following conditions:

1. During power-up initialization
2. Upon reset
3. If the MCLK to LRCK ratio is incorrect
4. Upon receipt of 512 consecutive samples of zero
5. During power-down

The MUTEC pin will only go active on static zero data only if all 6 channels satisfy the 512 sample requirement. If any channel receives non-zero data, the mute pin will return low (inactive).

Use of the mute control function is not mandatory but is recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the mute control function can enable the system designer to achieve idle channel noise and signal-to-noise ratios that are only limited by the external mute circuit. The MUTEC pin is an active-high CMOS driver. See Figure 13 below for a suggested active-high mute circuit.

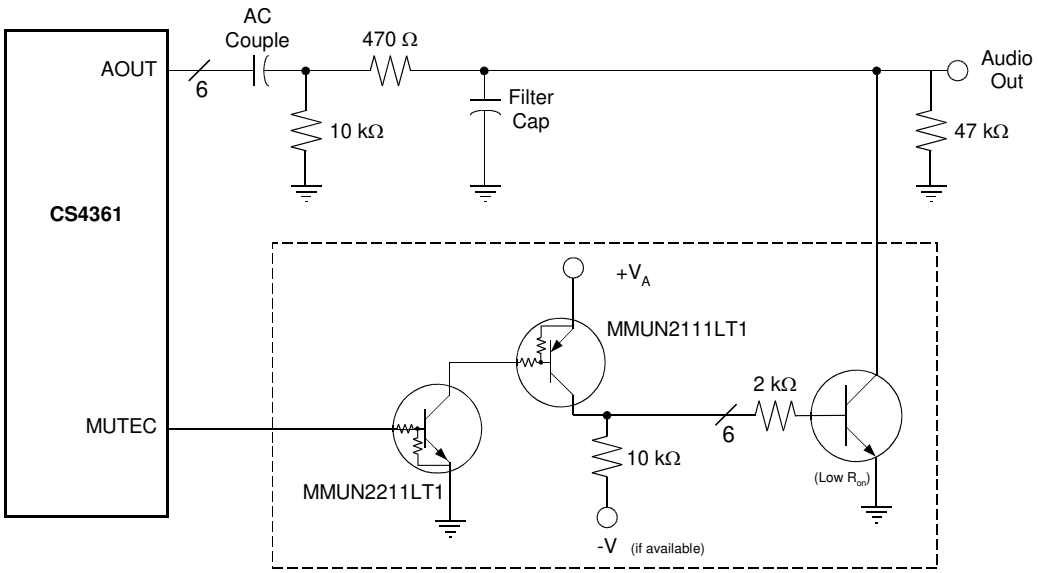


Figure 13. Suggested Active-Low Mute Circuit

5. PERFORMANCE PLOTS

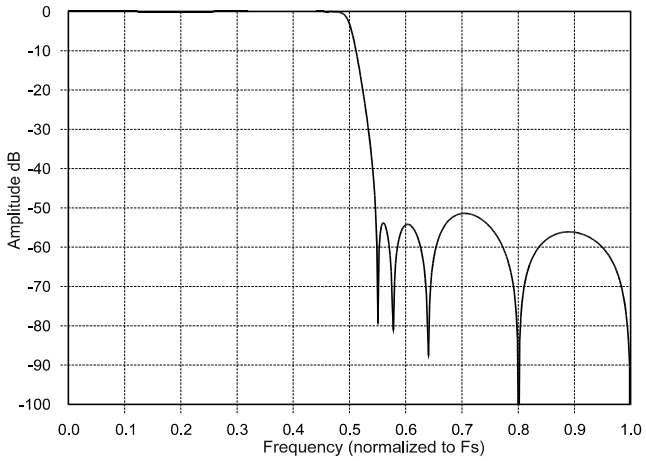


Figure 14. Single-Speed Stopband Rejection

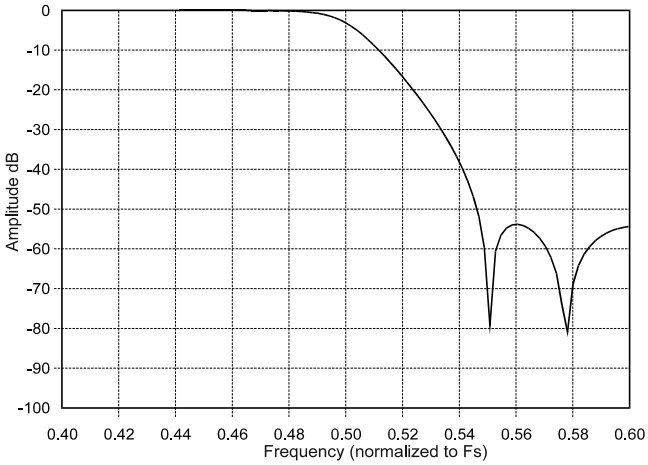


Figure 15. Single-Speed Transition Band

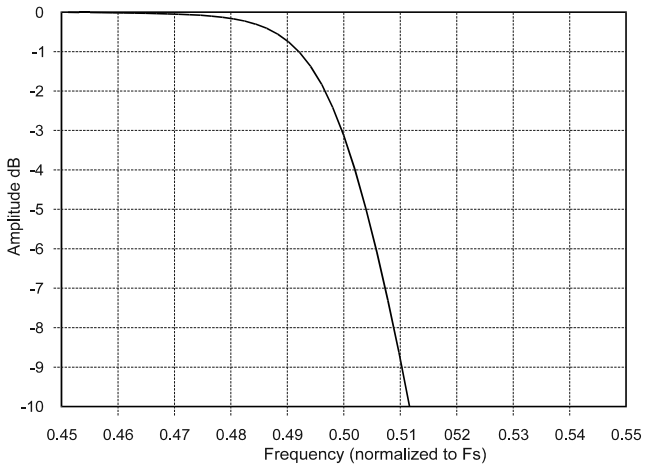


Figure 16. Single-Speed Transition Band

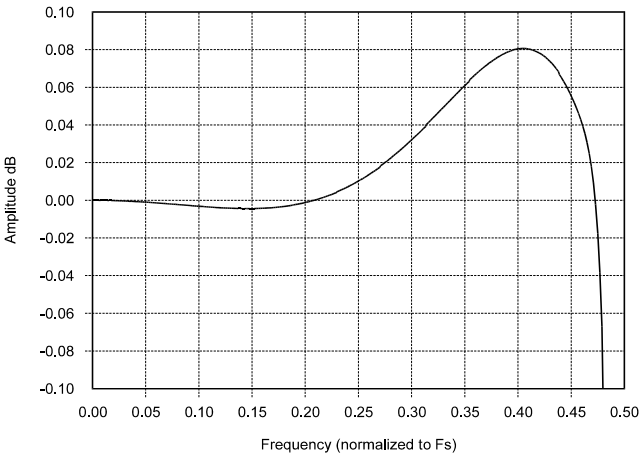


Figure 17. Single-Speed Passband Ripple

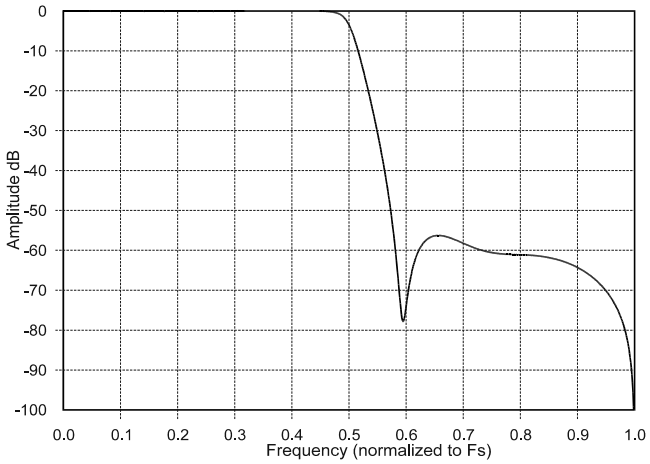


Figure 18. Double-Speed Stopband Rejection

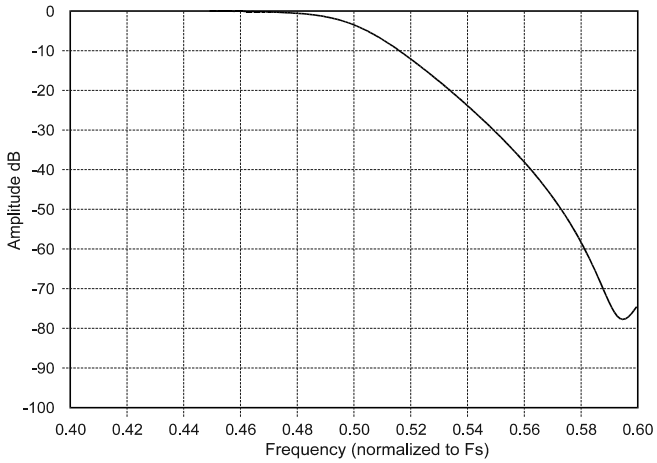


Figure 19. Double-Speed Transition Band

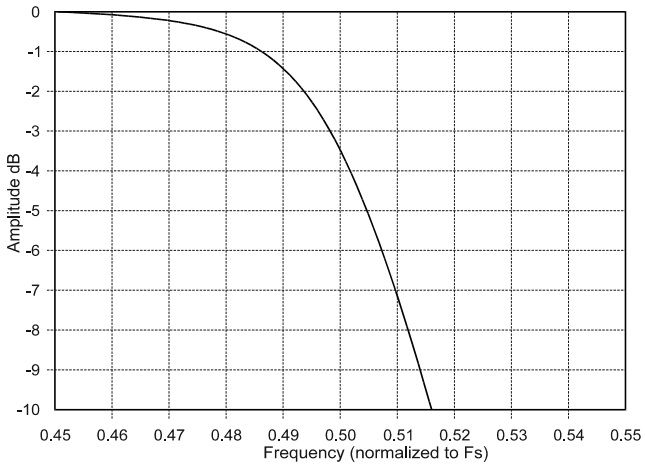


Figure 20. Double-Speed Transition Band

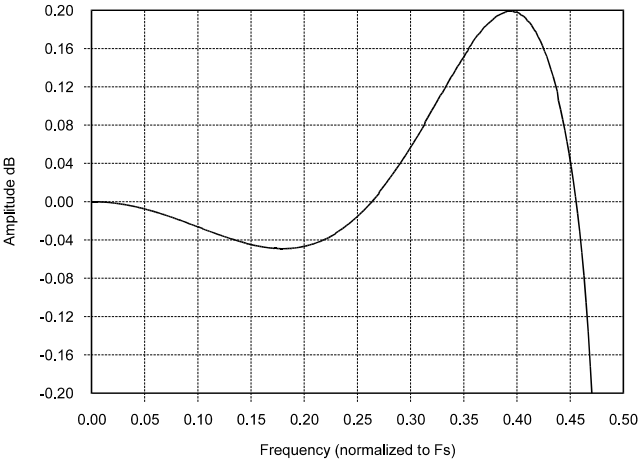


Figure 21. Double-Speed Passband Ripple

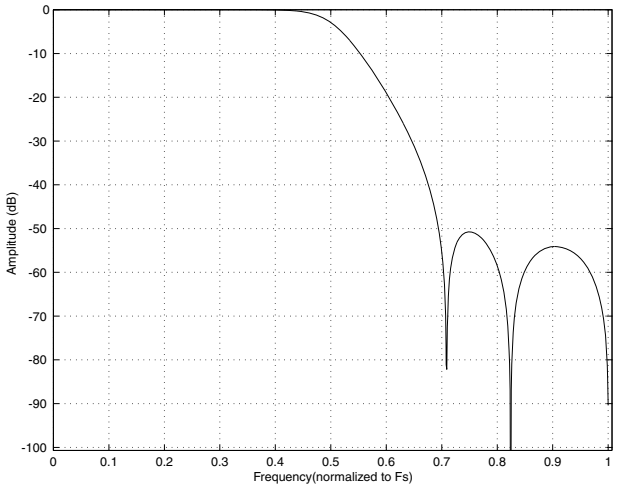


Figure 22. Quad-Speed Stopband Rejection

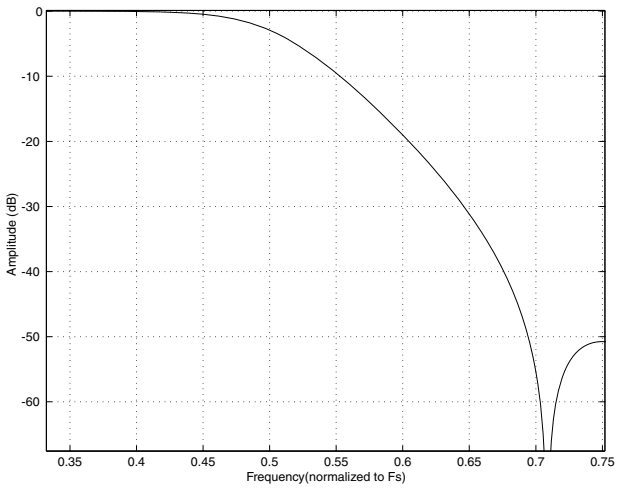


Figure 23. Quad-Speed Transition Band

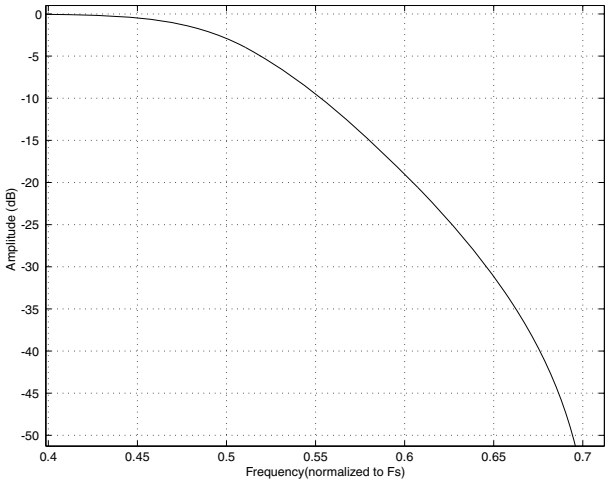


Figure 24. Quad-Speed Transition Band

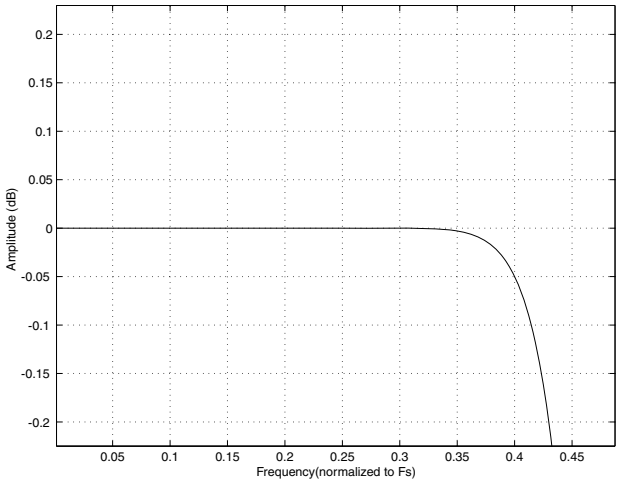


Figure 25. Quad-Speed Passband Ripple

6. PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Dynamic Range

The ratio of the full-scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

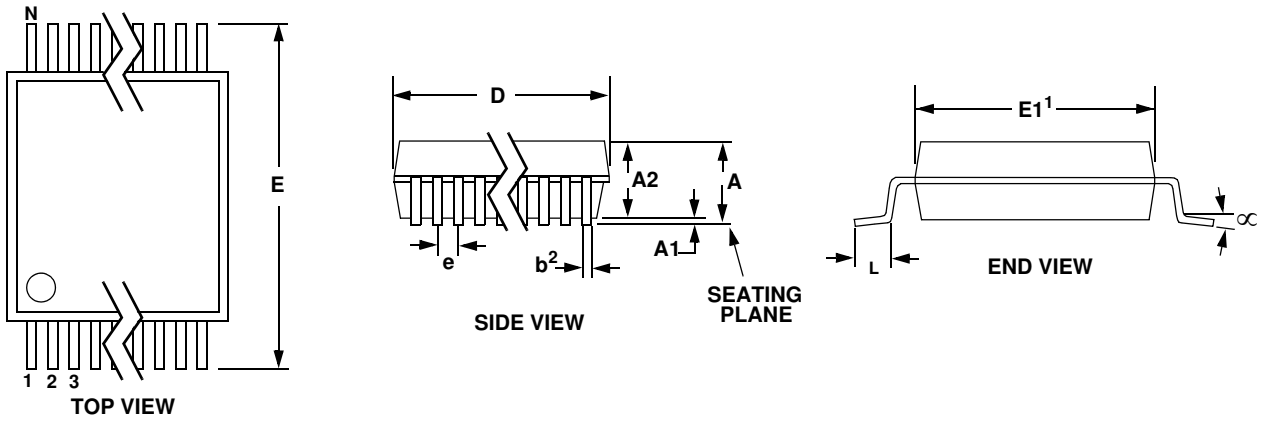
The deviation from the nominal full scale analog output for a full scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

7. PACKAGE INFORMATION

20L TSSOP (4.4 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.043	--	--	1.10	
A1	0.002	0.004	0.006	0.05	--	0.15	
A2	0.03346	0.0354	0.037	0.85	0.90	0.95	
b	0.00748	0.0096	0.012	0.19	0.245	0.30	
D	0.252	0.256	0.259	6.40	6.50	6.60	2,3
E	0.248	0.2519	0.256	6.30	6.40	6.50	1
E1	0.169	0.1732	0.177	4.30	4.40	4.50	
e	--	--	0.026	--	--	0.65	1
L	0.020	0.024	0.028	0.50	0.60	0.70	
µ	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-153

Controlling Dimension is Millimeters.

Notes:

1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

8. ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS4361	20-pin, 24-bit, 192 kHz, 6-channel D/A Converter	20-Plastic TSSOP	Yes	Commercial	-40 to 85° C	Tube	CS4361-CZZ
						Tape and Reel	CS4361-CZZR
CDB4361	CS4361 Evaluation Board		-	-	-	-	CDB4361

9. REVISION HISTORY

Release	Changes
A1	Initial Release.
A2	Correction to PDF file size.
F1	Removed VA = 3.3 V operation. Updated Typ and Max THD+N and Dynamic Range specs in "DAC Analog Characteristics - Commercial" on page 6. Corrected "Output Transient Control" on page 16 and "CS4361 Initialization and Power-Down Sequence" on page 15 to show ramp down when MCLK is removed. Corrected MUTEC description "512 LRCK cycles" in "Mute Control" on page 17. Removed -DZZ ordering option.
F2	Changed from footnote to "DAC Analog Characteristics - Commercial" on page 6 to read "One LSB of triangular PDF dither added to data," instead of "One-half LSB..." Added -CZZR ordering option and removed references to -CZZ from the specifications..

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.