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CS4364

103 dB, 192 kHz 6-Channel D/A Converter

Features

- Advanced Multi-bit Delta Sigma Architecture
- 24-bit Conversion
- Automatic Detection of Sample Rates up to 192 kHz
- 103 dB Dynamic Range
- -88 dB THD+N
- Single-Ended Output Architecture
- Direct Stream Digital® (DSD™) Mode
  - Non-Decimating Volume Control
  - On-Chip 50 kHz Filter
  - Matched PCM and DSD Analog Output Levels
- Selectable Digital Filters
- Volume Control with 1/2-dB Step Size and Soft Ramp
- Low Clock-Jitter Sensitivity
- +5 V Analog Supply, +2.5 V Digital Supply
- Separate 1.8 to 5 V Logic Supplies for the Control and Serial Ports

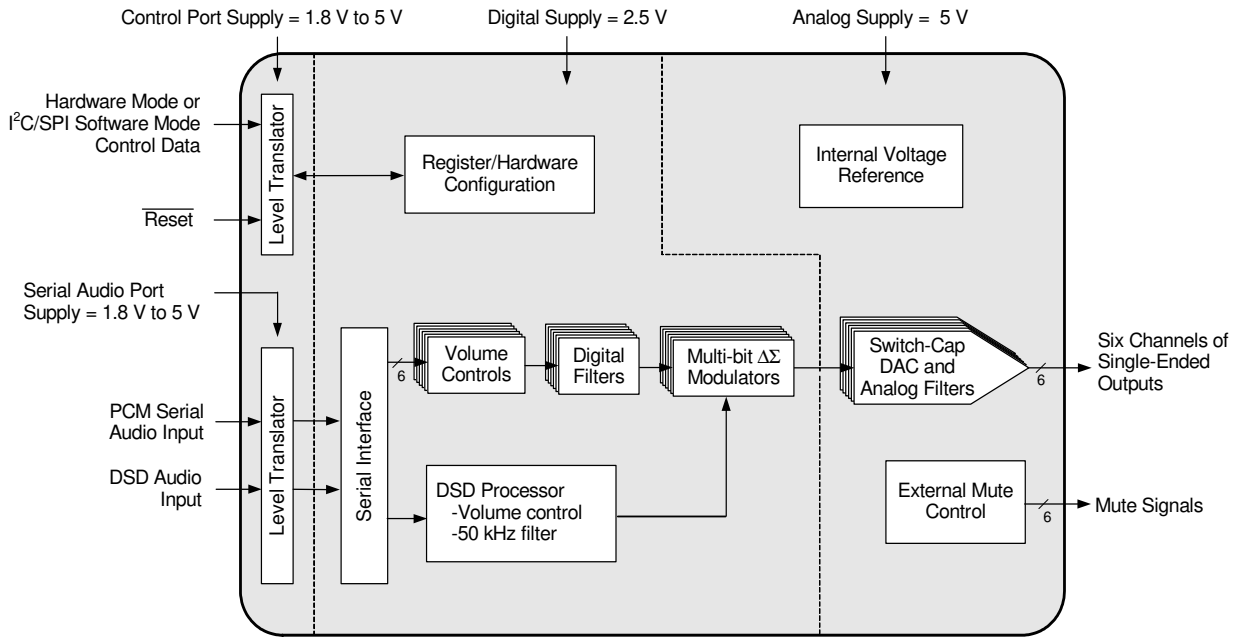
Description

The CS4364 is a complete 6-channel digital-to-analog system. This D/A system includes digital de-emphasis, half-dB step size volume control, ATAPI channel mixing, selectable fast and slow digital interpolation filters followed by an oversampled, multi-bit delta sigma modulator which includes mismatch shaping technology that eliminates distortion due to capacitor mismatch. Following this stage is a multi-element switched capacitor stage and low-pass filter with single-ended analog outputs.

The CS4364 also has a proprietary DSD processor which allows for volume control and 50 kHz on-chip filtering without an intermediate decimation stage. It also offers an optional path for direct DSD conversion by directly using the multi-element switched capacitor array.

The CS4364 accepts PCM data at sample rates from 4 kHz to 216 kHz, DSD audio data, and delivers excellent sound quality. These features are ideal for multi-channel audio systems including SACD players, A/V receivers, digital TV's, mixing consoles, effects processors, and sound cards.

This product is available in 48-pin LQFP package in Commercial (-40°C to +85°C) temperature grade. See "Ordering Information" on page 49 for complete details.



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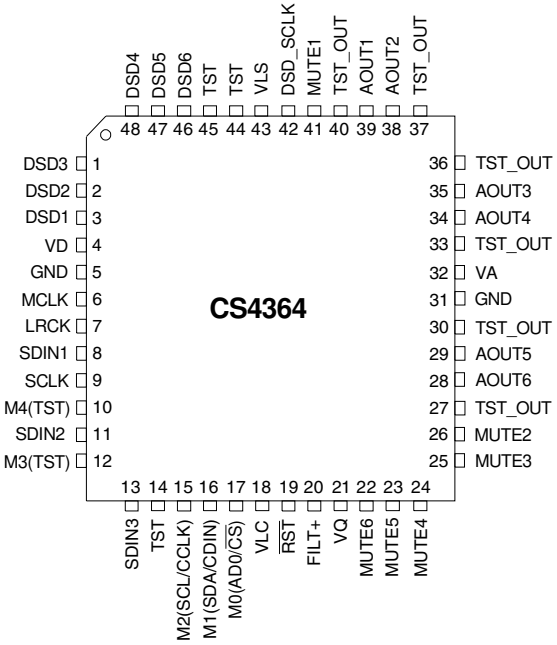
1. PIN DESCRIPTION



Pin Name	#	Pin Description
VD	4	**Digital Power** (*Input*) **-** Positive power supply for the digital section. Refer to the Recommended Operating Conditions for appropriate voltages.
GND	5 31	**Ground** (*Input*) - Ground reference. Should be connected to analog ground.
MCLK	6	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters. Table 1 illustrates several standard audio sample rates and the required master clock frequencies.
LRCK	7	**Left Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line. The frequency of the left/right clock must be at the audio sample rate, Fs.
SDIN1 SDIN2 SDIN3	8 11 13	**Serial Data Input** (*Input*) - Input for two's complement serial audio data.
SCLK	9	**Serial Clock** (*Input*) - Serial clocks for the serial audio interface.
TST	14 44 45	**Test** - These pins need to be tied to analog ground.
$\overline{\text{RST}}$	19	**Reset** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings when low.
VA	32	**Analog Power** (*Input*) **-** Positive power supply for the analog section. Refer to the Recommended Operating Conditions for appropriate voltages.
VLS	43	**Serial Audio Interface Power** (*Input*) **-** Determines the required signal level for the serial audio interface. Refer to the Recommended Operating Conditions for appropriate voltages.
VLC	18	**Control Port Power** (*Input*) **-** Determines the required signal level for the control port and hardware mode configuration pins. Refer to the Recommended Operating Conditions for appropriate voltages.
VQ	21	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage.

Pin Name	#	Pin Description
FILT+	20	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits. Requires the capacitive decoupling to analog ground as shown in the Typical Connection Diagram.
AOUT1 AOUT2 AOUT3 AOUT4 AOUT5 AOUT6	39 38 35 34 29 28	**Analog Output** (*Output*) - The full scale analog output level is specified in the Analog Characteristics specification table.
MUTEC1 MUTEC2 MUTEC3 MUTEC4 MUTEC5 MUTEC6	41 26 25 24 23 22	**Mute Control** (*Output*) - These pins are intended to be used as a control for external mute circuits on the line outputs to prevent the clicks and pops that can occur in any single supply system.
TST_OUT	40, 37 36, 33 30, 27	Test Output - These pins need to be floating and not connected to any trace or plane.
Hardware Mode Definitions		
M0 M1 M2 M3 M4	17 16 15 12 10	**Mode Selection** (*Input*) - Determines the operational mode of the device as detailed in Tables 4 and 5.
Software Mode Definitions		
SCL/CCLK	15	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port. Requires an external pull-up resistor to the logic interface voltage in I²C® mode as shown in the Typical Connection Diagram.
SDA/CDIN	16	**Serial Control Port Data** (*Input/Output*) - SDA is a data I/O line in I²C mode and is open drain, requiring an external pull-up resistor to the logic interface voltage, as shown in the Typical Connection Diagram; CDIN is the input data line for the control port interface in SPI™ mode.
AD0/$\overline{CS}$	17	**Address Bit 0 (I²C) / Control Port Chip Select (SPI)** (*Input*) - AD0 is a chip address pin in I²C mode; $\overline{CS}$ is the chip select signal for SPI mode.
TST	10 12	**Test -** These pins need to be tied to analog ground.
DSD Definitions		
DSD1, DSD2 DSD3, DSD4 DSD5, DSD6	3, 2 1, 48 47,46	**Direct Stream Digital Input** (*Input)* - Input for Direct Stream Digital serial audio data.
DSD_SCLK	42	**DSD Serial Clock** *(Input)* - Serial clock for the Direct Stream Digital serial audio interface.

2. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

(GND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Typ	Max	Units
DC Power Supply	Analog power	VA	4.75	5.0	5.25	V
	Digital internal power	VD	2.37	2.5	2.63	V
	Serial data port interface power	VLS	1.71	5.0	5.25	V
	Control port interface power	VLC	1.71	5.0	5.25	V
Ambient Operating Temperature (Power Applied)	-CQZ	T_A	-40	-	+85	°C

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Max	Units
DC Power Supply	Analog power	VA	-0.3	6.0	V
	Digital internal power	VD	-0.3	3.2	V
	Serial data port interface power	VLS	-0.3	6.0	V
	Control port interface power	VLC	-0.3	6.0	V
Input Current	Any Pin Except Supplies	I_{in}	-	±10	mA
Digital Input Voltage	Serial data port interface	V_{IND-S}	-0.3	VLS+ 0.4	V
	Control port interface	V_{IND-C}	-0.3	VLC+ 0.4	V
Ambient Operating Temperature (power applied)		T_{op}	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

DAC ANALOG CHARACTERISTICS

Test Conditions (unless otherwise indicated): VA = VLS = VLC = 5 V; VD = 2.5 V; TA = 25 °C; Full-Scale 997 Hz input sine wave (Note 1); Tested under max ac-load resistance; Valid with FILT+ and VQ capacitors as shown in "Typical Connection Diagram" on page 18; Measurement Bandwidth 10 Hz to 20 kHz.

Parameters			Symbol	Min	Typ	Max	Unit
FS = 48 kHz, 96 kHz, 192 kHz and DSD							
Dynamic Range	24-bit	A-weighted		97	103	-	dB
		unweighted		94	100	-	dB
	16-bit	A-weighted		-	97	-	dB
	(Note 2)	unweighted		-	94	-	dB
Total Harmonic Distortion + Noise	24-bit	-0 dB	THD+N	-	-88	-82	dB
		-20 dB		-	-80	-74	dB
		-60 dB		-	-40	-34	dB
	(Note 2) 16-bit	0 dB		-	-88	-	dB
		-20 dB		-	-74	-	dB
		-60 dB		-	-34	-	dB
Idle Channel Noise / Signal-to-noise ratio				-	100	-	dB
Interchannel Isolation		(1 kHz)		-	110	-	dB
DC Accuracy							
Interchannel Gain Mismatch				-	0.1	-	dB
Gain Drift				-	100	-	ppm/°C
Analog Output							
Full Scale Differential-Output Voltage (Note 3)	PCM, DSD processor		V_{FS}	64%•V_A	66%•V_A	68%•V_A	Vpp
	Direct DSD Mode			47%•V_A	48%•V_A	49%•V_A	Vpp
Output Impedance			Z_{OUT}	-	130	-	Ω
Max DC Current draw from an AOUT pin			I_{OUTmax}	-	1.0	-	mA
Min AC-Load Resistance			R_L	-	3	-	kΩ
Max Load Capacitance			C_L	-	100	-	pF
Quiescent Voltage			V_Q	-	50% V_A	-	VDC
Max Current draw from V_Q			I_{QMAX}	-	10	-	µA

Notes:

1. One-half LSB of triangular PDF dither is added to data.
2. Performance limited by 16-bit quantization noise.
3. V_{FS} is tested under load R_L and includes attenuation due to Z_{OUT}

POWER AND THERMAL CHARACTERISTICS

Parameters		Symbol	Min	Typ	Max	Units
Power Supplies						
Power Supply Current	normal operation, VA= 5 V	I_A	-	63	69	mA
(Note 4)	VD= 2.5 V	I_D	-	18	22	mA
	(Note 5) Interface current, VLC=5 V	I_{LC}	-	2	-	µA
	VLS=5 V	I_{LS}	-	84	-	µA
	(Note 6) power-down state (all supplies)	I_{pd}	-	200	-	µA
Power Dissipation (Note 4)	VA = 5 V, VD = 2.5 V					
	normal operation		-	360	400	mW
	(Note 6) power-down		-	1	-	mW
Package Thermal Resistance	multi-layer	θ_{JA}	-	48	-	°C/Watt
	dual-layer	θ_{JA}	-	65	-	°C/Watt
		θ_{JC}	-	15	-	°C/Watt
Power Supply Rejection Ratio (Note 7)	(1 kHz)	PSRR	-	60	-	dB
	(60 Hz)		-	40	-	dB

Notes:

4. Current consumption increases with increasing FS within a given speed mode and is signal dependant. Max values are based on highest FS and highest MCLK.
5. I_{LC} measured with no external loading on the SDA pin.
6. Power Down Mode is defined as $\overline{RST}$ pin = Low with all clock and data lines held static.
7. Valid with the recommended capacitor values on FILT+ and VQ as shown in Figures 6 and 7.

COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

The filter characteristics have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs.
(See (Note 12))

Parameter		Fast Roll-Off Min	Fast Roll-Off Typ	Fast Roll-Off Max	Unit
Combined Digital and On-chip Analog Filter Response - Single-Speed Mode - 48 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.454	Fs
	to -3 dB corner	0	-	.499	Fs
Frequency Response	10 Hz to 20 kHz	-0.01	-	+0.01	dB
StopBand		0.547	-	-	Fs
StopBand Attenuation	(Note 10)	102	-	-	dB
Group Delay		-	10.4/Fs	-	s
De-emphasis Error (Note 11)	Fs = 32 kHz	-	-	±0.36	dB
(Relative to 1 kHz)	Fs = 44.1 kHz	-	-	±0.21	dB
	Fs = 48 kHz	-	-	±0.14	dB
Combined Digital and On-chip Analog Filter Response - Double-Speed Mode - 96 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.430	Fs
	to -3 dB corner	0	-	.499	Fs
Frequency Response	10 Hz to 20 kHz	-0.01	-	+0.01	dB
StopBand		.583	-	-	Fs
StopBand Attenuation	(Note 10)	80	-	-	dB
Group Delay		-	6.15/Fs	-	s
Combined Digital and On-chip Analog Filter Response - Quad-Speed Mode - 192 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.105	Fs
	to -3 dB corner	0	-	.490	Fs
Frequency Response	10 Hz to 20 kHz	-0.01	-	+0.01	dB
StopBand		.635	-	-	Fs
StopBand Attenuation	(Note 10)	90	-	-	dB
Group Delay		-	7.1/Fs	-	s

Notes:

8. Slow Roll-off interpolation filter is only available in Software Mode.
9. Response is clock dependent and will scale with Fs.
10. For Single-Speed Mode, the Measurement Bandwidth is from stopband to 3 Fs.
    For Double-Speed Mode, the Measurement Bandwidth is from stopband to 3 Fs.
    For Quad-Speed Mode, the Measurement Bandwidth is from stopband to 1.34 Fs.
11. De-emphasis is available only in Single-Speed Mode; Only 44.1 kHz De-emphasis is available in Hardware Mode.
12. Amplitude vs. Frequency plots of this data are available in the “Filter Response Plots” on page 43.

COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

(CONTINED)

Parameter		Slow Roll-Off (Note 8) Min	Typ	Max	Unit
Single-Speed Mode - 48 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	0.417	Fs
	to -3 dB corner	0	-	0.499	Fs
Frequency Response	10 Hz to 20 kHz	-0.01	-	+0.01	dB
StopBand		.583	-	-	Fs
StopBand Attenuation	(Note 10)	64	-	-	dB
Group Delay		-	7.8/Fs	-	s
De-emphasis Error (Note 11)	Fs = 32 kHz	-	-	±0.36	dB
(Relative to 1 kHz)	Fs = 44.1 kHz	-	-	±0.21	dB
	Fs = 48 kHz	-	-	±0.14	dB
Double-Speed Mode - 96 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.296	Fs
	to -3 dB corner	0	-	.499	Fs
Frequency Response	10 Hz to 20 kHz	-0.01	-	+0.01	dB
StopBand		.792	-	-	Fs
StopBand Attenuation	(Note 10)	70	-	-	dB
Group Delay		-	5.4/Fs	-	s
Quad-Speed Mode - 192 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.104	Fs
	to -3 dB corner	0	-	.481	Fs
Frequency Response	10 Hz to 20 kHz	-0.01	-	+0.01	dB
StopBand		.868	-	-	Fs
StopBand Attenuation	(Note 10)	75	-	-	dB
Group Delay		-	6.6/Fs	-	s

DSD COMBINED DIGITAL & ON-CHIP ANALOG FILTER RESPONSE

Parameter		Min	Typ	Max	Unit
DSD Processor Mode					
Passband (Note 9)	to -3 dB corner	0	-	50	kHz
Frequency Response	10 Hz to 20 kHz	-0.05	-	+0.05	dB
Roll-off		27	-	-	dB/Oct
Direct DSD Mode					
Passband (Note 9)	to -0.1 dB corner	0	-	26.9	kHz
	to -3 dB corner	0	-	176.4	kHz
Frequency Response 10 Hz to 20 kHz		-0.1	-	0	dB

DIGITAL CHARACTERISTICS

Parameters		Symbol	Min	Typ	Max	Units
Input Leakage Current	(Note 13)	I_{in}	-	-	±10	µA
Input Capacitance			-	8	-	pF
High-Level Input Voltage	Serial I/O	V_{IH}	70%	-	-	V_{LS}
	Control I/O	V_{IH}	70%	-	-	V_{LC}
Low-Level Input Voltage	Serial I/O	V_{IL}	-	-	30%	V_{LS}
	Control I/O	V_{IL}	-	-	30%	V_{LC}
Low-Level Output Voltage (I_{OL} = -1.2 mA)	Control I/O = 3.3 V, 5 V	V_{OL}	-	-	20%	V_{LC}
	Control I/O = 1.8 V, 2.5 V	V_{OL}	-	-	25%	V_{LC}
MUTEC auto detect input high voltage		V_{IH}	70%	-	-	VA
MUTEC auto detect input low voltage		V_{IL}	-	-	30%	VA
Maximum MUTEC Drive Current		I_{max}	-	3	-	mA
MUTEC High-Level Output Voltage		V_{OH}	-	VA	-	V
MUTEC Low-Level Output Voltage		V_{OL}	-	0	-	V

13. Any pin except supplies. Transient currents of up to ±100 mA on the input pins will not cause SCR latch-up

SWITCHING CHARACTERISTICS - PCM

(Inputs: Logic 0 = GND, Logic 1 = VLS, C_L = 30 pF)

Parameters		Symbol	Min	Max	Units
$\overline{\text{RST}}$ pin Low Pulse Width (Note 14)			1	-	ms
MCLK Frequency			1.024	55.2	MHz
MCLK Duty Cycle (Note 15)			45	55	%
Input Sample Rate - LRCK (Manual selection)	Single-Speed Mode	F_s	4	54	kHz
	Double-Speed Mode	F_s	50	108	kHz
	Quad-Speed Mode	F_s	100	216	kHz
Input Sample Rate - LRCK (Auto detect)	Single-Speed Mode	Fs	4	54	kHz
	Double-Speed Mode	Fs	84	108	kHz
	Quad-Speed Mode	Fs	170	216	kHz
LRCK Duty Cycle			45	55	%
SCLK Duty Cycle			45	55	%
SCLK High Time		t_{sckh}	8	-	ns
SCLK Low Time		t_{sckl}	8	-	ns
LRCK Edge to SCLK Rising Edge		t_{lcks}	5	-	ns
SCLK Rising Edge to LRCK Falling Edge		t_{lckd}	5	-	ns
SDIN Setup Time Before SCLK Rising Edge		t_{ds}	3	-	ns
SDIN Hold Time After SCLK Rising Edge		t_{dh}	5	-	ns

Notes:

14. After powering up, $\overline{\text{RST}}$ should be held low until after the power supplies and clocks are settled.
15. See Tables 1 - 3 for suggested MCLK frequencies.

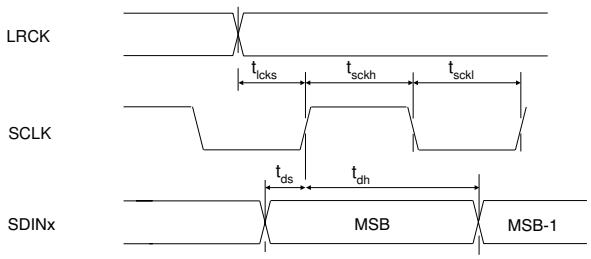


Figure 1. Serial Audio Interface Timing

SWITCHING CHARACTERISTICS - DSD

(Logic 0 = AGND = DGND; Logic 1 = VLS; C_L = 30 pF)

Parameter	Symbol	Min	Typ	Max	Unit
MCLK Duty Cycle		40	-	60	%
DSD_SCLK Pulse Width Low	t_{sclkl}	160	-	-	ns
DSD_SCLK Pulse Width High	t_{sclkh}	160	-	-	ns
DSD_SCLK Frequency (64x Oversampled) (128x Oversampled)		1.024 2.048	- -	3.2 6.4	MHz MHz
DSD_A / _B valid to DSD_SCLK rising setup time	t_{sdlrs}	20	-	-	ns
DSD_SCLK rising to DSD_A or DSD_B hold time	t_{sdh}	20	-	-	ns
DSD clock to data transition (Phase Modulation Mode)	t_{dpm}	-20	-	20	ns

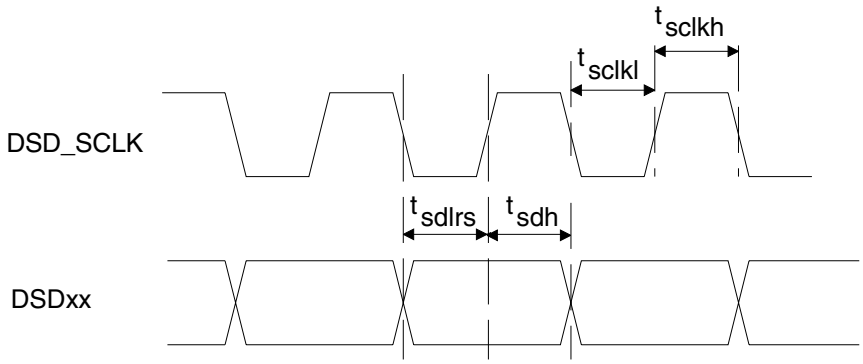


Figure 2. Direct Stream Digital - Serial Audio Input Timing

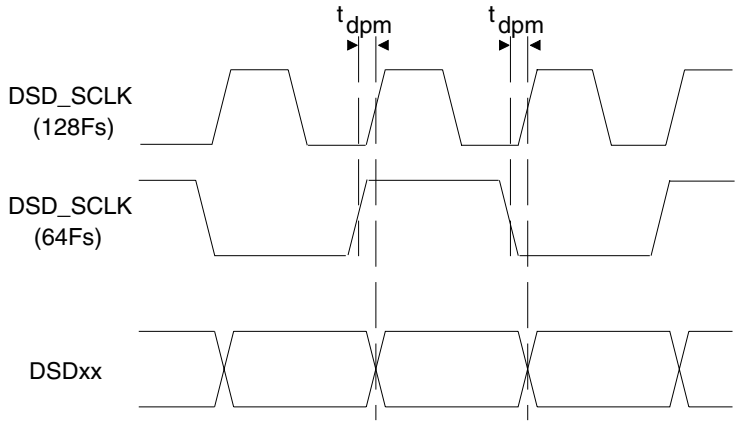


Figure 3. Direct Stream Digital - Serial Audio Input Timing for Phase Modulation Mode

SWITCHING CHARACTERISTICS - CONTROL PORT - I²C FORMAT

(Inputs: Logic 0 = GND, Logic 1 = VLC, C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{\text{RST}}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 16)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}, t_{rc}	-	1	µs
Fall Time SCL and SDA	t_{fc}, t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	1000	ns

Notes:

16. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

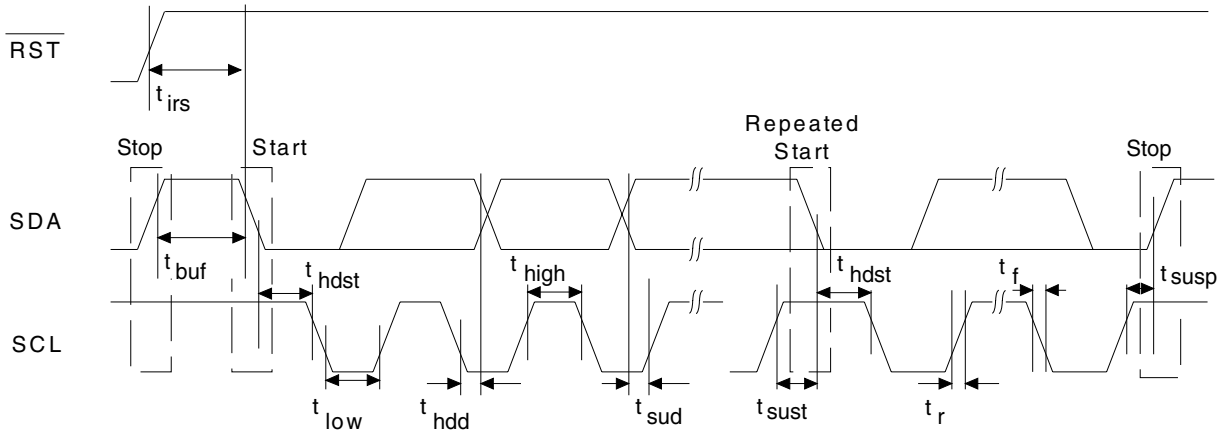


Figure 4. Control Port Timing - I²C Format

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI FORMAT

(Inputs: Logic 0 = GND, Logic 1 = VLC, C_L = 30 pF)

Parameter		Symbol	Min	Max	Unit
CCLK Clock Frequency		f_{sclk}	-	6	MHz
$\overline{RST}$ Rising Edge to CS Falling		t_{srs}	500	-	ns
CCLK Edge to $\overline{CS}$ Falling	(Note 17)	t_{spi}	500	-	ns
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 18)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN	(Note 19)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 19)	t_{f2}	-	100	ns

Notes:

17. t_{spi} only needed before first falling edge of $\overline{CS}$ after $\overline{RST}$ rising edge. t_{spi} = 0 at all other times.
18. Data must be held for sufficient time to bridge the transition time of CCLK.
19. For F_{SCK} < 1 MHz.

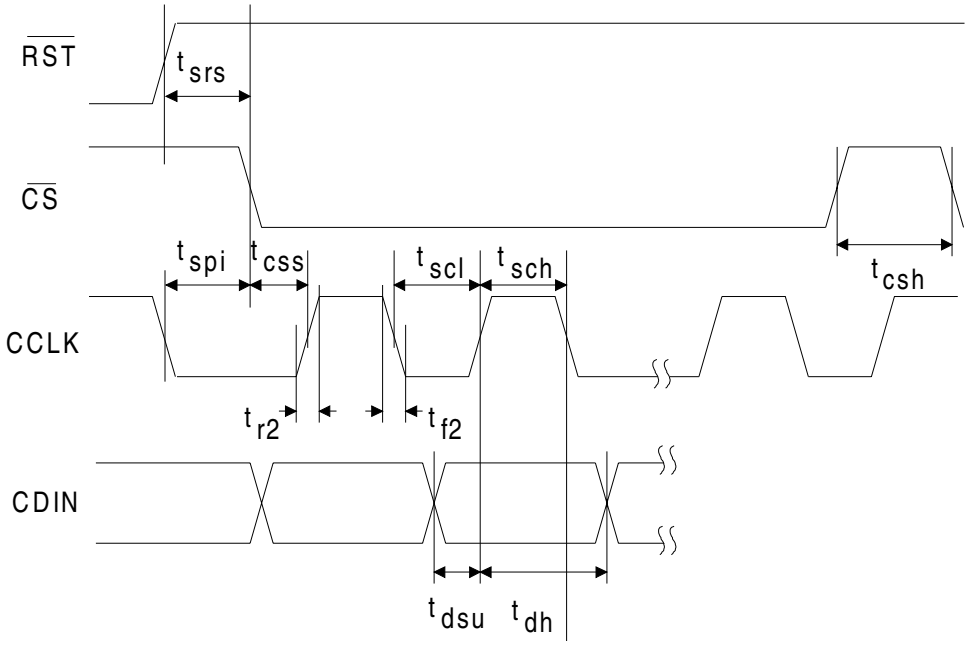


Figure 5. Control Port Timing - SPI Format

3. TYPICAL CONNECTION DIAGRAM

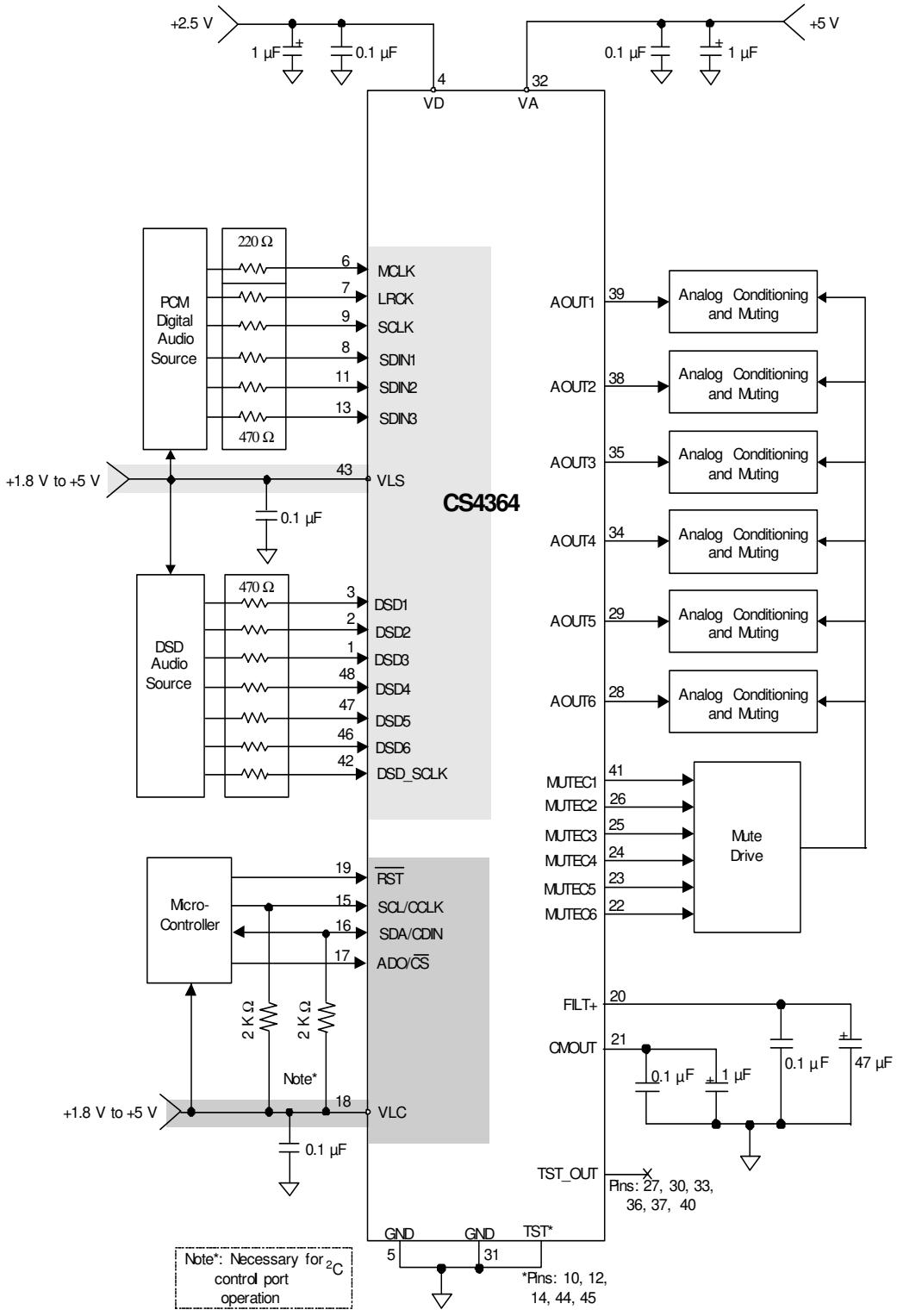


Figure 6. Typical Connection Diagram, Software Mode

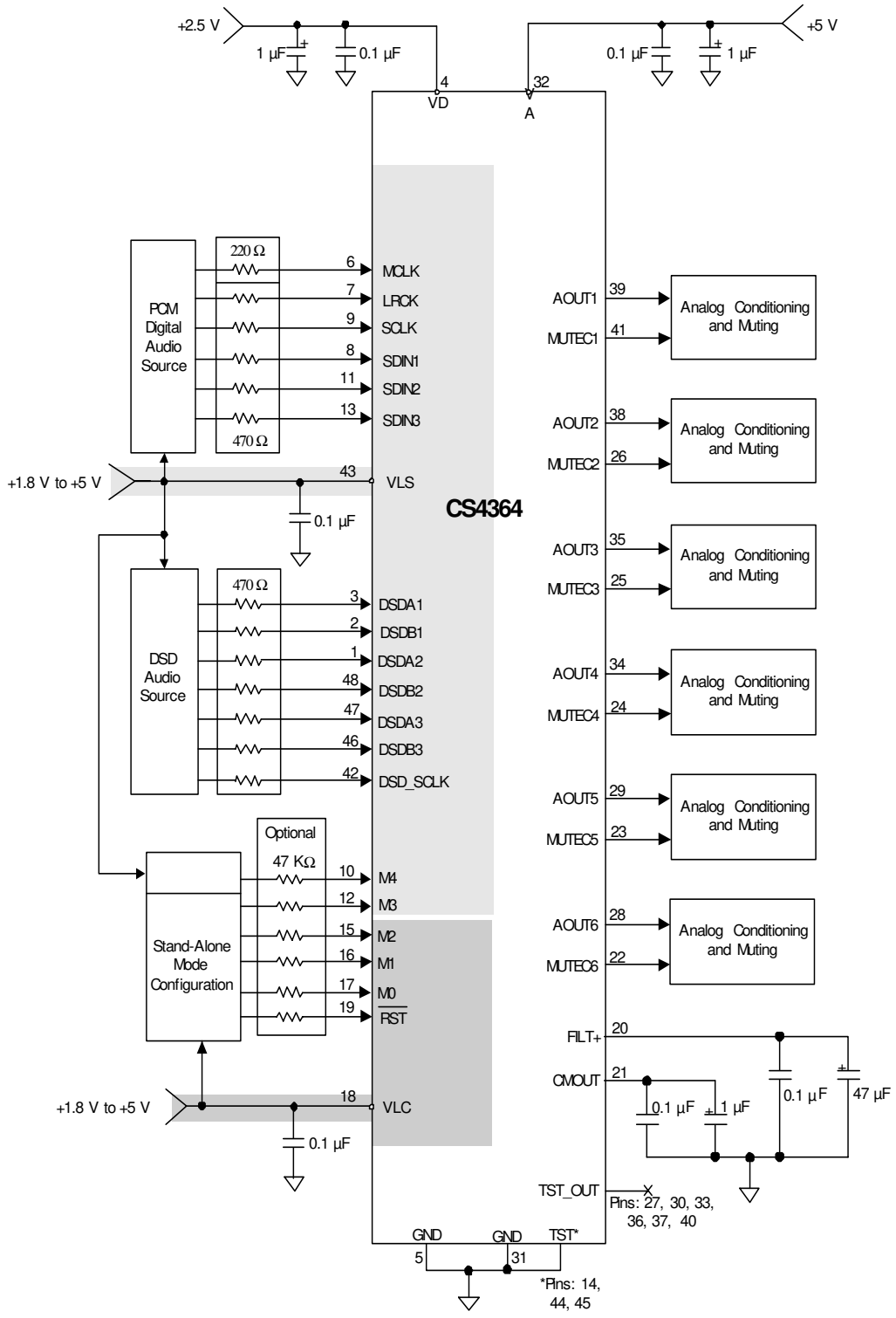


Figure 7. Typical Connection Diagram, Hardware Mode

4. APPLICATIONS

The CS4364 serially accepts twos complement formatted PCM data at standard audio sample rates including 48, 44.1 and 32 kHz in SSM, 96, 88.2 and 64 kHz in DSM, and 192, 176.4 and 128 kHz in QSM. Audio data is input via the serial data input pins (SDINx). The Left/Right Clock (LRCK) determines which channel is currently being input on SDINx, and the Serial Clock (SCLK) clocks audio data into the input data buffer. For more information on serial audio interfaces see AN282 “The 2-Channel Serial Audio Interface: A Tutorial”.

The CS4364 can be configured in Hardware Mode by the M0, M1, M2, M3 and M4 pins and in Software Mode through I²C or SPI.

4.1 Master Clock

MCLK/LRCK must be an integer ratio as shown in Tables 1 - 3. The LRCK frequency is equal to Fs, the frequency at which words for each channel are input to the device. The MCLK-to-LRCK frequency ratio and speed mode is detected automatically during the initialization sequence by counting the number of MCLK transitions during a single LRCK period and by detecting the absolute speed of MCLK. Internal dividers are then set to generate the proper internal clocks. Tables 1 - 3 illustrate several standard audio sample rates and the required MCLK and LRCK frequencies. Please note there is no required phase relationship, but MCLK, LRCK and SCLK must be synchronous.

Sample Rate (kHz)	MCLK (MHz)					
	256x	384x	512x	768x	1024x	1152x
32	8.1920	12.2880	16.3840	24.5760	32.7680	36.8640
44.1	11.2896	16.9344	22.5792	33.8688	45.1584	
48	12.2880	18.4320	24.5760	36.8640	49.1520	

Table 1. Single-Speed Mode Standard Frequencies

Sample Rate (kHz)	MCLK (MHz)				
	128x	192x	256x	384x	512x
64	8.1920	12.2880	16.3840	24.5760	32.7680
88.2	11.2896	16.9344	22.5792	33.8688	45.1584
96	12.2880	18.4320	24.5760	36.8640	49.1520

Table 2. Double-Speed Mode Standard Frequencies

Sample Rate (kHz)	MCLK (MHz)				
	64x	96x	128x	192x	256x
176.4	11.2896	16.9344	22.5792	33.8688	45.1584
192	12.2880	18.4320	24.5760	36.8640	49.1520

Table 3. Quad-Speed Mode Standard Frequencies

= Denotes clock ratio and sample rate combinations which are NOT supported under auto speed-mode detection. Please see “Switching Characteristics - PCM” on page 14.

4.2 Mode Select

In Hardware Mode, operation is determined by the Mode Select pins. The states of these pins are continually scanned for any changes; however, the mode should only be changed while the device is in reset ($\overline{RST}$ pin low) to ensure proper switching from one mode to another. These pins require connection to supply or ground as outlined in Figure 7. For M0, M1, and M2, supply is VLC. For M3 and M4, supply is VLS. Tables 4 - 6 show the decode of these pins.

In Software Mode, the operational mode and data format are set in the FM and DIF registers. See "PCM Control (Address 03h)" on page 34.

M1 (DIF1)	M0 (DIF0)	DESCRIPTION	FORMAT	FIGURE
0	0	Left Justified, up to 24-bit data	0	8
0	1	I^2S, up to 24-bit data	1	9
1	0	Right Justified, 16-bit Data	2	10
1	1	Right Justified, 24-bit Data	3	11

Table 4. PCM Digital Interface Format, Hardware Mode Options

M4	M3	M2 (DEM)	M1	M0	DESCRIPTION
0	0	0	Table 4		Single-Speed without De-Emphasis (4 kHz to 50 kHz sample rates)
0	0	1			Single-Speed with 44.1 kHz De-Emphasis; see Figure 16
0	1	0			Double-Speed (50 kHz to 100 kHz sample rates)
0	1	1			Quad-Speed (100 kHz to 200 kHz sample rates)
1	0	0			Auto Speed-Mode Detect (32 kHz to 200 kHz sample rates)
1	0	1			Auto Speed-Mode Detect with 44.1 kHz De-Emphasis; see Figure 16
1	1	Table 6			DSD Processor Mode

Table 5. Mode Selection, Hardware Mode Options

M2	M1	M0	DESCRIPTION
0	0	0	64x oversampled DSD data with a 4x MCLK to DSD data rate
0	0	1	64x oversampled DSD data with a 6x MCLK to DSD data rate
0	1	0	64x oversampled DSD data with a 8x MCLK to DSD data rate
0	1	1	64x oversampled DSD data with a 12x MCLK to DSD data rate
1	0	0	128x oversampled DSD data with a 2x MCLK to DSD data rate
1	0	1	128x oversampled DSD data with a 3x MCLK to DSD data rate
1	1	0	128x oversampled DSD data with a 4x MCLK to DSD data rate
1	1	1	128x oversampled DSD data with a 6x MCLK to DSD data rate

Table 6. Direct Stream Digital (DSD), Hardware Mode Options

4.3 Digital Interface Formats

The serial port operates as a slave and supports the I²S, Left-Justified, Right-Justified, and One-Line Mode (OLM) digital interface formats with varying bit depths from 16 to 32 as shown in Figures 8-15. Data is clocked into the DAC on the rising edge. OLM configurations are only supported in Software Mode.

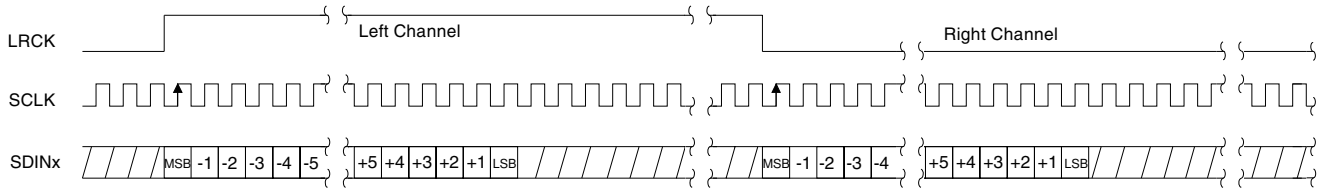


Figure 8. Format 0 - Left-Justified up to 24-bit Data

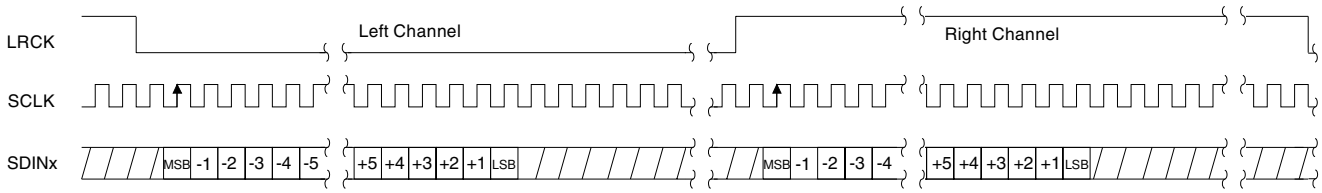


Figure 9. Format 1 - I²S up to 24-bit Data

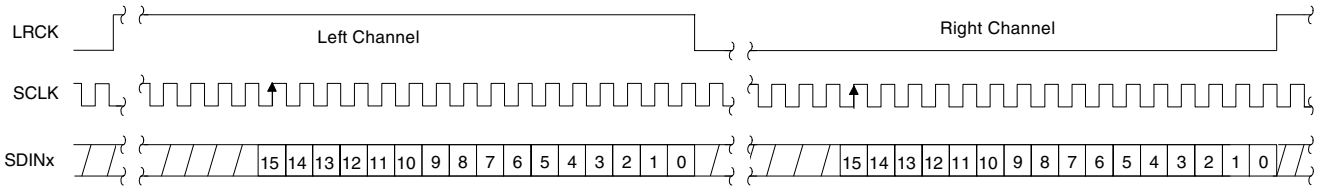


Figure 10. Format 2 - Right-Justified 16-bit Data

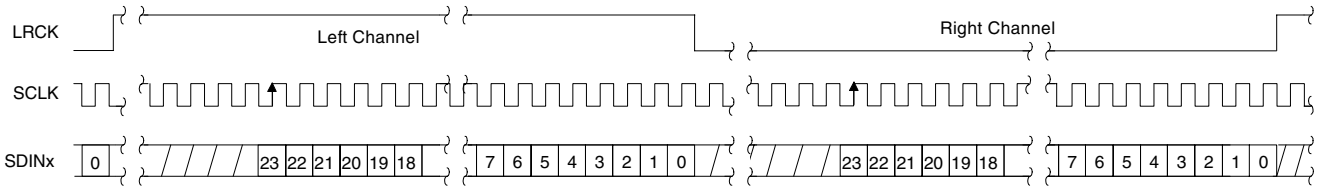


Figure 11. Format 3 - Right-Justified 24-bit Data

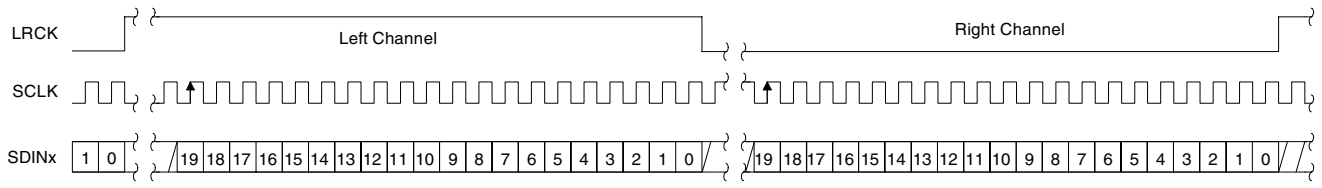


Figure 12. Format 4 - Right-Justified 20-bit Data

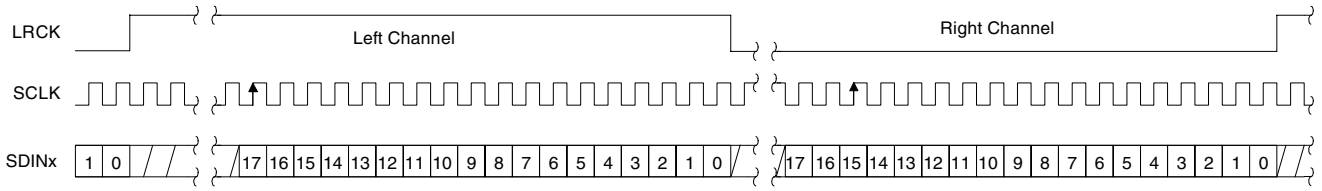


Figure 13. Format 5 - Right-Justified 18-bit Data

4.3.1 OLM #1

OLM #1 serial audio interface format operates in Single-, Double-, or Quad-Speed Mode and will slave to SCLK at 128 Fs. Six channels of MSB first 20-bit PCM data are input on SDIN1.

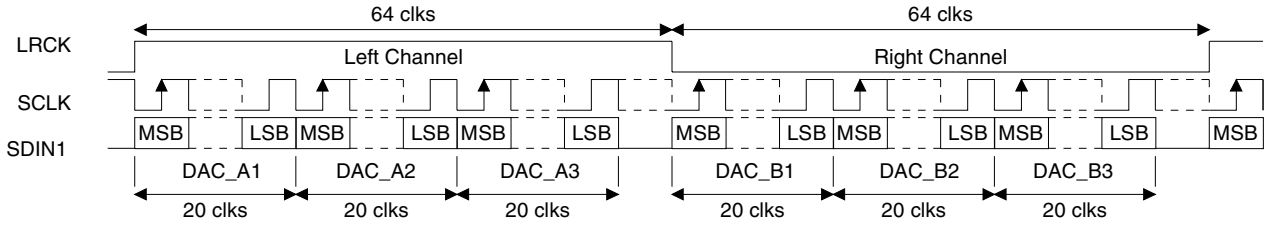


Figure 14. Format 8 - One Line Mode 1

4.3.2 OLM #2

OLM #2 serial audio interface format operates in Single-, Double-, or Quad-Speed Mode and will slave to SCLK at 256 Fs. Six channels of MSB first 24-bit PCM data are input on SDIN1.

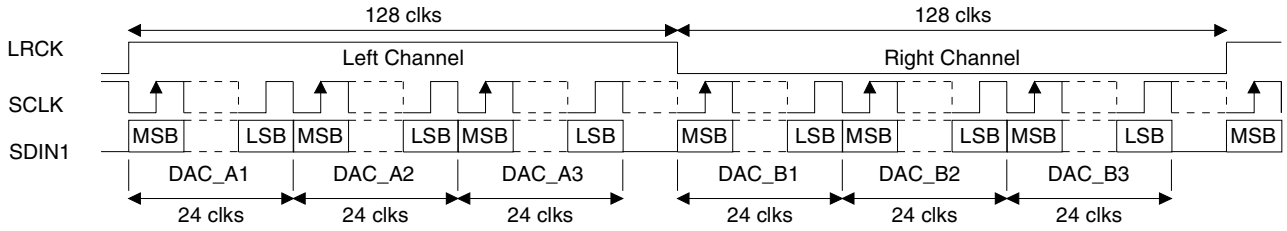


Figure 15. Format 9 - One Line Mode 2

4.4 Oversampling Modes

The CS4364 operates in one of three oversampling modes based on the input sample rate. Mode selection is determined by the M4, M3 and M2 pins in Hardware Mode or the FM bits in Software Mode. Single-Speed Mode supports input sample rates up to 50 kHz and uses a 128x oversampling ratio. Double-Speed Mode supports input sample rates up to 100 kHz and uses an oversampling ratio of 64x. Quad-Speed Mode supports input sample rates up to 200 kHz and uses an oversampling ratio of 32x.

The auto speed-mode detect feature allows for the automatic selection of speed mode based off of the incoming sample rate. This allows the CS4364 to accept a wide range of sample rates with no external intervention necessary. The auto speed-mode detect feature is available in both Hardware and Software Mode.

4.5 Interpolation Filter

To accommodate the increasingly complex requirements of digital audio systems, the CS4364 incorporates selectable interpolation filters for each mode of operation. A “fast” and a “slow” roll-off filter is available in each of Single-, Double-, or Quad-Speed Modes. These filters have been designed to accommodate a variety of musical tastes and styles. The FILT_SEL bit is used to select which filter is used (see the “Parameter Definitions” on page 47 for more details).

When in Hardware Mode, only the “fast” roll-off filter is available.

Filter specifications can be found in Section 2, and filter response plots can be found in Figures 24 to 47.

4.6 De-Emphasis

The CS4364 includes on-chip digital de-emphasis filters. The de-emphasis feature is included to accommodate older audio recordings that utilize pre-emphasis equalization as a means of noise reduction. Figure 16 shows the de-emphasis curve. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, Fs if the input sample rate does not match the coefficient which has been selected.

In Software Mode the required de-emphasis filter coefficients for 32 kHz, 44.1 kHz, or 48 kHz are selected via the de-emphasis control bits.

In Hardware Mode only the 44.1 kHz coefficient is available (enabled through the M2 pin). If the input sample rate is not 44.1 kHz and de-emphasis has been selected then the corner frequencies of the de-emphasis filter will be scaled by a factor of the actual Fs over 44,100.

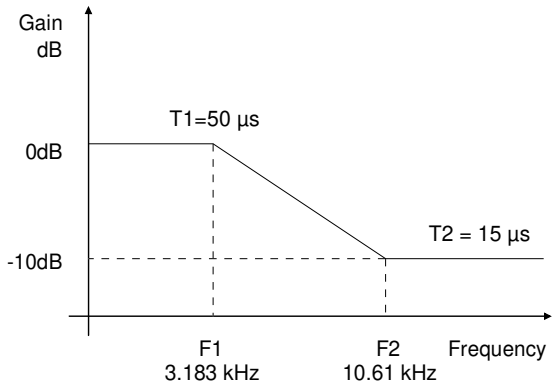


Figure 16. De-Emphasis Curve

4.7 ATAPI Specification

The CS4364 implements the channel mixing functions of the ATAPI CD-ROM specification. The ATAPI functions are applied per A-B pair. Refer to Table 9 on page 41 and Figure 17 for additional information.

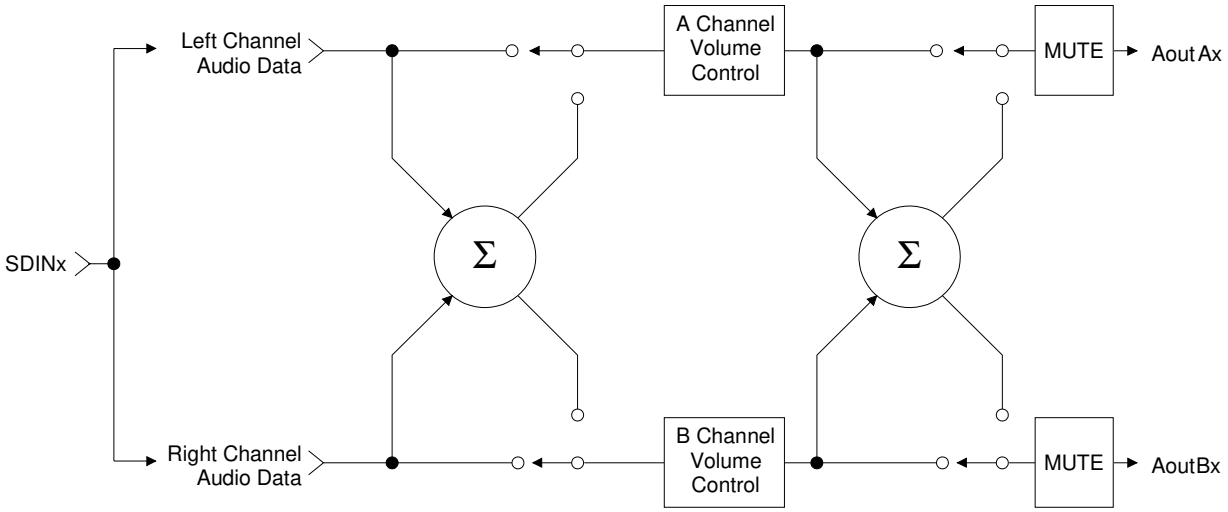


Figure 17. ATAPI Block Diagram (x = channel pair 1, 2, or 3)

4.8 Direct Stream Digital (DSD) Mode

In Software Mode the DSD/$\overline{\text{PCM}}$ bits (Reg. 02h) are used to configure the device for DSD mode. The DSD_DIF bits (Reg 04h) then control the expected DSD rate and MCLK ratio.

The DIR_DSD bit (Reg 04h) selects between two proprietary methods for DSD to analog conversion. The first method uses a decimation free DSD processing technique which allows for features such as matched PCM level output, DSD volume control, and 50kHz on chip filter. The second method sends the DSD data directly to the on-chip switched-capacitor filter for conversion (without the above mentioned features).

The DSD_PM_EN bit (Reg. 04h) selects Phase Modulation (data plus data inverted) as the style of data input. In this mode the DSD_PM_Mode bit selects whether a 128Fs or 64x clock is used for phase modulated 64x data (see Figure 18). Use of Phase Modulation Mode may not directly effect the performance of the CS4364, but may lower the sensitivity to board level routing of the DSD data signals.

The CS4364 can detect errors in the DSD data which does not comply with the SACD specification. The STATIC_DSD and INVALID_DSD bits (Reg. 04h) allow the CS4364 to alter the incoming invalid DSD data. Depending on the error, the data may either be attenuated or replaced with a muted DSD signal (the MUTEC pins would be set according to the DAMUTE bit (Reg. 08h)).

More information for any of these register bits can be found in the "Parameter Definitions" on page 47.

The DSD input structure and analog outputs are designed to handle a nominal 0 dB-SACD (50% modulation index) at full rated performance. Signals of +3 dB-SACD may be applied for brief periods of time however, performance at these levels is not guaranteed. If sustained +3 dB-SACD levels are required, the digital volume control should be set to -3.0 dB. This same volume control register affects PCM output levels. There is no need to change the volume control setting between PCM and DSD in order to have the 0 dB output levels match (both 0 dBFS and 0 dB-SACD will output at -3 dB in this case).