Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

CS4373A

Low-power, High-performance ΔΣ Test DAC

Features

- Digital ΔΣ Input from CS5376A Digital Filter
- Selectable Differential Analog Outputs
  - Precision output (OUT±) for electronics tests
  - Buffered output (BUF±) for sensor tests
- Multiple AC and DC Operational Modes
  - Signal bandwidth: DC to 100 Hz
  - Max AC amplitude: 5 V_{PP} differential
  - Max DC amplitude: + 2.5 V_{dc} differential
- Selectable Attenuation for CS3301A / CS3302A
  - 1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64
- Outstanding Performance
  - AC (OUT): -116 dB THD typical, -112 dB max
  - AC (BUF): -108 dB THD typical, -90 dB max
  - DC absolute accuracy: 0.4% typical, 1% max
- Low Power Consumption
  - AC modes / DC modes: 40 mW / 20 mW
  - Sleep mode / Power Down: 1 mW / 10 µW
- Extremely Small Footprint
  - 28-pin SSOP package, 8 mm x 10 mm
- Bipolar Power Supply Configuration
  - VA+ = +2.5 V;VA- = -2.5 V; VD = +3.3 V

Description

The CS4373A is a high-performance, differential output digital-to-analog converter (DAC) with programmable attenuation and multiple operational modes. AC test modes measure system dynamic performance through THD and CMRR tests while DC test modes are for gain calibration and pulse tests.

The CS4373A is driven by a ΔΣ digital bit stream from the CS5376A digital filter test bit stream (TBS) generator. It has two sets of differential analog outputs, *OUT* and *BUF*, to simplify system design as dedicated outputs for testing the electronics channel and for in-circuit sensor tests. Analog output attenuation is selected by simple pin settings and matches the gain of the CS3301A / CS3302A differential amplifiers for full-scale testing at all gain ranges.

The CS4373A test DAC provides self-test and precision calibration capability for high-resolution, low-frequency multi-channel measurement systems designed from CS3301A / CS3302A differential amplifiers, CS5371A / CS5372A ΔΣ modulators and the CS5376A digital filter.

ORDERING INFORMATION

See page 34.

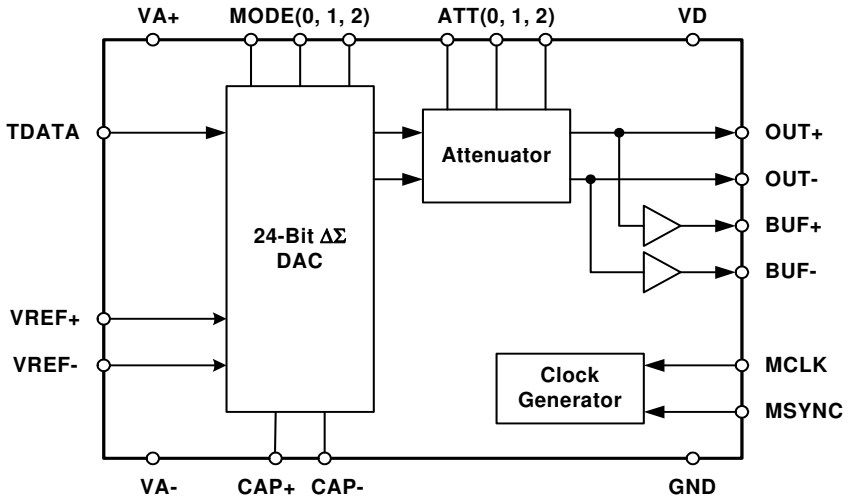

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. CHARACTERISTICS AND SPECIFICATIONS

- Min / Max characteristics and specifications are guaranteed over the *Specified Operating Conditions*.
- Typical performance characteristics and specifications are measured at nominal supply voltages and T_A = 25°C.
- GND = 0 V. Single-ended voltages with respect to GND, differential voltages with respect to opposite half.
- Device is connected as shown in Figure 6 on page 17, unless otherwise noted.

SPECIFIED OPERATING CONDITIONS

Parameter		Symbol	Min	Nom	Max	Unit
Bipolar Power Supplies						
Positive Analog	±2%	VA+	2.45	2.50	2.55	V
Negative Analog	(Note 1) ±2%	VA-	-2.45	-2.50	-2.55	V
Positive Digital	±3%	VD	3.20	3.30	3.40	V
Voltage Reference Input						
{VREF+} - {VREF-}	(Note 2, 3)	VREF	-	2.500	-	V
VREF-	(Note 4)	VREF-	-	VA -	-	V
Thermal						
Ambient Operating Temperature	Industrial (-IS, -ISZ)	T_A	-40	25	85	°C

Notes: 1. VA- must always be the most-negative input voltage to avoid potential SCR latch-up conditions.
2. By design, a 2.500 V voltage reference input results in the best signal-to-noise performance.
3. Full-scale accuracy is directly proportional to the voltage reference absolute accuracy.
4. VREF inputs must satisfy: VA- ≤ VREF- < VREF+ ≤ VA+.

Modes of Operation		
Selection	**MODE[2:0]**	**Mode Description**
0	0 0 0	Sleep mode.
1	0 0 1	AC OUT and BUF outputs.
2	0 1 0	AC OUT only, BUF high-z.
3	0 1 1	AC BUF only, OUT high-z.
4	1 0 0	DC common mode output.
5	1 0 1	DC differential output.
6	1 1 0	AC common mode output.
7	1 1 1	Sleep mode.

Attenuation			
Selection	**ATT[2:0]**	**Attenuation**	**dB**
0	0 0 0	1/1	0 dB
1	0 0 1	1/2	-6.02 dB
2	0 1 0	1/4	-12.04 dB
3	0 1 1	1/8	-18.06 dB
4	1 0 0	1/16	-24.08 dB
5	1 0 1	1/32	-30.10 dB
6	1 1 0	1/64	-36.12 dB
7	1 1 1	reserved	reserved

Table 1. Selections for Operational Mode and Attenuation

TEMPERATURE CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Operating Temperature	T_A	-40	-	+85	ºC
Storage Temperature Range	T_{STG}	-65	-	150	ºC
Allowable Junction Temperature	T_{JCT}	-	-	125	ºC
Junction to Ambient Thermal Impedance (4-layer PCB)	Θ_{JA}	-	65	-	ºC / W

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Parameter
DC Power Supplies	Positive Analog	VA+	-0.5	6.8	V
	Negative Analog	VA-	-6.8	0.5	V
	Digital	VD	-0.5	6.8	V
Analog Supply Differential	(VA+) - (VA-)	VA_{DIFF}	-	6.8	V
Digital Supply Differential	(VD) - (VA-)	VD_{DIFF}	-	7.6	V
Input Current, Power Supplies	(Note 5)	I_{IN}	-	±50	mA
Input Current, Any Pin Except Supplies	(Note 5)	I_{IN}	-	±10	mA
Output Current	(Note 5)	I_{OUT}	-	±25	mA
Power Dissipation		PDN	-	500	mW
Analog Input Voltages		V_{INA}	(VA-) - 0.5	(VA+) + 0.5	V
Digital Input Voltages		V_{IND}	-0.5	(VD) + 0.5	V

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 5. Transient currents up to ±100 mA will not cause SCR latch-up.

ANALOG CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
VREF Input						
{VREF+} - {VREF-}	(Note 2, 3)	VREF	-	2.500	-	V
VREF-	(Note 4)	VREF-	-	VA -	-	V
VREF Input Current, AC modes		$VREF_{IAC}$	-	80	-	µA
VREF Input Current, DC modes		$VREF_{IDC}$	-	40	-	µA
VREF Input Noise	(Note 6)	$VREF_{IN}$	-	-	1	μV_{rms}
Analog OUT± Output						
Analog External Load at OUT± (Note 7, 8)	Load Resistance Load Capacitance	R_{LOUT} C_{LOUT}	50 -	- -	- 50	MΩ pF
Differential Output Impedance	1/1 1/2 1/4 1/8 1/16 1/32 1/64	$ZDIF_{OUT}$	- - - - - - -	1.4 10.1 7.9 5.1 3.3 2.3 1.7	- - - - - - -	kΩ kΩ kΩ kΩ kΩ kΩ kΩ
Single-ended Output Impedance	1/1 1/2 1/4 1/8 1/16 1/32 1/64	ZSE_{OUT}	- - - - - - -	0.7 7.4 9.0 9.4 9.5 9.5 9.4	- - - - - - -	kΩ kΩ kΩ kΩ kΩ kΩ kΩ
High-Z Impedance	(Note 8)	HZ_{OUT}	-	3	-	MΩ
Crosstalk to BUF± High-Z Output	(Note 8)	XT_{OUT}	-	-120	-	dB
Analog BUF± Output						
Analog External Load at BUF± (Note 8)	Load Resistance Load Capacitance	R_{LBUF} C_{LBUF}	1 -	- -	- 2	kΩ nF
Differential Output Impedance	1/1 - 1/64	$ZDIF_{BUF}$	-	6	-	Ω
Single-ended Output Impedance	1/1 - 1/32 (Note 9) (BUF-) 1/64 (Note 9) (BUF+) 1/64	ZSE_{BUF}	- - -	3 3 50	- - -	Ω
High-Z Impedance	(Note 8)	HZ_{BUF}	-	4.5	-	MΩ
Crosstalk to OUT± High-Z Output	(Note 8)	XT_{BUF}	-	-120	-	dB

Notes:
6. Maximum integrated noise over the measurement bandwidth for the voltage reference device attached to the VREF± inputs.
7. Load on the precision OUT± outputs is normally from the CS3301A / CS3302A amplifiers, which have 1 GΩ/1 TΩ typical input impedance and 18 pF typical input capacitance.
8. Guaranteed by design and/or characterization.
9. Single-ended output impedance at 1/64 is different for BUF+ and BUF- due to the output attenuator architecture.

AC DIFFERENTIAL MODES 1, 2, 3

Parameter		Symbol	Min	Typ	Max	Unit
AC Differential Characteristics						
Full-scale Differential AC Output	1/1	VAC_{FS}	-	5	-	V_{pp}
	1/2		-	2.5	-	V_{pp}
	1/4		-	1.25	-	V_{pp}
	1/8		-	625	-	mV_{pp}
	1/16		-	312.5	-	mV_{pp}
	1/32		-	156.25	-	mV_{pp}
	1/64		-	78.125	-	mV_{pp}
Full-scale Bandwidth	(Note 8)	VAC_{BW}	-	-	100	Hz
Impulse Amplitude	(Note 8, 10)	VAC_{IMP}	-	-	-20	dBfs
AC Differential Accuracy						
Full-scale Accuracy (Note 3, 11)	1/1	VAC_{ABS}	- 0.5	- 0.2	0.2	%FS
Relative Accuracy (Note 12)	1/2	VAC_{REL}	- 0.2	± 0.1	0.2	%
	1/4		-	± 0.1	-	%
	1/8		-	± 0.1	-	%
	1/16		-	- 0.1 ± 0.2	-	%
	1/32		-	- 0.2 ± 0.3	-	%
	1/64		-	- 0.5 ± 0.5	-	%
Full-scale Drift	(Note 14)	VAC_{TC}	-	25	-	µV/°C
DC Common Mode Characteristics						
Common Mode	(Note 13)	VAC_{CM}	-	(VA-)+2.35	-	V
Common Mode Drift	(Note 13, 14)	VAC_{CMTC}	-	300	-	µV/°C

Notes: 10. Maximum amplitude for operation above 100 Hz. A reduced amplitude for higher frequencies is required to guarantee stability of the low-power delta-sigma architecture.

11. Full-scale accuracy compares the defined full-scale 1/1 amplitude to the measured 1/1 amplitude. Specification is for unloaded outputs. Applying a differential load lowers the output amplitude ratiometric to the differential output impedance.

12. Relative accuracy compares the measured 1/2,1/4,1/8,1/16,1/32,1/64 amplitude to the measured 1/1 amplitude.

13. Common mode voltage is defined as [(SIG+) + (SIG-)] / 2.

14. Specification is for the parameter over the specified temperature range and is for the device only. It does not include the effects of external components.

AC DIFFERENTIAL MODES 1, 2, 3 (CONT.)

Parameter		Symbol	Min	Typ	Max	Unit
Signal to Noise						
Signal to Noise	1/1 -> 1x	SNR_{OUT}	-	114	-	dB
(OUT± Unloaded)	1/2 -> 2x		-	114	-	dB
(Note 15)	1/4 -> 4x		-	114	-	dB
	1/8 -> 8x		-	113	-	dB
	1/16 -> 16x		-	111	-	dB
	1/32 -> 32x		-	108	-	dB
	1/64 -> 64x		-	103	-	dB
Signal to Noise	1/1 -> 1x	SNR_{BUF}	-	110	-	dB
(BUF± Unloaded, 1 kΩ Load)	1/2 -> 2x		-	106	-	dB
(Note 15, 16)	1/4 -> 4x		-	101	-	dB
	1/8 -> 8x		-	95	-	dB
	1/16 -> 16x		-	89	-	dB
	1/32 -> 32x		-	83	-	dB
	1/64 -> 64x		-	77	-	dB
Total Harmonic Distortion						
Total Harmonic Distortion	1/1 -> 1x	THD_{OUT}	-	- 116	- 112	dB
(OUT± Unloaded)	1/2 -> 2x		-	- 115	-	dB
(Note 17, 18)	1/4 -> 4x		-	- 114	-	dB
	1/8 -> 8x		-	- 112	-	dB
	1/16 -> 16x		-	- 111	-	dB
	1/32 -> 32x		-	- 110	-	dB
	1/64 -> 64x		-	- 106	-	dB
Total Harmonic Distortion	1/1 -> 1x	THD_{BUF}	-	- 108	- 90	dB
(BUF± Unloaded)	1/2 -> 2x		-	- 105	-	dB
(Note 16, 17, 18)	1/4 -> 4x		-	- 100	-	dB
	1/8 -> 8x		-	- 94	-	dB
	1/16 -> 16x		-	- 88	-	dB
	1/32 -> 32x		-	- 82	-	dB
	1/64 -> 64x		-	- 76	-	dB
Total Harmonic Distortion	1/1 -> 1x	THD_{BUFL}	-	- 102	- 80	dB
(BUF± 1 kΩ Load)	1/2 -> 2x		-	- 101	-	dB
(Note 16, 17, 18)	1/4 -> 4x		-	- 97	-	dB
	1/8 -> 8x		-	- 92	-	dB
	1/16 -> 16x		-	- 87	-	dB
	1/32 -> 32x		-	- 82	-	dB
	1/64 -> 64x		-	- 76	-	dB

Notes: 15. Specification measured using CS3301A amplifier at corresponding gain with the CS5371A / CS5372A modulator measuring a 430 Hz bandwidth. Amplified noise dominates for x16, x32, x64 amplifier gains.

16. Buffered outputs (BUF±) include 1/f noise not present on the precision outputs (OUT±).

17. Tested with a 31.25 Hz sine wave at -1 dB amplitude.

18. Specification measured using CS3301A amplifier at corresponding gain using the CS5371A / CS5372A modulator measuring a 430 Hz bandwidth. Amplified noise in the harmonic bins dominates THD measurements for x16, x32, x64 amplifier gains.

DC COMMON MODE 4

Parameter		Symbol	Min	Typ	Max	Unit
DC Common Mode Characteristics						
Common Mode Output		VDC_{CM}	-	(VA-)+2.35	-	V
Common Mode Drift	(Note 14)	VDC_{CMTC}	-	300	-	µV/°C
DC Common Mode Accuracy						
Common Mode Match	1/1	VDC_{CMM}	- 5	± 1	5	mV
Noise						
Noise (OUT± Unloaded)	1/1 -> 1x	N_{OUT}	-	6	-	μV_{rms}
(Note 15)	1/2 -> 2x		-	7	-	μV_{rms}
	1/4 -> 4x		-	7	-	μV_{rms}
	1/8 -> 8x		-	7	-	μV_{rms}
	1/16 -> 16x		-	7	-	μV_{rms}
	1/32 -> 32x		-	9	-	μV_{rms}
	1/64 -> 64x		-	14	-	μV_{rms}
Noise (BUF± Unloaded, 1 kΩ Load)	1/1 -> 1x	N_{BUF}	-	7	-	μV_{rms}
(Note 15, 16)	1/2 -> 2x		-	10	-	μV_{rms}
	1/4 -> 4x		-	17	-	μV_{rms}
	1/8 -> 8x		-	33	-	μV_{rms}
	1/16 -> 16x		-	64	-	μV_{rms}
	1/32 -> 32x		-	130	-	μV_{rms}
	1/64 -> 64x		-	257	-	μV_{rms}

DC DIFFERENTIAL MODE 5

Parameter		Symbol	Min	Typ	Max	Unit
DC Differential Mode Characteristics						
Full-scale Differential DC Output (Note 19)	1/1	VDC_{FS}	-	2.5	-	V
	1/2		-	1.25	-	V
	1/4		-	625	-	mV
	1/8		-	312.5	-	mV
	1/16		-	156.25	-	mV
	1/32		-	78.125	-	mV
	1/64		-	39.0625	-	mV
DC Differential Accuracy						
Full-scale Accuracy (Note 3, 11)	1/1	VDC_{ABS}	- 1.0	- 0.4	0.2	%FS
Relative Accuracy (Note 12)	1/2	VDC_{REL}	- 0.2	± 0.1	0.2	%
	1/4		-	± 0.1	-	%
	1/8		-	-0.1 ± 0.4	-	%
	1/16		-	-0.2 ± 0.9	-	%
	1/32		-	-0.5 ± 1.7	-	%
	1/64		-	-1.0 ± 3.6	-	%
Full-scale Drift	(Note 14)	VDC_{TC}	-	25	-	µV/°C
DC Common Mode Characteristics						
Common Mode	(Note 13)	VDC_{CM}	-	(VA-)+2.35	-	V
Common Mode Drift	(Note 13, 14)	VDC_{CMTC}	-	300	-	µV/°C
Noise						
Noise (OUT± Unloaded) (Note 15, 19)	1/1 -> 1x	N_{OUT}	-	9	-	μV_{rms}
	1/2 -> 2x		-	9	-	μV_{rms}
	1/4 -> 4x		-	9	-	μV_{rms}
	1/8 -> 8x		-	9	-	μV_{rms}
	1/16 -> 16x		-	10	-	μV_{rms}
	1/32 -> 32x		-	11	-	μV_{rms}
	1/64 -> 64x		-	15	-	μV_{rms}
Noise (BUF± Unloaded, 1 kΩ Load) (Note 15, 16, 19)	1/1 -> 1x	N_{BUF}	-	10	-	μV_{rms}
	1/2 -> 2x		-	12	-	μV_{rms}
	1/4 -> 4x		-	18	-	μV_{rms}
	1/8 -> 8x		-	32	-	μV_{rms}
	1/16 -> 16x		-	67	-	μV_{rms}
	1/32 -> 32x		-	122	-	μV_{rms}
	1/64 -> 64x		-	265	-	μV_{rms}

Notes: 19. DC differential output is chopper stabilized and includes low-level 32 kHz out-of-band noise which is rejected by the digital filter during acquisition.

AC COMMON MODE 6

Parameter		Symbol	Min	Typ	Max	Unit
AC Common Mode Characteristics						
Full-scale Common Mode AC Output (Note 20)	1/1	VCM_{FS}	-	2.5	-	V_{pp}
	1/2		-	1.25	-	V_{pp}
	1/4		-	625	-	mV_{pp}
	1/8		-	312.5	-	mV_{pp}
	1/16		-	156.25	-	mV_{pp}
	1/32		-	78.125	-	mV_{pp}
Full-scale Bandwidth	(Note 8)	VCM_{BW}	-	-	100	Hz
Impulse Amplitude	(Note 8, 10)	VCM_{IMP}	-	-	-20	dBfs
AC Common Mode Accuracy						
Common Mode Match (OUT± Unloaded) (Note 17, 20)		VCM_{CMM}	-	-115	-105	dB
Common Mode Match (BUF± Unloaded, 1 kΩ Load) (Note 16, 17, 20)		VCM_{CMM}	-	-95	-85	dB
Full-scale Accuracy (Note 3, 11)	1/1	VAC_{ABS}	-	- 0.3	-	%FS
Relative Accuracy (Note 12, 20)	1/2	VAC_{REL}	-	- 0.1	-	%
	1/4		-	- 0.5	-	%
	1/8		-	- 1.0	-	%
	1/16		-	-2.0	-	%
	1/32		-	-5.0	-	%
Full-scale Drift	(Note 14)	VCM_{TC}	-	25	-	µV/°C
DC Common Mode Characteristics						
Common Mode Mean	(Note 21)	VCM_{CM}	-	(VA-)+2.35	-	V
Common Mode Mean Drift	(Note 14, 21)	VCM_{CMTC}	-	300	-	µV/°C

Notes: 20. No AC common mode signal is output at 1/64 attenuation due to the attenuator architecture.

21. Common mode mean is defined as $[(SIG_{max}) + (SIG_{min})] / 2$.

DIGITAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Digital Inputs						
High-level Input Drive Voltage	(Note 22)	V_{IH}	0.6*VD	-	VD	V
Low-level Input Drive Voltage	(Note 22)	V_{IL}	0.0	-	0.8	V
Input Leakage Current		I_{IN}	-	±1	±10	µA
Digital Input Capacitance	(Note 8)	C_{IN}	-	9	-	pF
Rise Times Except MCLK	(Note 8)	t_{RISE}	-	-	100	ns
Fall Times Except MCLK	(Note 8)	t_{FALL}	-	-	100	ns
TDATA Input						
TDATA Input Bit Rate	(Note 23)	f_{tdata}	-	256	-	kbits/s
TDATA Input One's Density Range	(Note 8)	INR_{OD}	25	-	75	%
TBSGAIN Full-scale Code	(Note 24)	TBS_{FS}	-	0x04B8F2	-	
TBSGAIN -20 dB Code	(Note 24)	TBS_{-20dB}	-	0x0078E5	-	

Notes: 22. Device is intended to be driven with CMOS logic levels.

23. TDATA is generated by the test bit stream generator in the CS5376A digital filter.

24. TBSGAIN register value in the CS5376A digital filter.

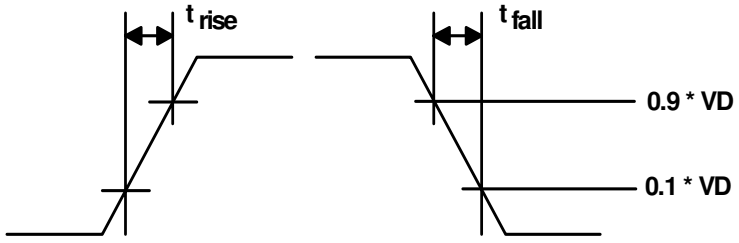

Figure 1. Digital Input Rise and Fall Times

DIGITAL CHARACTERISTICS (CONT.)

Parameter		Symbol	Min	Typ	Max	Unit
Master Clock						
MCLK Frequency	(Note 25)	f_{CLK}	-	2.048	-	MHz
MCLK Period	(Note 25)	t_{mclk}	-	488	-	ns
MCLK Duty Cycle	(Note 8)	$MCLK_{DC}$	40	-	60	%
MCLK Rise Time	(Note 8)	t_{RISE}	-	-	50	ns
MCLK Fall Time	(Note 8)	t_{FALL}	-	-	50	ns
MCLK Jitter (In-band or aliased in-band)	(Note 8)	$MCLK_{IBJ}$	-	-	300	ps
MCLK Jitter (Out-of-band)	(Note 8)	$MCLK_{OBJ}$	-	-	1	ns
Master Sync						
MSYNC Setup Time to MCLK rising	(Note 8, 26)	t_{mss}	20	122	-	ns
MSYNC Period	(Note 8, 26)	t_{msync}	40	976	-	ns
MSYNC Hold Time after MCLK falling	(Note 8, 26)	t_{msh}	20	122	-	ns
MSYNC Instant to TDATA Start	(Note 8, 27)	t_{tdata}	-	1220	-	ns

Notes: 25. MCLK is generated by the CS5376A digital filter. If MCLK is disabled, the device automatically enters a power-down state.

26. MSYNC is generated by the CS5376A digital filter and is latched on MCLK rising edge, synchronization instant ($\mathbf{t_0}$) on next MCLK rising edge.

27. TDATA can be delayed from 0 to 63 full bit periods by the CS5376A test bit stream generator. The timing diagram shows no TBSDATA delay.

DIGITAL CHARACTERISTICS (CONT.)

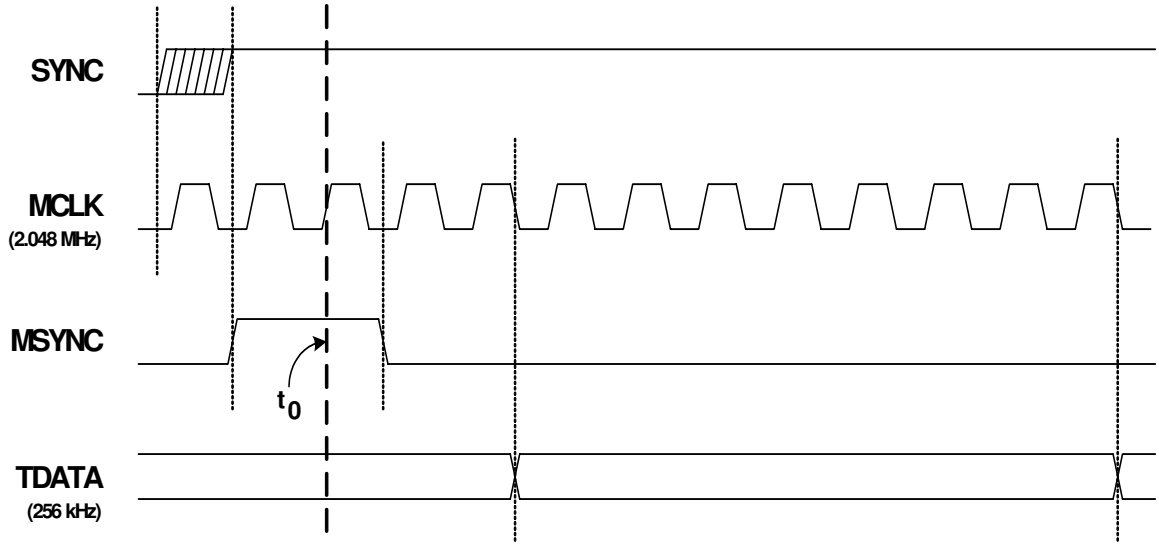

Figure 2. System Timing Diagram

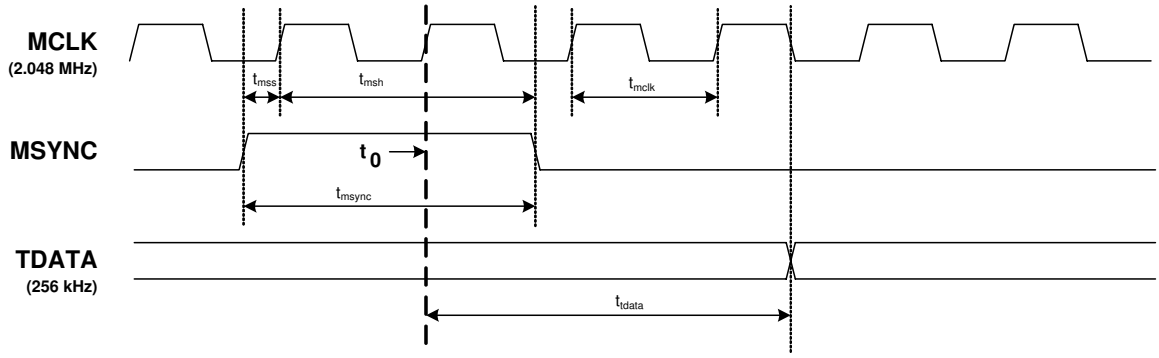

Figure 3. MCLK / MSYNC Timing Detail

POWER SUPPLY CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
AC Mode Supply Current (MODE = 1, 2, 3, 6)						
Analog Power Supply Current	(Note 28)	I_A	-	8	10	mA
Digital Power Supply Current	(Note 28)	I_D	-	20	-	µA
DC Mode Supply Current (MODE = 4)						
Analog Power Supply Current	(Note 28)	I_A	-	2.7	-	mA
Digital Power Supply Current	(Note 28)	I_D	-	20	-	µA
DC Mode Supply Current (MODE = 5)						
Analog Power Supply Current	(Note 28)	I_A	-	4.2	-	mA
Digital Power Supply Current	(Note 28)	I_D	-	20	-	µA
Sleep Mode Supply Current (MODE = 0, 7)						
Analog Power Supply Current	(Note 28)	I_A	-	200	-	µA
Digital Power Supply Current	(Note 28)	I_D	-	260	-	µA
Power Down Supply Current (MCLK = 0)						
Analog Power Supply Current	(Note 28)	I_A	-	1	-	µA
Digital Power Supply Current	(Note 28)	I_D	-	20	-	µA
Time to Enter Power Down (MCLK disabled)	(Note 8)	PD_{TC}	-	40	-	µS
Power Supply Rejection						
Power Supply Rejection Ratio	(Note 29)	PSRR	-	90	-	dB

Notes: 28. All outputs unloaded. Digital inputs forced to VD or DGND respectively.

29. Power supply rejection is characterized by applying a 100 mVp-p 50-Hz sine wave to each supply.

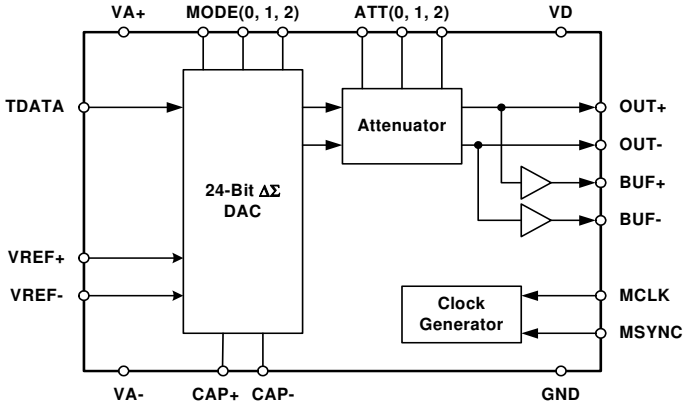

Figure 4. CS4373A Block Diagram

2. GENERAL DESCRIPTION

The CS4373A is a differential output digital-to-analog converter with multiple operational modes and programmable output attenuation. It provides self-test and precision calibration capability for high-resolution, low-frequency measurement systems designed from CS3301A / CS3302A differential amplifiers, CS5371A / CS5372A ΔΣ modulators, and the CS5376A digital filter.

2.1 Digital Inputs

The CS4373A is driven by a ΔΣ digital bit stream from the CS5376A digital filter test bit stream (TBS) generator. The digital filter also provides clock and sync signals as well as GPIO control signals to set the operational mode and attenuation.

2.2 Analog Outputs

Two sets of differential analog outputs, *OUT* and *BUF*, simplify system design as dedicated outputs for testing the electronics channel and for in-circuit sensor tests. Output attenuator settings are binary weighted (1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64) and match the CS3301A / CS3302A amplifier input levels for full-scale testing at all gain ranges.

For maximum performance, the precision outputs (OUT±) must drive only high-impedance loads such as the CS3301A / CS3302A amplifier inputs. The buffered outputs (BUF±) can drive lower-impedance loads, down to 1 kΩ, but with reduced performance compared to the precision outputs.

2.3 Multiple Operational Modes

The CS4373A operates in either AC or DC test modes. AC test modes (MODE 1, 2, 3, 6) are used to measure system THD and CMRR performance. DC test modes (MODE 4, 5) are for gain calibration and pulse tests.

2.4 Low Power

The CS4373A is optimized for low-power operation and has a restricted operational bandwidth in the AC modes. For stable operation, full-scale AC test signals must not contain frequencies above 100 Hz. AC test signals above 100 Hz (TBS impulse mode, for example) must have a -20 dB reduced amplitude to ensure stability of the CS4373A low-power ΔΣ architecture.

3. SYSTEM DIAGRAMS

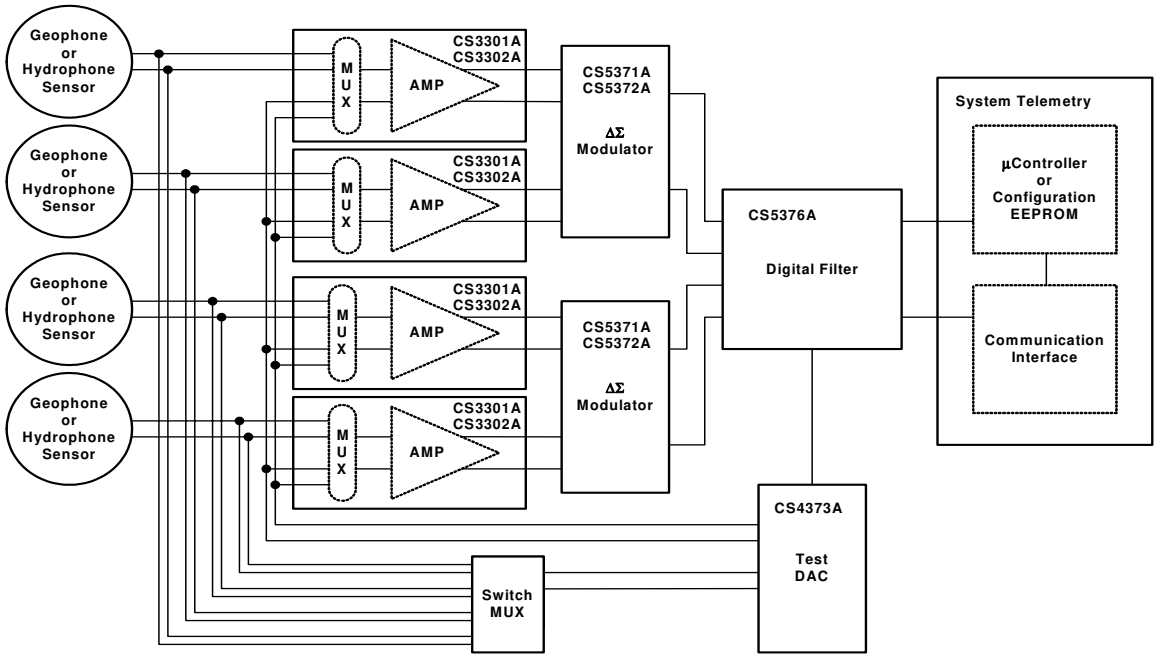

Figure 5. System Diagram

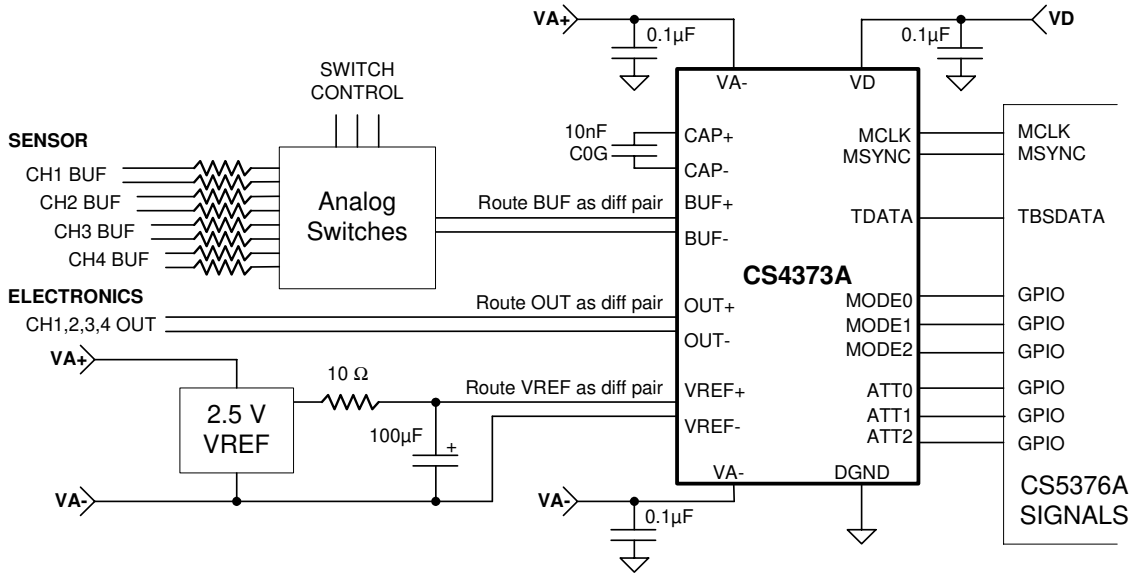

Figure 6. Connection Diagram

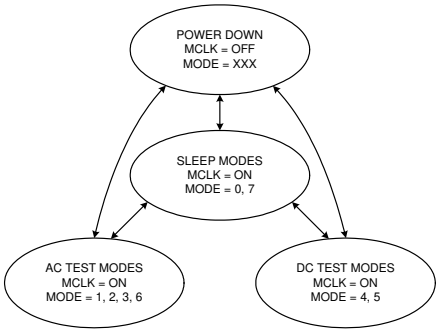

Figure 7. Power Mode Diagram

4. POWER MODES

The CS4373A has four power modes. AC test modes and DC test modes are operational modes, while the power down and sleep modes are non-operational, standby modes.

4.1 Power Down

If MCLK is stopped, an internal loss-of-clock detection circuit automatically places the CS4373A into power down. Power down is independent of the MODE and ATT pin settings, and is automatically invoked after approximately 40 µs without an incoming MCLK edge.

In power down the AC and DC test circuitry is inactive and the analog outputs are high impedance. When used with the CS5376A digital filter, the CS4373A is powered down immediately after reset since MCLK is disabled by default.

4.2 Sleep Modes

With MCLK enabled, selecting either of the sleep modes (MODE 0, 7) places the CS4373A into a micropower sleep state. Following completion of the AC and DC system self-tests, the CS4373A is typically set into sleep mode for normal data acquisition. In sleep mode the AC and DC test circuitry is inactive and the analog outputs are high impedance.

4.3 AC Test Modes

With MCLK and TDATA active, selecting an AC test mode (MODE 1, 2, 3, 6) causes the CS4373A to output AC waveforms on the enabled analog outputs. AC test modes use the low-power $\Delta\Sigma$ circuitry in the CS4373A to create precision differential or common mode analog AC output signals from the encoded digital test bit stream (TBS) input.

4.4 DC Test Modes

With MCLK active, selecting a DC test mode (MODE 4, 5) causes the CS4373A to generate precision DC voltages on the analog outputs. DC test modes use switch-capacitor level-shifting buffer circuitry in the CS4373A to create differential or common mode DC analog output voltages from the voltage reference input.

5. OPERATIONAL MODES

The CS4373A has six operational modes and two sleep modes selected by the MODE2, MODE1, and MODE0 pins.

Selection	MODE[2:0]	Mode Description
0	0 0 0	Sleep mode.
1	0 0 1	AC OUT and BUF outputs.
2	0 1 0	AC OUT only, BUF high-z.
3	0 1 1	AC BUF only, OUT high-z.
4	1 0 0	DC common mode output.
5	1 0 1	DC differential output.
6	1 1 0	AC common mode output.
7	1 1 1	Sleep mode.

Table 2. Operational Modes

5.1 Sleep Modes

Sleep modes (MODE 0, 7) save power during normal acquisition by turning off the AC and DC test circuitry after system self-tests are complete. In sleep mode the *OUT* and *BUF* analog outputs are high impedance.

5.2 AC Test Modes

AC test modes use the digital test bit stream (TBS) input from the CS5376A digital filter to construct analog AC waveforms. The digital bit stream input to the TDATA pin encodes the analog waveform as over-sampled one bit ΔΣ data, which is then converted into precision differential or common mode analog AC signals by the CS4373A.

5.2.1 AC Differential

The first three AC test modes (MODE 1, 2, 3) create precision differential analog signals for THD and impulse testing of the measurement channel. In mode 1, both sets of differential analog outputs (*OUT* and *BUF*) are enabled. In mode 2 only the *OUT* analog output is enabled, and *BUF* is high impedance. In mode 3 only the *BUF* analog output is enabled, and *OUT* is high impedance.

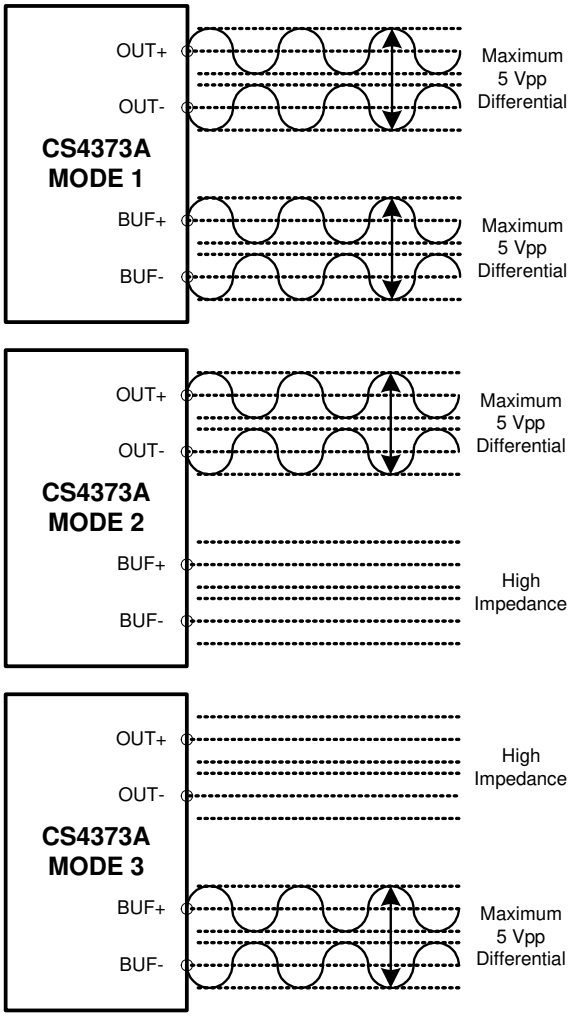

Figure 8. AC Differential Modes

Differential AC signals out of the CS4373A consist of two halves with equal but opposite magnitude, varying about a common mode voltage. A full-scale 5 V_{PP} differential AC signal centered on a -0.15 V common mode voltage will have:

SIG+ = -0.15 V + 1.25 V = +1.1 V

SIG- = -0.15 V - 1.25 V = -1.4 V

SIG+ is +2.5 V relative to SIG-

For the opposite case:

SIG+ = -0.15 V - 1.25 V = -1.4 V

SIG- = -0.15 V + 1.25 V = +1.1 V

SIG+ is -2.5 V relative to SIG-

So the total swing for SIG+ relative to SIG- is (+2.5 V) - (-2.5 V) = 5 V_{pp} differential. A similar calculation can be done for SIG- relative to SIG+. It's important to note that a 5 V_{pp} differential signal centered on a -0.15 V common mode voltage never exceeds +1.1 V with respect to ground and never drops below -1.4 V with respect to ground on either half. By definition, differential voltages are measured with respect to the opposite half, not relative to ground. A voltmeter differentially measuring between SIG+ and SIG- in the above example would read 1.767 V_{rms}, or 5 V_{pp}.

5.2.2 AC Common Mode

The final AC test mode (MODE 6) creates a matched AC common mode analog signal for CMRR testing of the measurement channel. In mode 6, both sets of analog outputs (OUT and BUF) are enabled. There is no common mode AC waveform output for an attenuator setting of 1/64.

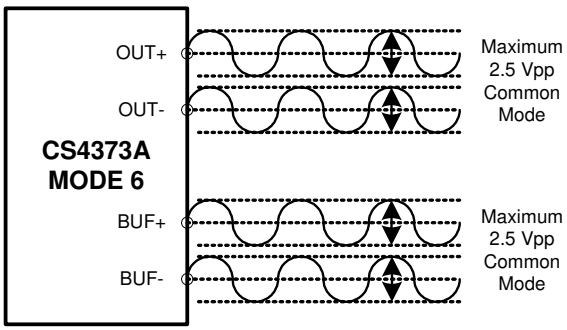

Figure 9. AC Common Mode

Gross leakage in the sensor channel can be detected by applying a full-scale AC common mode signal. If there is a significant differential mismatch in the channel due to sensor leakage, the AC common mode signal will be converted to a measurable differential signal at the fundamental frequency.

5.2.3 AC Stability

For the CS4373A low-power ΔΣ architecture to remain stable, the TDATA input bit stream should only encode 100 Hz or lower bandwidth analog signals. For TDATA bit stream frequencies above 100 Hz (for example, TBS impulse mode), the encoded amplitude must be reduced -20 dB below full scale to guarantee stability.

If the CS4373A low-power ΔΣ architecture becomes unstable, persistent elevated noise will be present on the analog outputs and AC linearity will be poor. To recover stability, place the CS4373A into power down or sleep mode and restart the CS5376A test bit stream generator before placing the CS4373A back into an AC test mode.

5.3 DC Test Modes

DC test modes create precision level-shifted and buffered versions of the voltage reference input as precision DC common mode and DC differential analog outputs. The absolute accuracy of the DC test modes is highly dependent on the absolute accuracy of the voltage reference input voltage.

5.3.1 DC Common Mode

The first DC test mode (MODE 4) creates a matched DC common mode analog output voltage as a baseline measurement for gain calibration and differential pulse tests. In mode 4, both sets of analog outputs (*OUT* and *BUF*) are enabled.

5.3.2 DC Differential

The second DC test mode (MODE 5) creates a precision differential DC analog output voltage as the final measurement for gain calibration and as the step/pulse output for differential pulse tests. In mode 5, both sets of analog outputs (*OUT* and *BUF*) are enabled.

In DC differential output mode (MODE 5) the level-shifting buffer circuitry adds low-level 32 kHz switched-capacitor noise to the DC output. This noise is out of the measurement bandwidth for systems designed with CS3301A / CS3302A amplifiers and CS5371A / CS5372A modulators, and is rejected by the CS5376A digital filter. This 32 kHz switch-capacitor noise does not affect DC system tests, though it may be visible on an oscilloscope at high gain levels.

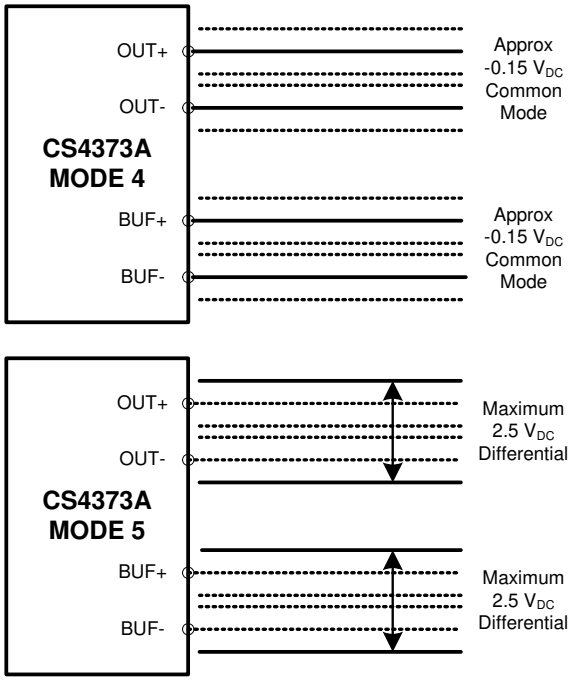

Figure 10. DC Test Modes

By measuring both DC test modes (MODE 4, 5), precision gain-calibration coefficients can be calculated for the measurement channel. By first measuring the differential offset of the DC common mode output (MODE 4) and then measuring the DC differential mode amplitude (MODE 5), a precise offset corrected volts-to-codes conversion ratio can be calculated. This known ratio is then used to normalize the full-scale amplitude using the CS5376A digital filter GAIN registers to match other channels in the measurement network.

By switching between DC common mode (MODE 4) and DC differential mode (MODE 5), pulse waveforms can be created to characterize the step response of the measurement channel. If a pulse test requires precise timing control, an external controller should directly toggle the MODE pins of the CS4373A to avoid delays associated with writing to the CS5376A digital filter GPIO registers.

Sensor impedance can be measured using DC differential mode (MODE 5), provided matched series resistors are installed between the *BUF* analog outputs and the sensor. Applying the known DC differential voltage to the resistor-sensor-resistor string permits a ratiometric sensor impedance calculation from the measured voltage drop across the sensor.

Switching between DC differential mode (MODE 5) and sleep mode (MODE 0, 7) can, in the case of a moving-coil geophone, test basic parameters of the electro-mechanical transfer function. The voltage relaxation characteristic of the sensor when switching the analog outputs from a differential DC voltage to high impedance depends primarily on the geophone resonant frequency and damping factor.

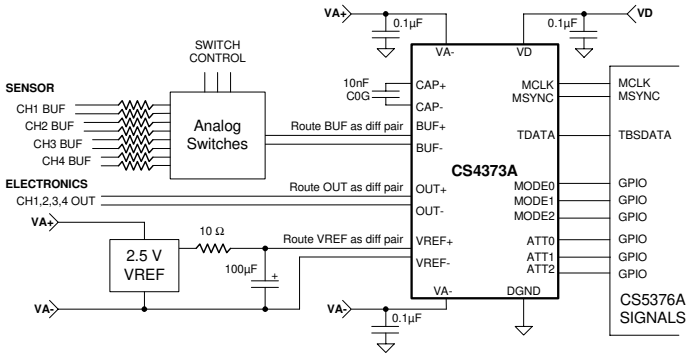

Figure 11. Digital Inputs

6. DIGITAL INPUTS

The CS4373A is designed to operate with the CS5376A digital filter. The digital filter generates one-bit ΔΣ test bit stream data (TDATA), a master clock (MCLK) and a synchronization signal (MSYNC). In addition, the digital filter GPIO pins control the CS4373A operational mode (MODE) and attenuator (ATT) settings.

6.1 TDATA Connection

The TDATA digital input expects encoded one-bit ΔΣ data nominally at a 256 kHz rate. The one's density input range is approximately 25% minimum to 75% maximum, with differential mid-scale at 50% one's density.

The CS5376A digital filter test bit stream (TBS) generator can encode two types of AC signals as over-sampled, one-bit ΔΣ data - a pure sine wave for THD and CMRR testing or a triggerable impulse waveform for synchronization testing and impulse response characterization. In the AC operational modes, the CS4373A converts the over-sampled bit stream digital data into precision differential or common mode analog AC signals.

The CS5376A TBS sine mode encodes an approximately 5 V_{pp} full-scale sine wave signal with a digital filter TBSGAIN register setting of 0x04B8F2. Because TBS impulse mode encodes frequencies above 100 Hz, a maximum 0x0078E5 TBSGAIN impulse mode register setting is specified to guarantee stability of the CS4373A low-power ΔΣ circuitry. Details on the setup and operation of the digital filter TBS generator can be found in the CS5376A data sheet.

6.2 MCLK Connection

The CS5376A digital filter generates the master clock for CS4373A, typically 2.048 MHz, from a synchronous CLK input from the external system. By default, MCLK is disabled at reset and is enabled by writing the digital filter CONFIG register. If MCLK is disabled during operation, the CS4373A will enter power down after approximately 40 µS.

MCLK must have low in-band jitter to guarantee full analog performance, requiring a crystal- or VCXO-based system clock into the digital filter. Clock jitter on the digital filter external CLK input directly translates to jitter on MCLK.

6.3 MSYNC Connection

The CS5376A digital filter also provides a synchronization signal to the CS4373A. The MSYNC signal is generated following a rising edge received on the digital filter SYNC input. By default MSYNC generation is disabled at reset and is enabled by writing to the digital filter CONFIG register.

The input SYNC signal to the CS5376A digital filter sets a common reference time t_0 for mea-

surement events, thereby synchronizing analog sampling across a measurement network. The timing accuracy of the input SYNC signal from measurement node to measurement node must be +/- 1 MCLK to maximize MSYNC analog sample synchronization accuracy.

The CS4373A MSYNC input is rising-edge triggered and resets the internal MCLK counter/divider to guarantee synchronous operation with other system devices. While the MSYNC signal synchronizes the internal operation of the CS4373A, by default, it does not synchronize the phase of the encoded digital test bit stream (TBS) sine wave unless enabled in the digital filter TBSCFG register.

6.4 GPIO Connections

The CS5376A controls 12 general-purpose input output (GPIO) pins through the digital filter GPCFG registers. These GPIO pins are typically assigned to operate the CS4373A mode and attenuator pins, along with the CS3301A / CS3302A amplifiers input mux and gain pins. The gain and attenuation settings of the CS3301A / CS3302A amplifiers and CS4373A are identically decoded to allow full-scale performance testing at all system gain ranges with shared GAIN and ATT control signals.

If precise timing control of operational modes is required (for example, switching between DC modes for pulse generation), an external controller should directly toggle the MODE pins of the CS4373A to avoid the delay associated with writing to the CS5376A digital filter GPCFG registers.

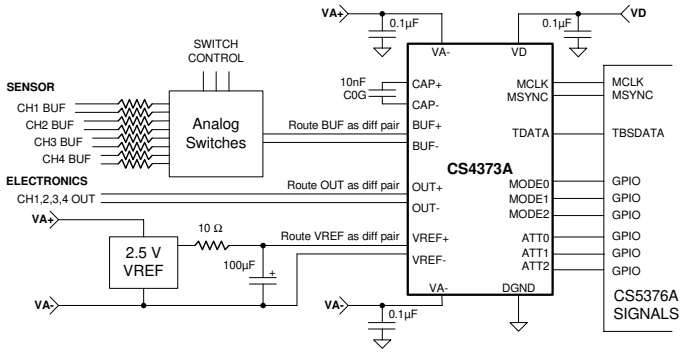

Figure 12. Analog Outputs

7. ANALOG OUTPUTS

The CS4373A has multiple differential analog outputs. The best possible analog performance is achieved from the precision outputs (OUT±), but with only minimal drive capability. A buffered output (BUF±) can drive an external load, but with reduced analog performance. The internal anti-alias filter requires a dedicated capacitor connection (CAP±) to eliminate undesired high-frequency signals.

7.1 Differential Signals

Differential AC signals out of the CS4373A consist of two halves with equal but opposite magnitude varying about a common mode voltage. A full-scale 5 V_{PP} differential AC signal centered on a -0.15 V common mode voltage will have:

SIG+ = -0.15 V + 1.25 V = +1.1 V

SIG- = -0.15 V - 1.25 V = -1.4 V

SIG+ is +2.5 V relative to SIG-

For the opposite case:

SIG+ = -0.15 V - 1.25 V = -1.4 V

SIG- = -0.15 V + 1.25 V = +1.1 V

SIG+ is -2.5 V relative to SIG-

So the total swing for SIG+ relative to SIG- is (+2.5 V) - (-2.5 V) = 5 V_{pp} differential. A similar calculation can be done for SIG- relative to SIG+. It's important to note that a 5 V_{pp} differential signal centered on a -0.15 V common mode voltage never exceeds +1.1 V with respect to ground and never drops below -1.4 V with respect to ground on either half. By definition, differential voltages are measured with respect to the opposite half, not relative to ground. A voltmeter differentially measuring between SIG+ and SIG- in the above example would read 1.767 V_{rms}, or 5 V_{pp}.

7.2 Analog Output Attenuation

The CS4373A has seven analog output attenuation settings from 1/1 to 1/64 selected with the ATT2, ATT1, and ATT0 pins. At 1/64 attenuation in AC Common Mode (MODE 6) there is no output signal amplitude due to the attenuator architecture.

Selection	ATT[2:0]	Attenuation	dB
0	0 0 0	1/1	0 dB
1	0 0 1	1/2	-6.02 dB
2	0 1 0	1/4	-12.04 dB
3	0 1 1	1/8	-18.06 dB
4	1 0 0	1/16	-24.08 dB
5	1 0 1	1/32	-30.10 dB
6	1 1 0	1/64	-36.12 dB
7	1 1 1	reserved	reserved

Table 3. Output Attenuation Settings

When enabled, attenuation is applied to both the *OUT* and *BUF* differential analog outputs. The OUT± pins connect directly into the internal attenuator resistors and so attenuation accuracy is highly sensitive to load impedance on the OUT± pins. Loading on the BUF± pins does not affect attenuator accuracy.

The attenuation settings of CS4373A match the gain ranges of the CS3301A / CS3302A differential amplifiers to enable full-scale testing at all gain ranges. The CS3301A / CS3302A amplifier gain settings (GAIN) are decoded identical to the CS4373A attenuator settings (ATT) and so can share GPIO signals from the digital filter.

7.3 OUT± Precision Output

The OUT± pins are precision differential analog outputs for testing the high-performance electronics measurement channel. These precision outputs have higher performance specifications than the BUF outputs, but with a much higher sensitivity to external loading. Excessive resistive or capacitive loading on the OUT± pins will degrade the analog performance characteristics of the CS4373A in all operational modes.

The OUT± precision output is optimized for direct connection to the CS3301A / CS3302A amplifier differential inputs, which have very high input impedance. These amplifiers include a pin-controlled input multiplexer to switch between an internal differential termination for noise tests and two external differential inputs. One external amplifier input is typically dedicated to sensor measurements and the other to testing the electronics channel.

The OUT± outputs are enabled in all operational modes except “AC BUF Only” mode (MODE 3) and sleep modes (MODE 0, 7). In AC BUF Only and sleep modes the OUT± pins are high impedance.

7.4 BUF± Buffered Output

The BUF± pins are buffered differential analog outputs for testing external sensors such as geophones or hydrophones. The buffered outputs have reduced performance specifications compared with the OUT outputs, but are less sensitive to external loading.

The BUF± outputs are enabled in all operational modes except “AC OUT Only” mode (MODE 2) and sleep modes (MODE 0, 7). In AC OUT Only and sleep modes the BUF± pins are high impedance to ensure they do not interfere with sensor operation during normal data acquisition.

For sensor impedance testing, it is required to place matched series resistors in between the BUF± outputs and the differential sensor. With known series resistors and a known DC differential source voltage, sensor resistance can be calculated ratiometrically from the measured voltage drop across the sensor.

7.5 CAP± Analog Output

The CS4373A requires a 10 nF C0G or NPO-type capacitor connected differentially across the CAP± pins. This capacitor creates an internal anti-alias filter to eliminate high-frequency signals from the OUT± and BUF± analog outputs and helps to maintain the stability of the low-power $\Delta\Sigma$ circuitry.

A COG, NPO or similar high-quality capacitor is required for CAP± since other capacitor types, such as X7R, do not have the required linearity. Using a poor-quality capacitor on CAP± will significantly degrade THD performance in the AC operational modes.