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CS4382

114 dB, 192 kHz 8-Channel D/A Converter

Features

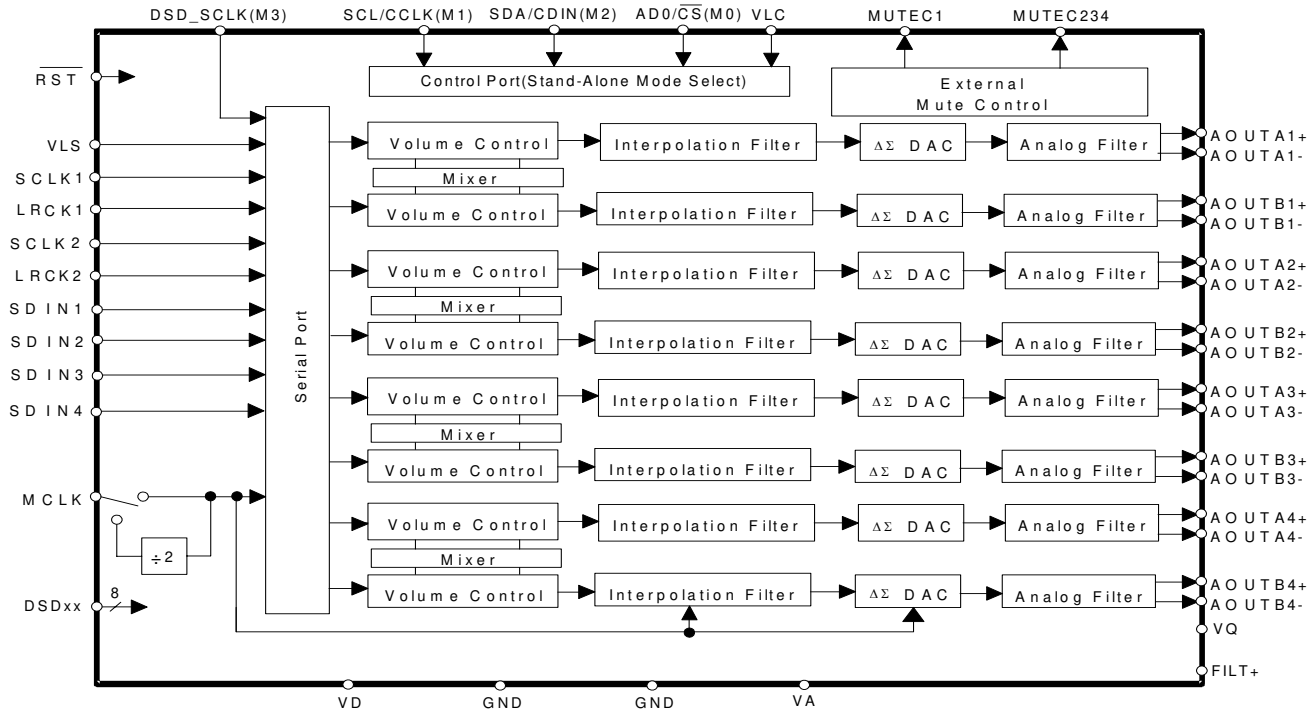
- 24-bit Conversion
- Up to 192 kHz Sample Rates
- 114 dB Dynamic Range
- -100 dB THD+N
- Supports PCM and DSD Data Formats
- Selectable Digital Filters
- Volume Control with Soft Ramp
  - 1 dB Step Size
  - Zero Crossing Click-Free Transitions
- Dedicated DSD Inputs
- Low Clock-Jitter Sensitivity
- Simultaneous Support for Two Synchronous Sample Rates for DVD Audio
- µC or Stand-Alone Operation

Description

The CS4382 is a complete 8-channel digital-to-analog system including digital interpolation, fifth-order delta-sigma digital-to-analog conversion, digital de-emphasis, volume control and analog filtering. The advantages of this architecture include: ideal differential linearity, no distortion mechanisms due to resistor matching errors, no linearity drift over time and temperature and a high tolerance to clock jitter.

The CS4382 is available in a 48-pin LQFP package in Commercial grade (-10°C to +70°C). The CDB4382 Customer Demonstration Board is also available for device evaluation and implementation suggestions. Please see "Ordering Information" on page 42 for complete details.

The CS4382 accepts PCM data at sample rates from 4 kHz to 192 kHz, DSD audio data, and operates over a wide power supply range. These features are ideal for multi-channel audio systems including DVD players, SACD players, A/V receivers, digital TV's, mixing consoles, effects processors, and automotive audio systems.



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1. CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARACTERISTICS

(Full-Scale Output Sine Wave, 997 Hz; Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified; Test load R_L = 3 kΩ, C_L = 100 pF, VA = 5 V, VD = 3.3 V (see Figure 5)
For Single-Speed Mode, Fs = 48 kHz, SCLK = 3.072 MHz, MCLK = 12.288 MHz;
For Double-Speed Mode, Fs = 96 kHz, SCLK = 6.144 MHz, MCLK = 12.288 MHz;
For Quad-Speed Mode, Fs = 192 kHz, SCLK = 12.288 MHz, MCLK = 24.576 MHz;
For Direct Stream Digital Mode, Fs = 128 x 48 kHz, DSD_SCLK = 6.144 MHz, MCLK = 12.288 MHz).

Parameters			Symbol	Min	Typ	Max	Unit
CS4382-KQZ Dynamic Performance - All PCM modes and DSD (Note 1)							
Specified Temperature Range			T_A	-10	-	70	°C
Dynamic Range (Note 2)	24-bit	unweighted		105	111	-	dB
		A-Weighted		108	114	-	dB
	16-bit	unweighted		-	94	-	dB
	(Note 3)	A-Weighted		-	97	-	dB
Total Harmonic Distortion + Noise		(Note 2)	THD+N				
	24-bit	0 dB		-	-100	-94	dB
		-20 dB		-	-91	-	dB
		-60 dB		-	-51	-	dB
	16-bit	0 dB		-	-94	-	dB
	(Note 3)	-20 dB		-	-74	-	dB
		-60 dB		-	-34	-	dB
Idle Channel Noise / Signal-to-noise ratio				-	114	-	dB
Interchannel Isolation		(1 kHz)		-	90	-	dB

Notes:

1. CS4382-KQZ parts are tested at 25°C.
2. One-half LSB of triangular PDF dither is added to data.
3. Performance limited by 16-bit quantization noise.

ANALOG CHARACTERISTICS

(Continued)

Parameters	Symbol	Min	Typ	Max	Units
Analog Output - All PCM modes and DSD					
Full Scale Differential Output Voltage (Note 4)	V_{FS}	86% V_A	91% V_A	96% V_A	Vpp
Quiescent Voltage	V_Q	-	50% V_A	-	VDC
Max Current from V_Q	I_{QMAX}	-	1	-	µA
Interchannel Gain Mismatch		-	0.1	-	dB
Gain Drift		-	100	-	ppm/°C
Output Impedance (Note 4)	Z_{OUT}	-	100	-	Ω
AC-Load Resistance	R_L	3	-	-	kΩ
Load Capacitance	C_L	-	-	100	pF

POWER AND THERMAL CHARACTERISTICS

Parameters		Symbol	Min	Typ	Max	Units
Power Supplies						
Power Supply Current	normal operation, V_A= 5 V	I_A	-	60	66	mA
(Note 5)	V_D= 5 V	I_D	-	45	70	mA
	V_D= 3.3 V	I_D	-	30	46	mA
	Interface current, VLC=5 V (Notes 6, 7)	I_{LC}	-	2	-	µA
	VLS=5 V	I_{LS}	-	84	-	µA
	power-down state (all supplies) (Note 8)	I_{pd}	-	200	-	µA
Power Dissipation	(Note 5)					
VA = 5 V, VD = 3.3 V	normal operation		-	400	485	mW
	power-down (Note 8)		-	1	-	mW
VA = 5 V, VD = 5 V	normal operation		-	525	680	mW
	power-down (Note 8)		-	1	-	mW
Package Thermal Resistance	multi-layer	θ_{JA}	-	48	-	°C/Watt
	dual-layer	θ_{JA}	-	65	-	°C/Watt
		θ_{JC}	-	15	-	°C/Watt
Power Supply Rejection Ratio (Note 9)	(1 kHz)	PSRR	-	60	-	dB
	(60 Hz)		-	40	-	dB

Notes:

4. V_{FS} is tested under load R_L and includes attenuation due to Z_{OUT}
5. Current consumption increases with increasing FS within a given speed mode and is signal dependant. Max values are based on highest FS and highest MCLK.
6. I_{LC} measured with no external loading on the SDA pin.
7. This specification is violated when the VLC supply is greater than VD and when pin 16 (M1/SDA) is tied or pulled low. Logic tied to pin 16 needs to be able to sink this current.
8. Power Down Mode is defined as $\overline{RST}$ pin = Low with all clock and data lines held static.
9. Valid with the recommended capacitor values on FILT+ and VQ as shown in Figures 5 and 6.

ANALOG FILTER RESPONSE

Parameter		Fast Roll-Off Min	Fast Roll-Off Typ	Fast Roll-Off Max	Slow Roll-Off (Note 10) Min	Slow Roll-Off (Note 10) Typ	Slow Roll-Off (Note 10) Max	Unit
Combined Digital and On-chip Analog Filter Response - Single-Speed Mode (Note 11)								
Passband (Note 12)	to -0.01 dB corner	0	-	.454	0	-	0.417	Fs
	to -3 dB corner	0	-	.499	0	-	0.499	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	+0.01	-0.01	-	+0.01	dB
StopBand		.547	-	-	.583	-	-	Fs
StopBand Attenuation	(Note 13)	90	-	-	64	-	-	dB
Group Delay		-	12/Fs	-	-	6.5/Fs	-	s
Passband Group Delay Deviation	0 - 20 kHz	-	-	±0.41/Fs		-	±0.14/Fs	s
De-emphasis Error (Note 14)	Fs = 32 kHz	-	-	±0.23	-	-	±0.23	dB
(Relative to 1 kHz)	Fs = 44.1 kHz	-	-	±0.14	-	-	±0.14	dB
	Fs = 48 kHz	-	-	±0.09	-	-	±0.09	dB
Combined Digital and On-chip Analog Filter Response - Double-Speed Mode - 96 kHz (Note 11)								
Passband (Note 12)	to -0.01 dB corner	0	-	.430	0	-	.296	Fs
	to -3 dB corner	0	-	.499	0	-	.499	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	-0.01	-	0.01	dB
StopBand		.583	-	-	.792	-	-	Fs
StopBand Attenuation	(Note 13)	80	-	-	70	-	-	dB
Group Delay		-	4.6/Fs	-	-	3.9/Fs	-	s
Passband Group Delay Deviation	0 - 20 kHz	-	-	±0.03/Fs		-	±0.01/Fs	s
Combined Digital and On-chip Analog Filter Response - Quad-Speed Mode - 192 kHz (Note 11)								
Passband (Note 12)	to -0.01 dB corner	0	-	.105	0	-	.104	Fs
	to -3 dB corner	0	-	.490	0	-	.481	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	-0.01	-	0.01	dB
StopBand		.635	-	-	.868	-	-	Fs
StopBand Attenuation	(Note 13)	90	-	-	75	-	-	dB
Group Delay		-	4.7/Fs	-	-	4.2/Fs	-	s
Passband Group Delay Deviation	0 - 20 kHz	-	-	±0.01/Fs		-	±0.01/Fs	s
Combined Digital and On-chip Analog Filter Response - DSD Mode (Note 11)								
Passband (Note 12)	to -0.1 dB corner	-	-	-	0	-	20	kHz
	to -3 dB corner	-	-	-	0	-	120	kHz
Frequency Response 10 Hz to 20 kHz		-	-	-	-.01	-	0.1	dB

Notes:

10. Slow Roll-Off interpolation filter is only available in Control Port Mode.
11. Filter response is not tested but is guaranteed by design.
12. Response is clock dependent and will scale with Fs. Note that the response plots (Figures 9 to 32) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
13. Single and Double-Speed Mode Measurement Bandwidth is from stopband to 3 Fs.
    Quad-Speed Mode Measurement Bandwidth is from stopband to 1.34 Fs.
14. De-emphasis is available only in Single-Speed Mode; Only 44.1 kHz De-emphasis is available in Stand-Alone Mode

DIGITAL CHARACTERISTICS

(For KQZ T_A = -10°C to +70°C; VLC = VLS = 1.8 V to 5.5 V)

Parameters		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	Serial Data Port	V_{IH}	70% VLS	-	-	V
	Control Port	V_{IH}	70% VLC	-	-	V
Low-Level Input Voltage	Serial Data Port	V_{IL}	-	-	20% VLS	V
	Control Port	V_{IL}	-	-	20% VLC	V
Input Leakage Current	(Note 7)	I_{in}	-	-	±10	µA
Input Capacitance			-	8	-	pF
Maximum MUTEC Drive Current			-	3	-	mA
MUTEC High-Level Output Voltage		V_{OH}	-	VA	-	V
MUTEC Low-Level Output Voltage		V_{OL}	-	0	-	V

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Max	Units
DC Power Supply	Analog power	VA	-0.3	6.0	V
	Digital internal power	VD	-0.3	6.0	V
	Serial data port interface power	VLS	-0.3	6.0	V
	Control port interface power	VLC	-0.3	6.0	V
Input Current, Any Pin Except Supplies		I_{in}	-	±10	mA
Digital Input Voltage	Serial data port interface	V_{IND-S}	-0.3	VLS+ 0.4	V
	Control port interface	V_{IND-C}	-0.3	VLC+ 0.4	V
Ambient Operating Temperature (power applied)		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(GND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Typ	Max	Units
DC Power Supply	Analog power	VA	4.5	5.0	5.5	V
	Digital internal power	VD	3.0	3.3	5.5	V
	Serial data port interface power	VLS	1.8	5.0	5.5	V
	Control port interface power	VLC	1.8	5.0	5.5	V

SWITCHING CHARACTERISTICS

(For KQZ T_A = -10°C to +70°C; VLS = 1.8 V to 5.5 V; Inputs: Logic 0 = GND, Logic 1 = VLS, C_L = 30 pF)

Parameters		Symbol	Min	Typ	Max	Units
MCLK Frequency	(Note 15)					
	Single-Speed Mode		1.024	-	51.2	MHz
	Double-Speed Mode		6.400	-	51.2	MHz
	Quad-Speed Mode		6.400	-	51.2	MHz
MCLK Duty Cycle			40	50	60	%
Input Sample Rate	Single-Speed Mode	Fs	4	-	50	kHz
	Double-Speed Mode	Fs	50	-	100	kHz
	Quad-Speed Mode	Fs	100	-	200	kHz
LRCK Duty Cycle			45	50	55	%
SCLK Pulse Width Low		t_{sclkl}	20	-	-	ns
SCLK Pulse Width High		t_{sclkh}	20	-	-	ns
SCLK Period		t_{sclkw}	$\frac{2}{MCLK}$	-	-	ns
	(Note 16)	t_{sclkw}	$\frac{4}{MCLK}$	-	-	ns
SCLK rising to LRCK edge delay		t_{slrd}	20	-	-	ns
SCLK rising to LRCK edge setup time		t_{slrs}	20	-	-	ns
SDATA valid to SCLK rising setup time		t_{sdlrs}	20	-	-	ns
SCLK rising to SDATA hold time		t_{sdh}	20	-	-	ns
LRCK1 to LRCK2 frequency ratio	(Note 17)		0.25	1.00	4.00	

Notes:

15. See Table 5 on page 27 for suggested MCLK frequencies.
16. This serial clock is available only in Control Port Mode when the MCLK Divide bit is enabled.
17. The higher frequency LRCK must be an exact integer multiple (1, 2, or 4) of the lower frequency LRCK.

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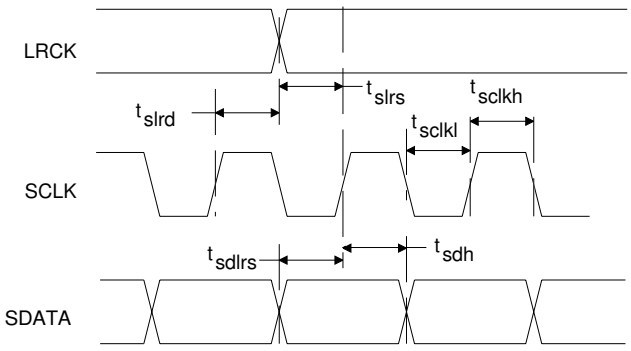


Figure 1. Serial Mode Input Timing

DSD - SWITCHING CHARACTERISTICS

(For KQZ T_A = -10°C to +70°C; Logic 0 = GND; VLS = 1.8 V to 5.5 V; Logic 1 = VLS Volts; C_L = 30 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Master Clock Frequency (Note 18)		4.096	-	38.4	MHz
MCLK Duty Cycle (All DSD modes)		40	50	60	%
DSD_SCLK Pulse Width Low	t_{sclkl}	20	-	-	ns
DSD_SCLK Pulse Width High	t_{sclkh}	20	-	-	ns
DSD_SCLK Frequency (64x Oversampled) (128x Oversampled)		1.024 2.048	- -	3.2 6.4	MHz MHz
DSD_L / _R valid to DSD_SCLK rising setup time	t_{sdlrs}	20	-	-	ns
DSD_SCLK rising to DSD_L or DSD_R hold time	t_{sdh}	20	-	-	ns

Note:

18. Min is 4 times 64x DSD or 2 times 128x DSD, and Max is 12 times 64x DSD or 6 times 128x DSD. The proper MCLK to DSD_SCLK ratio must be set either by the DIF registers or the M0:2 pins

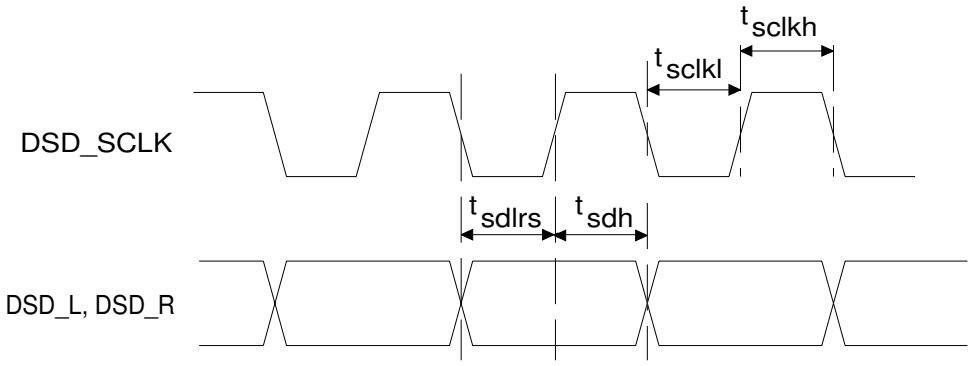


Figure 2. Direct Stream Digital - Serial Audio Input Timing

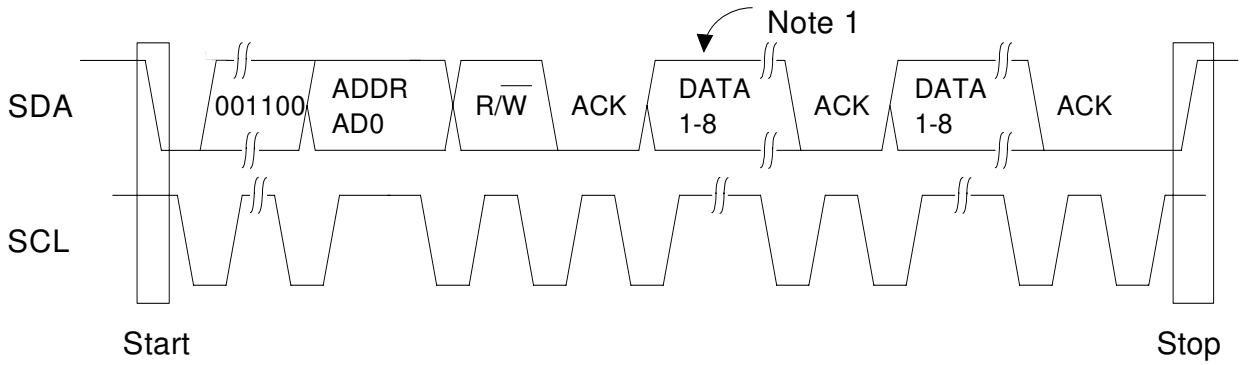
SWITCHING CHARACTERISTICS - CONTROL PORT - I²C® FORMAT

(For KQZ T_A = -10°C to +70°C; VLC = 1.8 V to 5.5 V; Inputs: Logic 0 = GND, Logic 1 = VLC, C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{RST}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 19)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}, t_{rc}	-	1	µs
Fall Time SCL and SDA	t_{fc}, t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling (Note 20)	t_{ack}	-	(Note 21)	ns

Notes:

19. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.
20. The acknowledge delay is based on MCLK and can limit the maximum transaction speed.
21. $\frac{15}{256 \times Fs}$ for Single-Speed Mode, $\frac{15}{128 \times Fs}$ for Double-Speed Mode, $\frac{15}{64 \times Fs}$ for Quad-Speed Mode.



Note: If operation is a write, this byte contains the Memory Address Pointer, MAP.

Figure 3. Control Port Timing - I²C Format

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI™ FORMAT

(For KQZ T_A = -10°C to +70°C; VLC = 1.8 V to 5.5 V; Inputs: Logic 0 = GND, Logic 1 = VLC, C_L = 30 pF)

Parameter		Symbol	Min	Max	Unit
CCLK Clock Frequency		f_{sclk}	-	$\frac{MCLK}{2}$	MHz
$\overline{RST}$ Rising Edge to CS Falling		t_{srs}	500	-	ns
CCLK Edge to $\overline{CS}$ Falling	(Note 22)	t_{spi}	500	-	ns
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	$\frac{1}{MCLK}$	-	ns
CCLK High Time		t_{sch}	$\frac{1}{MCLK}$	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 23)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN	(Note 24)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 24)	t_{f2}	-	100	ns

Notes:

22. t_{spi} only needed before first falling edge of $\overline{CS}$ after $\overline{RST}$ rising edge. t_{spi} = 0 at all other times.
23. Data must be held for sufficient time to bridge the transition time of CCLK.
24. For F_{SCK} < 1 MHz.

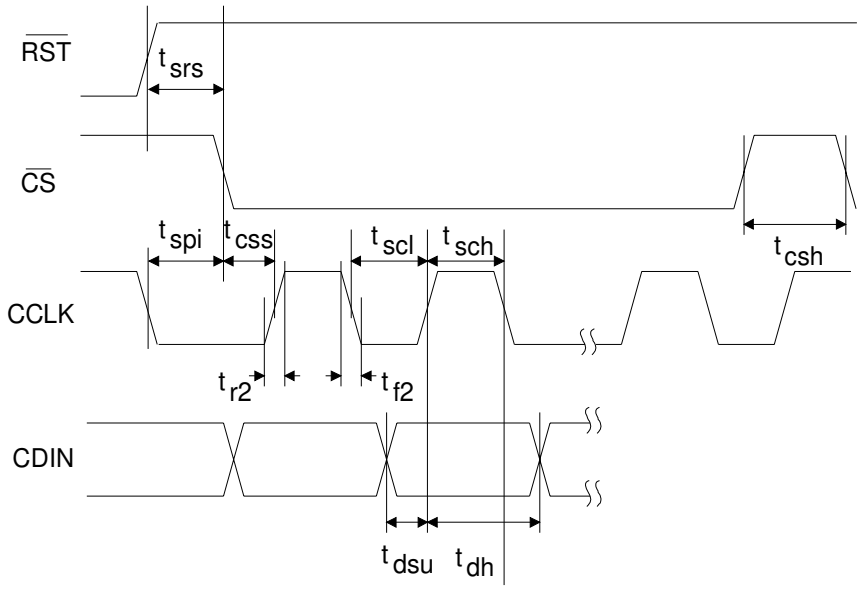


Figure 4. Control Port Timing - SPI Format

2. TYPICAL CONNECTION DIAGRAM

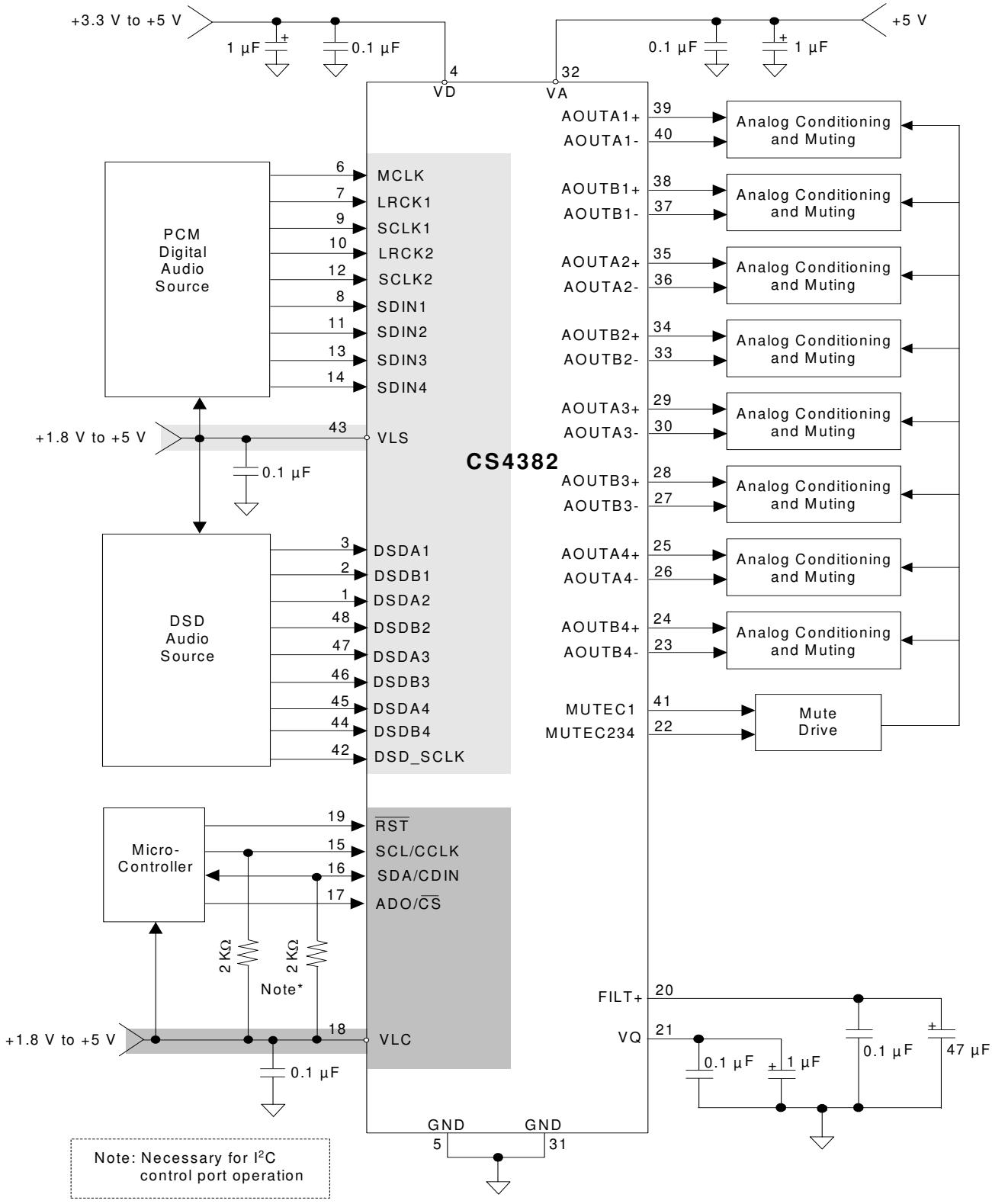


Figure 5. Typical Connection Diagram Control Port

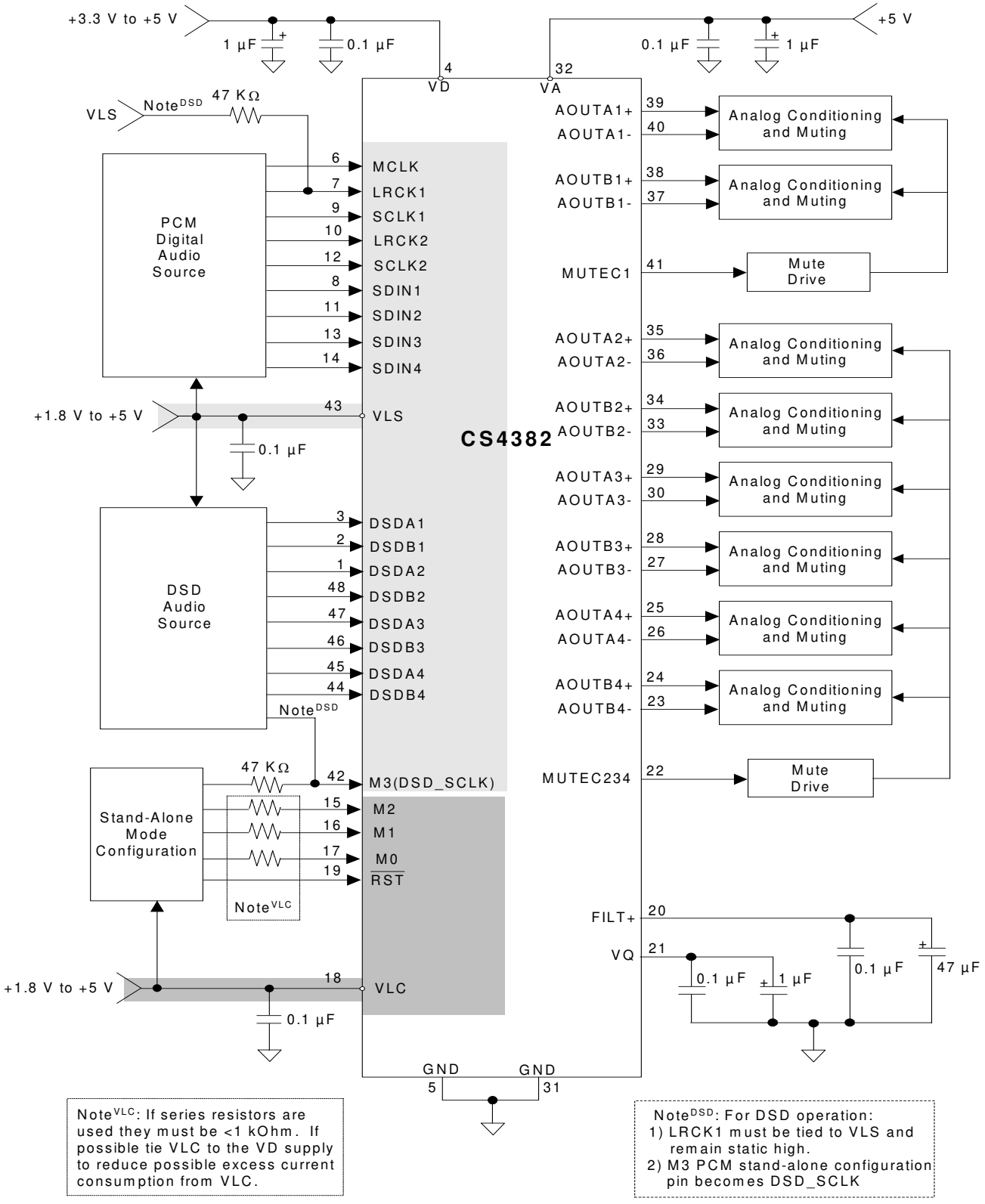


Figure 6. Typical Connection Diagram Stand-Alone

3. REGISTER QUICK REFERENCE

Addr	Function	7	6	5	4	3	2	1	0
01h	Mode Control 1	CPEN	FREEZE	MCLKDIV	DAC4_DIS	DAC3_DIS	DAC2_DIS	DAC1_DIS	PDN
	default	0	0	0	0	0	0	0	1
02h	Mode Control 2	Reserved	DIF2	DIF1	DIF0	SDIN4CLK	SDIN3CLK	SDIN2CLK	SDIN1CLK
	default	0	0	0	0	0	0	0	0
03h	Mode Control 3	SZC1	SZC0	SNGLVOL	RMP_UP	MUTEC+/-	AMUTE	Reserved	MUTEC
	default	1	0	0	0	0	1	0	0
04h	Filter Control	Reserved	Reserved	Reserved	FILT_SEL	Reserved	DEM1	DEM0	RMP_DN
	default	0	0	0	0	0	0	0	0
05h	Invert Control	INV_B4	INV_A4	INV_B3	INV_A3	INV_B2	INV_A2	INV_B1	INV_A1
	default	0	0	0	0	0	0	0	0
06h	Mixing Control Pair 1 (AOUTx1)	P1_A=B	P1ATAPI4	P1ATAPI3	P1ATAPI2	P1ATAPI1	P1ATAPI0	P1FM1	P1FM0
	default	0	0	1	0	0	1	0	0
07h	Vol. Control A1	A1_MUTE	A1_VOL6	A1_VOL5	A1_VOL4	A1_VOL3	A1_VOL2	A1_VOL1	A1_VOL0
	default	0	0	0	0	0	0	0	0
08h	Vol. Control B1	B1_MUTE	B1_VOL6	B1_VOL5	B1_VOL4	B1_VOL3	B1_VOL2	B1_VOL1	B1_VOL0
	default	0	0	0	0	0	0	0	0
09h	Mixing Control Pair 2 (AOUTx2)	P2_A=B	P2ATAPI4	P2ATAPI3	P2ATAPI2	P2ATAPI1	P2ATAPI0	P2FM1	P2FM0
	default	0	0	1	0	0	1	0	0
0Ah	Vol. Control A2	A2_MUTE	A2_VOL6	A2_VOL5	A2_VOL4	A2_VOL3	A2_VOL2	A2_VOL1	A2_VOL0
	default	0	0	0	0	0	0	0	0
0Bh	Vol. Control B2	B2_MUTE	B2_VOL6	B2_VOL5	B2_VOL4	B2_VOL3	B2_VOL2	B2_VOL1	B2_VOL0
	default	0	0	0	0	0	0	0	0
0Ch	Mixing Control Pair 3 (AOUTx3)	P3_A=B	P3ATAPI4	P3ATAPI3	P3ATAPI2	P3ATAPI1	P3ATAPI0	P3FM1	P3FM0
	default	0	0	1	0	0	1	0	0
0Dh	Vol. Control A3	A3_MUTE	A3_VOL6	A3_VOL5	A3_VOL4	A3_VOL3	A3_VOL2	A3_VOL1	A3_VOL0
	default	0	0	0	0	0	0	0	0
0Eh	Vol. Control B3	B3_MUTE	B3_VOL6	B3_VOL5	B3_VOL4	B3_VOL3	B3_VOL2	B3_VOL1	B3_VOL0
	default	0	0	0	0	0	0	0	0
0Fh	Mixing Control Pair 4 (AOUTx4)	P4_A=B	P4ATAPI4	P4ATAPI3	P4ATAPI2	P4ATAPI1	P4ATAPI0	P4FM1	P4FM0
	default	0	0	1	0	0	1	0	0
10h	Vol. Control A4	A4_MUTE	A4_VOL6	A4_VOL5	A4_VOL4	A4_VOL3	A4_VOL2	A4_VOL1	A4_VOL0
	default	0	0	0	0	0	0	0	0
11h	Vol. Control B4	B4_MUTE	B4_VOL6	B4_VOL5	B4_VOL4	B4_VOL3	B4_VOL2	B4_VOL1	B4_VOL0
	default	0	0	0	0	0	0	0	0
12h	Chip Revision	PART3	PART2	PART1	PART0	Reserved	Reserved	Reserved	Reserved
	default	1	0	1	0	-	-	-	-

4. REGISTER DESCRIPTION

Note: All registers are read/write in I²C Mode and write-only in SPI, unless otherwise noted.

4.1 Mode Control 1 (Address 01h)

7	6	5	4	3	2	1	0
CPEN	FREEZE	MCLKDIV	DAC4_DIS	DAC3_DIS	DAC2_DIS	DAC1_DIS	PDN
0	0	0	0	0	0	0	1

4.1.1 Control Port Enable (CPEN)

Default = 0
0 - Disabled
1 - Enabled

Function:

This bit defaults to 0, allowing the device to power-up in Stand-Alone Mode. The Control Port Mode can be accessed by setting this bit to 1. This will allow the operation of the device to be controlled by the registers and the pin definitions will conform to Control Port Mode. To accomplish a clean power-up, the user should write this bit within 10 ms following the release of Reset.

4.1.2 Freeze Controls (FREEZE)

Default = 0
0 - Disabled
1 - Enabled

Function:

This function allows modifications to be made to the registers without the changes taking effect until the FREEZE is disabled. To make multiple changes in the Control port registers take effect simultaneously, enable the FREEZE bit, make all register changes, then Disable the FREEZE bit.

4.1.3 Master Clock Divide Enable (MCLKDIV)

Default = 0
0 - Disabled
1 - Enabled

Function:

The MCLKDIV bit enables a circuit which divides the externally applied MCLK signal by 2 prior to all other internal circuitry.

4.1.4 DAC Pair Disable (DACx_DIS)

Default = 0
0 - DAC Pair x Enabled
1 - DAC Pair x Disabled

Function:

When the bit is set, the respective DAC channel pair (AOUTAx and AOUTBx) will remain in a reset state. It is advised that changes to these bits be made while the power-down (PDN) bit is enabled to eliminate the possibility of audible artifacts.

4.1.5 Power Down (PDN)

Default = 1
0 - Disabled
1 - Enabled

Function:

The entire device will enter a low-power state when this function is enabled, and the contents of the control registers are retained in this mode. The power-down bit defaults to 'enabled' on power-up and must be disabled before normal operation in Control Port Mode can occur.

4.2 Mode Control 2 (Address 02h)

7	6	5	4	3	2	1	0
Reserved	DIF2	DIF1	DIF0	SDIN4CLK	SDIN3CLK	SDIN2CLK	SDIN1CLK
0	0	0	0	0	0	0	0

4.2.1 Digital Interface Format (DIF)

Default = 000 - Format 0 (Left Justified, up to 24-bit data)

Function:

These bits select the interface format for the serial audio input. The Functional Mode bits determine whether PCM or DSD Mode is selected.

PCM Mode: The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in Figures 33-38.

Note: While in PCM Mode, the DIF bits should only be changed when the power-down (PDN) bit is set to ensure proper switching from one mode to another.

DIF2	DIF1	DIF0	DESCRIPTION	Format	FIGURE
0	0	0	Left Justified, up to 24-bit data	0	33
0	0	1	I²S, up to 24-bit data	1	34
0	1	0	Right Justified, 16-bit data	2	35
0	1	1	Right Justified, 24-bit data	3	36
1	0	0	Right Justified, 20-bit data	4	37
1	0	1	Right Justified, 18-bit data	5	38
1	1	0	Reserved		
1	1	1	Reserved		

Table 1. Digital Interface Formats - PCM Mode

DSD Mode: The relationship between the oversampling ratio of the DSD audio data and the required Master clock to DSD data rate is defined by the Digital Interface Format pins. An additional write of 99h to register 00h and 80h to register 1Ah is required to access the modes denoted with *.

DIF2	DIF1	DIFO	DESCRIPTION	Note
0	0	0	64x oversampled DSD data with a 4x MCLK to DSD data rate	
0	0	1	64x oversampled DSD data with a 6x MCLK to DSD data rate	*
0	1	0	64x oversampled DSD data with a 8x MCLK to DSD data rate	*
0	1	1	64x oversampled DSD data with a 12x MCLK to DSD data rate	*
1	0	0	128x oversampled DSD data with a 2x MCLK to DSD data rate	
1	0	1	128x oversampled DSD data with a 3x MCLK to DSD data rate	*
1	1	0	128x oversampled DSD data with a 4x MCLK to DSD data rate	*
1	1	1	128x oversampled DSD data with a 6x MCLK to DSD data rate	*

Table 2. Digital Interface Formats - DSD Mode

4.2.2 Serial Audio Data Clock Source (SDINXCLK)

Default = 0
0 - SDINx clocked by SCLK1 and LRCK1
1 - SDINx clocked by SCLK2 and LRCK2

Function:

The SDINxCLK bit specifies which SCLK/LRCK input pair is used to clock in the data on the given SDINx line. For more details see “Clock Source Selection” on page 29.

4.3 Mode Control 3 (Address 03h)

7	6	5	4	3	2	1	0
SZC1	SZC0	SNGLVOL	RMP_UP	Reserved	AMUTE	Reserved	MUTEC
1	0	0	0	0	1	0	0

4.3.1 Soft Ramp and Zero Cross Control (SZC)

Default = 10
00 - Immediate Change
01 - Zero Cross
10 - Soft Ramp
11 - Soft Ramp on Zero Crossings

Function:

Immediate Change

When Immediate Change is selected all level changes will take effect immediately in one step.

Zero Cross

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Soft Ramp

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods.

Soft Ramp on Zero Crossing

Soft Ramp and Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

4.3.2 Single Volume Control (SNGLVOL)

Default = 0
0 - Disabled
1 - Enabled

Function:

The individual channel volume levels are independently controlled by their respective Volume Control Bytes when this function is disabled. The volume on all channels is determined by the A1 Channel Volume Control Byte, and the other Volume Control Bytes are ignored when this function is enabled.

4.3.3 Soft Volume Ramp-Up After Error (RMP_UP)

Default = 0
0 - Disabled
1 - Enabled

Function:

An un-mute will be performed after executing a filter mode change, after a LRCK/MCLK ratio change or error, and after changing the Functional Mode. When this feature is enabled, this un-mute is effected, similar to attenuation changes, by the Soft and Zero Cross bits in the Mode Control 3 register. When disabled, an immediate un-mute is performed in these instances.

Note: For best results, it is recommended that this feature be used in conjunction with the RMP_DN bit.

4.3.4 Mutec Polarity (MUTEC+/-)

Default = 0
0 - Active High
1 - Active Low

Function:

The active polarity of the MUTEC pin(s) is determined by this register. When set to 0 (default), the MUTEC pins are high when active. When set to 1 the MUTEC pin(s) are low when active.

Note: When the onboard mute circuitry is designed for active low, the MUTEC outputs will be high (unmuted) for the period of time during reset and before this bit is enabled to 1.

4.3.5 Auto-Mute (AMUTE)

Default = 1
0 - Disabled
1 - Enabled

Function:

The Digital-to-Analog converter output will mute following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-static data will release the mute. Detection and muting is done independently for each channel. The quiescent voltage on the output will be retained and the Mute Control pin will go active during the mute period. The muting function is affected, similar to volume control changes, by the Soft and Zero Cross bits in the Mode Control 3 register.

4.3.6 Mutec Pin Control (MUTEC)

Default = 0
0 - Two Mute control signals
1 - Single mute control signal on MUTEC1

Function:

Selects how the internal mute signals are routed to the MUTEC1 and MUTEC234 pins. When set to '0', a logical AND of DAC pair 1 mute control signals are output on MUTEC1 and a logical AND of the mute control signals of DAC pairs 2, 3, and 4 are output on MUTEC234. When set to '1', a logical AND of all DAC pair mute control signals is output on the MUTEC1 pin, MUTEC234 will remain static. For more information on the use of the mute control function see the MUTEC1 and MUTEC234 pins in Section 5. Pin Description.

4.4 Filter Control (Address 04h)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	FILT_SEL	Reserved	DEM1	DEM0	RMP_DN
0	0	0	0	0	0	0	0

4.4.1 Interpolation Filter Select (FILT_SEL)

Default = 0
0 - Fast roll-off
1 - Slow roll-off

Function:

This Function allows the user to select whether the interpolation filter has a fast or slow roll off. For filter characteristics please see Section 1.

4.4.2 De-Emphasis Control (DEM)

Default = 00
00 - Disabled
01 - 44.1 kHz
10 - 48 kHz
11 - 32 kHz

Function:

Selects the appropriate digital filter to maintain the standard 15 ms/50 ms digital de-emphasis filter response at 32, 44.1 or 48 kHz sample rates. (see Figure 39)

De-emphasis is only available in Single-Speed Mode.

4.4.3 Soft Ramp-Down Before Filter Mode Change (RMP_DN)

Default = 0
0 - Disabled
1 - Enabled

Function:

A mute will be performed prior to executing a filter mode change. When this feature is enabled, this mute is effected, similar to attenuation changes, by the Soft and Zero Cross bits in the Mode Control 3 register. When disabled, an immediate mute is performed prior to executing a filter mode change.

Note: For best results, it is recommended that this feature be used in conjunction with the RMP_UP bit.

4.5 Invert Control (Address 05h)

7	6	5	4	3	2	1	0
INV_B4	INV_A4	INV_B3	INV_A3	INV_B2	INV_A2	INV_B1	INV_A1
0	0	0	0	0	0	0	0

4.5.1 Invert Signal Polarity (INV_XX)

Default = 0
0 - Disabled
1 - Enabled

Function:

When enabled, these bits will invert the signal polarity of their respective channels.

4.6 Mixing Control Pair 1 (Channels A1 & B1)(Address 06h)
Mixing Control Pair 2 (Channels A2 & B2)(Address 09h)
Mixing Control Pair 3 (Channels A3 & B3)(Address 0Ch)
Mixing Control Pair 4 (Channels A4 & B4)(Address 0Fh)

7	6	5	4	3	2	1	0
Px_A=B	PxATAPI4	PxATAPI3	PxATAPI2	PxATAPI1	PxATAPI0	PxFM1	PxFM0
0	0	1	0	0	1	0	0

4.6.1 Channel A Volume = Channel B Volume (A=B)

Default = 0
0 - Disabled
1 - Enabled

Function:

The AOUTAx and AOUTBx volume levels are independently controlled by the A and the B Channel Volume Control Bytes when this function is disabled. The volume on both AOUTAx and AOUTBx are determined by the A Channel Attenuation and Volume Control Bytes (per A-B pair), and the B Channel Bytes are ignored when this function is enabled.

4.6.2 ATAPI Channel Mixing and Muting (ATAPI)

Default = 01001 - AOUTAx=aL, AOUTBx=bR (Stereo)

Function:

The CS4382 implements the channel mixing functions of the ATAPI CD-ROM specification. The ATAPI functions are applied per A-B pair. Refer to Table 3 and Figure 41 for additional information.

ATAPI4	ATAPI3	ATAPI2	ATAPI1	ATAPI0	AOUTAx	AOUTBx
0	0	0	0	0	MUTE	MUTE
0	0	0	0	1	MUTE	bR
0	0	0	1	0	MUTE	bL
0	0	0	1	1	MUTE	b[(L+R)/2]
0	0	1	0	0	aR	MUTE
0	0	1	0	1	aR	bR
0	0	1	1	0	aR	bL
0	0	1	1	1	aR	b[(L+R)/2]
0	1	0	0	0	aL	MUTE
0	1	0	0	1	aL	bR
0	1	0	1	0	aL	bL
0	1	0	1	1	aL	b[(L+R)/2]
0	1	1	0	0	a[(L+R)/2]	MUTE
0	1	1	0	1	a[(L+R)/2]	bR
0	1	1	1	0	a[(L+R)/2]	bL
0	1	1	1	1	a[(L+R)/2]	b[(L+R)/2]
1	0	0	0	0	MUTE	MUTE
1	0	0	0	1	MUTE	bR
1	0	0	1	0	MUTE	bL
1	0	0	1	1	MUTE	[(aL+bR)/2]
1	0	1	0	0	aR	MUTE
1	0	1	0	1	aR	bR
1	0	1	1	0	aR	bL
1	0	1	1	1	aR	[(bL+aR)/2]
1	1	0	0	0	aL	MUTE
1	1	0	0	1	aL	bR
1	1	0	1	0	aL	bL
1	1	0	1	1	aL	[(aL+bR)/2]
1	1	1	0	0	[(aL+bR)/2]	MUTE
1	1	1	0	1	[(aL+bR)/2]	bR
1	1	1	1	0	[(bL+aR)/2]	bL
1	1	1	1	1	[(aL+bR)/2]	[(aL+bR)/2]

Table 3. ATAPI Decode

4.6.3 Functional Mode (FM)

Default = 00
00 - Single-Speed Mode (4 to 50 kHz sample rates)
01 - Double-Speed Mode (50 to 100 kHz sample rates)
10 - Quad-Speed Mode (100 to 200 kHz sample rates)
11 - Direct Stream Digital Mode

Function:

Selects the required range of input sample rates or DSD Mode. When DSD Mode is selected for any channel pair then all pairs will switch to DSD Mode.

4.7 Volume Control (Addresses 07h, 08h, 0Ah, 0Bh, 0Dh, 0Eh, 10h, 11h)

7	6	5	4	3	2	1	0
xx_MUTE	xx_VOL6	xx_VOL5	xx_VOL4	xx_VOL3	xx_VOL2	xx_VOL1	xx_VOL0
0	0	0	0	0	0	0	0

4.7.1 Mute (MUTE)

Default = 0
0 - Disabled
1 - Enabled

Function:

The Digital-to-Analog converter output will mute when enabled. The quiescent voltage on the output will be retained. The muting function is effected, similar to attenuation changes, by the Soft and Zero Cross bits. The MUTEC pins will go active during the mute period according to the MUTEC register.

4.7.2 Volume Control (xx_VOL)

Default = 0 (No attenuation)

Function:

The Digital Volume Control registers allow independent control of the signal levels in 1 dB increments from 0 to -127 dB. Volume settings are decoded as shown in Table 4. The volume changes are implemented as dictated by the Soft and Zero Cross bits. All volume settings less than -127 dB are equivalent to enabling the MUTE bit.

Binary Code	Decimal Value	Volume Setting
0000000	0	0 dB
0010100	20	-20 dB
0101000	40	-40 dB
0111100	60	-60 dB
1011010	90	-90 dB

Table 4. Example Digital Volume Settings

4.8 Chip Revision (Address 12h)

7	6	5	4	3	2	1	0
PART3	PART2	PART1	PART0	Reserved	Reserved	Reserved	Reserved
1	0	1	0	-	-	-	-

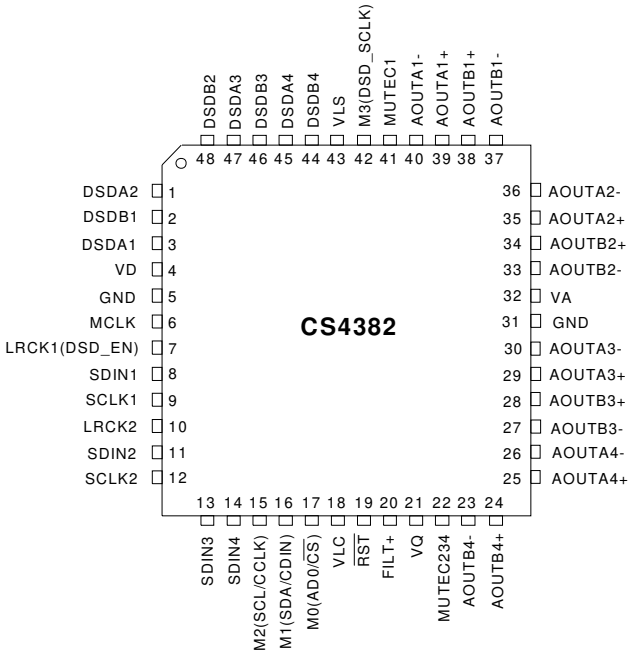
4.8.1 Part Number ID (PART) [Read Only]

1010 - CS4382

Function:

This read-only register can be used to identify the model number of the device.

5. PIN DESCRIPTION



Pin Name	#	Pin Description
VD	4	**Digital Power** (*Input*) **-** Positive power supply for the digital section. Refer to the Recommended Operating Conditions for appropriate voltages.
GND	5 31	**Ground** (*Input*) - Ground reference. Should be connected to analog ground.
MCLK	6	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters. Table 5 illustrates several standard audio sample rates and the required master clock frequency.
LRCK1 LRCK2	7 10	**Left Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line. The frequency of the left/right clock must be at the audio sample rate, Fs.
SDIN1 SDIN2 SDIN3 SDIN4	8 11 13 14	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
SCLK1 SCLK2	9 12	**Serial Clock** (*Input*) - Serial clock for the serial audio interface.
VLC	18	**Control Port Power** (*Input*) **-** Determines the required signal level for the control port. Refer to the Recommended Operating Conditions for appropriate voltages.
$\overline{\text{RST}}$	19	**Reset** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings when low.
FILT+	20	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits. Requires the capacitive decoupling to analog ground, as shown in the Typical Connection Diagram.
VQ	21	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage. VQ must be capacitively coupled to analog ground, as shown in the Typical Connection Diagram. The nominal voltage level is specified in the Analog Characteristics and Specifications section. VQ presents an appreciable source impedance and any current drawn from this pin will alter device performance. However, VQ can be used to bias the analog circuitry assuming there is no AC signal component and the DC current is less than the maximum specified in the Analog Characteristics and Specifications section.