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103 dB, 192 kHz 8-Channel D/A Converter

Features

- ◆ Advanced Multi-bit Delta Sigma Architecture
- ◆ 24-bit Conversion
- ◆ Automatic Detection of Sample Rates up to 192 kHz
- ◆ 103 dB Dynamic Range
- ◆ -88 dB THD+N
- ◆ Single-Ended Output Architecture
- ◆ Direct Stream Digital® (DSD™) Mode
 - Non-Decimating Volume Control
 - On-Chip 50 kHz Filter
 - Matched PCM and DSD Analog Output Levels
- ◆ Compatible with Industry-Standard Time Division Multiplexed (TDM) Serial Interface
- ◆ Selectable Digital Filters
- ◆ Volume Control with 1/2-dB Step Size and Soft Ramp
- ◆ Low Clock-Jitter Sensitivity
- ◆ +5 V Analog Supply, +2.5 V Digital Supply
- ◆ Separate 1.8 to 5 V Logic Supplies for the Control and Serial Ports

Description

The CS4384 is a complete 8-channel digital-to-analog system. This D/A system includes digital de-emphasis, half-dB step size volume control, ATAPI channel mixing, selectable fast and slow digital interpolation filters followed by an oversampled, multi-bit delta sigma modulator which includes mismatch shaping technology that eliminates distortion due to capacitor mismatch. Following this stage is a multi-element switched capacitor stage and low-pass filter with single-ended analog outputs.

The CS4384 also has a proprietary DSD processor which allows for volume control and 50 kHz on-chip filtering without an intermediate decimation stage. It also offers an optional path for direct DSD conversion by directly using the multi-element switched capacitor array.

The CS4384 accepts PCM data at sample rates from 4 kHz to 216 kHz, DSD audio data, and delivers excellent sound quality. These features are ideal for multi-channel audio systems including SACD players, A/V receivers, digital TV's, mixing consoles, effects processors, and sound cards.

This product is available in 48-pin LQFP package in Commercial (-40°C to +85°C) temperature grade. See "Ordering Information" on page 51 for complete details.

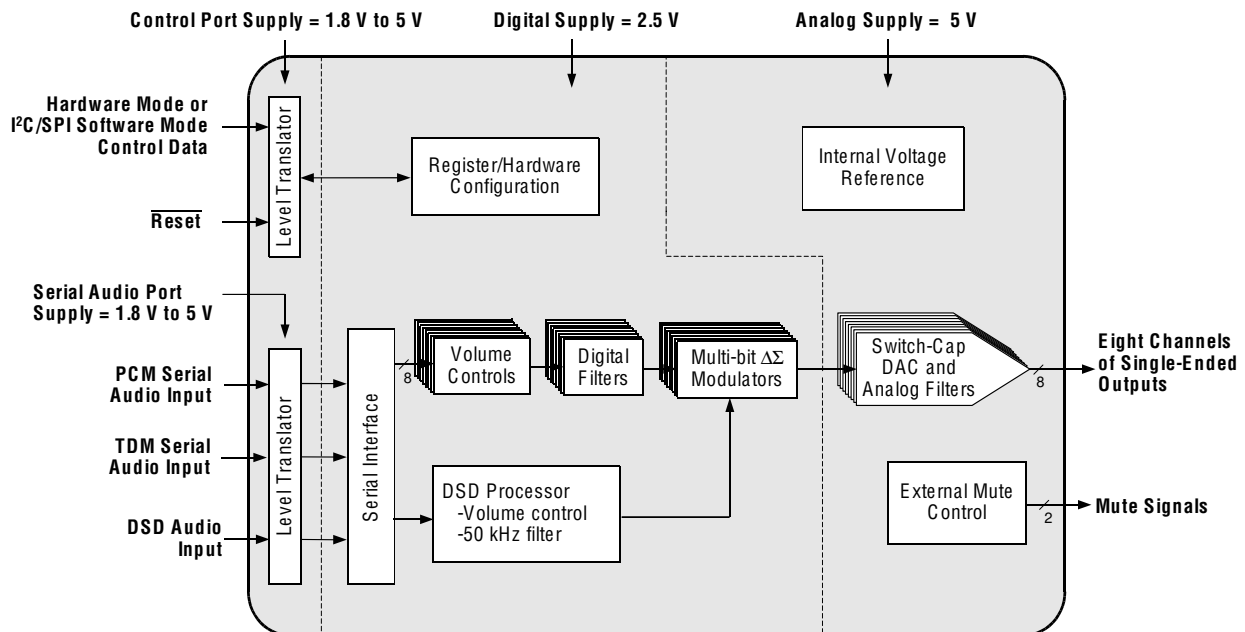


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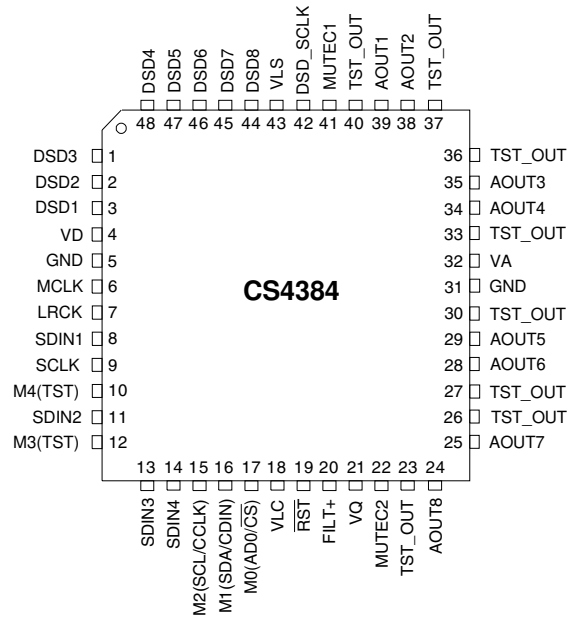
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1. PIN DESCRIPTION



Pin Name	#	Pin Description
VD	4	Digital Power (Input) - Positive power supply for the digital section. Refer to the Recommended Operating Conditions for appropriate voltages.
GND	5 31	Ground (Input) - Ground reference. Should be connected to analog ground.
MCLK	6	Master Clock (Input) - Clock source for the delta-sigma modulator and digital filters. Table 1 illustrates several standard audio sample rates and the required master clock frequencies.
LRCK	7	Left Right Clock (Input) - Determines which channel, Left or Right, is currently active on the serial audio data line. The frequency of the left/right clock must be at the audio sample rate, Fs.
SDIN1 SDIN2 SDIN3 SDIN4	8 11 13 14	Serial Data Input (Input) - Input for two's complement serial audio data.
SCLK	9	Serial Clock (Input) - Serial clocks for the serial audio interface.
VLC	18	Control Port Power (Input) - Determines the required signal level for the control port and hardware mode configuration pins. Refer to the Recommended Operating Conditions for appropriate voltages.
$\overline{\text{RST}}$	19	Reset (Input) - The device enters a low power mode and all internal registers are reset to their default settings when low.
FILT+	20	Positive Voltage Reference (Output) - Positive reference voltage for the internal sampling circuits. Requires the capacitive decoupling to analog ground as shown in the Typical Connection Diagram.
VQ	21	Quiescent Voltage (Output) - Filter connection for internal quiescent voltage.
MUTE1 MUTE234	41 22	Mute Control (Output) - These pins are intended to be used as a control for external mute circuits on the line outputs to prevent the clicks and pops that can occur in any single supply system.

Pin Name	#	Pin Description
AOUT1 AOUT2 AOUT3 AOUT4 AOUT5 AOUT6 AOUT7 AOUT8	39 38 35 34 29 28 25 24	Analog Output (Output) - The full scale analog output level is specified in the Analog Characteristics specification table.
VA	32	Analog Power (Input) - Positive power supply for the analog section. Refer to the Recommended Operating Conditions for appropriate voltages.
VLS	43	Serial Audio Interface Power (Input) - Determines the required signal level for the serial audio interface. Refer to the Recommended Operating Conditions for appropriate voltages.
TST_OUT	23, 26 27, 30 33, 36 37, 40	Test Output - These pins need to be floating and not connected to any trace or plane.
Hardware Mode Definitions		
M0 M1 M2 M3 M4	17 16 15 12 10	Mode Selection (Input) - Determines the operational mode of the device as detailed in Tables 4 and 5 .
Software Mode Definitions		
SCL/CCLK	15	Serial Control Port Clock (Input) - Serial clock for the serial control port. Requires an external pull-up resistor to the logic interface voltage in I ² C [®] mode as shown in the Typical Connection Diagram.
SDA/CDIN	16	Serial Control Port Data (Input/Output) - SDA is a data I/O line in I ² C mode and is open drain, requiring an external pull-up resistor to the logic interface voltage, as shown in the Typical Connection Diagram; CDIN is the input data line for the control port interface in SPI [™] mode.
AD0/ $\overline{\text{CS}}$	17	Address Bit 0 (I²C) / Control Port Chip Select (SPI) (Input) - AD0 is a chip address pin in I ² C mode; CS is the chip select signal for SPI mode.
TST	10 12	Test - These pins need to be tied to analog ground.
DSD Definitions		
DSD1, DSD2 DSD3, DSD4 DSD5, DSD6 DSD7, DSD8	3, 2 1, 48 47, 46 45, 44	Direct Stream Digital Input (Input) - Input for Direct Stream Digital serial audio data.
DSD_SCLK	42	DSD Serial Clock (Input) - Serial clock for the Direct Stream Digital serial audio interface.

2. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

(GND = 0 V; all voltages with respect to ground.)

Parameters	Symbol	Min	Typ	Max	Units	
DC Power Supply	Analog power	VA	4.75	5.0	5.25	V
	Digital internal power	VD	2.37	2.5	2.63	V
	Serial data port interface power	VLS	1.71	5.0	5.25	V
	Control port interface power	VLC	1.71	5.0	5.25	V
Ambient Operating Temperature (Power Applied)	-CQZ T _A	-40	-	+85	°C	

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V; all voltages with respect to ground.)

Parameters	Symbol	Min	Max	Units	
DC Power Supply	Analog power	VA	-0.3	6.0	V
	Digital internal power	VD	-0.3	3.2	V
	Serial data port interface power	VLS	-0.3	6.0	V
	Control port interface power	VLC	-0.3	6.0	V
Input Current	Any Pin Except Supplies	I _{in}	-	±10	mA
Digital Input Voltage	Serial data port interface	V _{IND-S}	-0.3	VLS+ 0.4	V
	Control port interface	V _{IND-C}	-0.3	VLC+ 0.4	V
Ambient Operating Temperature (power applied)	T _{op}	-55	125	°C	
Storage Temperature	T _{stg}	-65	150	°C	

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

DAC ANALOG CHARACTERISTICS

Test Conditions (unless otherwise indicated): $V_A = V_{LS} = V_{LC} = 5\text{ V}$; $V_D = 2.5\text{ V}$; $T_A = 25\text{ °C}$; Full-Scale 997 Hz input sine wave (Note 1); Tested under max ac-load resistance; Valid with FILT+ and VQ capacitors as shown in “Typical Connection Diagram” on page 18; Measurement Bandwidth 10 Hz to 20 kHz.

Parameters			Symbol	Min	Typ	Max	Unit
FS = 48 kHz, 96 kHz, 192 kHz and DSD							
Dynamic Range	24-bit	A-weighted		97	103	-	dB
		unweighted		94	100	-	dB
	16-bit (Note 2)	A-weighted		-	97	-	dB
		unweighted		-	94	-	dB
Total Harmonic Distortion + Noise (Note 2)	24-bit	-0 dB	THD+N	-	-88	-82	dB
		-20 dB		-	-80	-74	dB
		-60 dB		-	-40	-34	dB
	16-bit	0 dB		-	-88	-	dB
		-20 dB		-	-74	-	dB
		-60 dB		-	-34	-	dB
Idle Channel Noise / Signal-to-noise ratio				-	100	-	dB
Interchannel Isolation			(1 kHz)	-	110	-	dB
DC Accuracy							
Interchannel Gain Mismatch				-	0.1	-	dB
Gain Drift				-	100	-	ppm/ °C
Analog Output							
Full Scale Differential- Output Voltage (Note 3)	PCM, DSD processor		V_{FS}	$64\% \cdot V_A$	$66\% \cdot V_A$	$68\% \cdot V_A$	Vpp
	Direct DSD Mode			$47\% \cdot V_A$	$48\% \cdot V_A$	$49\% \cdot V_A$	Vpp
Output Impedance			Z_{OUT}	-	130	-	Ω
Max DC Current draw from an AOUT pin			I_{OUTmax}	-	1.0	-	mA
Min AC-Load Resistance			R_L	-	3	-	k Ω
Max Load Capacitance			C_L	-	100	-	pF
Quiescent Voltage			V_Q	-	$50\% V_A$	-	VDC
Max Current draw from V_Q			I_{QMAX}	-	10	-	μA

Notes:

- One-half LSB of triangular PDF dither is added to data.
- Performance limited by 16-bit quantization noise.
- V_{FS} is tested under load R_L and includes attenuation due to Z_{OUT}

POWER AND THERMAL CHARACTERISTICS

Parameters	Symbol	Min	Typ	Max	Units	
Power Supplies						
Power Supply Current (Note 4)	normal operation, VA= 5 V	I _A	-	83	92	mA
	VD= 2.5 V	I _D	-	20	25	mA
	(Note 5) Interface current, VLC=5 V	I _{LC}	-	2	-	μA
	VLS=5 V	I _{LS}	-	84	-	μA
(Note 6) power-down state (all supplies)	I _{pd}	-	200	-	μA	
Power Dissipation (Note 4)	VA = 5 V, VD = 2.5 V		-	465	520	mW
	normal operation (Note 6) power-down		-	1	-	mW
Package Thermal Resistance	multi-layer	θ _{JA}	-	48	-	°C/Watt
	dual-layer	θ _{JA}	-	65	-	°C/Watt
		θ _{JC}	-	15	-	°C/Watt
Power Supply Rejection Ratio (Note 7)	(1 kHz)	PSRR	-	60	-	dB
	(60 Hz)		-	40	-	dB

Notes:

- Current consumption increases with increasing FS within a given speed mode and is signal dependant. Max values are based on highest FS and highest MCLK.
- I_{LC} measured with no external loading on the SDA pin.
- Power Down Mode is defined as \overline{RST} pin = Low with all clock and data lines held static.
- Valid with the recommended capacitor values on FILT+ and VQ as shown in [Figures 7 and 8](#).

COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

The filter characteristics have been normalized to the sample rate (F_s) and can be referenced to the desired sample rate by multiplying the given characteristic by F_s .

(See (Note 12))

Parameter	Fast Roll-Off			Unit	
	Min	Typ	Max		
Combined Digital and On-chip Analog Filter Response - Single-Speed Mode - 48 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.454	F_s
	to -3 dB corner	0	-	.499	F_s
Frequency Response	10 Hz to 20 kHz	-0.01	-	+0.01	dB
StopBand		0.547	-	-	F_s
StopBand Attenuation	(Note 10)	102	-	-	dB
Group Delay		-	10.4/ F_s	-	s
De-emphasis Error (Note 11)	$F_s = 32$ kHz	-	-	± 0.36	dB
(Relative to 1 kHz)	$F_s = 44.1$ kHz	-	-	± 0.21	dB
	$F_s = 48$ kHz	-	-	± 0.14	dB
Combined Digital and On-chip Analog Filter Response - Double-Speed Mode - 96 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.430	F_s
	to -3 dB corner	0	-	.499	F_s
Frequency Response	10 Hz to 20 kHz	-0.01	-	+0.01	dB
StopBand		.583	-	-	F_s
StopBand Attenuation	(Note 10)	80	-	-	dB
Group Delay		-	6.15/ F_s	-	s
Combined Digital and On-chip Analog Filter Response - Quad-Speed Mode - 192 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.105	F_s
	to -3 dB corner	0	-	.490	F_s
Frequency Response	10 Hz to 20 kHz	-0.01	-	+0.01	dB
StopBand		.635	-	-	F_s
StopBand Attenuation	(Note 10)	90	-	-	dB
Group Delay		-	7.1/ F_s	-	s

Notes:

8. Slow Roll-off interpolation filter is only available in Software Mode.
9. Response is clock dependent and will scale with F_s .
10. For Single-Speed Mode, the Measurement Bandwidth is from stopband to 3 F_s .
For Double-Speed Mode, the Measurement Bandwidth is from stopband to 3 F_s .
For Quad-Speed Mode, the Measurement Bandwidth is from stopband to 1.34 F_s .
11. De-emphasis is available only in Single-Speed Mode; Only 44.1 kHz De-emphasis is available in Hardware Mode.
12. Amplitude vs. Frequency plots of this data are available in the ["Filter Response Plots"](#) on page 45.

COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

(CONTINUED)

Parameter	Slow Roll-Off (Note 8)			Unit	
	Min	Typ	Max		
Single-Speed Mode - 48 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	0.417	Fs
	to -3 dB corner	0	-	0.499	Fs
Frequency Response	10 Hz to 20 kHz	-0.01	-	+0.01	dB
StopBand		.583	-	-	Fs
StopBand Attenuation	(Note 10)	64	-	-	dB
Group Delay		-	7.8/Fs	-	s
De-emphasis Error (Note 11) (Relative to 1 kHz)	Fs = 32 kHz	-	-	±0.36	dB
	Fs = 44.1 kHz	-	-	±0.21	dB
	Fs = 48 kHz	-	-	±0.14	dB
Double-Speed Mode - 96 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.296	Fs
	to -3 dB corner	0	-	.499	Fs
Frequency Response	10 Hz to 20 kHz	-0.01	-	+0.01	dB
StopBand		.792	-	-	Fs
StopBand Attenuation	(Note 10)	70	-	-	dB
Group Delay		-	5.4/Fs	-	s
Quad-Speed Mode - 192 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.104	Fs
	to -3 dB corner	0	-	.481	Fs
Frequency Response	10 Hz to 20 kHz	-0.01	-	+0.01	dB
StopBand		.868	-	-	Fs
StopBand Attenuation	(Note 10)	75	-	-	dB
Group Delay		-	6.6/Fs	-	s

DSD COMBINED DIGITAL & ON-CHIP ANALOG FILTER RESPONSE

Parameter	Min	Typ	Max	Unit	
DSD Processor Mode					
Passband (Note 9)			50	kHz	
Frequency Response			+0.05	dB	
Roll-off	27	-	-	dB/Oct	
Direct DSD Mode					
Passband (Note 9)	to -0.1 dB corner	0	-	26.9	kHz
	to -3 dB corner	0	-	176.4	kHz
Frequency Response	10 Hz to 20 kHz	-0.1	-	0	dB

DIGITAL CHARACTERISTICS

Parameters	Symbol	Min	Typ	Max	Units
Input Leakage Current (Note 13)	I_{in}	-	-	±10	μA
Input Capacitance		-	8	-	pF
High-Level Input Voltage	Serial I/O	V_{IH}	70%	-	V_{LS}
	Control I/O	V_{IH}	70%	-	V_{LC}
Low-Level Input Voltage	Serial I/O	V_{IL}	-	-	V_{LS}
	Control I/O	V_{IL}	-	-	V_{LC}
Low-Level Output Voltage ($I_{OL} = -1.2$ mA)	Control I/O = 3.3 V, 5 V	V_{OL}	-	-	V_{LC}
	Control I/O = 1.8 V, 2.5 V	V_{OL}	-	-	V_{LC}
MUTECH auto detect input high voltage	V_{IH}	70%	-	-	VA
MUTECH auto detect input low voltage	V_{IL}	-	-	30%	VA
Maximum MUTECH Drive Current	I_{max}	-	3	-	mA
MUTECH High-Level Output Voltage	V_{OH}	-	VA	-	V
MUTECH Low-Level Output Voltage	V_{OL}	-	0	-	V

13. Any pin except supplies. Transient currents of up to ±100 mA on the input pins will not cause SCR latch-up

SWITCHING CHARACTERISTICS - PCM

(Inputs: Logic 0 = GND, Logic 1 = VLS, $C_L = 30$ pF)

Parameters		Symbol	Min	Max	Units
$\overline{\text{RST}}$ pin Low Pulse Width	(Note 14)		1	-	ms
MCLK Frequency			1.024	55.2	MHz
MCLK Duty Cycle	(Note 15)		45	55	%
Input Sample Rate - LRCK (Manual selection)	Single-Speed Mode	F_s	4	54	kHz
	Double-Speed Mode	F_s	50	108	
	Quad-Speed Mode	F_s	100	216	
Input Sample Rate - LRCK (Auto detect)	Single-Speed Mode	F_s	4	54	kHz
	Double-Speed Mode	F_s	84	108	
	Quad-Speed Mode	F_s	170	216	
LRCK Duty Cycle	(Note 16)		45	55	%
SCLK Duty Cycle			45	55	%
SCLK High Time		t_{sckh}	8	-	ns
SCLK Low Time		t_{sckl}	8	-	ns
LRCK Edge to SCLK Rising Edge		t_{lcks}	5	-	ns
SCLK Rising Edge to LRCK Falling Edge		t_{lckd}	5	-	ns
SDIN Setup Time Before SCLK Rising Edge		t_{ds}	3	-	ns
SDIN Hold Time After SCLK Rising Edge		t_{dh}	5	-	ns

Notes:

14. After powering up, $\overline{\text{RST}}$ should be held low until after the power supplies and clocks are settled.
15. See [Tables 1 - 3](#) for suggested MCLK frequencies.
16. Not required for TDM Mode.

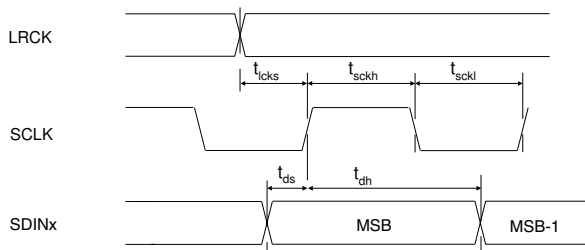


Figure 1. Serial Audio Interface Timing

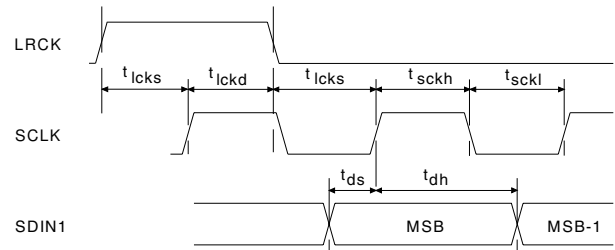


Figure 2. TDM Serial Audio Interface Timing

SWITCHING CHARACTERISTICS - DSD

(Logic 0 = AGND = DGND; Logic 1 = VLS; $C_L = 30$ pF)

Parameter	Symbol	Min	Typ	Max	Unit
MCLK Duty Cycle		40	-	60	%
DSD_SCLK Pulse Width Low	t_{sckl}	160	-	-	ns
DSD_SCLK Pulse Width High	t_{sckh}	160	-	-	ns
DSD_SCLK Frequency	(64x Oversampled)	1.024	-	3.2	MHz
	(128x Oversampled)	2.048	-	6.4	MHz
DSD_A / _B valid to DSD_SCLK rising setup time	t_{sdhrs}	20	-	-	ns
DSD_SCLK rising to DSD_A or DSD_B hold time	t_{sdh}	20	-	-	ns
DSD clock to data transition (Phase Modulation Mode)	t_{dpm}	-20	-	20	ns

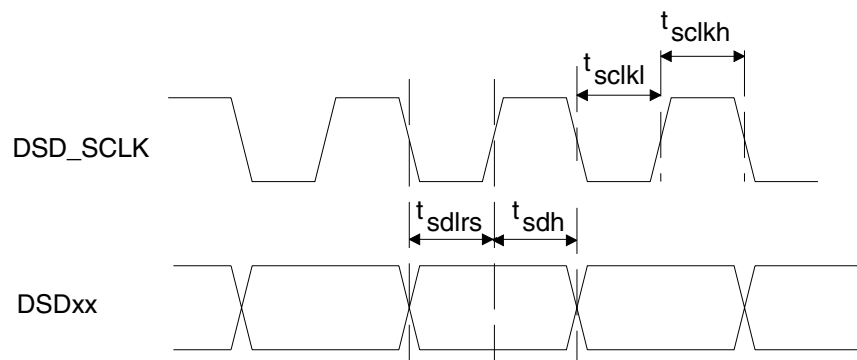


Figure 3. Direct Stream Digital - Serial Audio Input Timing

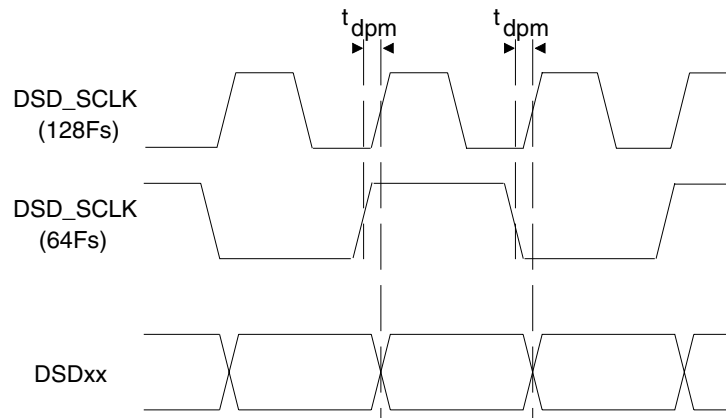


Figure 4. Direct Stream Digital - Serial Audio Input Timing for Phase Modulation Mode

SWITCHING CHARACTERISTICS - CONTROL PORT - I²C FORMAT

(Inputs: Logic 0 = GND, Logic 1 = VLC, C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f _{scl}	-	100	kHz
$\overline{\text{RST}}$ Rising Edge to Start	t _{irs}	500	-	ns
Bus Free Time Between Transmissions	t _{buf}	4.7	-	μs
Start Condition Hold Time (prior to first clock pulse)	t _{hdst}	4.0	-	μs
Clock Low time	t _{low}	4.7	-	μs
Clock High Time	t _{high}	4.0	-	μs
Setup Time for Repeated Start Condition	t _{sust}	4.7	-	μs
SDA Hold Time from SCL Falling (Note 17)	t _{hdd}	0	-	μs
SDA Setup time to SCL Rising	t _{sud}	250	-	ns
Rise Time of SCL and SDA	t _{rc} , t _{rc}	-	1	μs
Fall Time SCL and SDA	t _{fc} , t _{fc}	-	300	ns
Setup Time for Stop Condition	t _{susp}	4.7	-	μs
Acknowledge Delay from SCL Falling	t _{ack}	300	1000	ns

Notes:

17. Data must be held for sufficient time to bridge the transition time, t_{rc}, of SCL.

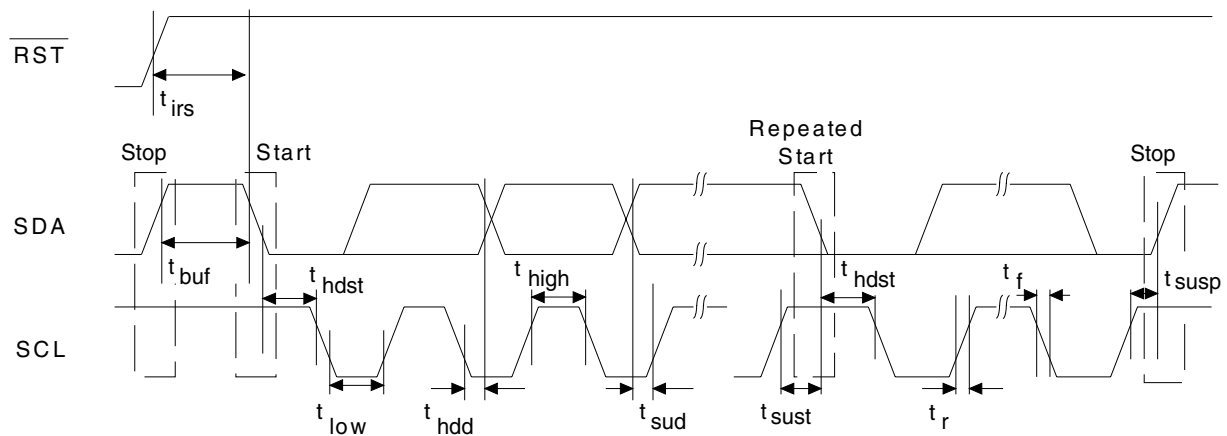


Figure 5. Control Port Timing - I²C Format

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI FORMAT

(Inputs: Logic 0 = GND, Logic 1 = VLC, $C_L = 30$ pF)

Parameter	Symbol	Min	Max	Unit
CCLK Clock Frequency	f_{sclk}	-	6	MHz
\overline{RST} Rising Edge to \overline{CS} Falling	t_{srs}	500	-	ns
CCLK Edge to \overline{CS} Falling (Note 18)	t_{spi}	500	-	ns
\overline{CS} High Time Between Transmissions	t_{csh}	1.0	-	μ s
\overline{CS} Falling to CCLK Edge	t_{css}	20	-	ns
CCLK Low Time	t_{scl}	66	-	ns
CCLK High Time	t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time	t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time (Note 19)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN (Note 20)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN (Note 20)	t_{f2}	-	100	ns

Notes:

18. t_{spi} only needed before first falling edge of \overline{CS} after \overline{RST} rising edge. $t_{spi} = 0$ at all other times.
19. Data must be held for sufficient time to bridge the transition time of CCLK.
20. For $F_{SCK} < 1$ MHz.

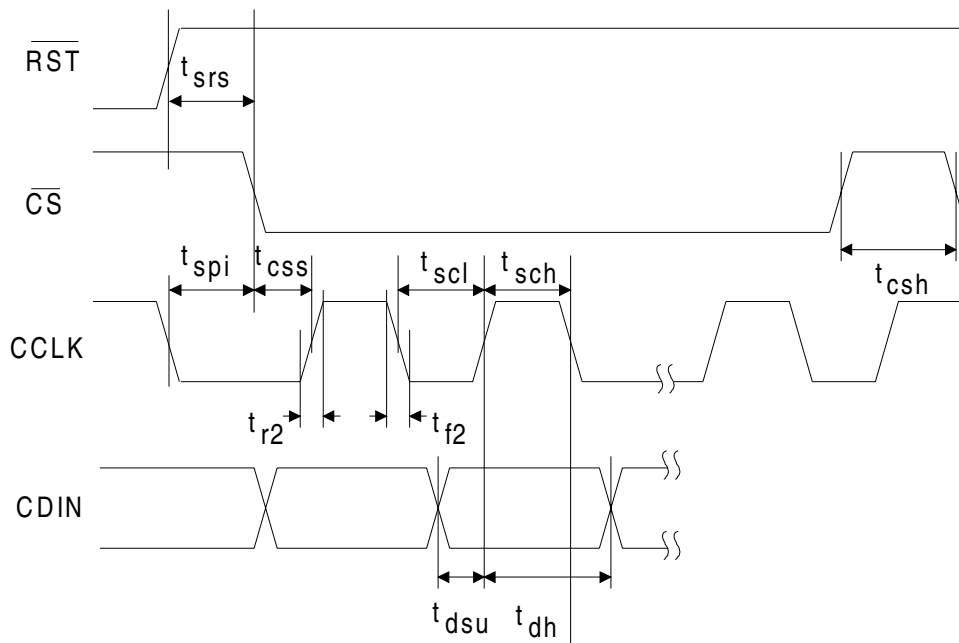


Figure 6. Control Port Timing - SPI Format

3. TYPICAL CONNECTION DIAGRAM

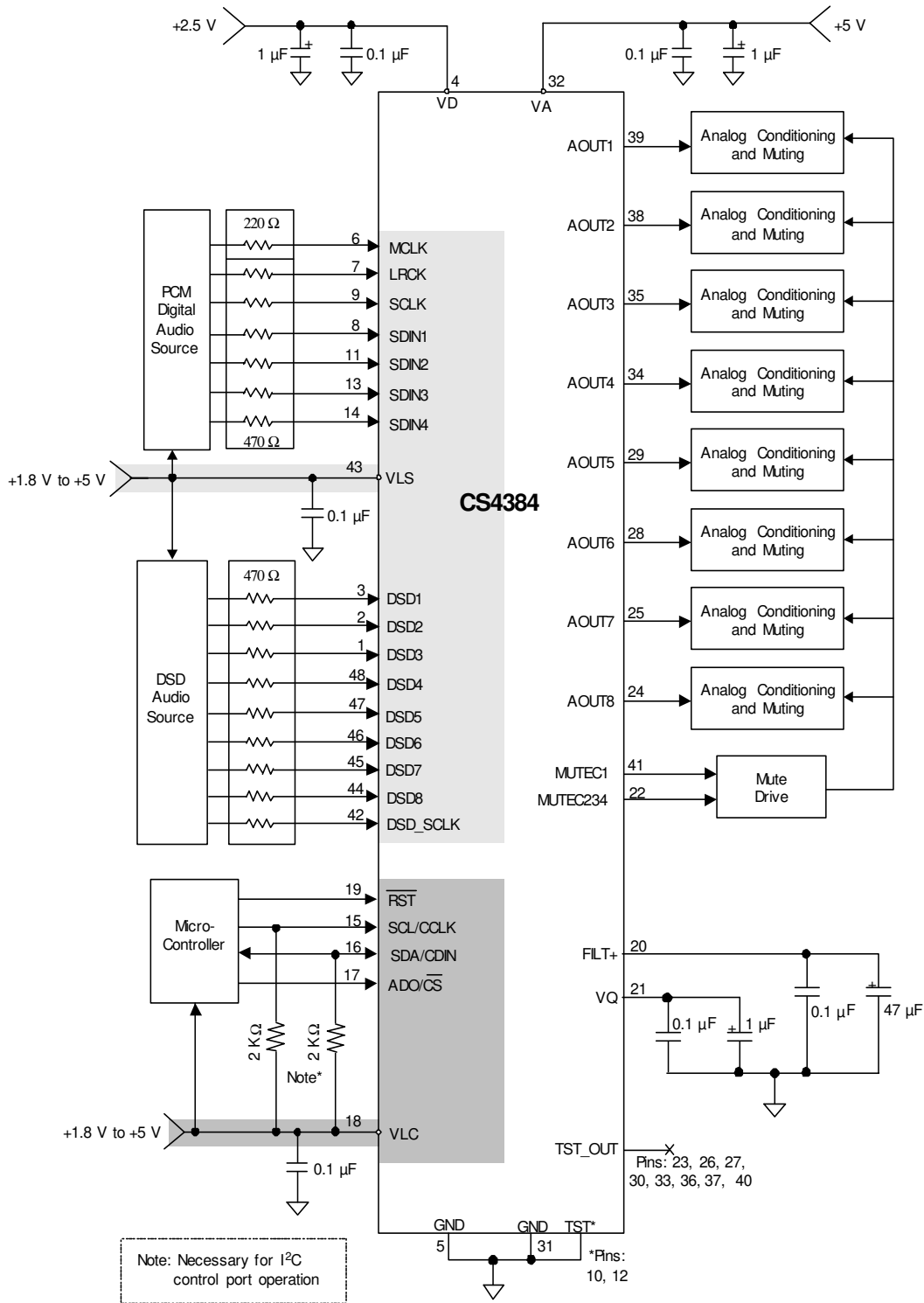
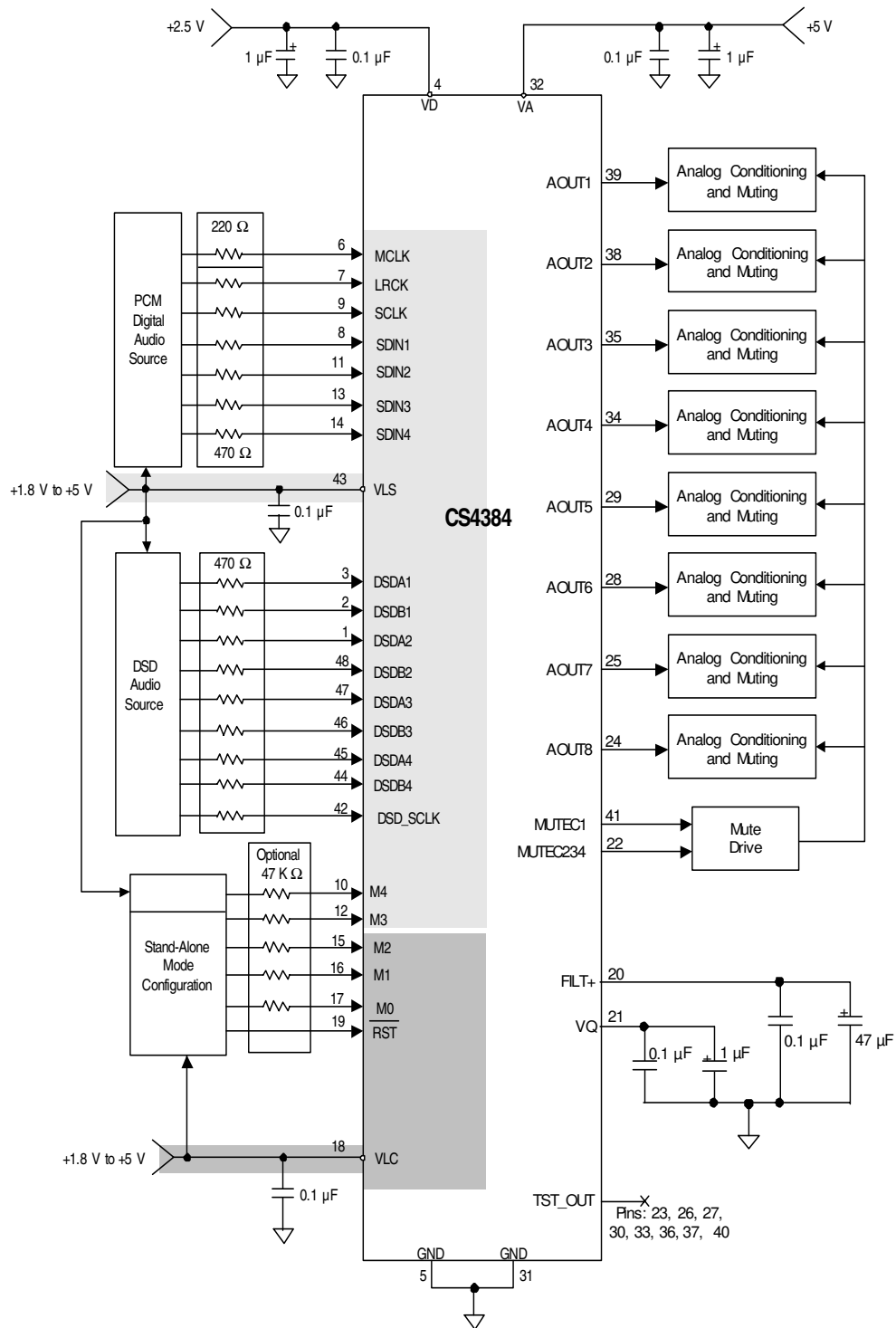


Figure 7. Typical Connection Diagram, Software Mode


Figure 8. Typical Connection Diagram, Hardware Mode

4. APPLICATIONS

The CS4384 serially accepts two complement formatted PCM data at standard audio sample rates including 48, 44.1 and 32 kHz in SSM, 96, 88.2 and 64 kHz in DSM, and 192, 176.4 and 128 kHz in QSM. Audio data is input via the serial data input pins (SDINx). The Left/Right Clock (LRCK) determines which channel is currently being input on SDINx, and the Serial Clock (SCLK) clocks audio data into the input data buffer. For more information on serial audio interfaces see AN282 “The 2-Channel Serial Audio Interface: A Tutorial”.

The CS4384 can be configured in Hardware Mode by the M0, M1, M2, M3 and M4 pins and in Software Mode through I²C or SPI.

4.1 Master Clock

MCLK/LRCK must be an integer ratio as shown in [Tables 1 - 3](#). The LRCK frequency is equal to Fs, the frequency at which words for each channel are input to the device. The MCLK-to-LRCK frequency ratio and speed mode is detected automatically during the initialization sequence by counting the number of MCLK transitions during a single LRCK period and by detecting the absolute speed of MCLK. Internal dividers are then set to generate the proper internal clocks. [Tables 1 - 3](#) illustrate several standard audio sample rates and the required MCLK and LRCK frequencies. Please note there is no required phase relationship, but MCLK, LRCK and SCLK must be synchronous.

Sample Rate (kHz)	MCLK (MHz)					
	256x	384x	512x	768x	1024x	1152x
32	8.1920	12.2880	16.3840	24.5760	32.7680	36.8640
44.1	11.2896	16.9344	22.5792	33.8688	45.1584	
48	12.2880	18.4320	24.5760	36.8640	49.1520	

Table 1. Single-Speed Mode Standard Frequencies

Sample Rate (kHz)	MCLK (MHz)				
	128x	192x	256x	384x	512x
64	8.1920	12.2880	16.3840	24.5760	32.7680
88.2	11.2896	16.9344	22.5792	33.8688	45.1584
96	12.2880	18.4320	24.5760	36.8640	49.1520

Table 2. Double-Speed Mode Standard Frequencies

Sample Rate (kHz)	MCLK (MHz)				
	64x	96x	128x	192x	256x
176.4	11.2896	16.9344	22.5792	33.8688	45.1584
192	12.2880	18.4320	24.5760	36.8640	49.1520

Table 3. Quad-Speed Mode Standard Frequencies

= Denotes clock ratio and sample rate combinations which are NOT supported under auto speed-mode detection. Please see [“Switching Characteristics - PCM”](#) on page 14.

4.2 Mode Select

In Hardware Mode, operation is determined by the Mode Select pins. The states of these pins are continually scanned for any changes; however, the mode should only be changed while the device is in reset (RST pin low) to ensure proper switching from one mode to another. These pins require connection to supply or ground as outlined in [Figure 8](#). For M0, M1, and M2, supply is VLC. For M3 and M4, supply is VLS. [Tables 4 - 6](#) show the decode of these pins.

In Software Mode, the operational mode and data format are set in the FM and DIF registers. See [“PCM Control \(Address 03h\)”](#) on page 36.

M1 (DIF1)	M0 (DIF0)	DESCRIPTION	FORMAT	FIGURE
0	0	Left Justified, up to 24-bit data	0	9
0	1	I ² S, up to 24-bit data	1	10
1	0	Right Justified, 16-bit Data	2	11
1	1	Right Justified, 24-bit Data	3	12

Table 4. PCM Digital Interface Format, Hardware Mode Options

M4	M3	M2 (DEM)	M1	M0	DESCRIPTION
0	0	0	Table 4		Single-Speed without De-Emphasis (4 kHz to 50 kHz sample rates)
0	0	1			Single-Speed with 44.1 kHz De-Emphasis; see Figure 20
0	1	0			Double-Speed (50 kHz to 100 kHz sample rates)
0	1	1			Quad-Speed (100 kHz to 200 kHz sample rates)
1	0	0			Auto Speed-Mode Detect (32 kHz to 200 kHz sample rates)
1	0	1			Auto Speed-Mode Detect with 44.1 kHz De-Emphasis; see Figure 20
1	1		Table 6		DSD Processor Mode

Table 5. Mode Selection, Hardware Mode Options

M2	M1	M0	DESCRIPTION
0	0	0	64x oversampled DSD data with a 4x MCLK to DSD data rate
0	0	1	64x oversampled DSD data with a 6x MCLK to DSD data rate
0	1	0	64x oversampled DSD data with a 8x MCLK to DSD data rate
0	1	1	64x oversampled DSD data with a 12x MCLK to DSD data rate
1	0	0	128x oversampled DSD data with a 2x MCLK to DSD data rate
1	0	1	128x oversampled DSD data with a 3x MCLK to DSD data rate
1	1	0	128x oversampled DSD data with a 4x MCLK to DSD data rate
1	1	1	128x oversampled DSD data with a 6x MCLK to DSD data rate

Table 6. Direct Stream Digital (DSD), Hardware Mode Options

4.3 Digital Interface Formats

The serial port operates as a slave and supports the I²S, Left-Justified, Right-Justified, One-Line Mode (OLM) and TDM digital interface formats with varying bit depths from 16 to 32 as shown in [Figures 9-19](#). Data is clocked into the DAC on the rising edge. OLM and TDM configurations are only supported in Software Mode.

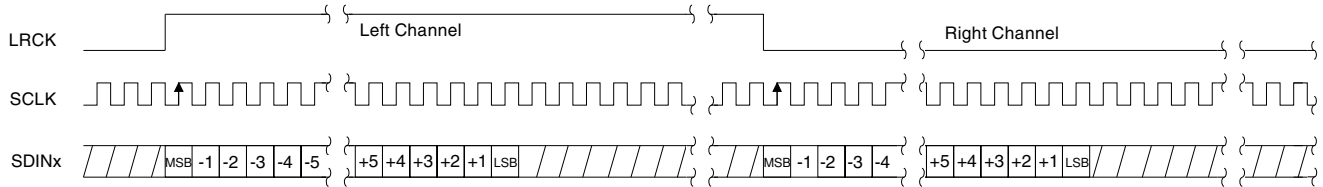


Figure 9. Format 0 - Left-Justified up to 24-bit Data

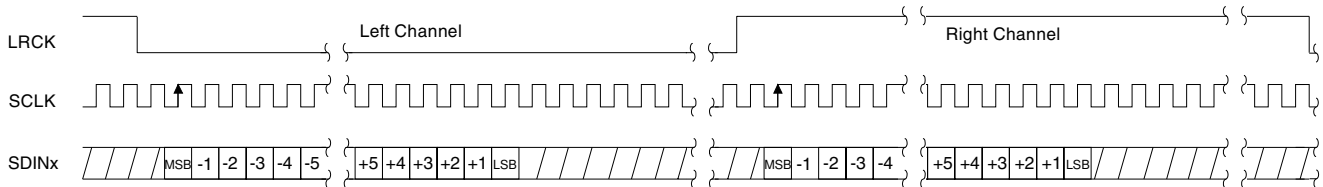


Figure 10. Format 1 - I²S up to 24-bit Data

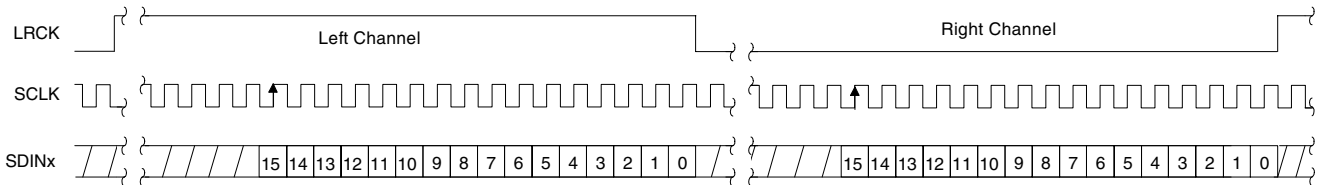


Figure 11. Format 2 - Right-Justified 16-bit Data

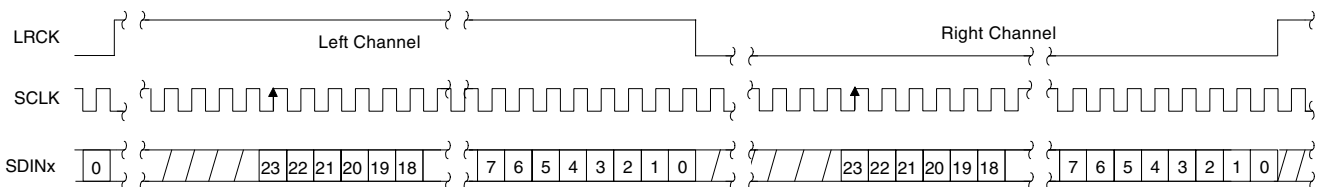


Figure 12. Format 3 - Right-Justified 24-bit Data

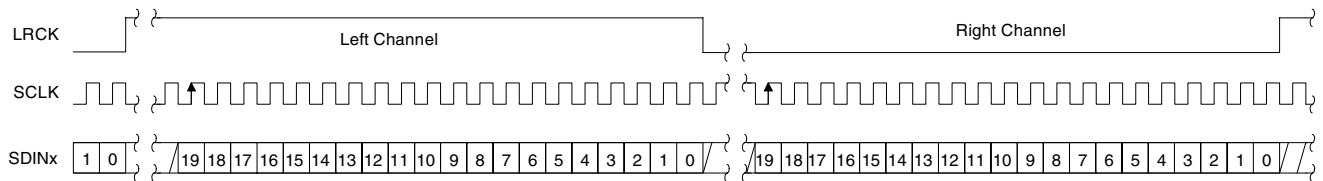


Figure 13. Format 4 - Right-Justified 20-bit Data

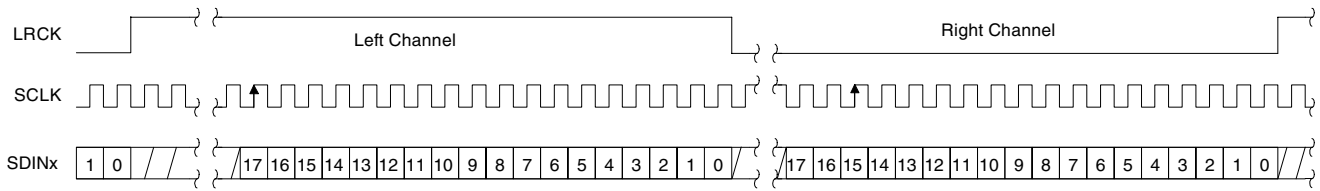


Figure 14. Format 5 - Right-Justified 18-bit Data

4.3.1 OLM #1

OLM #1 serial audio interface format operates in Single-, Double-, or Quad-Speed Mode and will slave to SCLK at 128 Fs. Six channels of MSB first 20-bit PCM data are input on SDIN1. The last two channels are input on SDIN4.

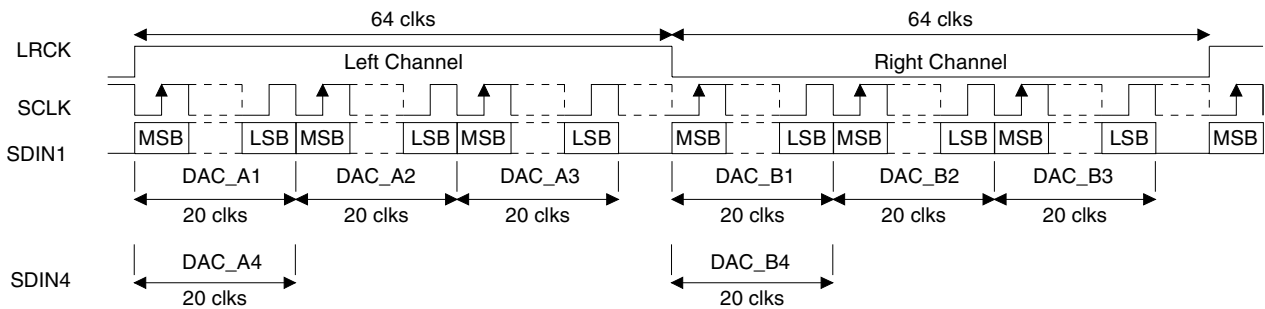


Figure 15. Format 8 - One Line Mode 1

4.3.2 OLM #2

OLM #2 serial audio interface format operates in Single-, Double-, or Quad-Speed Mode and will slave to SCLK at 256 Fs. Six channels of MSB first 24-bit PCM data are input on SDIN1. The last two channels are input on SDIN4.

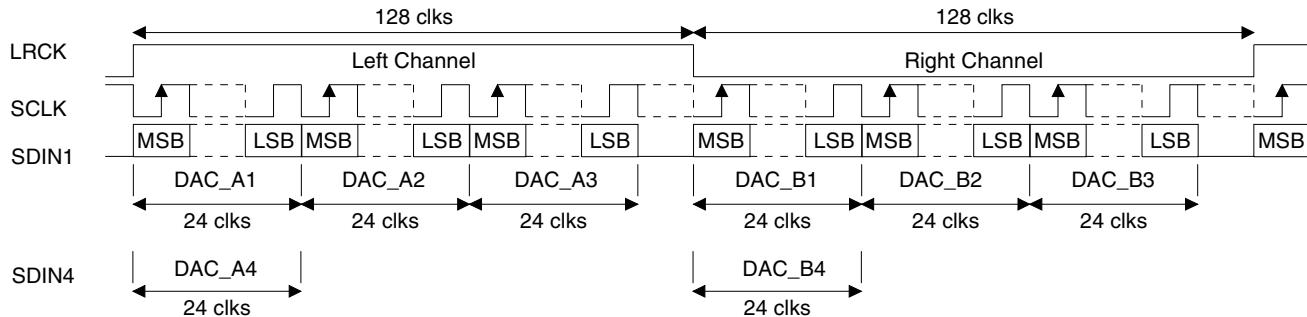


Figure 16. Format 9 - One Line Mode 2

4.3.3 OLM #3

OLM #3 serial audio interface format operates in Single-, Double-, or Quad-Speed Mode and will slave to SCLK at 256 Fs. Eight channels of MSB first 20-bit PCM data are input on SDIN1.

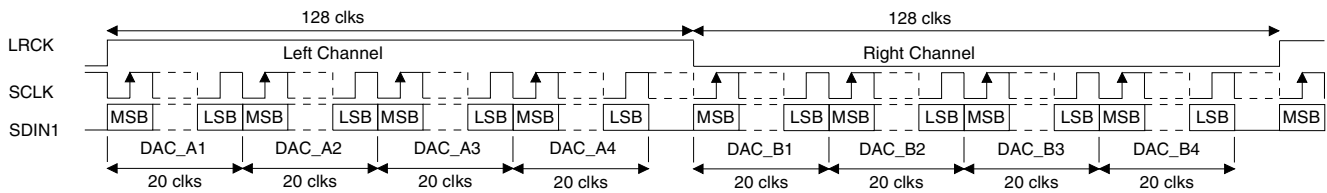


Figure 17. Format 10 - One Line Mode 3

4.3.4 OLM #4

OLM #4 serial audio interface format operates in Single-, Double-, or Quad-Speed Mode and will slave to SCLK at 256 Fs. Eight channels of MSB first 24-bit PCM data are input on SDIN1.

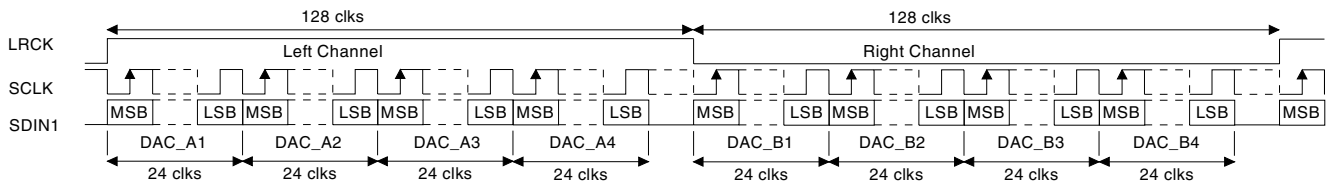


Figure 18. Format 11 - One Line Mode 4

4.3.5 TDM

The TDM serial audio interface format operates in Single-, Double-, or Quad-Speed Mode and will slave to SCLK at 256 Fs. Data is received most significant bit first on the first SCLK after an LTRCK transition and is valid on the rising edge of SCLK. LTRCK identifies the start of a new frame and is equal to the sample rate, Fs. LTRCK is sampled as valid on the rising SCLK edge preceding the most significant bit of the first data sample and must be held valid for one SCLK period. Each time slot is 32 bits wide, with the valid data sample left justified within the time slot with the remaining bits being zero padded.

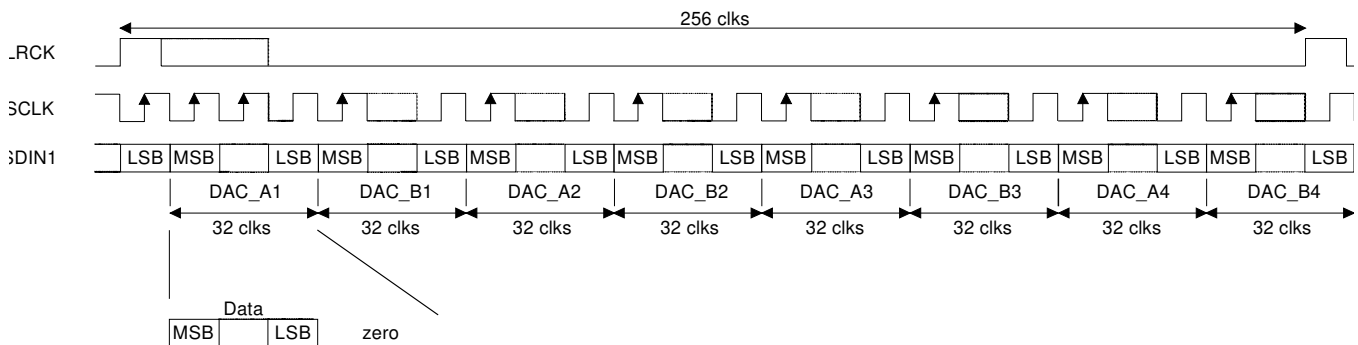


Figure 19. Format 12 - TDM Mode

4.4 Oversampling Modes

The CS4384 operates in one of three oversampling modes based on the input sample rate. Mode selection is determined by the M4, M3 and M2 pins in Hardware Mode or the FM bits in Software Mode. Single-Speed Mode supports input sample rates up to 50 kHz and uses a 128x oversampling ratio. Double-Speed Mode supports input sample rates up to 100 kHz and uses an oversampling ratio of 64x. Quad-Speed Mode supports input sample rates up to 200 kHz and uses an oversampling ratio of 32x.

The auto speed-mode detect feature allows for the automatic selection of speed mode based off of the incoming sample rate. This allows the CS4384 to accept a wide range of sample rates with no external intervention necessary. The auto speed-mode detect feature is available in both Hardware and Software Mode.

4.5 Interpolation Filter

To accommodate the increasingly complex requirements of digital audio systems, the CS4384 incorporates selectable interpolation filters for each mode of operation. A “fast” and a “slow” roll-off filter is available in each of Single-, Double-, or Quad-Speed Modes. These filters have been designed to accommodate a variety of musical tastes and styles. The `FILT_SEL` bit is used to select which filter is used (see the “[Parameter Definitions](#)” on page 49 for more details).

When in Hardware Mode, only the “fast” roll-off filter is available.

Filter specifications can be found in [Section 2](#), and filter response plots can be found in [Figures 28 to 51](#).

4.6 De-Emphasis

The CS4384 includes on-chip digital de-emphasis filters. The de-emphasis feature is included to accommodate older audio recordings that utilize pre-emphasis equalization as a means of noise reduction. [Figure 20](#) shows the de-emphasis curve. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, F_s if the input sample rate does not match the coefficient which has been selected.

In Software Mode the required de-emphasis filter coefficients for 32 kHz, 44.1 kHz, or 48 kHz are selected via the de-emphasis control bits.

In Hardware Mode only the 44.1 kHz coefficient is available (enabled through the M2 pin). If the input sample rate is not 44.1 kHz and de-emphasis has been selected then the corner frequencies of the de-emphasis filter will be scaled by a factor of the actual F_s over 44,100.

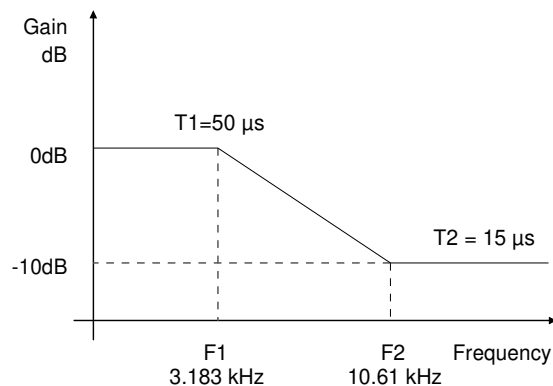


Figure 20. De-Emphasis Curve