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CIRRUS LOGIC®

CS4392

24-Bit, 192 kHz Stereo DAC with Volume Control

Features

- Complete Stereo DAC System: Interpolation, D/A, Output Analog Filtering
- 114 dB Dynamic Range
- 100 dB THD+N
- Up to 192kHz Sample Rates
- Direct Stream Digital Mode
- Low Clock Jitter Sensitivity
- Single +5 V Power Supply
- Selectable Digital Filters
  - Fast and Slow roll-off
- Volume Control with Soft Ramp
  - 1 dB Step Size
  - Zero Crossing Click-Free Transitions
- Direct Interface with 5 V to 1.8 V Logic
- ATAPI Mixing Functions
- Pin Compatible with the CS4391

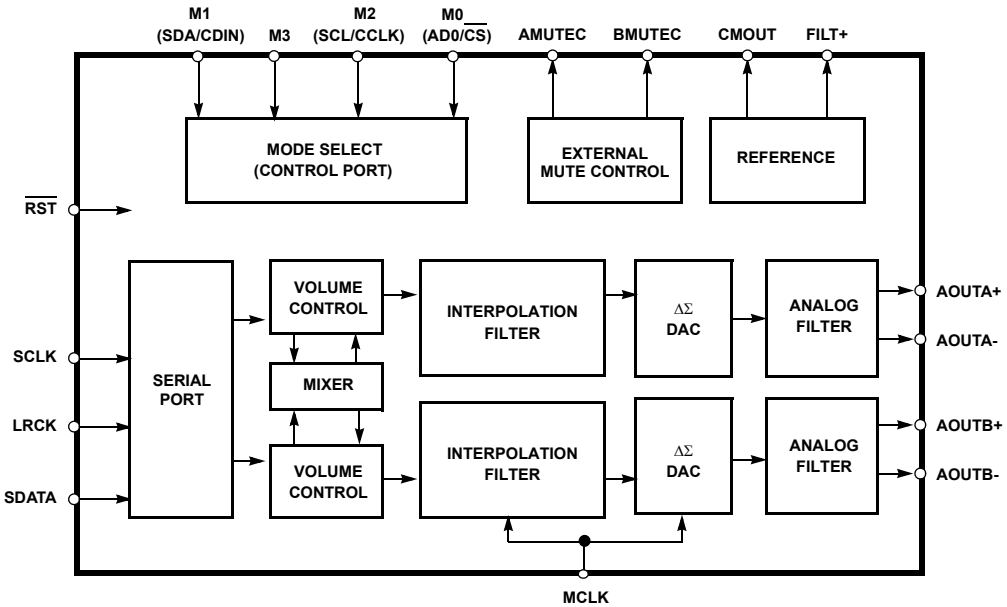
Description

The CS4392 is a complete stereo digital-to-analog system including digital interpolation, fifth-order delta-sigma digital-to-analog conversion, digital de-emphasis, volume control, channel mixing and analog filtering. The advantages of this architecture include: ideal differential linearity, no distortion mechanisms due to resistor matching errors, no linearity drift over time and temperature, and a high tolerance to clock jitter.

The CS4392 accepts PCM data at sample rates from 4 kHz to 192 kHz, DSD audio data, has selectable digital filters, and consumes very little power. These features are ideal for DVD, SACD players, A/V receivers, CD and set-top box systems. The CS4392 is pin and register compatible with the CS4391, making easy performance upgrades possible.

ORDERING INFORMATION

CS4392-KS	-10 to 70 °C	20-pin SOIC
CS4392-KZ	-10 to 70 °C	20-pin TSSOP
CS4392-KZZ, Lead Free	-10 to 70 °C	20-pin TSSOP
CDB4392		Evaluation Board



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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To find one nearest you go to **http://www.cirrus.com/corporate/contacts/sales.cfm**

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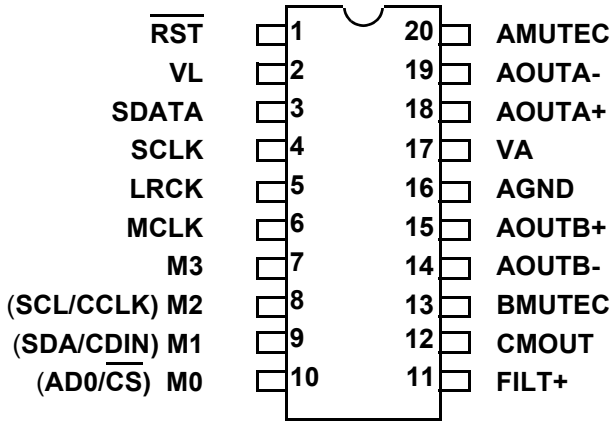
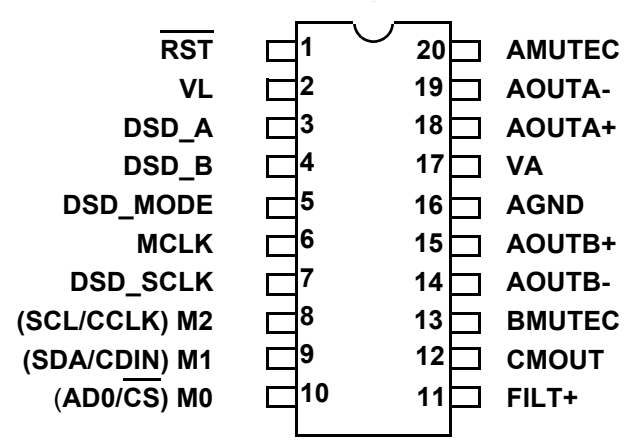
1. PIN DESCRIPTION - PCM DATA MODE



RST	1	**Reset** (*Input*) - Powers down device and resets all internal registers to their default settings.
VL	2	**Logic Power** (*Input*) **-** Positive power for the digital input/output.
SDATA	3	**Serial Audio Data** (*Input*) - Input for two's complement serial audio data.
SCLK	4	**Serial Clock** (*Input*/*Output*) - Serial clock for the serial audio interface.
LRCK	5	**Left Right Clock** (*Input*/*Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	6	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
FILT+	11	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.
CMOUT	12	**Common Mode Voltage** (*Output*) - Filter connection for internal quiescent voltage.
AMUTEC **BMUTEC**	20 13	**Mute Control** (*Output*) - The Mute Control pin goes high during power-up initialization, reset, muting, power-down or if the master clock to left/right clock frequency ratio is incorrect.
AOUTB- **AOUTB+** **AOUTA+** **AOUTA**	14 15 18 19	**Differential Analog Output** (*Outputs*) - The full scale differential analog output level is specified in the Analog Characteristics specification table.
AGND	16	**Ground** (*Input*)
VA	17	**Analog Power** (*Input*) **-** Positive power for the analog section.
Control Port Mode Definitions		
M3	7	**Mode Selection** (*Input*) - This pins should be tied to GND level during control port mode.
SCL/CCLK	8	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port.
SDA/CDIN	9	**Serial Control Data** (*Input/Output*) - SDA is a data I/O line in I^2C mode. CDIN is the input data line for the control port interface in SPI mode.
AD0/CS	10	**Address Bit 0 (I^2C) / Control Port Chip Select (SPI)** (*Input/Output*) - AD0 is a chip address pin in I^2C mode; $\overline{CS}$ is the chip select signal for SPI format.
Stand-Alone Mode Definitions		
M3 **M2** **M1** **M0**	7 8 9 10	**Mode Selection** (*Input*) - Determines the operational mode of the device.

1.1 PIN DESCRIPTION - DSD mode



DSD_A **DSD_B**	3 4	**DSD Data** (*Input*) - Input for Direct Stream Digital serial audio data.
DSD_Mode	5	**DSD Mode** *(Input)* - In stand alone mode, this pin must be set to a logic '1' for operation of DSD Mode.
DSD_SCLK	7	**DSD Serial Clock** (*Input*/*Output*) - Serial clock for the Direct Stream Digital audio interface.

2. TYPICAL CONNECTION DIAGRAMS

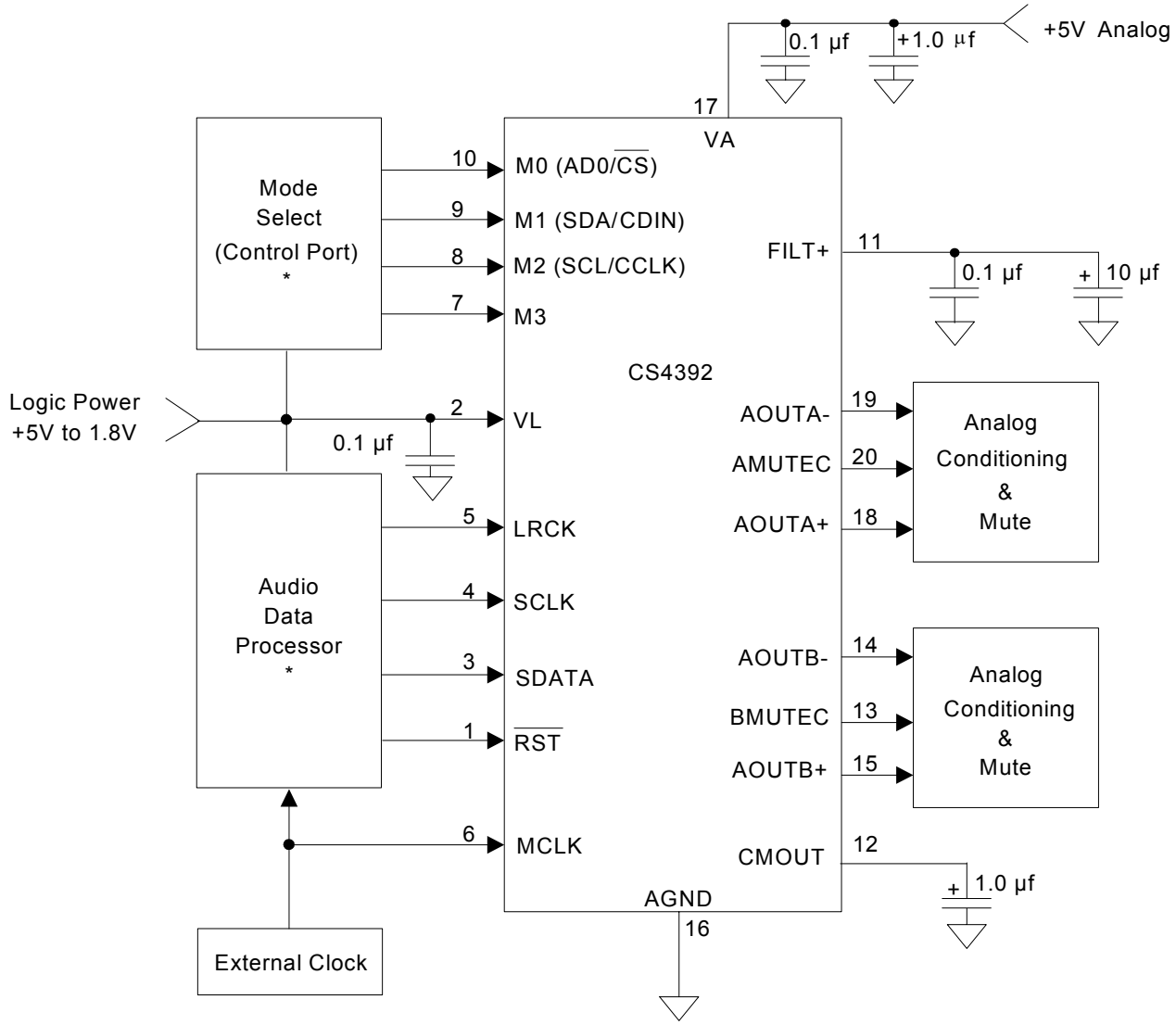


Figure 1. Typical Connection Diagram - PCM Mode
* A high logic level for all digital inputs should not exceed VL.

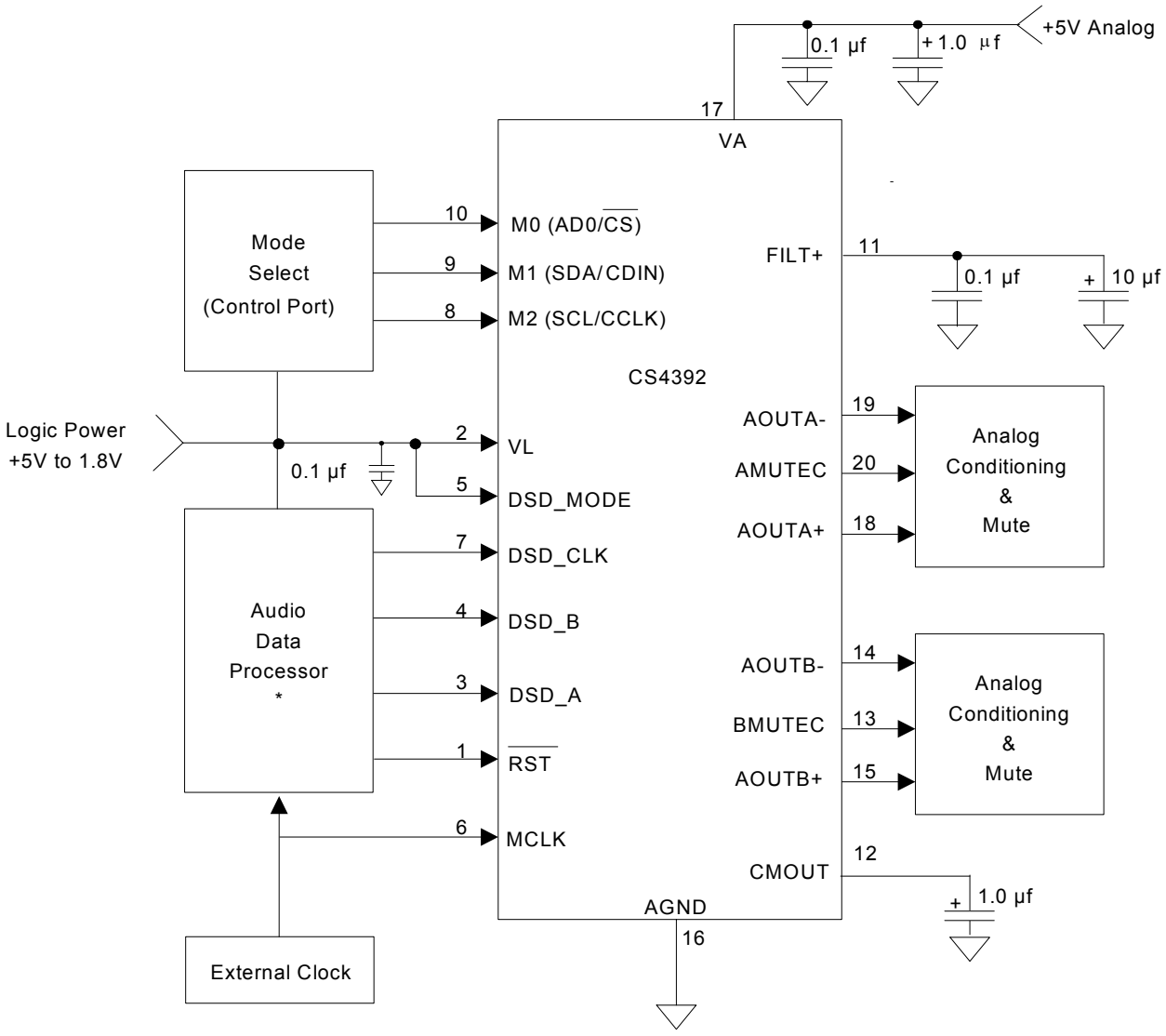


Figure 2. Typical Connection Diagram - DSD Mode

* A high logic level for all digital inputs should not exceed VL.

3. APPLICATIONS

3.1 Recommended Power-up Sequence for Hardware Mode

1) Hold $\overline{\text{RST}}$ low until the power supplies, master, and left/right clocks are stable.
2) Bring $\overline{\text{RST}}$ high. After 10ms the device will begin normal operation.

3.2 Recommended Power-up Sequence and Access to Control Port Mode

1) Hold $\overline{\text{RST}}$ low until the power supply, master, and left/right clocks are stable. In this state, the control port is reset to its default settings and FILT+ will remain low.
2) Bring $\overline{\text{RST}}$ high. The device will remain in a low power state with FILT+ low and the control port is accessible.
3) Write 30h to register 05h within 10 ms cycles following the release of $\overline{\text{RST}}$. If after 10ms the control port has not been initiated with this command, the device will enter stand-alone mode. The CPEN bit, however, may be written at any time after 10ms. It is recommended to write CPEN before 10ms in order to reduce the possibility of any extraneous click or pop noise from occurring.
4) The desired register settings can be loaded while keeping the PDN bit set to 1.
5) Set the PDN bit to 0. This will initiate the power-up sequence which requires approximately 10 µS.

3.3 Analog Output and Filtering

The application note "Design Notes for a 2-Pole Filter with Differential Input" discusses the second-order Butterworth filter and differential to single-ended converter as seen in Figure 3. An alternate configuration can be seen on the CDB4392. This alternate filter configuration accounts for the differing AC loads on the + and - differential output pins which are normally present in a circuit like Figure 3. It also shows an AC coupling configuration which reduces the number of required AC coupling capacitors to 2 caps per channel. The circuit in figure 3 may also be DC coupled, however the filter on the CDB4392 must be AC coupled. The CS4392 is a linear phase design and does not include phase or amplitude compensation for an external filter. Therefore, the DAC system phase and amplitude response will be dependent on the external analog circuitry.

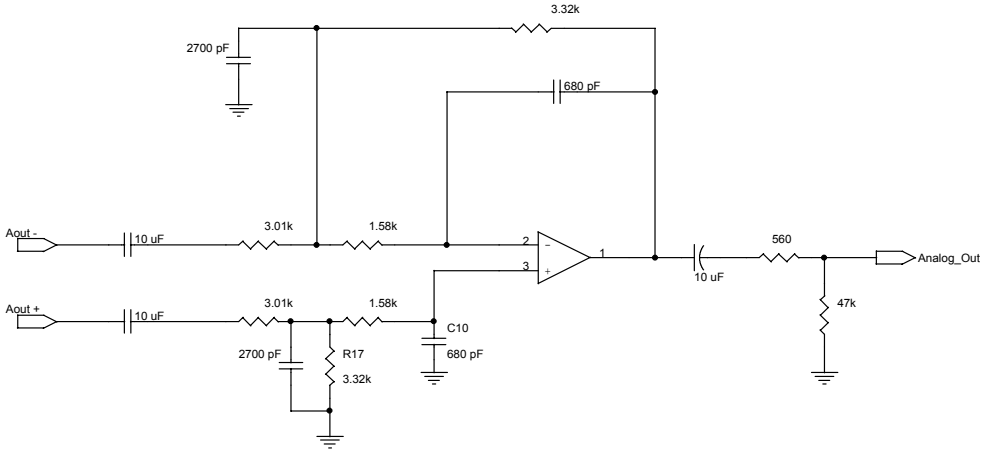


Figure 3. CS4392 Output Filter

3.4 Interpolation Filter

To accommodate the increasingly complex requirements of digital audio systems, the CS4392 incorporates selectable interpolation filters for each mode of operation. A fast and a slow roll-off filter is available in each of Single, Double, and Quad Speed modes. These filters have been designed to accommodate a variety of musical tastes and styles. Bit 5 of the Mode Control 3 register (06h) is used to select which filter is used. Filter specifications can be found in Section 8, and filter response plots can be found in Figures 12 to 35.

In stand-alone mode, only the fast roll-off filter is available.

3.5 System Clocking

The required MCLK to LRCK and suggested SCLK to LRCK ratios are outlined in table 1. MCLK can be at any phase in regards to LRCK and SCLK. SCLK, LRCK and SDATA must meet the phase and timing relationships outlined in Section 7. Some common MCLK frequencies have been outlined in tables 2 to 4.

	MCLK/LRCK	SCLK/LRCK	LRCK
Single Speed	256, 384, 512, 768, 1024*	32, 48, 64, 96, 128	Fs
Double Speed	128, 192, 256, 384, 512*	32, 48, 64	Fs
Quad Speed	64	32 (16 bits only)	Fs
	96	32, 48	Fs
	128, 256*	32, 64	Fs
	192	32, 48, 64, 96	Fs

Table 1. Clock Ratios

Sample Rate (kHz)	MCLK (MHz)				See Note
	256x	384x	512x	768x	1024x*
32	8.1920	12.2880	16.3840	24.5760	32.7680
44.1	11.2896	16.9344	22.5792	33.8688	45.1584
48	12.2880	18.4320	24.5760	36.8640	49.1520

Table 2. Single Speed (4 to 50 kHz sample rates) Common Clock Frequencies

Sample Rate (kHz)	MCLK (MHz)				See Note
	128x	192x	256x	384x	512x*
64	8.1920	12.2880	16.3840	24.5760	32.7680
88.2	11.2896	16.9344	22.5792	33.8688	45.1584
96	12.2880	18.4320	24.5760	36.8640	49.1520

Table 3. Double Speed (50 to 100 kHz sample rates) Common Clock Frequencies

Sample Rate (kHz)	MCLK (MHz)				See Note
	64x	96x	128x	192x	256x*
176.4	11.2896	16.9344	22.5792	33.8688	45.1584
192	12.2880	18.4320	24.5760	36.8640	49.1520

Table 4. Quad Speed (100 to 200 kHz sample rates) Common Clock Frequencies

*Note:These clocking ratios are only available in Control Port Mode when the MCLK Divide bit is enabled.

3.6 Digital Interface Format

The device will accept audio samples in several digital interface formats as illustrated in Tables 5 and 8. The desired format is selected via the M0 and M1 pins for stand alone mode, and through the DIF2:0 bits in the control port. For an illustration of the required relationship between the Left/Right Clock, Serial Clock and Serial Audio Data, see Figures 4-6.

M1	M0	DESCRIPTION	FORMAT	FIGURE
0	0	Left Justified, up to 24-bit data	0	4
0	1	I^2S, up to 24-bit data	1	5
1	0	Right Justified, 16-bit Data	2	6
1	1	Right Justified, 24-bit Data	3	6

Table 5. Digital Interface Format, Stand-Alone Mode Options

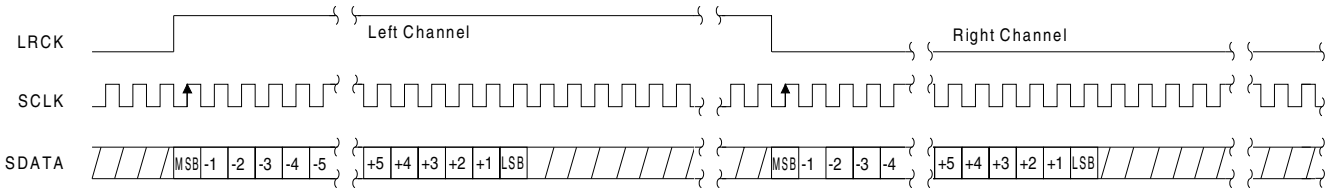


Figure 4. Format 0, Left Justified up to 24-Bit Data

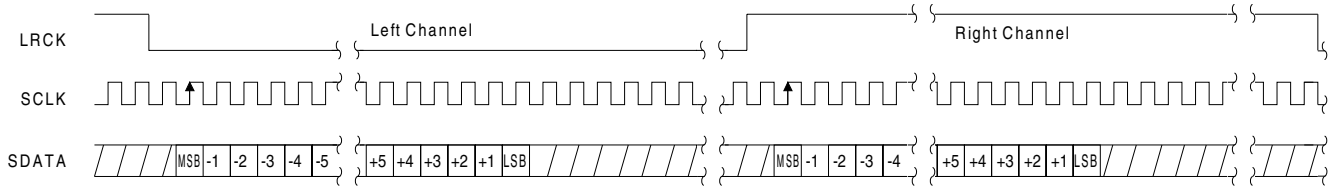


Figure 5. Format 1, I^2S up to 24-Bit Data

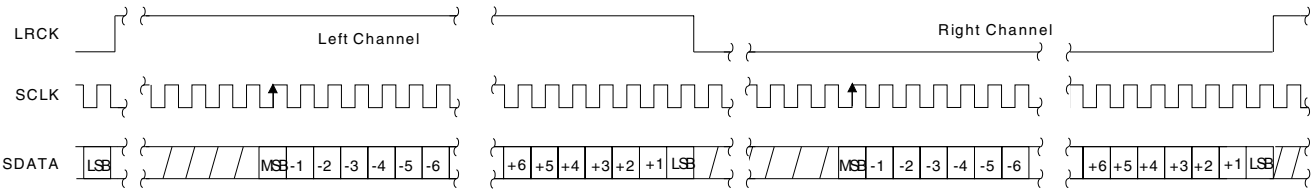


Figure 6. Format 2, Right Justified 16-Bit Data
Format 3, Right Justified 24-Bit Data
Format 4, Right Justified 20-Bit Data. (Available in Control Port Mode only)
Format 5, Right Justified 18-Bit Data. (Available in Control Port Mode only)

3.7 De-Emphasis

The device includes on-chip digital de-emphasis. Figure 7 shows the de-emphasis curve for F_S equal to 44.1 kHz. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, F_S. Please see Table 5 for the desired de-emphasis control for Stand-alone mode and Table 10 for control port mode.

The de-emphasis feature is included to accommodate audio recordings that utilize 50/15 µS pre-emphasis equalization as a means of noise reduction.
De-emphasis is only available in Single Speed Mode.

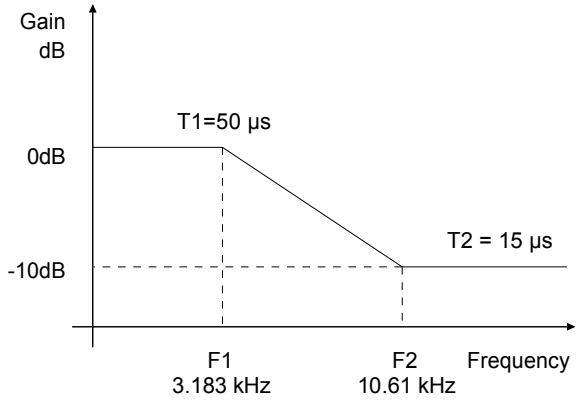


Figure 7. De-Emphasis Curve

M2 (DEM)	DESCRIPTION	FIGURE
0	No De-Emphasis	
1	De-Emphasis Enabled	7

Table 5. De-Emphasis Select, Stand-Alone Mode

3.8 Oversampling Modes

The CS4392 operates in one of three oversampling modes based on the input sample rate. Mode selection is determined by the M3 and M2 pins in Stand-Alone mode or the FM bits in Control Port mode. Single-Speed mode supports input sample rates up to 50 kHz and uses a 128x oversampling ratio. Double-Speed mode supports input sample rates up to 100 kHz and uses an oversampling ratio of 64x. Quad-Speed mode supports input sample rates up to 200 kHz and uses an oversampling ratio of 32x

M3	M2	DESCRIPTION
0	0	Single-Speed without De-Emphasis (4 to 50 kHz sample rates)
0	1	Single-Speed with 44.1kHz De-Emphasis
1	0	Double-Speed (50 to 100 kHz sample rates)
1	1	Quad-Speed (100 to 200 kHz sample rates)

Table 6. Mode Selection, Stand-Alone Mode Options

3.9 Using DSD mode

In stand-alone mode, DSD operation is selected by holding DSD_EN(LRCK) high and applying the DSD data and clocks to the appropriate pins. The M2:0 pins set the expected DSD rate and MCLK ratio.

In control-port mode the FM bits set the device into DSD mode (DSD_EN pin is not required to be held high). The DIF register then controls the expected DSD rate and MCLK ratio.

DSD_Mode	M2	M1	M0	DESCRIPTION
1	0	0	0	64x oversampled DSD data with a 4x MCLK to DSD data rate
1	0	0	1	64x oversampled DSD data with a 6x MCLK to DSD data rate
1	0	1	0	64x oversampled DSD data with a 8x MCLK to DSD data rate
1	0	1	1	64x oversampled DSD data with a 12x MCLK to DSD data rate
1	1	0	0	128x oversampled DSD data with a 2x MCLK to DSD data rate
1	1	0	1	128x oversampled DSD data with a 3x MCLK to DSD data rate
1	1	1	0	128x oversampled DSD data with a 4x MCLK to DSD data rate
1	1	1	1	128x oversampled DSD data with a 6x MCLK to DSD data rate

Table 7. Direct Stream Digital (DSD), Stand-Alone Mode Options

3.10 Mute Control

The Mute Control pins go high during power-up initialization, reset, or if the Master Clock to Left Right Clock ratio is incorrect. These pins will also go high following the reception of 8192 consecutive audio samples of static 0 or -1 on both the left and right channels. A single sample of non-zero data on either channel will cause the Mute Control pins to go low. These pins are intended to be used as control for an external mute circuit in order to add off-chip mute capability.

Use of the Mute Control function is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the Mute Control function can enable the system designer to achieve idle channel noise/signal-to-noise ratios which are only limited by the external mute circuit. See the CDB4392 data sheet for a suggested mute circuit.

4. CONTROL PORT INTERFACE

The control port is used to load all the internal register settings (see section 6). The operation of the control port may be completely asynchronous with the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port operates in one of two modes: I^2C
or SPI.

Notes: MCLK must be applied during all I^2C communication.

4.0.1 MAP Auto Increment

The device has MAP (memory address pointer) auto increment capability enabled by the INCR bit (also the MSB) of the MAP. If INCR is set to 0, MAP will stay constant for successive I^2C writes or reads, and SPI writes. If INCR is set to 1, MAP will auto increment after each byte is written, allowing block reads or writes of successive registers.

4.0.2 I^2C Mode

In the I^2C mode, data is clocked into and out of the bi-directional serial control data line, SDA, by the serial control port clock, SCL (see Figure 8 for the clock to data relationship). There is no $\overline{CS}$ pin. Pin AD0 enables the user to alter the chip address (001000[AD0][R/$\overline{W}$]) and should be tied to VL or AGND as required, before powering up the device. If the device ever detects a high to low transition on the AD0/$\overline{CS}$ pin after power-up, SPI mode will be selected.

4.0.2a I^2C Write

To write to the device, follow the procedure below while adhering to the control port Switching Specifications in section 7.

1) Initiate a START condition to the I^2C bus followed by the address byte. The upper 6 bits must be 001000. The seventh bit must match the setting of the AD0 pin, and the eighth must be 0. The eighth bit of the address byte is the R/$\overline{W}$ bit.

2) Wait for an acknowledge (ACK) from the part, then write to the memory address pointer, MAP. This byte points to the register to be written.

3) Wait for an acknowledge (ACK) from the part, then write the desired data to the register pointed to by the MAP.

4) If the INCR bit (see section 4.0.1) is set to 1, repeat the previous step until all the desired registers are written, then initiate a STOP condition to the bus.

5) If the INCR bit is set to 0 and further I^2C writes to other registers are desired, it is necessary to initiate a repeated START condition and follow the procedure detailed from step 1. If no further writes to other registers are desired, initiate a STOP condition to the bus.

4.0.2b I²C Read

To read from the device, follow the procedure below while adhering to the control port *Switching Specifications*.

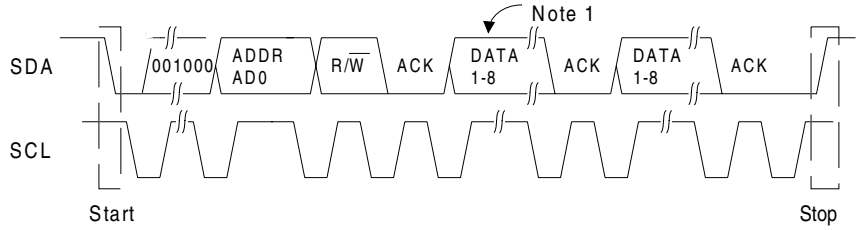
1) Initiate a START condition to the I²C bus followed by the address byte. The upper 6 bits must be 001000. The seventh bit must match the setting of the AD0 pin, and the eighth must be 1. The eighth bit of the address byte is the R/$\overline{W}$ bit.

2) After transmitting an acknowledge (ACK), the device will then transmit the contents of the register pointed to by the MAP. The MAP register will contain the address of the last register written to the MAP, or the default address (see section 4.1) if an I²C read is the first operation performed on the device.

3) Once the device has transmitted the contents of the register pointed to by the MAP, issue an ACK.

4) If the INCR bit is set to 1, the device will continue to transmit the contents of successive registers. Continue providing a clock and issue an ACK after each byte until all the desired registers are read, then initiate a STOP condition to the bus.

5) If the INCR bit is set to 0 and further I²C reads from other registers are desired, it is necessary to initiate a STOP condition and follow the procedure detailed from steps 1 and 2 from the I²C Write instructions followed by step 1 of the I²C Read section. If no further reads from other registers are desired, initiate a STOP condition to the bus.



Note: If operation is a write, this byte contains the Memory Address Pointer, MAP.

Figure 8. Control Port Timing, I²C Mode

4.0.3 SPI Mode

In SPI mode, data is clocked into the serial control data line, CDIN, by the serial control port clock, CCLK (see Figure 9 for the clock to data relationship). There is no AD0 pin. Pin $\overline{CS}$ is the chip select signal and is used to control SPI writes to the control port. When the device detects a high to low transition on the AD0/$\overline{CS}$ pin after power-up, SPI mode will be selected. All signals are inputs and data is clocked in on the rising edge of CCLK.

4.0.3a SPI Write

To write to the device, follow the procedure below while adhering to the control port Switching Specifications in section 7.

1) Bring $\overline{CS}$ low.

2) The address byte on the CDIN pin must then be 00100000.

3) Write to the memory address pointer, MAP. This byte points to the register to be written.

4) Write the desired data to the register pointed to by the MAP.

5) If the INCR bit (see section 4.0.1) is set to 1, repeat the previous step until all the desired registers are written, then bring $\overline{CS}$ high.

6) If the INCR bit is set to 0 and further SPI writes to other registers are desired, it is necessary to bring $\overline{CS}$ high, and follow the procedure detailed from step 1. If no further writes to other registers are desired, bring $\overline{CS}$ high.

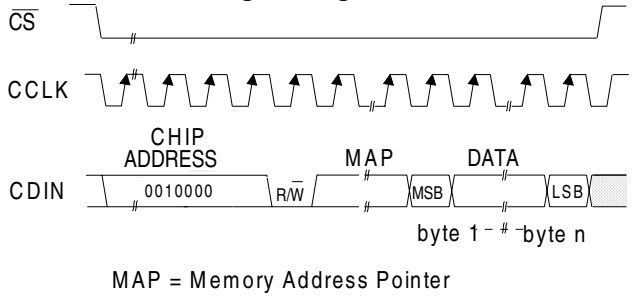


Figure 9. Control Port Timing, SPI mode

4.1 Memory Address Pointer (MAP)

7	6	5	4	3	2	1	0
INCR	Reserved	Reserved	Reserved	MAP3	MAP2	MAP1	MAP0
0	0	0	0	0	0	0	0

4.1.1 INCR (AUTO MAP INCREMENT ENABLE)

Default = '0'
0 - Disabled, the MAP will stay constant for successive writes
1 - Enabled, the MAP will auto increment after each byte is written, allowing block reads or writes of successive registers

4.1.2 MAP3-0 (MEMORY ADDRESS POINTER)

Default = '0000'

5. REGISTER QUICK REFERENCE

Addr	Function	7	6	5	4	3	2	1	0
01h	Mode Control 1	AMUTE	DIF2	DIF1	DIF0	DEM1	DEM0	FM1	FM0
		1	0	0	0	0	0	0	0
02h	Volume and MIxing Control	A = B	Soft	Zero Cross	ATAPI4	ATAPI3	ATAPI2	ATAPI1	ATAPI0
		0	1	0	0	1	0	0	1
03h	Channel A Volume Control	MUTE	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
		0	0	0	0	0	0	0	0
04h	Channel B Volume Control	MUTE	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
		0	0	0	0	0	0	0	0
05h	Mode Control 2	INVERT_A	INVERT_B	CPEN	PDN	MUTEC A = B	FREEZE	MCLKDIV2	Reserved
		0	0	0	1	0	0	0	0
06h	Mode Control 3	Reserved	Reserved	Reserved	FILT_SEL	RMP_UP	RMP_DN	Reserved	Reserved
		0	0	0	0	0	0	0	0
07h	Chip ID	PART3	PART2	PART1	PART0	REV3	REV2	REV1	REV0
		1	0	0	0	-	-	-	-

6. REGISTER DESCRIPTION

** All registers are read/write in Two-Wire mode and write only in SPI mode, unless otherwise noted**

6.1 Mode Control 1 - Address 01h

7	6	5	4	3	2	1	0
AMUTE	DIF2	DIF1	DIF0	DEM1	DEM0	FM1	FM0

6.1.1 Auto-Mute (Bit 7)

Function:

The Digital-to-Analog converter output will mute following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-static data will release the mute. Detection and muting is done independently for each channel. (However, Auto-Mute detection and muting can become dependent on either channel if the Mute A = B function is enabled.) The common mode on the output will be retained and the Mute Control pin for that channel will go active during the mute period. The muting function is effected, similar to volume control changes, by the Soft and Zero Cross bits in the Volume and Mixing Control register.

6.1.2 Digital Interface Formats (Bits 6:4)

Function:

PCM Mode - The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in Table 8 and Figures 4-6.

DIF2	DIF1	DIFO	DESCRIPTION	Format	Figure
0	0	0	Left Justified, up to 24-bit data (default)	0	4
0	0	1	I^2S, up to 24-bit data	1	5
0	1	0	Right Justified, 16-bit Data	2	6
0	1	1	Right Justified, 24-bit Data	3	6
1	0	0	Right Justified, 20-bit Data	4	6
1	0	1	Right Justified, 18-bit Data	5	6
1	1	0	Reserved		
1	1	1	Reserved		

Table 8. Digital Interface Formats - PCM Modes

DSD Mode - The relationship between the oversampling ratio of the DSD audio data and the required Master clock to DSD data rate is defined by the Digital interface Format pins. Note that the Functional Mode registers must be set to DSD Mode. See 9 for register options.

DIF2	DIF1	DIFO	DESCRIPTION
0	0	0	64x oversampled DSD data with a 4x MCLK to DSD data rate (default)
0	0	1	64x oversampled DSD data with a 6x MCLK to DSD data rate
0	1	0	64x oversampled DSD data with a 8x MCLK to DSD data rate
0	1	1	64x oversampled DSD data with a 12x MCLK to DSD data rate
1	0	0	128x oversampled DSD data with a 2x MCLK to DSD data rate
1	0	1	128x oversampled DSD data with a 3x MCLK to DSD data rate
1	1	0	128x oversampled DSD data with a 4x MCLK to DSD data rate
1	1	1	128x oversampled DSD data with a 6x MCLK to DSD data rate

Table 9. Digital Interface Formats - DSD Mode

6.1.3 De-Emphasis Control (Bits 3:2)

Function:

Implementation of the standard 15 μs/50 μs digital de-emphasis filter response, Figure 7, requires re-configuration of the digital filter to maintain the proper filter response for 32, 44.1 or 48 kHz sample rates. NOTE: De-emphasis is available only in Single-Speed Mode. See 10 below.

DEM1	DEMO	DESCRIPTION
0	0	Disabled (default)
0	1	44.1 kHz de-emphasis
1	0	48 kHz de-emphasis
1	1	32 kHz de-emphasis

Table 10. De-Emphasis Mode Selection

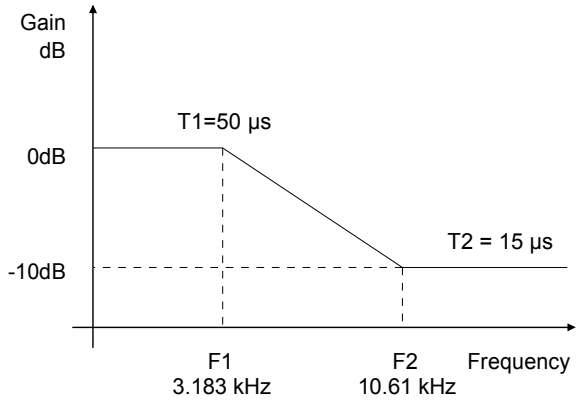


Figure 10. De-Emphasis Curve

6.1.4 Functional Mode (Bits 1:0)

Function:

Selects the required range of input sample rates or DSD Mode. See Table 11.

FM1	FM0	MODE
0	0	Single-Speed Mode: 4 to 50 kHz sample rates (default)
0	1	Double-Speed Mode: 50 to 100 kHz sample rates
1	0	Quad-Speed Mode: 100 to 200 kHz sample rates
1	1	Direct Stream Digital Mode

Table 11. Functional Mode Selection

6.2 Volume and Mixing Control (Address 02h)

7	6	5	4	3	2	1	0
A = B	Soft	Zero Cross	ATAPI4	ATAPI3	ATAPI2	ATAPI1	ATAPI0

6.2.1 Channel A Volume = Channel B Volume (Bit 7)

Function:

The AOUTA and AOUTB volume levels are independently controlled by the A and the B Channel Volume Control Bytes when this function is disabled. The volume on both AOUTA and AOUTB are determined by the A Channel Volume Control Byte and the B Channel Byte is ignored when this function is enabled.

6.2.2 Soft Ramp or Zero Cross Enable (Bits 6:5)

Function:

Soft Ramp Enable

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1dB per 8 left/right clock periods.

Zero Cross Enable

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Soft Ramp and Zero Cross Enable

Soft Ramp and Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel. See Table 12

SOFT	ZERO	Mode
0	0	Changes to affect immediately
0	1	Zero Cross enabled
1	0	Soft Ramp enabled (default)
1	1	Soft Ramp and Zero Cross enabled

Table 12. Soft Cross or Zero Cross Mode Selection

6.2.3 ATAPI Channel Mixing and Muting (Bits 4:0)

Function:

The CS4392 implements the channel mixing functions of the ATAPI CD-ROM specification. See Table 13 on page 21

ATAPI4	ATAPI3	ATAPI2	ATAPI1	ATAPI0	AOUTA	AOUTB
0	0	0	0	0	MUTE	MUTE
0	0	0	0	1	MUTE	bR
0	0	0	1	0	MUTE	bL
0	0	0	1	1	MUTE	b[(L+R)/2]
0	0	1	0	0	aR	MUTE
0	0	1	0	1	aR	bR
0	0	1	1	0	aR	bL
0	0	1	1	1	aR	b[(L+R)/2]
0	1	0	0	0	aL	MUTE
0	1	0	0	1	aL	bR
0	1	0	1	0	aL	bL
0	1	0	1	1	aL	b[(L+R)/2]
0	1	1	0	0	a[(L+R)/2]	MUTE
0	1	1	0	1	a[(L+R)/2]	bR
0	1	1	1	0	a[(L+R)/2]	bL
0	1	1	1	1	a[(L+R)/2]	b[(L+R)/2]
1	0	0	0	0	MUTE	MUTE
1	0	0	0	1	MUTE	bR
1	0	0	1	0	MUTE	bL
1	0	0	1	1	MUTE	[(bL+aR)/2]
1	0	1	0	0	aR	MUTE
1	0	1	0	1	aR	bR
1	0	1	1	0	aR	bL
1	0	1	1	1	aR	[(aL+bR)/2]
1	1	0	0	0	aL	MUTE
1	1	0	0	1	aL	bR
1	1	0	1	0	aL	bL
1	1	0	1	1	aL	[(aL+bR)/2]
1	1	1	0	0	[(aL+bR)/2]	MUTE
1	1	1	0	1	[(aL+bR)/2]	bR
1	1	1	1	0	[(bL+aR)/2]	bL
1	1	1	1	1	[(aL+bR)/2]	[(aL+bR)/2]

Table 13. ATAPI Decode

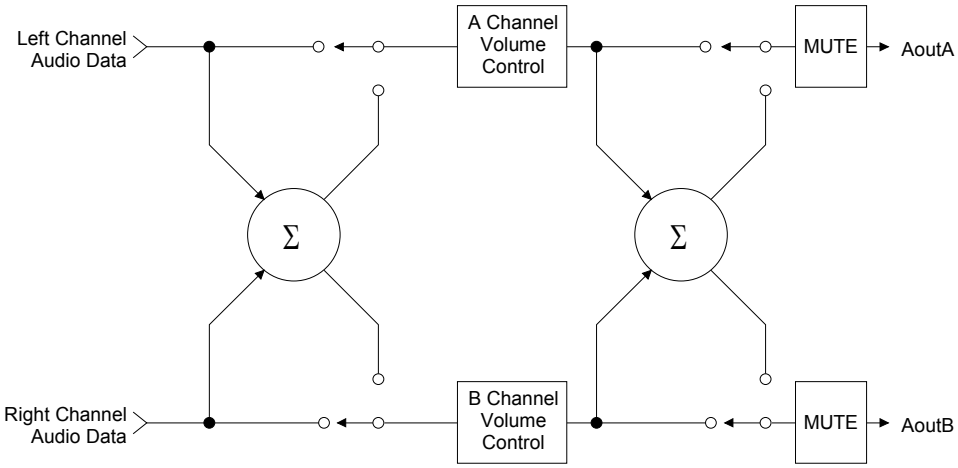


Figure 11. ATAPI Block Diagram

6.3 Channel A Volume Control - Address 03h

See 4.4 *Channel B Volume Control - Address 04h*

6.4 CHANNEL B VOLUME CONTROL - ADDRESS 04H

7	6	5	4	3	2	1	0
MUTE	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0

6.4.1 Mute (Bit 7)

Function:

The Digital-to-Analog converter output will mute when enabled. The common mode voltage on the output will be retained. The muting function is effected, similiar to attenuation changes, by the Soft and Zero Cross bits in the Volume and Mixing Control register. The MUTEC pin for that channel will go active during the mute period if the Mute function is enabled. Both the AMUTEC and BMUTEC will go active if either MUTE register is enabled and the MUTEC A = B bit (register 5) is enabled.

6.4.2 Volume Control (Bits 6:0)

Function:

The digital volume control allows the user to attenuate the signal in 1 dB increments from 0 to -127 dB. Volume settings are decoded as shown in Table 14. The volume changes are implemented as dictated by the Soft and Zero Cross bits in the Volume and Mixing Control register (see section 6.2.2).

Binary Code	Decimal Value	Volume Setting
0000000	0	0 dB
0010100	20	-20 dB
0101000	40	-40 dB
0111100	60	-60 dB
1011010	90	-90 dB

Table 14. Digital Volume Control Example Settings

6.5 Mode Control 2 - Address 05h

7	6	5	4	3	2	1	0
INVERT_A	INVERT_B	CPEN	PDN	MUTEC A = B	FREEZE	MCLKDIV2	Reserved

6.5.1 Invert Signal Polarity (Bits 7:6)

Function:

When set to 1, this bit inverts the signal polarity for the appropriate channel. This is useful if a board layout error has occurred, or an other situations where a 180 degree phase shift is desirable. Default is 0.

6.5.2 Control Port Enable (Bit 5)

Function:

This bit defaults to 0, allowing the device to power-up in Stand-Alone mode. The Control port mode can be accessed by setting this bit to 1. This will allow the operation of the device to be controlled by the registers and the pin definitions will conform to Control Port Mode. To accomplish a clean power-up, the user should write 30h to register 5 within 10 ms following the release of Reset.

6.5.3 Power Down (Bit 4)

Function:

The device will enter a low-power state whenever this function is activated (set to 1). The power-down bit defaults to 'enabled' (1) on power-up and must be disabled before normal operation will begin. The contents of the control registers are retained when the device is in power-down.

6.5.4 AMUTEC = BMUTEC (Bit 3)

Function:

When this function is enabled, the individual controls for AMUTEC and BMUTEC are internally connected through a AND gate prior to the output pins. Therefore, the external AMUTEC and BMUTEC pins will go active only when the requirements for both AMUTEC and BMUTEC are valid.

6.5.5 Freeze (Bit 2)

Function:

This function allows modifications to the control port registers without the changes taking effect until Freeze is disabled. To make multiple changes in the Control port registers take effect simultaneously, set the Freeze Bit, make all register changes, then Disable the Freeze bit.

6.5.6 Master Clock Divide (Bit 1)

Function:

This function allows the user to select an internal divide by 2 of the Master Clock. This selection is required to access the higher Master Clock rates as shown in Tables 2 through 4 on page 10.

6.6 Mode Control 3 - Address 06h

B7	B6	B5	B4	B3	B2	B1	B0
Reserved	Reserved	Reserved	FILT_SEL	RMP_UP	RMP_DN	Reserved	Reserved

6.6.1 Interpolation Filter Select (Bit 4)

Function:

This Function allows the user to select whether the Interpolation Filter has a fast (set to 0 - default) or slow (set to 1) roll off. The - 3dB corner is approximately the same for both filters, but the slope of the roll of is greater for the 'fast' roll off filter.

6.6.2 Soft Volume Ramp-up after Reset (Bit 3)

Function:

This function allows the user to control whether a soft ramp up in volume is applied when reset is released either by the reset pin or internal to the chip. The modes are as follows:

0 - An instantaneous change is made from max attenuation to the control port volume setting on release of reset (default setting).
1 - Volume is ramped up using the soft-ramp settings in Bits 6:5 of register 02h (see 6.2.2) from max attenuation to the control port volume setting on release of reset.

6.6.3 Soft Ramp-down before Reset (Bit 2)

Function:

This function allows the user to control if a soft ramp-down in volume is applied before a known reset condition. The modes are as follows:

0 - An instantaneous change is made from the control port volume setting to max attenuation when chip resets (default setting).
1 - Volume is ramped down using the soft-ramp settings in Bits 6:5 of register 02h (see 6.2.2) from the control port volume setting to max attenuation when chip resets.

6.7 Chip ID - Register 07h

B7	B6	B5	B4	B3	B2	B1	B0
PART3	PART2	PART1	PART0	REV3	REV2	REV1	REV0

Function:

This register is Read-Only. Bits 7 through 4 are the part number ID which is 1000b (8h) and the remaining Bits (3 through 0) are for the chip revision.

7. CHARACTERISTICS/SPECIFICATIONS

ANALOG CHARACTERISTICS (CS4392-KS/KZ/KZZ)

((Test conditions (unless otherwise specified): Input test signal is a 997 Hz sine wave at 0 dBFS; measurement bandwidth is 10 Hz to 20 kHz; test load R_L = 3kΩ, C_L = 10 pF. Typical performance characteristics are derived from measurements taken at T_A = 25 °C, VL = VA = 5.0V. Min/Max performance characteristics are guaranteed over the specified operating temperature and voltages.)

Parameter		Symbol	VA = 5.0V Min	Typ	Max	Unit
Dynamic Performance for All Speed Modes and DSD						
Dynamic Range (Note 1)	unweighted		105	111	-	dB
	A-Weighted		108	114	-	dB
Total Harmonic Distortion + Noise (Note 1)	0 dB	THD+N	-	-100	-94	dB
	-20 dB		-	-91	-	dB
	-60 dB		-	-51	-45	dB
Idle Channel Noise / Signal-to-Noise Ratio			-	114	-	dB
Interchannel Isolation	(1 kHz)		-	100	-	dB
DC Accuracy						
Interchannel Gain Mismatch		ICGM	-	0.1	-	dB
Gain Drift			-	100	-	ppm/°C
Analog Output Characteristics and Specifications						
Full Scale Differential Output Voltage		V_{FS}	0.95xVA	0.99xVA	1.05xVA	Vpp
Output Resistance	(Note 2)	Z_{out}	-	100	-	Ω
Minimum AC-Load Resistance		R_L	-	3	-	kΩ
Maximum Load Capacitance		C_L	-	100	-	pF

Notes: 1. One-half LSB of Triangular PDF dither is added to data.

2. V_{FS} is tested under load R_L but does not include attenuation due to Z_{OUT}