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24-Bit, Multi-Standard D/A Converter for Digital Audio

Features

- 24 Bit Conversion
- Up to 192 kHz Sample Rates
- 120 dB Dynamic Range
- -100 dB THD+N
- Supports PCM, DSD and External Interpolation filters
- Advanced Dynamic-Element Matching
- Low Clock Jitter Sensitivity
- Digital De-emphasis for 32 kHz, 44.1 kHz and 48 kHz
- External Reference Input

Description

The CS4397 is a complete high performance 24-bit 48/96/192 kHz stereo digital-to-analog conversion system. The device includes a digital interpolation filter followed by an oversampled multi-bit delta-sigma modulator which drives dynamic-element-matching (DEM) selection logic. The output from the DEM block controls the input to a multi-element switched capacitor DAC/low-pass filter, with fully-differential outputs. This multi-bit architecture features significantly lower out-of-band noise and jitter sensitivity than traditional 1-bit designs, and the advanced DEM guarantees low noise and distortion at all signal levels.

ORDERING INFORMATION

CS4397-KS -10° to 70° C 28-pin Plastic SOIC
 CS4397-KSZ -10° to 70° C 28-pin Plastic SOIC Lead free
 CDB4397 Evaluation Board

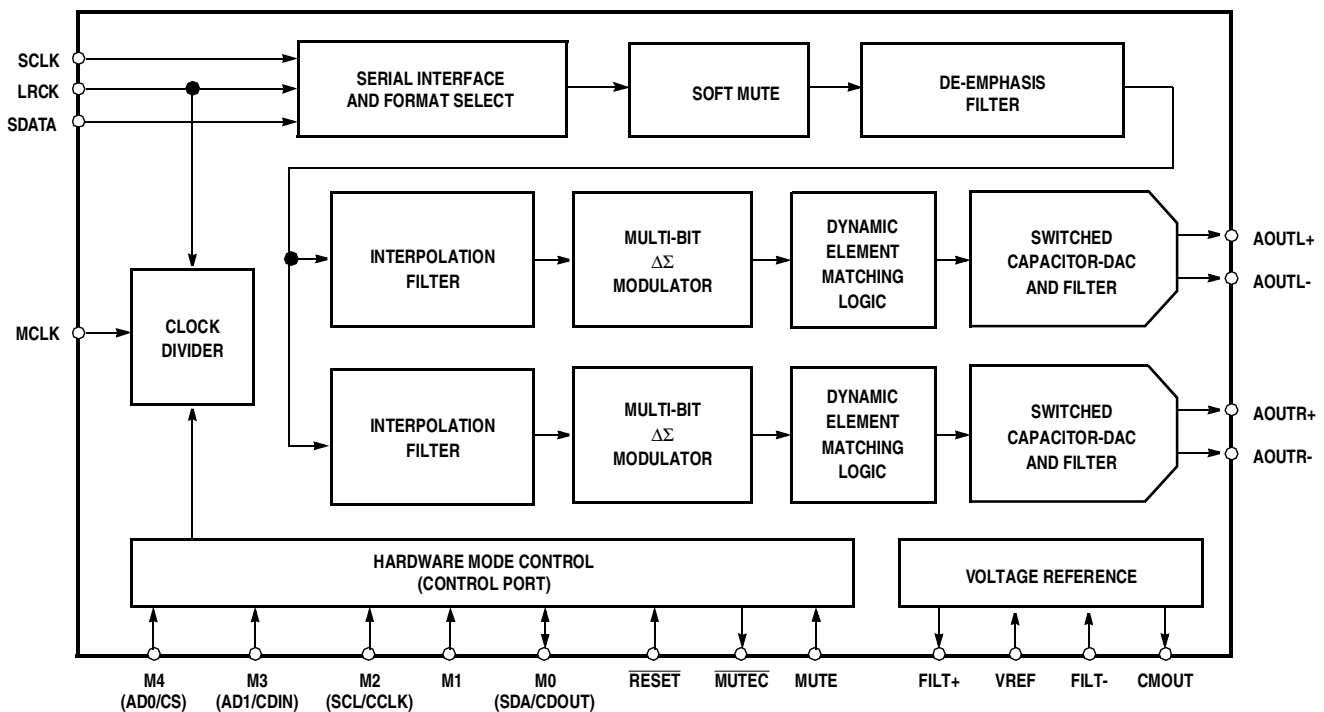


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"The I²C-Bus Specification: Version 2.0" Philips Semiconductors, December 1998.
<http://www.semiconductors.philips.com>

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1.0 CHARACTERISTICS/SPECIFICATIONS

ANALOG CHARACTERISTICS

($T_A = 25\text{ }^\circ\text{C}$; Logic "1" = $V_D = 5\text{ V}$; $V_A = 5\text{ V}$; Logic "0" = DGND; Full-Scale Output Sine Wave, 997 Hz; MCLK = 12.288 MHz; SCLK = 3.072 MHz, Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified. Test load $R_L = 1\text{ k}\Omega$, $C_L = 10\text{ pF}$)

Parameter	Symbol	Min	Typ	Max	Unit	
Dynamic Performance - Single Speed Mode - F_s equal to 48 kHz						
Dynamic Range 24-Bit 16-Bit (Note 2)	(Note 1) unweighted	TBD	117	-	dB	
	A-Weighted	TBD	120	-	dB	
	unweighted	-	95	-	dB	
	A-Weighted	-	98	-	dB	
Total Harmonic Distortion + Noise 24-Bit 16-Bit (Note 2)	(Note 1) 0 dB	THD+N	-	-100	TBD	dB
	-20 dB		-	-97	TBD	dB
	-60 dB		-	-57	TBD	dB
	0 dB		-	-95	-	dB
	-20 dB		-	-75	-	dB
	-60 dB		-	-35	-	dB
Dynamic Performance - Double Speed Mode - F_s equal to 96 kHz						
Dynamic Range 24-Bit 40 kHz bandwidth 16-Bit (Note 2)	(Note 1) unweighted	TBD	117	-	dB	
	A-Weighted	TBD	120	-	dB	
	unweighted	TBD	114	-	dB	
	unweighted	-	92	-	dB	
	A-Weighted	-	98	-	dB	
Total Harmonic Distortion + Noise 24-Bit 16-Bit (Note 2)	(Note 1) 0 dB	THD+N	-	-100	TBD	dB
	-20 dB		-	-97	TBD	dB
	-60 dB		-	-57	TBD	dB
	0 dB		-	-95	-	dB
	-20 dB		-	-75	-	dB
	-60 dB		-	-35	-	dB
Dynamic Performance - Quad-Speed Mode - F_s equal to 192 kHz						
Dynamic Range 24-Bit 40 kHz bandwidth 16-Bit (Note 2)	(Note 1) unweighted	TBD	117	-	dB	
	A-Weighted	TBD	120	-	dB	
	unweighted	TBD	114	-	dB	
	unweighted	-	92	-	dB	
	A-Weighted	-	98	-	dB	
Total Harmonic Distortion + Noise 24-Bit 16-Bit (Note 2)	(Note 1) 0 dB	THD+N	-	-100	TBD	dB
	-20 dB		-	-97	TBD	dB
	-60 dB		-	-57	TBD	dB
	0 dB		-	-95	-	dB
	-20 dB		-	-75	-	dB
	-60 dB		-	-35	-	dB

- Notes: 1. Triangular PDF dithered data.
2. Performance limited by 16-bit quantization noise.

ANALOG CHARACTERISTICS (Continued)

Parameter		Symbol	VD = 3 V			VD = 5 V			Unit
			Min	Typ	Max	Min	Typ	Max	
Power Supplies									
Supply Current VA = 5 V	normal operation	I_A	-	20	TBD	-	20	TBD	mA
	normal operation	I_D	-	TBD	TBD	-	TBD	TBD	mA
	power-down state	$I_D + I_A$	-	60	-	-	30	-	μ A
Power Dissipation VA = 5 V	normal operation		-	TBD	TBD	-	TBD	TBD	mW
	power-down		-	0.3	-	-	0.3	-	mW
Power Supply Rejection Ratio (1 kHz)	(Note 3) (120 Hz)	PSRR	-	60	-	-	60	-	dB
			-	40	-	-	40	-	dB

Parameter	Symbol	Min	Typ	Max	Unit
Analog Output					
Full Scale Differential Output Voltage		TBD	1.4VREF	TBD	Vpp
Common Mode Voltage		-	0.5VREF	-	VDC
Interchannel Gain Mismatch		-	0.1	-	dB
Gain Drift		-	100	-	ppm/°C
Differential DC Offset		-	2.0	TBD	mV
AC-Load Resistance	R_L	1	-	-	k Ω
Load Capacitance	C_L	-	-	100	pF
Interchannel Isolation	(1 kHz)	-	90	-	dB

Notes: 3. Valid with the recommended capacitor values on FILT+ and CMOUT as shown in Figure 1. Increasing the capacitance will also increase the PSRR.

ANALOG CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
Combined Digital and On-chip Analog Filter Response - Single Speed Mode					
Passband (Note 4) to -0.1 dB corner to -3 dB corner		-	-	0.470	Fs
		-	-	0.492	Fs
Frequency Response 10 Hz to 20 kHz		-0.020	-	+0.015	dB
Passband Ripple		-	-	±0.0001	dB
StopBand		.5465	-	-	Fs
StopBand Attenuation (Note 5)		102	-	-	dB
Group Delay (Note 6)	tgd	-	37/Fs	-	s
De-emphasis Error (Note 7) (Relative to 1 kHz)		-	-	±0.10	dB
	Fs = 32 kHz	-	-	±0.10	dB
	Fs = 48 kHz	-	-	±0.13	dB
Combined Digital and On-chip Analog Filter Response - Double Speed Mode					
Passband (Note 4) to -0.1 dB corner to -3 dB corner		0	-	0.448	Fs
		0	-	0.486	Fs
Frequency Response 10 Hz to 20 kHz		-0.017	-	0.035	dB
Passband Ripple		-	-	±0.0008	dB
StopBand		.570	-	-	Fs
StopBand Attenuation (Note 5)		82	-	-	dB
Group Delay	tgd	-	20/Fs	-	s
Combined Digital and On-chip Analog Filter Response - Quad-Speed Mode					
Passband (Note 4) to -0.1 dB corner to -3 dB corner		-	-	0.385	Fs
		-	-	0.472	Fs
Frequency Response 10 Hz to 20 kHz		0	-	+0.015	dB
Passband Ripple		-	-	±0.00065	dB
StopBand		0.635	-	-	Fs
StopBand Attenuation (Note 5)		83	-	-	dB
Group Delay	tgd	-	11/Fs	-	s

- Notes:
- Response is clock dependent and will scale with Fs. Note that the response plots (**Figures 9-28**) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
 - For Single-Speed Mode, the Measurement Bandwidth is 0.5465 Fs to 1.4 Fs.
For Double-Speed Mode, the Measurement Bandwidth is 0.570 Fs to 1.4 Fs.
For Quad-Speed Mode, the Measurement Bandwidth is 0.635 Fs to 1.3 Fs.
 - Group Delay for Fs=48 kHz 37/48 kHz=770 μs
 - De-emphasis is available only in Single Speed Mode.

ANALOG CHARACTERISTICS - DSD MODE ($T_A = 25\text{ }^\circ\text{C}$; Logic "1" = $V_D = 5\text{ V}$; $V_A = 5\text{ V}$; Logic "0" = AGND; Full-Scale Output Sine Wave, 997 Hz; Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified. Test load $R_L = 1\text{ k}\Omega$, $C_L = 10\text{ pF}$)

Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Performance - DSD Mode					
Dynamic Range (Note 1)	unweighted	TBD	117	-	dB
	A-Weighted	TBD	120	-	dB
Total Harmonic Distortion + Noise (Note 1)	0 dB	-	-100	TBD	dB
	-20 dB	-	-94	TBD	dB
	-60 dB	-	-54	TBD	dB
Analog Output - DSD Mode					
Full Scale Differential Output Voltage (Note 8)		TBD	1.2VREF	TBD	Vpp
Common Mode Voltage		-	0.5VREF	-	VDC
Interchannel Gain Mismatch		-	0.1	-	dB
Gain Drift		-	100	-	ppm/ $^\circ\text{C}$
Differential DC Offset		-	2.0	TBD	mV
Combined Digital and On-chip Analog Filter Response - DSD Mode					
Passband (Note 4)	to -0.1 dB corner	-	-	0.95	Fs
	to -3 dB corner	-	-	2.70	Fs
Frequency Response 10 Hz to 20 kHz		-0.013	-	0	dB
Group Delay	tgd	-	0.2/Fs	-	s

Notes: 8. Assumes a DSD modulation index of 0.7.

ANALOG CHARACTERISTICS - 8X INTERPOLATOR MODE ($T_A = 25\text{ }^\circ\text{C}$; Logic "1" = $V_D = 5\text{ V}$; $V_A = 5\text{ V}$; Logic "0" = AGND; Full-Scale Output Sine Wave, 997 Hz; Base Band $F_s = 48\text{ kHz}$, SCLK = 6.144 MHz, Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified. Test load $R_L = 1\text{ k}\Omega$, $C_L = 10\text{ pF}$)

Parameter	Symbol	Min	Typ	Max	Unit	
Dynamic Performance Mode						
Dynamic Range	(Note 1) unweighted A-Weighted	TBD	117	-	dB	
		TBD	120	-	dB	
Total Harmonic Distortion + Noise	(Note 1) 0 dB -20 dB -60 dB	THD+N	-	-100	TBD	dB
			-	-97	TBD	dB
			-	-57	TBD	dB
Analog Output						
Full Scale Differential Output Voltage		TBD	0.7VREF	TBD	Vpp	
Common Mode Voltage		-	0.5VREF	-	VDC	
Interchannel Gain Mismatch		-	0.1	-	dB	
Gain Drift		-	100	-	ppm/°C	
Differential DC Offset		-	2.0	TBD	mV	
Combined Digital and On-chip Analog Filter Response - 8x Interpolator Mode						
Passband	(Note 4) to -0.1 dB corner to -3 dB corner	-	-	2.10	Fs	
		-	-	3.52	Fs	
Frequency Response 10 Hz to 20 kHz		-0.0008	-	0	dB	
Passband Ripple		-	-	0	dB	
StopBand		6.08	-	-	Fs	
StopBand Attenuation	(Note 9)	56	-	-	dB	
Group Delay	tgd	-	0.9/Fs	-	s	

Notes: 9. Measurement Bandwidth is 6.08 to 9.6 Fs

DIGITAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$; $V_D = 3.0\text{V} - 5.25\text{V}$)

Parameters	Symbol	Min	Typ	Max	Units	
High-Level Input Voltage	$V_D = 5\text{ V}$	V_{IH}	2.0	-	-	V
	$V_D = 3\text{ V}$		2.0	-	-	V
Low-Level Input Voltage	$V_D = 5\text{ V}$	V_{IL}	-	-	0.8	V
	$V_D = 3\text{ V}$		-	-	0.8	V
Input Leakage Current	I_{in}	-	-	± 10	μA	
Input Capacitance		-	8	-	pF	
Maximum MUTE C Drive Current		-	3	-	mA	

ABSOLUTE MAXIMUM RATINGS ($AGND = 0\text{ V}$, all voltages with respect to ground.)

Parameter	Symbol	Min	Max	Unit
DC Power Supply: Positive Analog	VA	-0.3	6.0	V
	VD	-0.3	6.0	V
	VREF	-0.3	VA	V
Reference Voltage				
Input Current, Any Pin Except Supplies	I_{in}	-	± 10	mA
Digital Input Voltage	V_{IND}	-0.3	$(V_D)+0.4$	V
Ambient Operating Temperature (power applied)	T_A	-55	125	$^\circ\text{C}$
Storage Temperature	T_{stg}	-65	150	$^\circ\text{C}$

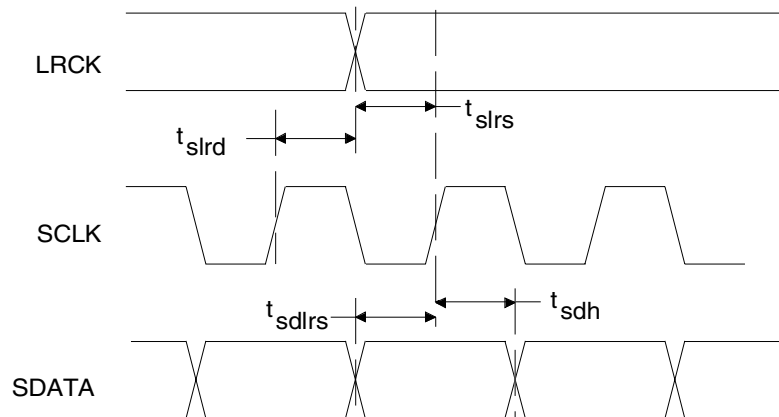
WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS ($DGND = 0\text{V}$; all voltages with respect to ground)

Parameter	Symbol	Min	Typ	Max	Unit
DC Power Supply: Positive Digital	VD	3.0	3.3	5.25	V
	VA	4.75	5.0	5.25	V
	VREF	TBD	5.0	VA	V
Positive Analog Reference Voltage					
Specified Temperature Range	T_A	-10	-	70	$^\circ\text{C}$

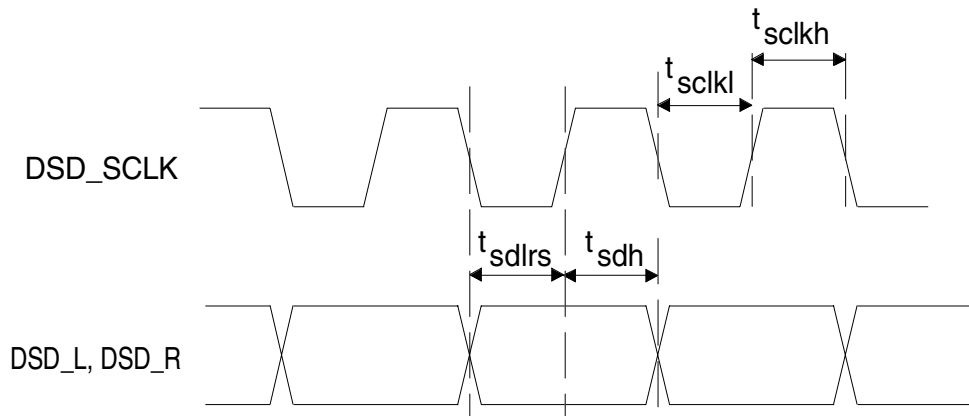
SWITCHING CHARACTERISTICS ($T_A = -10$ to 70°C ; Logic 0 = AGND = DGND; Logic 1 = VD = 5.25 to 3.0 Volts; $C_L = 20$ pF)

Parameter	Symbol	Min	Typ	Max	Unit
Input Sample Rate (Single-speed mode)	F_s	16	-	50	kHz
(Double-speed mode)	F_s	50	-	100	kHz
(Quad-speed mode)	F_s	100	-	200	kHz
LRCK Duty Cycle		45	50	55	%
MCLK Frequency (Single-speed 256 F_s , Double speed 128 F_s or Quad-speed 64 F_s)		4.096	-	12.8	MHz
MCLK Frequency (Single-speed 384 F_s , Double speed 192 F_s or Quad-speed, 96 F_s)		6.144	-	19.2	MHz
MCLK Frequency (Single-speed 512 F_s , Double speed 256 F_s or Quad-speed, 128 F_s)		8.192	-	25.6	MHz
MCLK Frequency (Single-speed 768 F_s , Double speed 384 F_s or Quad-speed, 192 F_s)		12.288	-	38.4	MHz
MCLK Duty Cycle		40	50	60	%
SCLK Frequency (Single-speed mode)		-	-	$256 \times F_s$	Hz
(Double-speed mode)		-	-	$128 \times F_s$	Hz
(Quad-speed mode)		-	-	$64 \times F_s$	Hz
SCLK rising to LRCK edge delay	t_{slrd}	20	-	-	ns
SCLK rising to LRCK edge setup time	t_{slrs}	20	-	-	ns
SDATA valid to SCLK rising setup time	t_{sdls}	20	-	-	ns
SCLK rising to SDATA hold time	t_{sdh}	20	-	-	ns


Figure 1. Serial Audio Input Timing

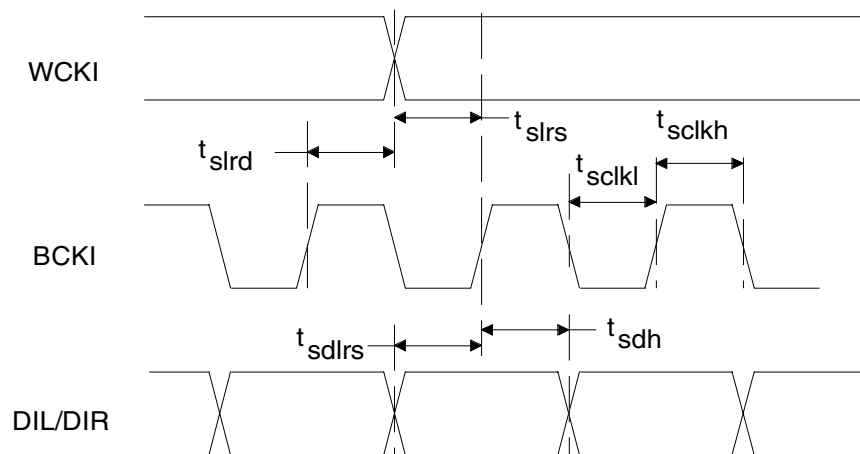
DSD - SWITCHING CHARACTERISTICS ($T_A = -10$ to 70°C ; Logic 0 = AGND = DGND; Logic 1 = VD = 5.25 to 3.0 Volts; $C_L = 20$ pF)

Parameter	Symbol	Min	Typ	Max	Unit
Input Bit Rate per Channel (64x Oversampled)		1.024	-	3.2	Mb/s
(128x Oversampled)		2.048	-	6.4	Mb/s
Master Clock Frequency (CLKMODE = 0)		4.096	-	12.8	MHz
(CLKMODE = 1)		6.144	-	19.2	MHz
MCLK Duty Cycle (All DSD modes)		40	-	60	%
DSD_SCLK Pulse Width Low	t_{sckl}	20	-	-	ns
DSD_SCLK Pulse Width High	t_{sckh}	20	-	-	ns
DSD_SCLK Frequency (64x Oversampled)		1.024	-	3.2	MHz
(128x Oversampled)		2.048	-	6.4	MHz
DSD_LI_R valid to DSD_SCLK rising setup time	t_{sdllrs}	20	-	-	ns
DSD_SCLK rising to DSD_L or DSD_R hold time	t_{sdh}	20	-	-	ns


Figure 2. Direct Stream Digital - Serial Audio Input Timing

8X INTERPOLATOR - SWITCHING CHARACTERISTICS ($T_A = -10$ to 70°C ;
 Logic 0 = AGND = DGND; Logic 1 = VD = 5.25 to 3.0 Volts; $C_L = 20$ pF)

Parameter	Symbol	Min	Typ	Max	Unit
Input Sample Rate (Note 10)	F_s	128	-	400	kHz
MCLK Frequency (MCLK = $32 \times F_s$)		4.096	-	12.8	MHz
(MCLK = $48 \times F_s$)		6.144	-	19.2	MHz
(MCLK = $64 \times F_s$)		8.192	-	25.6	MHz
(MCLK = $96 \times F_s$)		12.288	-	28.4	MHz
MCLK Duty Cycle		40	-	50	%
WCKI Duty Cycle		25	-	75	%
BCKI Frequency				$32 \times F_s$	MHz
BCKI rising to WCKI edge delay	t_{slrd}	20	-	-	ns
BCKI rising to WCKI edge setup time	t_{slrs}	20	-	-	ns
SDATA valid to BCKI rising setup time	t_{sdls}	20	-	-	ns
BCKI rising to DIL/DIR hold time	t_{sdh}	20	-	-	ns

 Notes: 10. F_s refers to the input sample rate to the Digital-to-Analog converter, i.e. $F_s = 44.1 \text{ kHz} \times 8 = 352.8 \text{ kHz}$.

Figure 3. Serial Audio Input Timing

SWITCHING CHARACTERISTICS - CONTROL PORT

($T_A = 25\text{ }^\circ\text{C}$; $V_D = 5.25\text{ V}$ to 3.0 Volts ; Inputs: logic 0 = AGND, logic 1 = V_D , $C_L = 30\text{ pF}$)

Parameter	Symbol	Min	Max	Unit
<i>I²C</i> Mode				
SCL Clock Frequency	f_{scl}	-	100	KHz
$\overline{\text{RST}}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	μs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	μs
Clock Low time	t_{low}	4.7	-	μs
Clock High Time	t_{high}	4.0	-	μs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	μs
SDA Hold Time from SCL Falling (Note 11)	t_{hdd}	0	-	μs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of Both SDA and SCL Lines	t_r	-	1	μs
Fall Time of Both SDA and SCL Lines	t_f	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	μs

Notes: 11. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

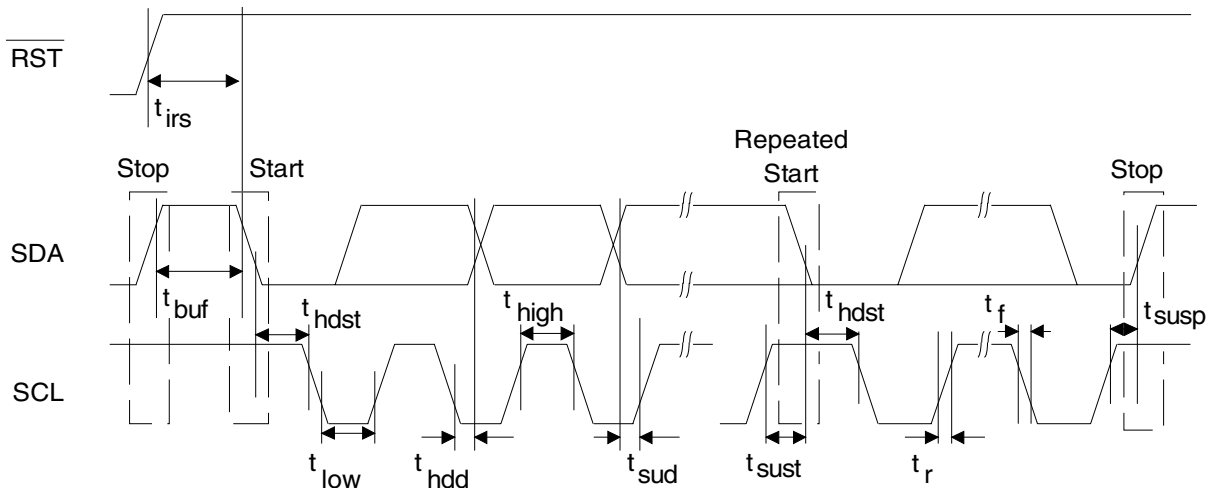


Figure 4. I²C Control Port Timing

SWITCHING CHARACTERISTICS - CONTROL PORT

($T_A = 25\text{ }^\circ\text{C}$; $V_D = 5.25\text{ V}$ to 3.0 Volts ; Inputs: logic 0 = AGND, logic 1 = V_D , $C_L = 30\text{ pF}$)

Parameter	Symbol	Min	Max	Unit
SPI Mode				
CCLK Clock Frequency	f_{sclk}	-	6	MHz
RST Rising Edge to CS Falling	t_{srs}	500	-	ns
CCLK Edge to $\overline{\text{CS}}$ Falling (Note 12)	t_{spl}	500	-	ns
$\overline{\text{CS}}$ High Time Between Transmissions	t_{csh}	1.0	-	μs
$\overline{\text{CS}}$ Falling to CCLK Edge	t_{css}	20	-	ns
CCLK Low Time	t_{scl}	66	-	ns
CCLK High Time	t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time	t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time (Note 13)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN (Note 14)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN (Note 14)	t_{f2}	-	100	ns
CCLK Falling to CDOUT valid	t_{ov}	45	-	ns

Notes: 12. t_{spl} only needed before first falling edge of $\overline{\text{CS}}$ after $\overline{\text{RST}}$ rising edge. $t_{\text{spl}} = 0$ at all other times.

13. Data must be held for sufficient time to bridge the transition time of CCLK.

14. For $F_{\text{SCK}} < 1\text{ MHz}$

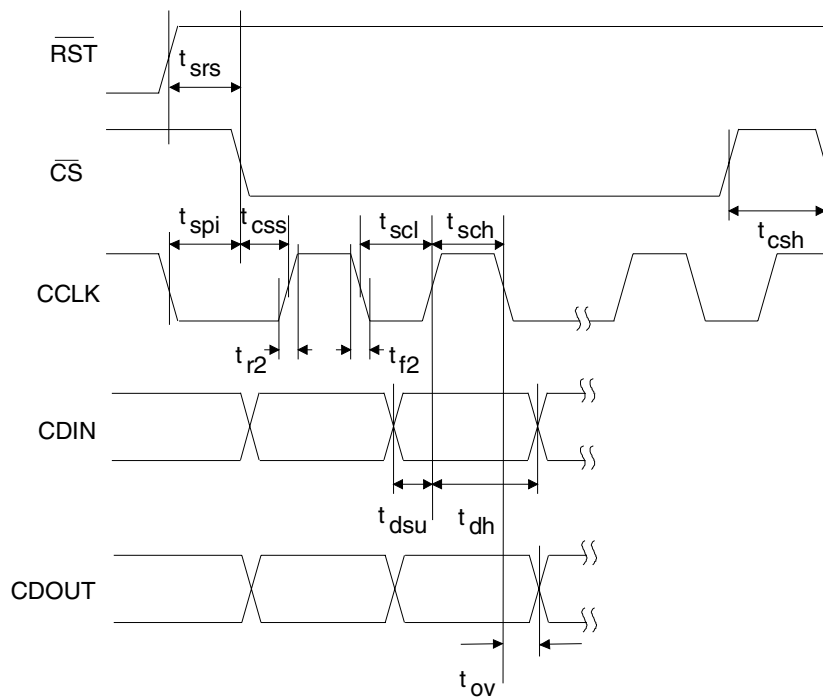


Figure 5. SPI Control Port Timing

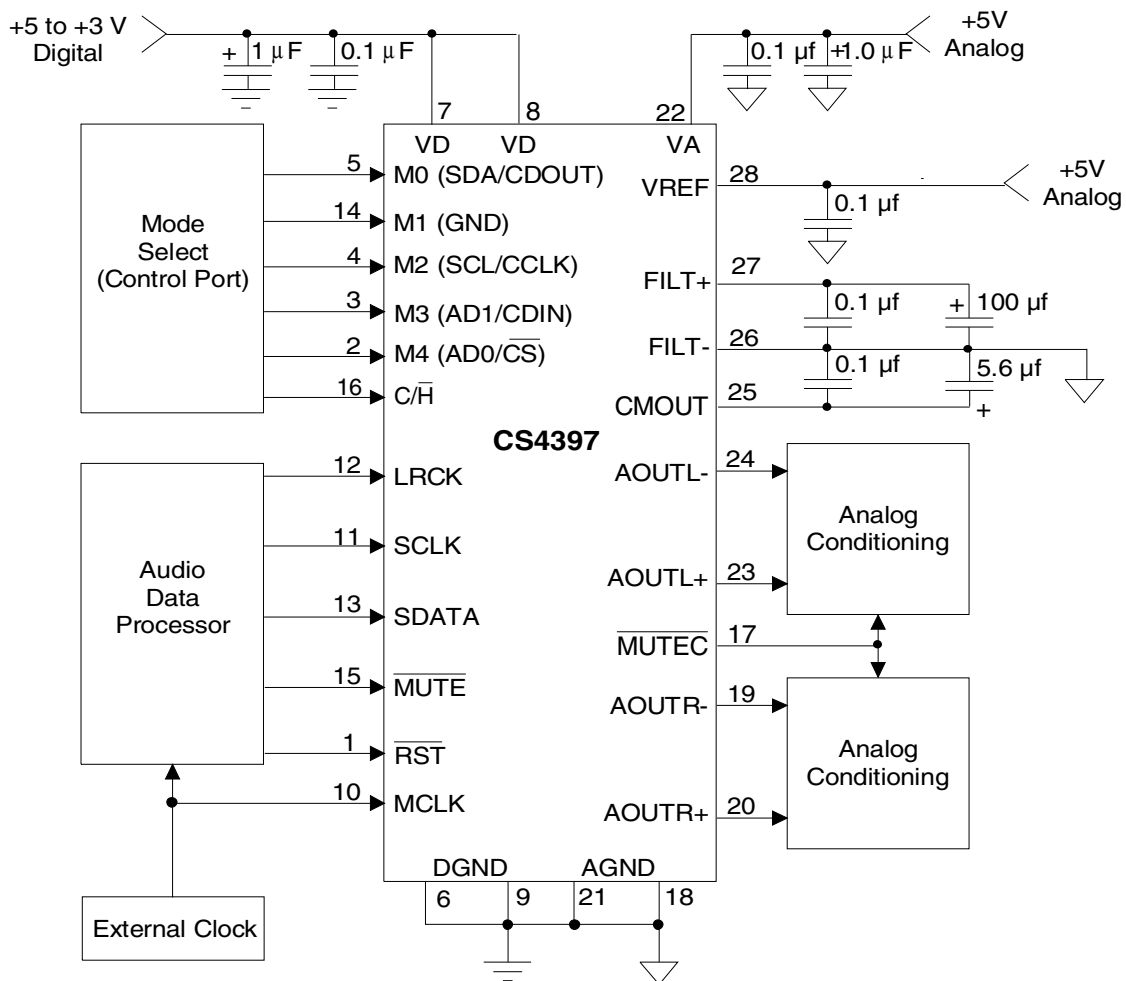
2.0 TYPICAL CONNECTION DIAGRAM


Figure 6. Typical Connection Diagram - Hardware Mode (Control Port Mode)

3.0 REGISTER DESCRIPTION

3.1 DIFFERENTIAL DC OFFSET CALIBRATION

Mode Control Register (address 01h)

7	6	5	4	3	2	1	0
CAL	$\overline{\text{MUTE}}$	M4	M3	M2	M1	M0	PDN

Access:

R/W in I²C and SPI.

Default:

0 - Disabled

Function:

Enabling this function will initiate a calibration to minimize the differential DC offset. This function will be automatically reset following completion of the calibration sequence.

CAL	MODE
0	Disabled : CAL complete
1	Enabled : CAL initiated

Table 1.

3.2 SOFT MUTE

Mode Control Register (address 01h)

7	6	5	4	3	2	1	0
CAL	$\overline{\text{MUTE}}$	M4	M3	M2	M1	M0	PDN

Access:

R/W in I²C and SPI.

Default:

0 - Enabled

Function:

The analog outputs will ramp to a muted state when enabled. The ramp requires 1152 left/right clock cycles in Single Speed, 2304 cycles in Double Speed and 4608 cycles in Quad Speed mode. The bias voltage on the outputs will be retained and MUTEC will go low at the completion of the ramp period.

The analog outputs will ramp to a normal state when this function transitions from the enabled to disabled state. The ramp requires 1152 left/right clock cycles in Single Speed, 2304 cycles in Double Speed and 4608 cycles in Quad Speed mode. The MUTEC will go high immediately on disabling of MUTE.

$\overline{\text{MUTE}}$	MODE
0	Enabled
1	Disabled

Table 2.

3.3 MODE SELECT

Mode Control Register (address 01h)

7	6	5	4	3	2	1	0
CAL	MUTE	M4	M3	M2	M1	M0	PDN

Access:

R/W in I²C and SPI.

Default:

00000

Function:

The Mode Select pins determine the operational mode of the device as detailed in Tables 9-14. The options include:

Selection of the Digital Interface Format which determines the required relationship between the Left/Right clock, serial clock and serial data as detailed in Figures 29-33

Selection of the standard 15 μ s/50 μ s digital de-emphasis filter response, Figure 28, which requires re-configuration of the digital filter to maintain the proper filter response for 32, 44.1 or 48 kHz sample rates.

Selection of the appropriate clocking mode to match the input sample rates.

Access to the Direct Stream Digital Mode

Access to the 8x Interpolation Input Mode

3.4 POWER DOWN

Mode Control Register (address 01h)

7	6	5	4	3	2	1	0
CAL	MUTE	M4	M3	M2	M1	M0	PDN

Access:

R/W in I²C and SPI.

Default:

1 - Powered Down

Function:

The analog and digital sections will be placed into a power-down mode when this function is enabled. This bit must be cleared to resume normal operation.

PDN	MODE
0	Disabled
1	Enabled

Table 3.

4.0 PIN DESCRIPTION - PCM MODE

Reset	RST	□ 1	28 □	VREF	Voltage Reference
See Description	M4(AD0/CS)	□ 2	27 □	FILT+	Reference Filter
See Description	M3(AD1/CDIN)	□ 3	26 □	FILT-	Reference Ground
See Description	M2(SCL/CCLK)	□ 4	25 □	CMOUT	Common ModeS Voltage
See Description	M0(SDA/CDOUT)	□ 5	24 □	AOUTL-	Differential Output
Digital Ground	DGND	□ 6	23 □	AOUTL+	Differential Output
Digital Power	VD	□ 7	22 □	VA	Analog Power
Digital Power	VD	□ 8	21 □	AGND	Analog Ground
Digital Ground	DGND	□ 9	20 □	AOUTR+	Differential Output
Master Clock	MCLK	□ 10	19 □	AOUTR-	Differential Output
Serial Clock	SCLK	□ 11	18 □	AGND	Analog Ground
Left/Right Clock	LRCK	□ 12	17 □	MUTE\overline{C}	Mute Control
Serial Data	SDATA	□ 13	16 □	C/H	Control port/Hardware select
See Description	M1	□ 14	15 □	MUTE	Soft Mute

Reset - \overline{RST}

Pin 1, Input

Function:

The device enters a low power mode and all internal state machines registers are reset when low. When high, the device will be in a normal operation mode .

\overline{RST}	DESCRIPTION
0	Enabled
1	Normal operation mode

Digital Ground - DGND

Pins 6 and 9, Inputs

Function:

Digital ground reference.

Digital Power - VD

Pins 7 and 8, Input

Function:

Digital power supply. Typically 5.0 to 3.0 VDC.

Master Clock - MCLK

Pin 10, Input

Function:

The master clock frequency must be either 256x, 384x, 512x or 768x the input sample rate in Single Speed Mode; either 128x, 192x 256x or 384x the input sample rate in Double Speed Mode; or 64x, 96x 128x or 192x the input sample rate in Quad Speed Mode. Tables 4-6 illustrate the standard audio sample rates and the required master clock frequencies.

Sample Rate (kHz)	MCLK (MHz)			
	256x	384x	512x	768x
32	8.1920	12.2880	16.3840	24.5760
44.1	11.2896	16.9344	22.5792	33.8688
48	12.2880	18.4320	24.5760	36.8640

Table 4. Single Speed (16 to 50 kHz sample rates) Common Clock Frequencies

Sample Rate (kHz)	MCLK (MHz)			
	128x	192x	256x	384x
64	8.1920	12.2880	16.3840	24.5760
88.2	11.2896	16.9344	22.5792	33.8688
96	12.2880	18.4320	24.5760	36.8640

Table 5. Double Speed (50 to 100 kHz sample rates) Common Clock Frequencies

Sample Rate (kHz)	MCLK (MHz)			
	64x	96x	128x	192x
176.4	11.2896	16.9344	22.5792	33.8688
192	12.2880	18.4320	24.5760	36.8640

Table 6. Quad Speed (100 to 200 kHz sample rates) Common Clock Frequencies
Serial Clock - SCLK
Pin 11, Input
Function:

Clocks individual bits of serial data into the SDATA pin. The required relationship between the Left/Right clock, serial clock and serial data is defined by either the Mode Control Byte in Control Port Mode or the M0 - M4 pins in Hardware Mode. The options are detailed in Figures 29-33

Left/Right Clock - LRCK
Pin 12, Input
Function:

The Left/Right clock determines which channel is currently being input on the serial audio data input, SDATA. The frequency of the Left/Right clock must be at the input sample rate. Audio samples in Left/Right sample pairs will be simultaneously output from the digital-to-analog converter whereas Right/Left pairs will exhibit a one sample period difference. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Mode Control Byte and the options are detailed in Figures 29-33

Serial Audio Data - SDATA
Pin 13, Input
Function:

Two's complement MSB-first serial data is input on this pin. The data is clocked into SDATA via the serial clock and the channel is determined by the Left/Right clock. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Mode Control Byte and the options are detailed in Figures 29-33

Soft Mute - $\overline{\text{MUTE}}$
Pin 15, Input
Function:

The analog outputs will ramp to a muted state when enabled. The ramp requires 1152 left/right clock cy-

cles in Single Speed, 2304 cycles in Double Speed and 4608 cycles in Quad Speed mode. The bias voltage on the outputs will be retained and MUTE \overline{C} will go active at the completion of the ramp period.

The analog outputs will ramp to a normal state when this function transitions from the enabled to disabled state. The ramp requires 1152 left/right clock cycles in Single Speed, 2304 cycles in Double Speed and 4608 cycles in Quad Speed mode. The MUTE \overline{C} will release immediately on setting MUTE = 1.

The converter analog outputs will mute when enabled. The bias voltage on the outputs will be retained and MUTE \overline{C} will go active during the mute period.

Mute	DESCRIPTION
0	Enabled
1	Normal operation mode

Control Port / Hardware Mode Select - C/H \overline{C}

Pin 16, Input

Function:

Determines if the device will operate in either the Hardware Mode or Control Port Mode.

C/H \overline{C}	DESCRIPTION
0	Hardware Mode Enabled
1	Control Port Mode Enabled

Mute Control - MUTE \overline{C}

Pin 17, Output

Function:

The Mute Control pin goes low during power-up initialization, reset, muting, master clock to left/right clock frequency ratio is incorrect or power-down. This pin is intended to be used as a control for an external mute circuit to prevent the clicks and pops that can occur in any single supply system. Use of Mute Control is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops.

Analog Ground - AGND

Pins 18 and 21, Inputs

Function:

Analog ground reference.

Differential Analog Output - AOUTR \overline{C} , AOUTR+ and AOUTL \overline{C} , AOUTL+

Pins 19, 20, 23 and 24, Outputs

Function:

The full scale differential analog output level is specified in the Analog Characteristics specifications table.

Analog Power - VA

Pin 22, Input

Function:

Power for the analog and reference circuits. Typically 5VDC.

Common Mode Voltage - CMOUT

Pin 25, Output

Function:

Filter connection for internal bias voltage, typically 50% of VREF. Capacitors must be connected from CMOUT to analog ground, as shown in Figure 6. CMOUT has a typical source impedance of 25 k Ω and any current drawn from this pin will alter device performance

Reference Ground - FILT-

Pin 26, Input

Function:

Ground reference for the internal sampling circuits. Must be connected to analog ground.

Reference Filter - FILT+

Pin 27, Output

Function:

Positive reference for internal sampling circuits. External capacitors are required from FILT+ to analog ground, as shown in Figure 6. The recommended values will typically provide 60 dB of PSRR at 1 kHz and 40 dB of PSRR at 120 Hz. FILT+ is not intended to supply external current.

Voltage Reference Input- VREF

Pin 28, Input

Function:

Analog voltage reference. Typically 5VDC.

HARDWARE MODE

Mode Select - M0, M1, M2, M3, M4

Pins 2, 3, 4, 5 and 14, Inputs

Function:

The Mode Select pins determine the operational mode of the device as detailed in Tables 9-14. The options include;

Selection of the Digital Interface Format which determines the required relationship between the Left/Right clock, serial clock and serial data as detailed in Figures 29-33

Selection of the standard 15 μ s/50 μ s digital de-emphasis filter response, Figure 28, which requires re-configuration of the digital filter to maintain the proper filter response for 32, 44.1 or 48 kHz sample rates.

Selection of the appropriate clocking mode to match the input sample rates.

Access to the Direct Stream Digital Mode

Access to the 8x Interpolation Input Mode

CONTROL PORT MODE

Address Bit 0 / Chip Select - AD0 / $\overline{\text{CS}}$

Pin 2, Input

Function:

In I²C mode, AD0 is a chip address bit. $\overline{\text{CS}}$ is used to enable the control port interface in SPI mode. The device will enter the SPI mode at anytime a high to low transition is detected on this pin. Once the device has entered the SPI mode, it will remain until either the part is reset or undergoes a power-down cycle.

Address Bit 1 / Control Data Input - AD1/CDIN

Pin 3, Input

Function:

In I²C mode, AD1 is a chip address bit. CDIN is the control data input line for the control port interface in SPI mode.

Serial Control Interface Clock - SCL/CCLK

Pin 4, Input

Function:

In I²C mode, SCL clocks the serial control data into or from SDA/CDOOUT.

In SPI mode, CCLK clocks the serial data into AD1/CDIN and out of SDA/CDOOUT.

Serial Control Data I/O - SDA/CDOOUT

Pin 5, Input/Output

Function:

In I²C mode, SDA is a data input/output. CDOOUT is the control data output for the control port interface in SPI mode.

M1 - Mode Select

Pin 14, Input

Function:

This pin is not used in Control Port Mode and must be terminated to ground.

5.0 PIN DESCRIPTION - DSD MODE

Refer to PCM mode	RST	1	28	VREF	Refer to PCM mode
Refer to PCM mode	M4(ADO/CS)	2	27	FILT+	Refer to PCM mode
Refer to PCM mode	M3(AD1/CDIN)	3	26	FILT-	Refer to PCM mode
Refer to PCM mode	M2(SCL/CCLK)	4	25	CMOUT	Refer to PCM mode
Refer to PCM mode	M0(SDA/CDOOUT)	5	24	AOUTL-	Refer to PCM mode
Refer to PCM mode	DGND	6	23	AOUTL+	Refer to PCM mode
Refer to PCM mode	VD	7	22	VA	Refer to PCM mode
Refer to PCM mode	VD	8	21	AGND	Refer to PCM mode
Refer to PCM mode	DGND	9	20	AOUTR+	Refer to PCM mode
Master Clock	MCLK	10	19	AOUTR-	Refer to PCM mode
DSD Serial Clock	DSD_SCLK	11	18	AGND	Refer to PCM mode
Master Clock Mode	CLKMODE	12	17	MUTE_C	Refer to PCM mode
Left Channel Data	DSD_L	13	16	C/H	Refer to PCM mode
Right Channel Data	DSD_R	14	15	MUTE	Refer to PCM mode

Master Clock - MCLK

Pin 10, Input

Function:

The master clock frequency must be either 4x or 6x the DSD data rate for 64x oversampled DSD data and 2x or 3x the DSD data rate for 128x oversampled DSD data, refer to Table 7.

CLKMODE

Pin 12, Input

Function:

This pin determines the allowable Master Clock to DSD data ratio as defined in Table 7.

		CLKMODE	
		0	1
DSD Over-Sampling Ratio	64x	4x	6x
	128x	2x	3x

Table 7. MCLK to DSD Data Rate Clock Ratios

DSD Serial Clock - DSD_SCLK

Pin 11, Input

Function:

Clocks the individual bits of the DSD audio data into the DSD_L and DSD_R pins.

Audio Data - DSD_L and DSD_R

Pins 13 and 14, Inputs

Function:

Direct Stream Digital audio data is clocked into DSD_L and DSD_R via the DSD serial clock.

6.0 PIN DESCRIPTION - 8X INTERPOLATOR MODE

Refer to PCM mode	RST	□ 1	28 □	VREF	Refer to PCM mode
Refer to PCM mode	M4(AD0/CS)	□ 2	27 □	FILT+	Refer to PCM mode
Refer to PCM mode	M3(AD1/CDIN)	□ 3	26 □	FILT-	Refer to PCM mode
Refer to PCM mode	M2(SCL/CCLK)	□ 4	25 □	CMOUT	Refer to PCM mode
Refer to PCM mode	M0(SDA/CDOUT)	□ 5	24 □	AOUTL-	Refer to PCM mode
Refer to PCM mode	DGND	□ 6	23 □	AOUTL+	Refer to PCM mode
Refer to PCM mode	VD	□ 7	22 □	VA	Refer to PCM mode
Refer to PCM mode	VD	□ 8	21 □	AGND	Refer to PCM mode
Refer to PCM mode	DGND	□ 9	20 □	AOUTR+	Refer to PCM mode
Master Clock	MCLK	□ 10	19 □	AOUTR-	Refer to PCM mode
Bit Clock	BCKI	□ 11	18 □	AGND	Refer to PCM mode
Word Clock	WCKI	□ 12	17 □	MUTE_C	Refer to PCM mode
Left Channel Data	DIL	□ 13	16 □	C/H	Refer to PCM mode
Right Channel Data	DIR	□ 14	15 □	MUTE	Refer to PCM mode

Master Clock - MCLK

Pin 10, Input

Function:

The master clock frequency must be either 32x, 48x, 64x or 96x the input sample rate. Table 8 illustrates the standard audio sample rates and the required master clock frequencies.

Sample Rate (kHz)	MCLK (MHz)			
	32x	48x	64x	96x
32 x 8	8.1920	12.2880	16.384	24.576
44.1 x 8	11.2896	16.9344	22.579	33.869
48 x 8	12.2880	18.4320	24.576	36.864

Table 8. Common Clock Frequencies

Bit Clock - BCKI

Pin 11, Input

Function:

Clocks the individual serial data bits into the DIL and DIR pins. Refer to Figure 33

Word Clock - WCKI

Pin 12, Input

Function:

The word clock determines which channel is currently being input on the serial audio data input, SDATA. The frequency of the word clock must be at 8x the baseband sample rate. Refer to Figure 33.

Serial Audio Data - DIR and DIL

Pins 12 and 13, Inputs

Function:

Two's complement MSB-first serial data is input on these pins. The data is clocked into DIL and DIR via the bit clock. Refer to Figure 33.

7.0 APPLICATIONS

7.1 Recommended Power-up Sequence

1. Hold $\overline{\text{RST}}$ low until the power supplies, master, and left/right clocks are stable.
2. Bring $\overline{\text{RST}}$ high.