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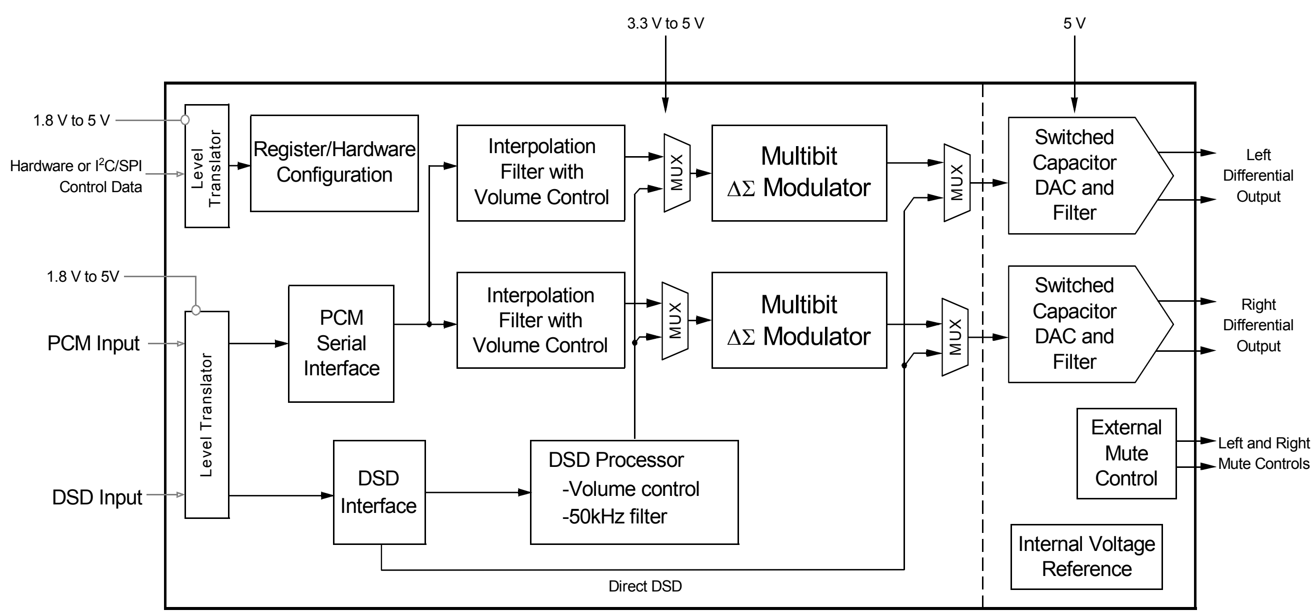
CS4398

120-dB, 192-kHz Multibit DAC with Volume Control

Features

- Advanced Multibit Delta-Sigma Architecture
  - 120 dB Dynamic Range
  - -107 dB THD+N
  - Low Clock Jitter Sensitivity
  - Differential Analog Outputs
- PCM input
  - 102 dB of Stopband Attenuation
  - Supports Sample Rates up to 192 kHz
  - Accepts up to 24 bit Audio Data
  - Supports All Industry Standard Audio Interface Formats
  - Selectable Digital Filter Response
  - Volume Control with 1/2 dB Step Size and Soft Ramp
  - Flexible Channel Routing and Mixing
  - Selectable De-Emphasis
- Supports Stand-Alone or I²C/SPI™ Configuration
  Embedded Level Translators
  - 1.8 V to 5 V Serial Audio Input
  - 1.8 V to 5 V Control Data Input
- Direct Stream Digital (DSD)
  - Dedicated DSD Input Pins
  - On-Chip 50 kHz Filter to Meet Scarlet Book SACD Recommendations
  - Matched PCM and DSD Analog Output Levels
  - Non-Decimating Volume Control with 1/2 dB Step Size and Soft Ramp
  - DSD Mute Detection
  - Supports Phase-Modulated Inputs
  - Optional Direct DSD Path to On-Chip Switched Capacitor Filter
- Control Output for External Muting
  - Independent Left and Right Mute Controls
  - Supports Auto Detection of Mute Output Polarity
- Typical Applications
  - DVD Players
  - SACD Players
  - A/V Receivers
  - Professional Audio Products



Stand-Alone Mode Features

- Selectable Oversampling Modes
  - 32 kHz to 54 kHz Sampling Rates
  - 50 kHz to 108 kHz Sampling Rates
  - 100 kHz to 216 kHz Sampling Rates
- Selectable Serial Audio Interface Formats
  - Left-Justified, up to 24 bit
  - I²S, up to 24 bit
  - Right-Justified 16 bit
  - Right-Justified 24 bit
- Auto Mute Output Polarity Detect
- Auto Mute on Static PCM Samples
- 44.1 kHz 50/15 µs De-Emphasis Available
- Soft Volume Ramp-up after Reset is Released

Control Port Mode Features

- Selectable Oversampling Modes
  - 32 kHz to 54 kHz Sampling Rates
  - 50 kHz to 108 kHz Sampling Rates
  - 100 kHz to 216 kHz Sampling Rates
- Selectable Serial Audio Interface Formats
  - Left-Justified, up to 24 bit
  - I²S, up to 24 bit
  - Right-Justified 16 bit
  - Right-Justified 18 bit
  - Right-Justified 20 bit
  - Right-Justified 24 bit
- Direct Stream Digital Mode
- Selectable Auto or Manual Mute Polarity
- Selectable Interpolation Filters
- Selectable 32, 44.1, and 48 kHz De-Emphasis
- Configurable ATAPI Mixing Functions
- Configurable Volume and Muting Controls

Description

The CS4398 is a complete stereo 24 bit/192 kHz digital-to-analog system. This D/A system includes digital de-emphasis, half dB step size volume control, ATAPI channel mixing, selectable fast and slow digital interpolation filters followed by an oversampled multi-bit delta-sigma modulator that includes mismatch shaping technology that eliminates distortion due to capacitor mismatch. Following this stage is a multi-element switched capacitor stage and low pass filter with differential analog outputs.

The CS4398 also has a proprietary DSD processor that allows for volume control and 50 kHz on-chip filtering without an intermediate decimation stage. It also offers an optional path for direct DSD conversion by directly using the multi-element switched capacitor array.

The CS4398 accepts PCM data at sample rates from 32 kHz to 216 kHz, DSD audio data, has selectable digital filters, consumes little power, and delivers excellent sound quality.

ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS4398	120 dB, 192 kHz Multi-Bit DAC with Volume Control	28-pin TSSOP	YES	Commercial	-10° to +70° C	Rail	CS4398-CZZ
						Tape & Reel	CS4398-CZZR
		28-pin QFN				Rail	CS4398-CNZ
						Tape & Reel	CS4398-CNZR
CDB4398	CS4398 Evaluation Board		-	-	-	-	CDB4398

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1. PINOUT DRAWING

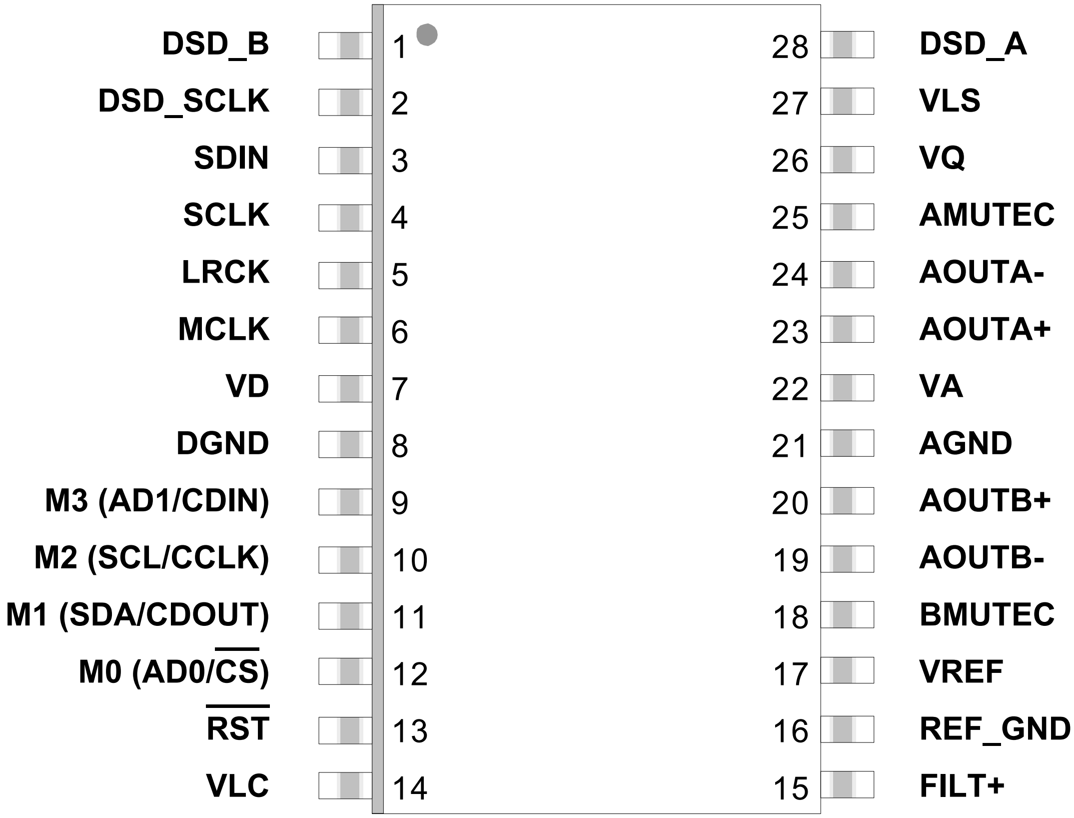

Figure 1. Pinout Drawing —TSSOP

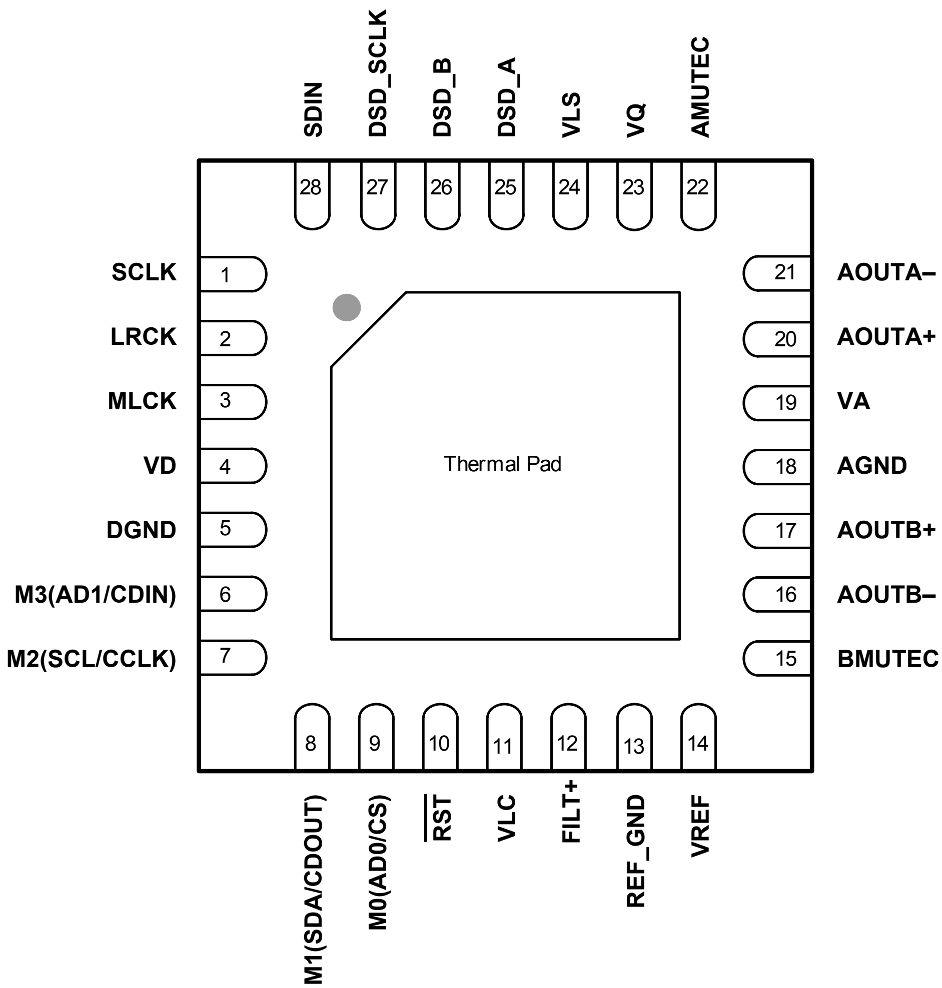

Figure 2. Pinout Drawing —QFN

Pin Name	TSSOP Pin #	QFN Pin #	Pin Description
DSD_A DSD_B	28 1	25 26	**Direct Stream Digital Input** (*Input*) - Input for Direct Stream Digital serial audio data.
DSD_SCLK	2	27	**DSD Serial Clock** (*Input*) - Serial clock for the Direct Stream Digital audio interface.
SDIN	3	28	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
SCLK	4	1	**Serial Clock** (*Input*) - Serial clock for the serial audio interface.
LRCK	5	2	**Left Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	6	3	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
VD	7	4	**Digital Power** (*Input*) **-** Positive power for the digital section.
DGND	8	5	**Digital Ground** (*Input*) - Ground reference for the digital section.
$\overline{\text{RST}}$	13	10	**Reset** (*Input*) - The device enters system reset when enabled.
VLC	14	11	**Control Port Power** (*Input*) **-** Positive power for Control Port I/O.
FILT+	15	12	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.
REF_GND	16	13	**Reference Ground** (*Input*) - Ground reference for the internal sampling circuits.
VREF	17	14	**Voltage Reference** (*Input*) - Positive voltage reference for internal sampling circuits.
BMUTEC AMUTEC	18 25	15 22	**Mute Control** (*Output*) - The Mute Control pin is active during power-up initialization, muting, power-down or if the master clock to left/right clock frequency ratio is incorrect. During reset, these outputs are set to a high impedance.
AOUTB+ AOUTB-	20 19	17 16	**Differential Right Channel Analog Output** (*Output*) - The full-scale differential analog output level is specified in the Analog Characteristics specification table.
AGND	21	18	**Analog Ground** (*Input*) - Ground reference for the analog section.
VA	22	19	**Analog Power** (*Input*) **-** Positive power for the analog section.
AOUTA+ AOUTA-	23 24	20 21	**Differential Left Channel Analog Output** (*Output*) - The full-scale differential analog output level is specified in the Analog Characteristics specification table.
VQ	26	23	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage.
VLS	27	24	**Serial Audio Interface Power** (*Input*) **-** Positive power for serial audio interface I/O.
Stand-Alone Mode Definitions			
M3 M2 M1 M0	9 10 11 12	6 7 8 9	**Mode Selection** (*Input*) - Determines the operational mode of the device.
Control Port Mode Definitions			
AD1/CDIN	9	6	**Address Bit 1 (I²C) / Control Data Input (SPI)** (*Input*) - AD1 is a chip address pin in I²C mode; CDIN is the input data line for the Control Port interface in SPI mode.
SCL/CCLK	10	7	**Serial Control Port Clock** (*Input*) - Serial clock for the serial Control Port.
SDA/CDOUT	11	8	**Serial Control Data (I²C) / Control Data Output (SPI)** (*Input/Output*) - SDA is a data I/O line in I²C mode. CDOUT is the output data line for the Control Port interface in SPI mode.
AD0/$\overline{\text{CS}}$	12	9	**Address Bit 0 (I²C) / Control Port Chip Select (SPI)** (*Input*) - AD0 is a chip address pin in I²C mode; $\overline{\text{CS}}$ is the chip select signal for SPI format.
Recommended Connection for QFN package			
Thermal Pad	N/A	—	**Thermal Pad** (QFN package only) - Tie to ground for thermal dissipation.

2. CHARACTERISTICS AND SPECIFICATIONS

(Min/Max performance characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics are derived from measurements taken at T_A = 25 °C, VA = 5.0 V, VD = 3.3 V.)

SPECIFIED OPERATING CONDITIONS

(AGND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Typ	Max	Units
DC Power Supply	Analog power	VA	4.75	5.0	5.25	V
	Voltage reference	VREF	4.75	5.0	5.25	V
	Digital power	VD	3.1	3.3	5.25	V
	Serial audio interface power	VLS	1.7	3.3	5.25	V
	Control port interface power	VLC	1.7	3.3	5.25	V
Specified Temperature Range	-CZ & -CZZ	T_A	-10	-	70	°C

ABSOLUTE MAXIMUM RATINGS

(AGND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Max	Units
DC Power Supply	Analog power	VA	-0.3	6.0	V
	Voltage reference	VREF	-0.3	6.0	V
	Digital power	VD	-0.3	6.0	V
	Serial audio interface power	VLS	-0.3	6.0	V
	Control port interface power	VLC	-0.3	6.0	V
Input Current	any pin except supplies	I_{in}	-	±10	mA
Digital Input Voltage	Serial audio interface	V_{IN-LS}	-0.3	VLS+ 0.4	V
	Control port interface	V_{IN-LC}	-0.3	VLC+ 0.4	V
Ambient Operating Temperature (power applied)		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

ANALOG CHARACTERISTICS

(Test conditions (unless otherwise specified): Input test signal is a 997 Hz sine wave at 0 dBFS; measurement bandwidth is 10 Hz to 20 kHz; test load R_L = 1 kΩ, C_L = 10 pF.)

Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Performance - All PCM modes and DSD Processor mode					
Dynamic Range (Note 1) 24-bit A-Weighted		114	120	-	dB
unweighted		111	117	-	dB
16-bit A-Weighted		-	97	-	dB
(Note 2) unweighted		-	94	-	dB
Total Harmonic Distortion + Noise (Note 1)	THD+N				
24-bit 0 dB		-	-107	-100	dB
-20 dB		-	-97	-	dB
-60 dB		-	-57	-	dB
16-bit 0 dB		-	-94	-	dB
(Note 2) -20 dB		-	-74	-	dB
-60 dB		-	-34	-	dB
Idle Channel Noise / Signal-to-noise ratio		-	120	-	dB
Dynamic Performance - Direct DSD					
Dynamic Range (Note 3) A-Weighted		111	117	-	dB
unweighted		108	114	-	dB
Total Harmonic Distortion + Noise (Note 3)	THD+N				
0 dB		-	-104	-98	dB
-20 dB		-	-94	-	dB
-60 dB		-	-54	-	dB
Dynamic Performance for All Modes					
Interchannel Isolation (1 kHz)		-	110	-	dB
DC Accuracy					
Interchannel Gain Mismatch	ICGM	-	0.1	-	dB
Gain Drift		-	100	-	ppm/°C
Analog Output Characteristics and Specifications					
Full Scale Differential Output Voltage PCM, DSD processor		132%•V_A	134%•V_A	136%•V_A	Vpp
Direct DSD mode		94%•V_A	96%•V_A	98%•V_A	Vpp
Output Impedance	Z_{OUT}	-	118	-	Ω
Minimum AC-Load Resistance	R_L	-	1	-	kΩ
Maximum Load Capacitance	C_L	-	100	-	pF

Notes:

1. One LSB of triangular PDF dither is added to data.
2. Performance limited by 16-bit quantization noise.
3. DSD performance may be limited by the source recording. 0 dB-SACD = 50% modulation index.

COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

The filter characteristics have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs.)
(See note 9.)

Parameter		Fast Roll-Off			Unit
		Min	Typ	Max	
Combined Digital and On-Chip Analog Filter Response - Single-Speed Mode - 48 kHz (Note 5)					
Passband (Note 6)	to -0.01 dB corner	0	-	.454	Fs
	to -3 dB corner	0	-	.499	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	+0.01	dB
StopBand		0.547	-	-	Fs
StopBand Attenuation	(Note 7)	102	-	-	dB
Group Delay		-	9.4/Fs	-	s
De-emphasis Error (Note 8)	Fs = 32 kHz	-	-	±0.23	dB
(Relative to 1 kHz)	Fs = 44.1 kHz	-	-	±0.14	dB
	Fs = 48 kHz	-	-	±0.09	dB
Combined Digital and On-Chip Analog Filter Response - Double-Speed Mode - 96 kHz (Note 5)					
Passband (Note 6)	to -0.01 dB corner	0	-	.430	Fs
	to -3 dB corner	0	-	.499	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	dB
StopBand		.583	-	-	Fs
StopBand Attenuation	(Note 7)	80	-	-	dB
Group Delay		-	4.6/Fs	-	s
Combined Digital and On-Chip Analog Filter Response - Quad-Speed Mode - 192 kHz (Note 5)					
Passband (Note 6)	to -0.01 dB corner	0	-	.105	Fs
	to -3 dB corner	0	-	.490	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	dB
StopBand		.635	-	-	Fs
StopBand Attenuation	(Note 7)	90	-	-	dB
Group Delay		-	4.7/Fs	-	s

4. Slow Roll-off interpolation filter is only available in Control Port mode.
5. Filter response is guaranteed by design.
6. Response is clock-dependent and will scale with Fs.
7. For Single-Speed Mode, the Measurement Bandwidth is from stopband to 3 Fs.
   For Double-Speed Mode, the Measurement Bandwidth is from stopband to 3 Fs.
   For Quad-Speed Mode, the Measurement Bandwidth is from stopband to 1.34 Fs.
8. De-emphasis is available only in Single-Speed Mode; Only 44.1 kHz De-emphasis is available in Stand-Alone mode.
9. Amplitude vs. Frequency plots of this data are available in the “Appendix” on page 44.

COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

(Continued)

Parameter		Slow Roll-Off (Note 4) Min	Typ	Max	Unit
Single-Speed Mode - 48 kHz (Note 5)					
Passband (Note 6)	to -0.01 dB corner	0	-	0.417	Fs
	to -3 dB corner	0	-	0.499	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	+0.01	dB
StopBand		.583	-	-	Fs
StopBand Attenuation	(Note 7)	64	-	-	dB
Group Delay		-	6.65/Fs	-	s
De-emphasis Error (Note 8)	Fs = 32 kHz	-	-	±0.23	dB
(Relative to 1 kHz)	Fs = 44.1 kHz	-	-	±0.14	dB
	Fs = 48 kHz	-	-	±0.09	dB
Double-Speed Mode - 96 kHz (Note 5)					
Passband (Note 6)	to -0.01 dB corner	0	-	.296	Fs
	to -3 dB corner	0	-	.499	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	dB
StopBand		.792	-	-	Fs
StopBand Attenuation	(Note 7)	70	-	-	dB
Group Delay		-	3.9/Fs	-	s
Quad-Speed Mode - 192 kHz (Note 5)					
Passband (Note 6)	to -0.01 dB corner	0	-	.104	Fs
	to -3 dB corner	0	-	.481	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	dB
StopBand		.868	-	-	Fs
StopBand Attenuation	(Note 7)	75	-	-	dB
Group Delay		-	4.2/Fs	-	s

DSD COMBINED DIGITAL & ON-CHIP ANALOG FILTER RESPONSE

Parameter		Min	Typ	Max	Unit
DSD Processor Mode (Note 5)					
Passband (Note 6)	to -3 dB corner	0	-	50	kHz
Frequency Response 10 Hz to 20 kHz		-0.05	-	0.05	dB
Roll-off		27	-	-	dB/Oct
Direct DSD Mode (Note 5)					
Passband (Note 6)	to -0.1 dB corner	0	-	26.9	kHz
	to -3 dB corner	0	-	176.4	kHz
Frequency Response 10 Hz to 20 kHz		-0.1	-	0	dB

SWITCHING CHARACTERISTICS

(Inputs: Logic 0 = GND, Logic 1 = VLS, CL = 20 pF)

Parameters		Symbol	Min	Typ	Max	Units
Input Sample Rate	Single-Speed Mode	Fs	30	-	54	kHz
	Double-Speed Mode	Fs	50	-	108	kHz
	Quad-Speed Mode	Fs	100	-	216	kHz
MCLK Frequency		See Tables 1 & 2 (page 22) for compatible frequencies				
MCLK Duty Cycle			40%	-	60%	
LRCK Duty Cycle			45%	50	55%	
SCLK Pulse Width Low		t_{sclkl}	20	-	-	ns
SCLK Pulse Width High		t_{sclkh}	20	-	-	ns
SCLK Period	Single-Speed Mode	t_{sclkw}	$\frac{1}{(128)Fs}$	-	-	ns
	Double-Speed Mode	t_{sclkw}	$\frac{1}{(64)Fs}$	-	-	ns
	Quad-Speed Mode	t_{sclkw}	$\frac{2}{MCLK}$	-	-	ns
SCLK rising to LRCK edge delay		t_{slrd}	20	-	-	ns
SCLK rising to LRCK edge setup time		t_{slrs}	20	-	-	ns
SDATA valid to SCLK rising setup time		t_{sdlrs}	22	-	-	ns
SCLK rising to SDATA hold time		t_{sdh}	20	-	-	ns

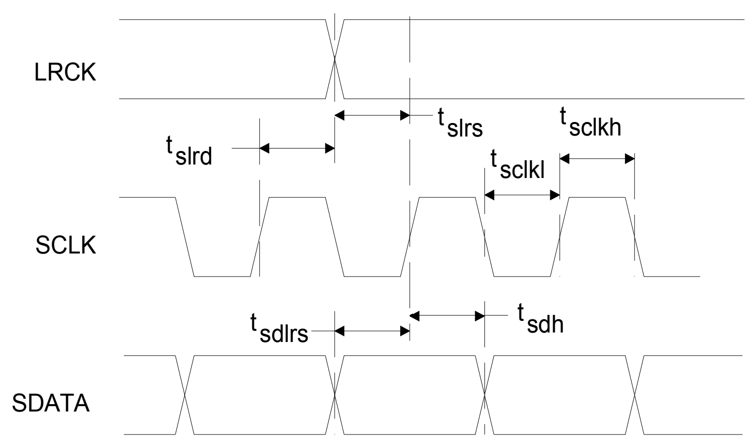

Figure 3. Serial Mode Input Timing

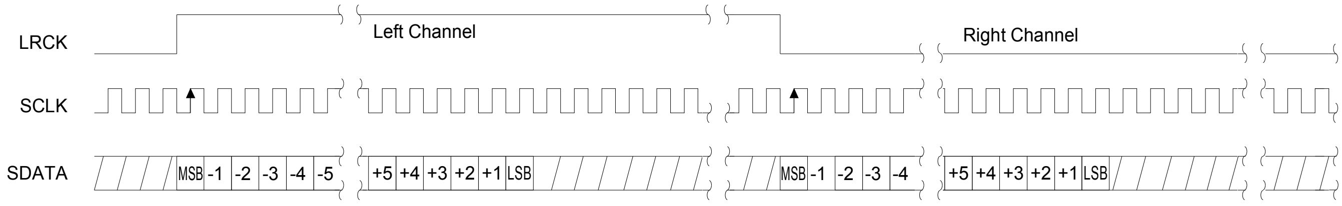

Figure 4. Format 0 - Left-Justified up to 24-bit Data

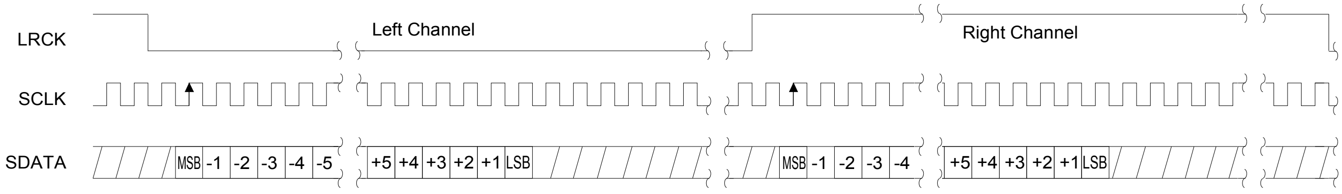

Figure 5. Format 1 - I²S up to 24-bit Data

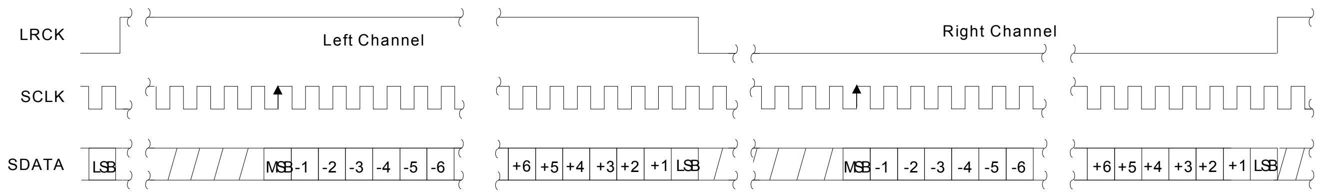

Figure 6. Format 2, Right-Justified 16-Bit Data.
Format 3, Right-Justified 24-Bit Data.
Format 4, Right-Justified 20-Bit Data. (Available in Control Port Mode only)
Format 5, Right-Justified 18-Bit Data. (Available in Control Port Mode only)

SWITCHING CHARACTERISTICS- DSD

(Logic 0 = AGND = DGND; Logic 1 = VLS Volts; C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
MCLK Duty Cycle		40	-	60	%
DSD_SCLK Pulse Width Low	t_{sclkl}	160	-	-	ns
DSD_SCLK Pulse Width High	t_{sclkh}	160	-	-	ns
DSD_SCLK Frequency (64x Oversampled) (128x Oversampled)		1.024 2.048	- -	3.2 6.4	MHz MHz
DSD_A / _B valid to DSD_SCLK rising setup time	t_{sdlrs}	20	-	-	ns
DSD_SCLK rising to DSD_A or DSD_B hold time	t_{sdh}	20	-	-	ns
DSD clock to data transition (Phase Modulation mode)	t_{dpm}	-20	-	20	ns

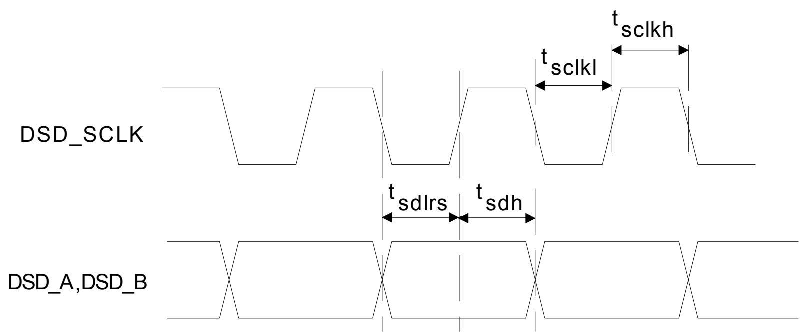

Figure 7. Direct Stream Digital - Serial Audio Input Timing

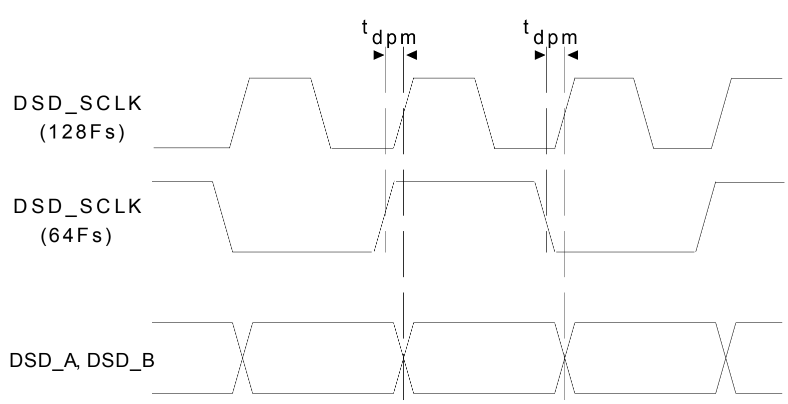

Figure 8. Direct Stream Digital - Serial Audio Input Timing for Phase Modulation Mode

SWITCHING CHARACTERISTICS- CONTROL PORT - I²C FORMAT

(Inputs: Logic 0 = GND, Logic 1 = VLC, C_L = 20 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{RST}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free-Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low Time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 10)	t_{hdd}	0	-	µs
SDA Setup Time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}, t_{rd}	-	1	µs
Fall Time SCL and SDA	t_{fc}, t_{fd}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	1000	ns

10. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

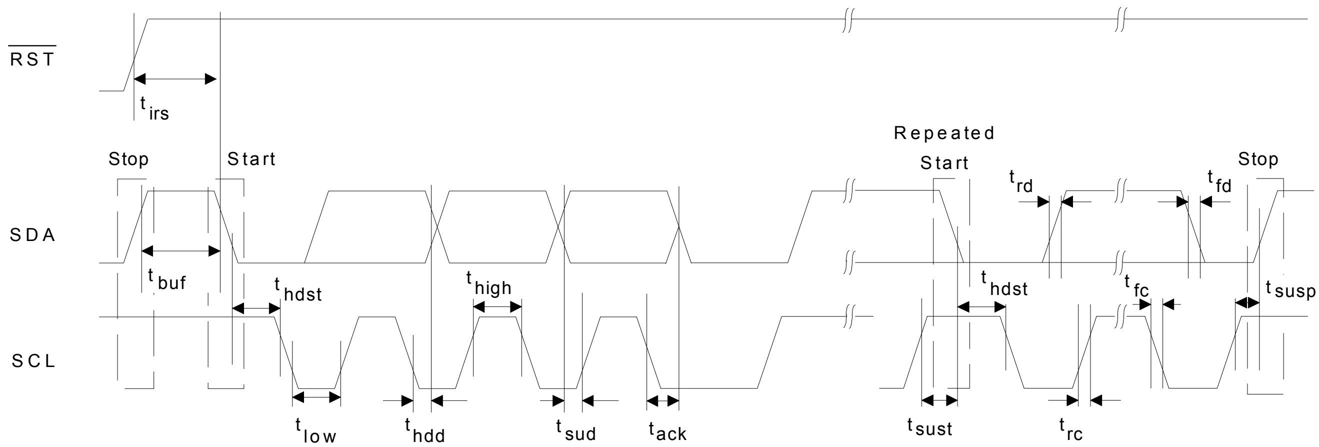

Figure 9. Control Port Timing - I²C Format

SWITCHING CHARACTERISTICS- CONTROL PORT - SPI™ FORMAT

(Inputs: Logic 0 = GND, Logic 1 = VLC, C_L = 20 pF)

Parameter		Symbol	Min	Max	Unit
CCLK Clock Frequency		f_{sclk}	-	6	MHz
$\overline{\text{RST}}$ Rising Edge to CS Falling		t_{srs}	500	-	ns
CCLK Edge to $\overline{\text{CS}}$ Falling	(Note 11)	t_{spi}	500	-	ns
$\overline{\text{CS}}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
$\overline{\text{CS}}$ Falling to CCLK Edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 12)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN	(Note 13)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 13)	t_{f2}	-	100	ns
Transition time from CCLK to CDOUT valid	(Note 14)	t_{scdov}	-	40	ns
Time from $\overline{\text{CS}}$ rising to CDOUT high-Z	(Note 15)	t_{cscdo}	-	20	ns

11. t_{spi} only needed before first falling edge of $\overline{\text{CS}}$ after $\overline{\text{RST}}$ rising edge. t_{spi} = 0 at all other times.
12. Data must be held for sufficient time to bridge the transition time of CCLK.
13. For F_{SCK} < 1 MHz.
14. CDOUT should *not* be sampled during this time period.
15. This time is by design and not tested.

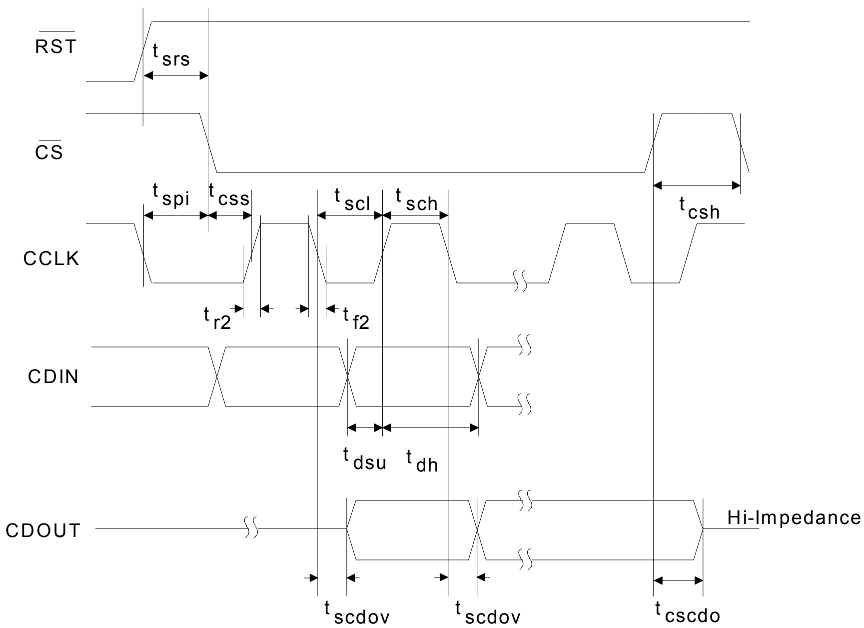

Figure 10. Control Port Timing - SPI Format (Read/Write)

DC ELECTRICAL CHARACTERISTICS

Parameters		Symbol	Min	Typ	Max	Units
Normal Operation (Note 16)						
Power Supply Current	V_A= 5 V (Note 17)	I_A	-	25	28	mA
	V_{ref}= 5 V	I_{ref}	-	1.5	2	mA
	V_D = 5 V	I_D	-	25	38	mA
	V_D = 3.3 V	I_D	-	18	27	mA
	Interface current (Note 18)	I_{LC}	-	2	-	µA
		I_{LS}	-	80	-	µA
Power Dissipation	VA = 5 V, VD = 5 V		-	258	340	mW
	VA = 5 V, VD = 3.3 V		-	192	240	mW
Power-Down Mode (Note 19)						
Power Supply Current		I_{pd}	-	200	-	µA
Power Dissipation	VA = 5 V, VD = 5 V		-	1	-	mW
	VA = 5 V, VD = 3.3 V		-	1	-	mW
All Modes of Operation						
Power Supply Rejection Ratio (Note 20)	(1 kHz)	PSRR	-	60	-	dB
	(60 Hz)		-	40	-	dB
Common Mode Voltage		V_Q	-	0.5•V_A	-	V
Max Current draw from VQ		I_{Qmax}	-	1	-	µA
FILT+ Nominal Voltage			-	0.93•V_A	-	V
Maximum MUTEC Drive Current	(Note 21)		-	3	-	mA
MUTEC High-Level Output Voltage		V_{OH}		VA		V
MUTEC Low-Level Output Voltage		V_{OL}		0		V

16. Normal operation is defined as $\overline{RST}$ pin = High with a 997 Hz, 0 dBFS input sampled at the highest Fs for each speed mode, and open outputs, unless otherwise specified.
17. I_A measured with no loading on the AMUTEC and BMUTEC pins.
18. I_{LC} measured with no external loading on pin 11 (SDA).
19. Power-Down mode is defined as $\overline{RST}$ pin = Low with all clock and data lines held static.
20. Valid with the recommended capacitor values on FILT+ and V_Q as shown in the “Typical Connection Diagram” on page 20.
21. This current is sourced/sinked directly from the VA supply.

DIGITAL INTERFACE SPECIFICATIONS

Parameters		Symbol	Min	Typ	Max	Units
Input Leakage Current		I_{in}	-	-	±10	µA
Input Capacitance			-	8	-	pF
High-Level Input Voltage	Serial I/O Control I/O	V_{IH} V_{IH}	70% 70%	- -	- -	V_{LS} V_{LC}
Low-Level Input Voltage	Serial I/O Control I/O	V_{IL} V_{IL}	- -	- -	30% 30%	V_{LS} V_{LC}
High-Level Output Voltage (I_{OH} = -1.2 mA)	Control I/O	V_{OH}	80%	-	-	V_{LC}
Low-Level Output Voltage (I_{OL} = 1.2 mA)	Control I/O	V_{OL}	-	-	20%	V_{LC}
MUTEC auto detect input high voltage			70%			VA
MUTEC auto detect input low voltage					30%	VA

3. TYPICAL CONNECTION DIAGRAM

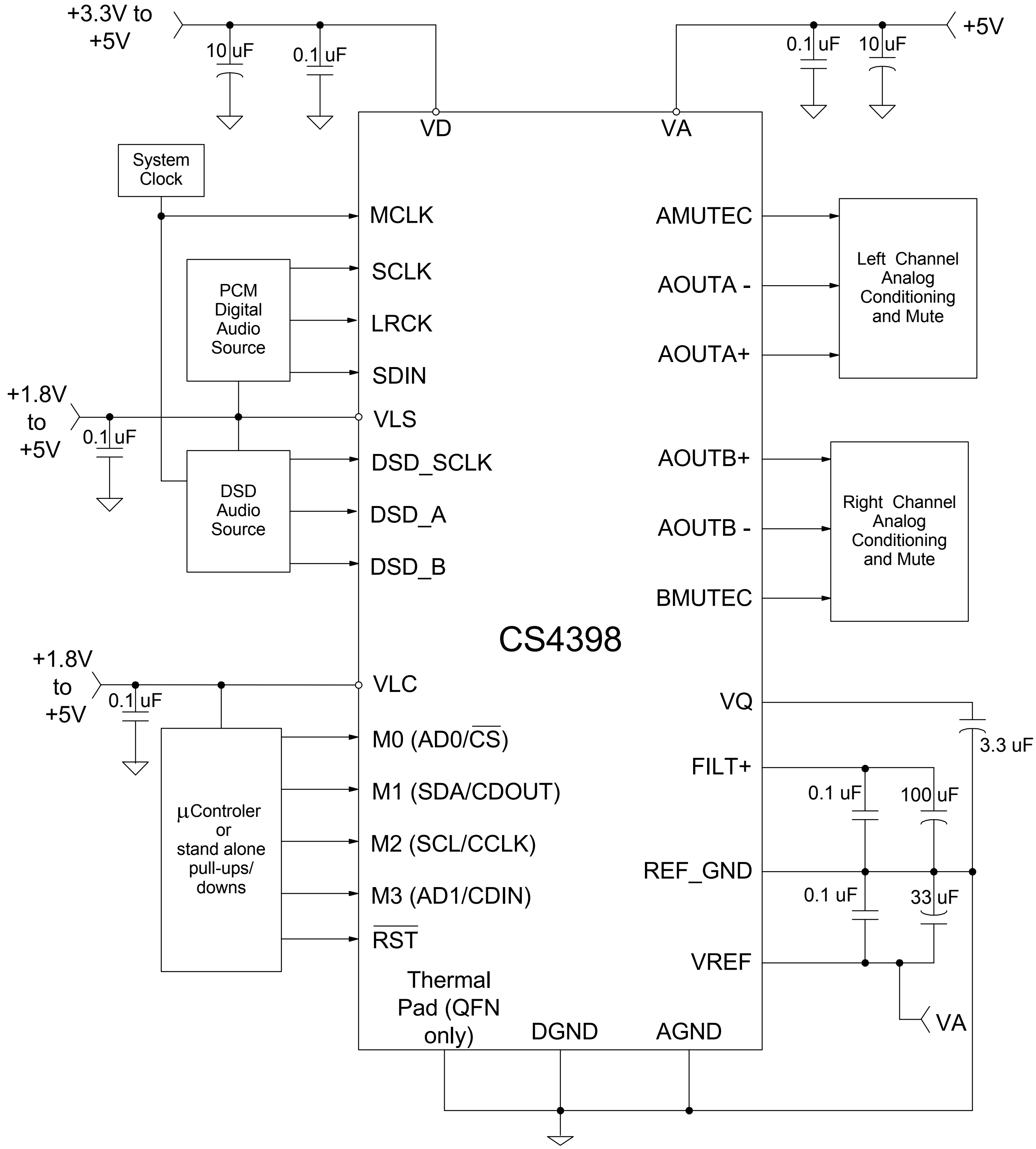

Figure 11. Typical Connection Diagram

4. APPLICATIONS

4.1 Grounding and Power Supply Decoupling

As with any high resolution converter, the CS4398 requires careful attention to power supply and grounding arrangements to optimize performance. The Typical Connection Diagram shows the recommended power arrangement with VA, VD, VLS and VLC connected to clean supplies. Decoupling capacitors should be located as close to the device package as possible. If desired, all supply pins may be connected to the same supply, but the recommended decoupling capacitors should still be placed on each supply pin. The AGND and DGND pins should be tied together with solid ground plane fill underneath the converter extending out to the GND side of the decoupling caps for VA, VD, VREF, and FILT+. This recommended layout can be seen in the CDB4398 evaluation board and datasheet. For the QFN package, the thermal pad should also be tied to ground for thermal dissipation.

4.2 Analog Output and Filtering

The Cirrus Logic application note “Design Notes for a 2-Pole Filter with Differential Input” (AN48) discusses the second-order Butterworth filter and differential to single-ended converter topology that was implemented on the CS4398 evaluation board, CDB4398, as seen in Figure 12.

The CS4398 does not include phase or amplitude compensation for an external filter. Therefore, the DAC system phase and amplitude response is dependent on the external analog circuitry.

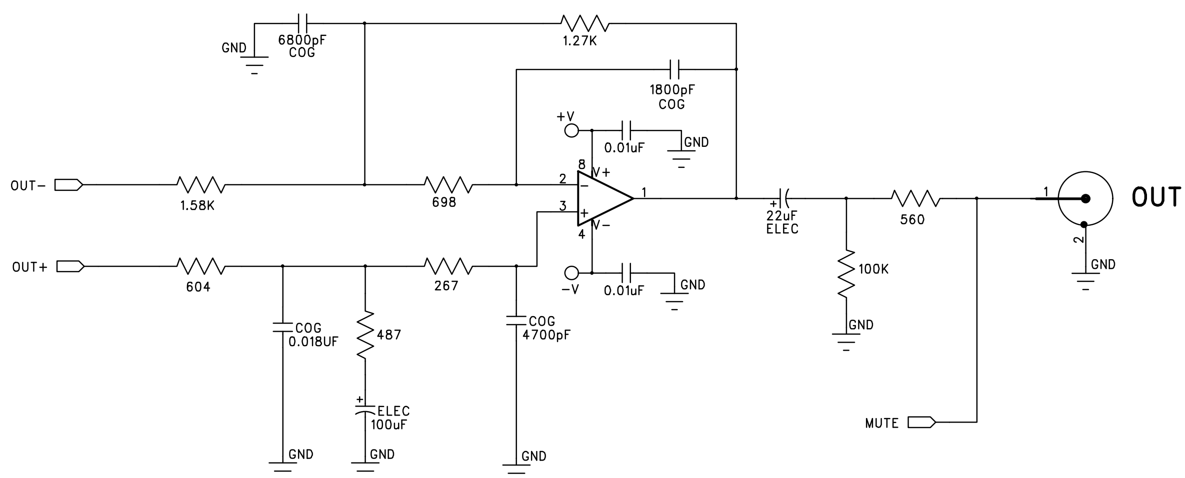

Figure 12. Recommended Output Filter

4.3 The MUTEC Outputs

The AMUTEC and BMUTEC pins have an auto-polarity detect feature. The MUTEC output pins are high impedance at the time of reset. The external mute circuitry needs to be self-biased into an active state in order to be muted during reset. Upon release of reset, the CS4398 detects the status of the MUTEC pins (high or low) and then selects that state as the polarity to drive when the mutes become active. The external-bias voltage level that the MUTEC pins see at the time of release of reset must meet the “MUTEC auto detect input high/low voltage” specifications as outlined in the Digital Characteristics in Section 2.

Figure 13 shows a single example of both an active-high and an active-low mute drive circuit. In these designs, the pull-up and pull-down resistors have been specifically chosen to meet the input high/low threshold when used with the MMUN2111 and MMUN2211 internal bias resistances of 10 kΩ.

Use of the Mute Control function is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the Mute Control function can enable the system designer to achieve idle channel noise/signal-to-noise ratios which are only limited by the external mute circuit.

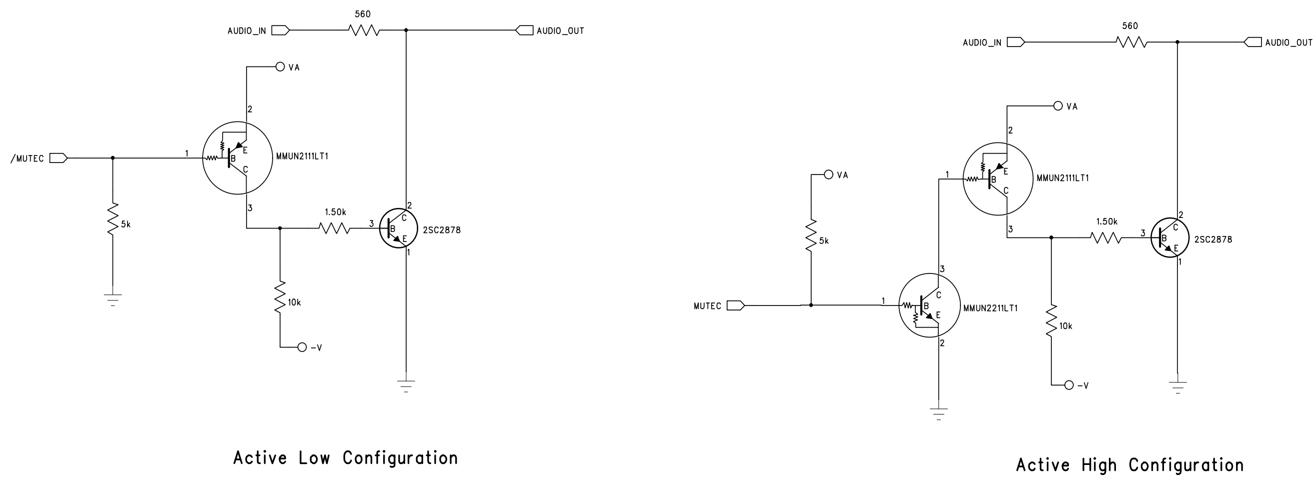

Figure 13. Recommended Mute Circuitry

4.4 Oversampling Modes

The CS4398 operates in one of three oversampling modes based on the input sample rate. Single-Speed mode supports input sample rates up to 50 kHz and uses a 128x oversampling ratio. Double-Speed mode supports input sample rates up to 100 kHz and uses an oversampling ratio of 64x. Quad-Speed mode supports input sample rates up to 200 kHz and uses an oversampling ratio of 32x.

4.5 Master and Serial Clock Ratios

The required MCLK-to-LRCK ratio and suggested SCLK-to-LRCK ratio are outlined in Table 1. MCLK can be at any phase in regards to LRCK and SCLK. SCLK, LRCK and SDATA must meet the phase and timing relationships outlined in Section 2. Some common MCLK frequencies have been outlined in Table 2.

	MCLK/LRCK	SCLK/LRCK	LRCK
Single-Speed	256, 384, 512, 768*, 1024*, 1152*	32, 48, 64, 96, 128	Fs
Double-Speed	128, 192, 256, 384, 512*	32, 48, 64	Fs
Quad-Speed	64	32 (16 bits only)	Fs
	96	32, 48	Fs
	128, 256*	32, 64	Fs
	192	32, 48, 64, 96	Fs
****These modes are only available in Control Port mode by setting the appropriate MCLKDIV bit.***			

Table 1. Clock Ratios

Mode (sample-rate range)	Sample Rate (kHz)	MCLK (MHz)					
					MCLKDIV2		MCLKDIV3
MCLK Ratio		256x	384x	512x	768x	1024x	1152x
Single-Speed (32 to 50 kHz)	32	8.1920	12.2880	16.3840	24.5760	32.7680	36.8640
	44.1	11.2896	16.9344	22.5792	33.8688	45.1584	-
	48	12.2880	18.4320	24.5760	36.8640	49.1520	-
MCLK Ratio		128x	192x	256x	384x	512x	-
Double-Speed (50 to 100 kHz)	64	8.1920	12.2880	16.3840	24.5760	32.7680	-
	88.2	11.2896	16.9344	22.5792	33.8688	45.1584	-
	96	12.2880	18.4320	24.5760	36.8640	49.1520	-
MCLK Ratio		64x*	96x	128x	192x	256x	-
Quad-Speed (100 to 200 kHz)	176.4	11.2896*	16.9344	22.5792	33.8688	45.1584	-
	192	12.2880*	18.4320	24.5760	36.8640	49.1520	-
These modes are only available in Control Port mode by setting the appropriate MCLKDIV bit.							
* This MCLK ratio limits the audio word length to 16 bits; see Table 1 on page 22							

Table 2. Common Clock Frequencies

4.6 Stand-Alone Mode Settings

In Stand-Alone mode (also referred to as "Hardware mode"), the device is configured using the M0 through M3 pins. These pins must be connected to either the VLC supply or ground. The Interface format is set by pins M0 and M1. The sample rate range/oversampling mode (Single/Double/Quad-Speed mode) and de-emphasis are set by pins M2 and M3. The settings can be found in Tables 3 and 4.

M1	M0	Description	Format	Figure
0	0	Left-Justified, up to 24-bit data	0	4
0	1	I²S, up to 24-bit data	1	5
1	0	Right-Justified, 16-bit Data	2	6
1	1	Right-Justified, 24-bit Data	3	6

Table 3. Digital Interface Format, Stand-Alone Mode Options

M3	M2	Description
0	0	Single-Speed without De-Emphasis (32 to 50 kHz sample rates)
0	1	Single-Speed with 44.1 kHz De-Emphasis; see Figure 18 on page 31
1	0	Double-Speed (50 to 100 kHz sample rates)
1	1	Quad-Speed (100 to 200 kHz sample rates)

Table 4. Mode Selection, Stand-Alone Mode Options

The following features are always enabled in Stand-Alone mode: Auto-mute on zero data, Auto MUTEC polarity detect, ramp volume from mute to 0dB by 1/8th dB steps every LRCK (soft ramp) after reset or clock mode change, and the fast roll-off interpolation filter is used.

The following features are not available in Stand-Alone mode: DSD mode, Right-Justified 20- and 18-bit serial audio interfaces, MCLK divide-by-2 and MCLK divide-by-3 (allows 1024 and 1152 clock ratios), slow roll-off interpolation filter, volume control, ATAPI mixing, 48 kHz and 32 kHz de-emphasis, and all other features enabled by registers that are not mentioned above.

4.6.1 Recommended Power-Up Sequence (Stand-Alone Mode)

1. Hold $\overline{RST}$ low until the power supply, master, and left/right clocks are stable. In this state, the Control Port is reset to its default settings.

2. Bring $\overline{RST}$ high. The device will remain in a low power state and will initiate the Stand-Alone power-up sequence following approximately 2^{18} MCLK cycles.

4.7 Control Port Mode

4.7.1 Recommended Power-Up Sequence (Control Port Mode)

1. Hold $\overline{RST}$ low until the power supply, master, and left/right clocks are stable. In this state, the Control Port is reset to its default settings.

2. Bring $\overline{RST}$ high. Set the CPEN bit (Reg. 8h) prior to the completion of the Stand-Alone power-up sequence (approximately 2^{18} MCLK cycles). Setting this bit halts the Stand-Alone power-up sequence and initializes the Control Port to its default settings. The desired register settings can be loaded while keeping the PDN bit (Reg. 8h) set to 1.

3. Clear the PDN bit to initiate the power-up sequence.

If the CPEN bit is not written within the allotted time, the device will start-up in stand-alone mode and begin converting data according to the current state of the M0 to M3 pins. Since these pins are also the control port pins, an undesired mode may be entered. For this reason, if the CPEN bit is not set before the allotted time elapses, the SDIN line must be kept at static 0 (not dithered) until the device is properly configured. This will keep the device from converting data improperly.

4.7.2 Sample Rate Range/Oversampling Mode (Control Port Mode)

Sample rate mode selection is determined by the FM bits (Reg. 02h).

4.7.3 Serial Audio Interface Formats (Control Port Mode)

The desired serial audio interface format is selected using the DIF2:0 bits (Reg. 02h).

4.7.4 MUTEC Pins (Control Port Mode)

The auto-mute polarity feature (mentioned in Section 4.3) is defeatable. The MUTEP1:0 bits in register 04h give the option to override the mute polarity which was auto detected at startup (see the Register Description section for more details).

4.7.5 Interpolation Filter (Control Port Mode)

To accommodate the increasingly complex requirements of digital audio systems, the CS4398 incorporates selectable interpolation filters. A fast and a slow roll-off filter are available in each of Single-, Double-, and Quad-Speed modes. These filters have been designed to accommodate a variety of musical tastes and styles. The FILT_SEL bit (Reg. 07h) is used to select which filter is used (see the Register Description section for more details).

Filter specifications can be found in Section 2, and filter response plots can be found in Figures 22 to 45 in the “Appendix” on page 44.

4.7.6 Direct Stream Digital (DSD) Mode (Control Port Mode)

In Control Port mode, the FM bits (Reg. 02h) are used to configure the device for DSD mode. The DIF bits (Reg 02h) then control the expected DSD rate and MCLK ratio.

The DSD_SRC bit (Reg. 02h) selects the input pins for DSD clocks and data. During DSD operation, the PCM-related pins should either be tied low or remain active with clocks. When the DSD related pins are not being used, they should either be tied low or remain active with clocks.

The DIR_DSD bit (Reg 07h) selects between two proprietary methods for DSD-to-analog conversion. The first method uses a decimation-free DSD processing technique that allows for features such as matched PCM level output, DSD volume control, and 50 kHz on-chip filter. The second method sends the DSD data directly to the on-chip switched-capacitor filter for conversion (without the above mentioned features).

The DSD_PM_EN bit (Reg. 09h) selects Phase Modulation (data plus data inverted) as the style of data input. In this mode, the DSD_PM_mode bit selects whether a 128Fs or 64x clock is used for phase modulated 64x data (see Figure 14). Use of phase modulation mode may not directly affect the performance of the CS4398, but may lower the sensitivity to board-level routing of the DSD data signals.

The CS4398 can detect errors in the DSD data that do not comply to the SACD specification. The STATIC_DSD and INVALID_DSD bits (Reg. 09h) allow the CS4398 to alter the incoming invalid DSD data. Depending on the error, the data may either be attenuated or replaced with a muted DSD signal (the MUTEC pins would set according to the DAMUTE bit (Reg. 04h)).

More information for any of these register bits can be found in the Register Description section.

The DSD input structure and analog outputs are designed to handle a nominal 0 dB-SACD (50% modulation index) at full rated performance. Signals of +3 dB-SACD may be applied for brief periods of time; however, performance at these levels is not guaranteed. If sustained +3 dB-SACD levels are required, the digital volume control should be set to -3.0 dB. This same volume control register affects PCM output levels. There is no need to change the volume control setting between PCM and DSD in order to have the 0 dB output levels match (both 0 dBFS and 0 dB-SACD will output at -3 dB in this case).

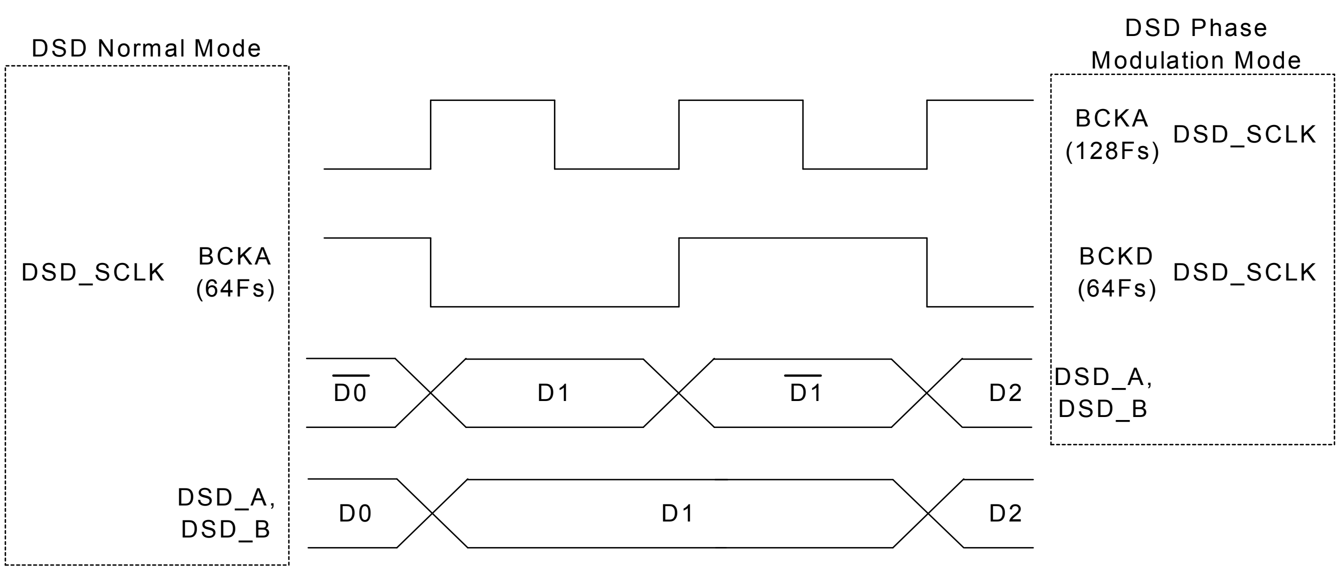

Figure 14. DSD Phase Modulation Mode Diagram