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CS43L21

Low-Power, Stereo Digital-to-Analog Converter

FEATURES

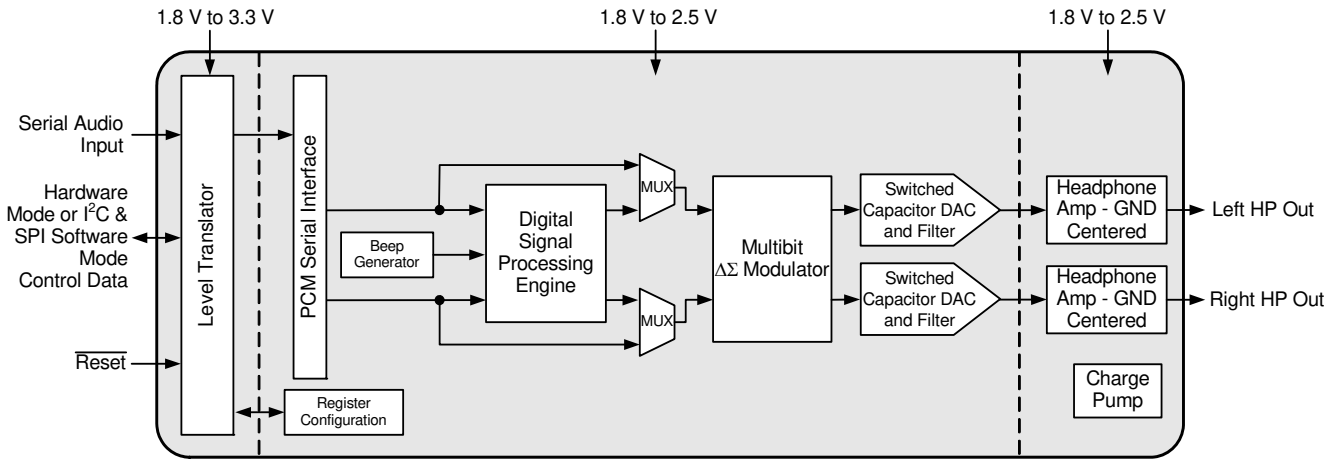
- 98 dB dynamic range (A-weighted)
- -86 dB THD+N
- Headphone amplifier–GND centered
  - On-chip charge pump provides -VA_HP
  - No DC-blocking capacitor required
  - 46 mW power into stereo 16 Ω @ 1.8 V
  - 88 mW power into stereo 16 Ω @ 2.5 V
  - -75 dB THD+N
- Digital signal processing engine
  - Bass and treble tone control, de-emphasis
  - PCM mix with independent volume control
  - Master digital volume control and limiter
  - Soft-ramp and zero-cross transitions
- Beep generator
  - Tone selections across two octaves
  - Separate volume control
  - Programmable On and Off time intervals
  - Continuous, periodic, or one-shot beep selections
- Programmable peak-detect and limiter
- Pop and click suppression

SYSTEM FEATURES

- 24-bit Conversion
- 4- to 96-kHz sample rate
- Multibit delta–sigma architecture
- Low power operation
  - Stereo playback: 12.93 mW @ 1.8 V
- Variable power supplies
  - 1.8- to 2.5-V digital and analog
  - 1.8- to 3.3-V interface logic
- Power-down management
- Software Mode (I²C™ and SPI™ control)
- Hardware mode (standalone control)
- Digital routing/mixes:
  - Mono mixes
- Flexible clocking options
  - Master or slave operation
  - High-impedance digital output option (for easy MUXing between DAC and other data sources)
  - Quarter-speed mode (allows 8-kHz Fs while maintaining a flat noise floor up to 16 kHz)

APPLICATIONS

- Portable audio players
- MD players
- PDAs
- Personal media players
- Portable game consoles
- Smart phones
- Wireless headsets



GENERAL DESCRIPTION

The CS43L21 is a highly integrated, 24-bit, 96 kHz, low power stereo DAC. Based on multi-bit, delta-sigma modulation, it allows infinite sample rate adjustment between 4 kHz and 96 kHz. The DAC offers many features suitable for low power, portable system applications.

The DAC output path includes a digital signal processing engine. Tone Control provides bass and treble adjustment of four selectable corner frequencies. The Mixer allows independent volume control for PCM mix, as well as a master digital volume control for the analog output. All volume level changes may be configured to occur on soft ramp and zero cross transitions. The DAC also includes de-emphasis, limiting functions and a beep generator delivering tones selectable across a range of two full octaves.

The stereo headphone amplifier is powered from a separate positive supply and the integrated charge pump provides a negative supply. This allows a ground-centered analog output with a wide signal swing and eliminates external DC-blocking capacitors.

In addition to its many features, the CS43L21 operates from a low-voltage analog and digital core, making this DAC ideal for portable systems that require extremely low power consumption in a minimal amount of space.

The CS43L21 is available in a 32-pin QFN package in both Commercial (-10 to +70° C) and Automotive grades (-40 to +85° C). The CS43L21 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please see “Ordering Information” on page 64 for complete details.

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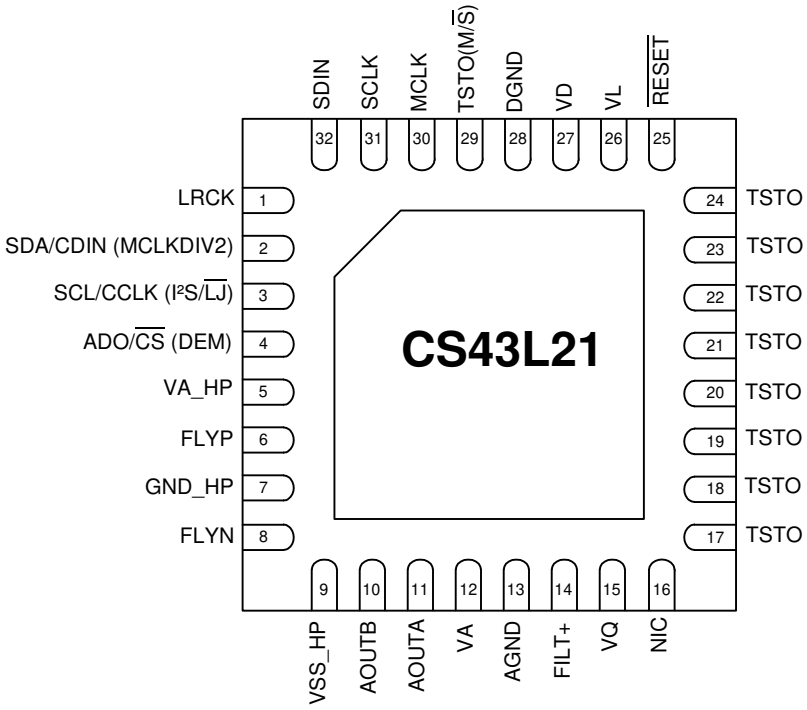
1. PIN DESCRIPTIONS - SOFTWARE (HARDWARE) MODE



Pin Name	#	Pin Description
LRCK	1	**Left Right Clock** (*Input/Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
SDA/CDIN (MCLKDIV2)	2	**Serial Control Data** (*Input/Output*) - SDA is a data I/O in I²C Mode. CDIN is the input data line for the control port interface in SPI Mode.
		MCLK Divide by 2 (*Input*) - Hardware Mode: Divides the MCLK by 2 prior to all internal circuitry.
SCL/CCLK (I²S/LJ)	3	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port.
		Interface Format Selection (*Input*) - Hardware Mode: Selects between I²S & Left-Justified interface formats for the DAC.
AD0/CS (DEM)	4	**Address Bit 0 (I²C) / Control Port Chip Select (SPI)** (*Input*) - AD0 is a chip address pin in I²C Mode; CS is the chip-select signal for SPI format.
		De-Emphasis *(Input)* - Hardware Mode: Enables/disables the de-emphasis filter.
VA_HP	5	**Analog Power For Headphone** *(Input)* **-** Positive power for the internal analog headphone section.
FLYP	6	**Charge Pump Cap Positive Node** *(Input)* **-** Positive node for the external charge pump capacitor.
GND_HP	7	**Analog Ground** (*Input*) - Ground reference for the internal headphone/charge pump section.
FLYN	8	**Charge Pump Cap Negative Node** *(Input)* **-** Negative node for the external charge pump capacitor.
VSS_HP	9	**Negative Voltage From Charge Pump** *(Output)* **-** Negative voltage rail for the internal analog headphone section.

AOUTB AOUTA	10 11	**Analog Audio Output** (*Output*) - The full-scale output level is specified in the DAC Analog Characteristics specification table
VA	12	**Analog Power** (*Input*) - Positive power for the internal analog section.
AGND	13	**Analog Ground** (*Input*) - Ground reference for the internal analog section.
FILT+	14	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.
VQ	15	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage.
NIC	16	**Not Internally Connected -** This pin is not connected internal to the device and may be connected to ground or left "floating". No other external connection should be made to this pin.
TSTO	17	**Test Out** (*Output*) - This pin is an output used for test purposes only and must be left "floating" (no connection external to the pin).
TSTO	18	**Test Out** (*Output*) - This pin is an output used for test purposes only and must be left "floating" (no connection external to the pin).
TSTO	19	**Test Out** (*Output*) - This pin is an output used for test purposes only and must be left "floating" (no connection external to the pin).
TSTO	20	**Test Out** (*Output*) - This pin is an output used for test purposes only and must be left "floating" (no connection external to the pin).
TSTO	21 22	**Test Out** (*Output*) - This pin is an output used for test purposes only and must be left "floating" (no connection external to the pin).
TSTO	23 24	**Test Out** (*Output*) - This pin is an output used for test purposes only and must be left "floating" (no connection external to the pin).
$\overline{\text{RESET}}$	25	**Reset** (*Input*) - The device enters a low power mode when this pin is driven low.
VL	26	**Digital Interface Power** (*Input*) - Determines the required signal level for the serial audio interface and host control port. Refer to the Recommended Operating Conditions for appropriate voltages.
VD	27	**Digital Power** (*Input*) - Positive power for the internal digital section.
DGND	28	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
TSTO (M/$\overline{\text{S}}$)	29	**Test Out** (*Output*) - This pin is an output used for test purposes only and must be left "floating" (no connection external to the pin). **Serial Port Master/Slave** (*Input/Output*) - Hardware Mode Startup Option: Selects between Master and Slave Mode for the serial port.
MCLK	30	**Master Clock** (*Input*) - Clock source for the delta-sigma modulators.
SCLK	31	**Serial Clock** *(Input/Output*) - Serial clock for the serial audio interface.
SDIN	32	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
Thermal Pad	-	Thermal relief pad for optimized heat dissipation. See "QFN Thermal Pad" on page 60.

1.1 Digital I/O Pin Characteristics

The logic level for each input should not exceed the maximum ratings for the VL power supply.

Pin Name SW/(HW)	I/O	Driver	Receiver
$\overline{\text{RESET}}$	Input	-	1.8 V - 3.3 V
SCL/CCLK (I²S/$\overline{\text{LJ}}$)	Input	-	1.8 V - 3.3 V, with Hysteresis
SDA/CDIN (MCLKDIV2)	Input/Output	1.8 V - 3.3 V, CMOS/Open Drain	1.8 V - 3.3 V, with Hysteresis
AD0/$\overline{\text{CS}}$ (DEM)	Input	-	1.8 V - 3.3 V
MCLK	Input	-	1.8 V - 3.3 V
LRCK	Input/Output	1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V
SCLK	Input/Output	1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V
TSTO (M/$\overline{\text{S}}$)	Input/Output	1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V
SDIN	Input	-	1.8 V - 3.3 V

Table 1. I/O Power Rails

2. TYPICAL CONNECTION DIAGRAMS

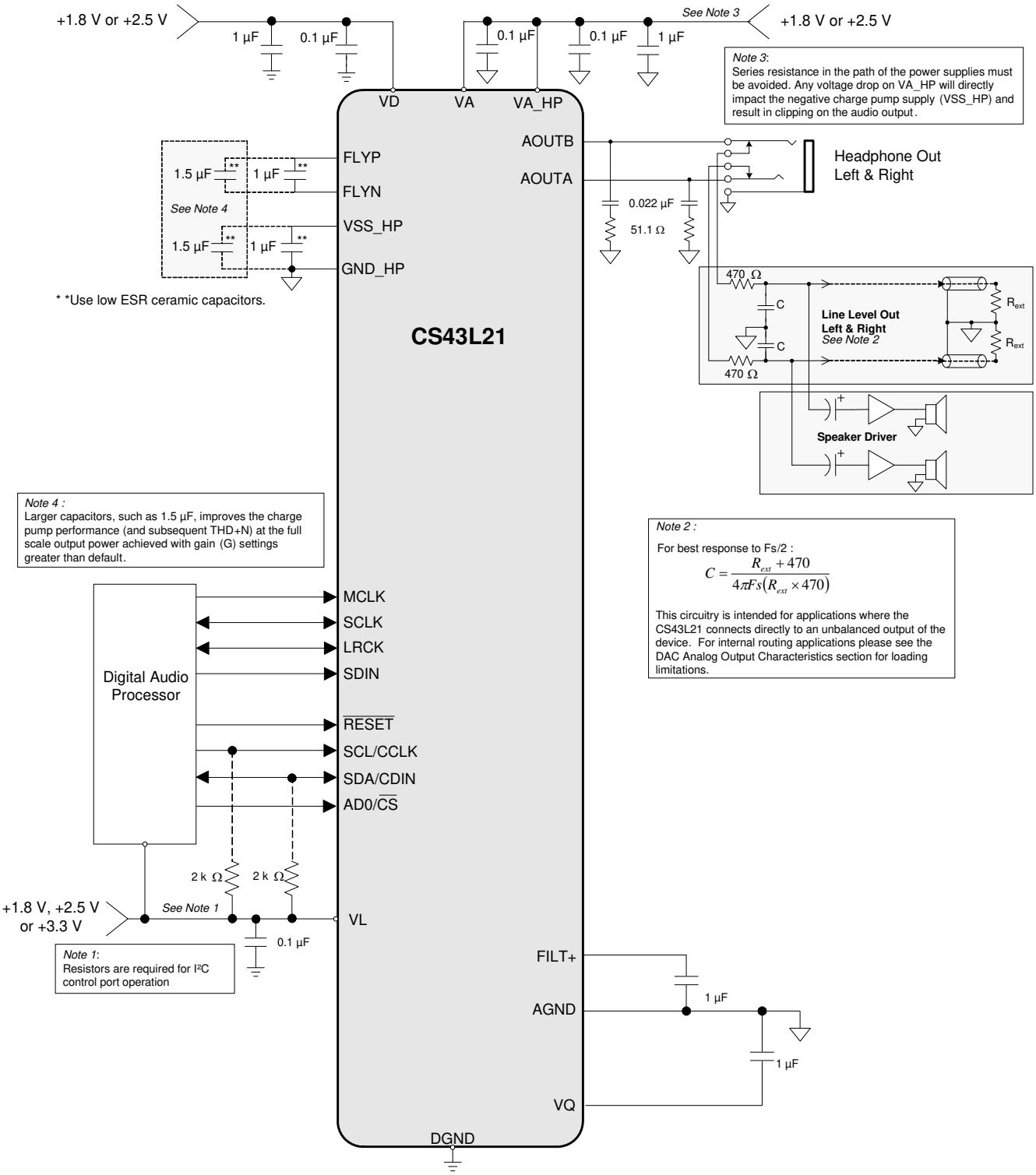


Figure 1. Typical Connection Diagram (Software Mode)

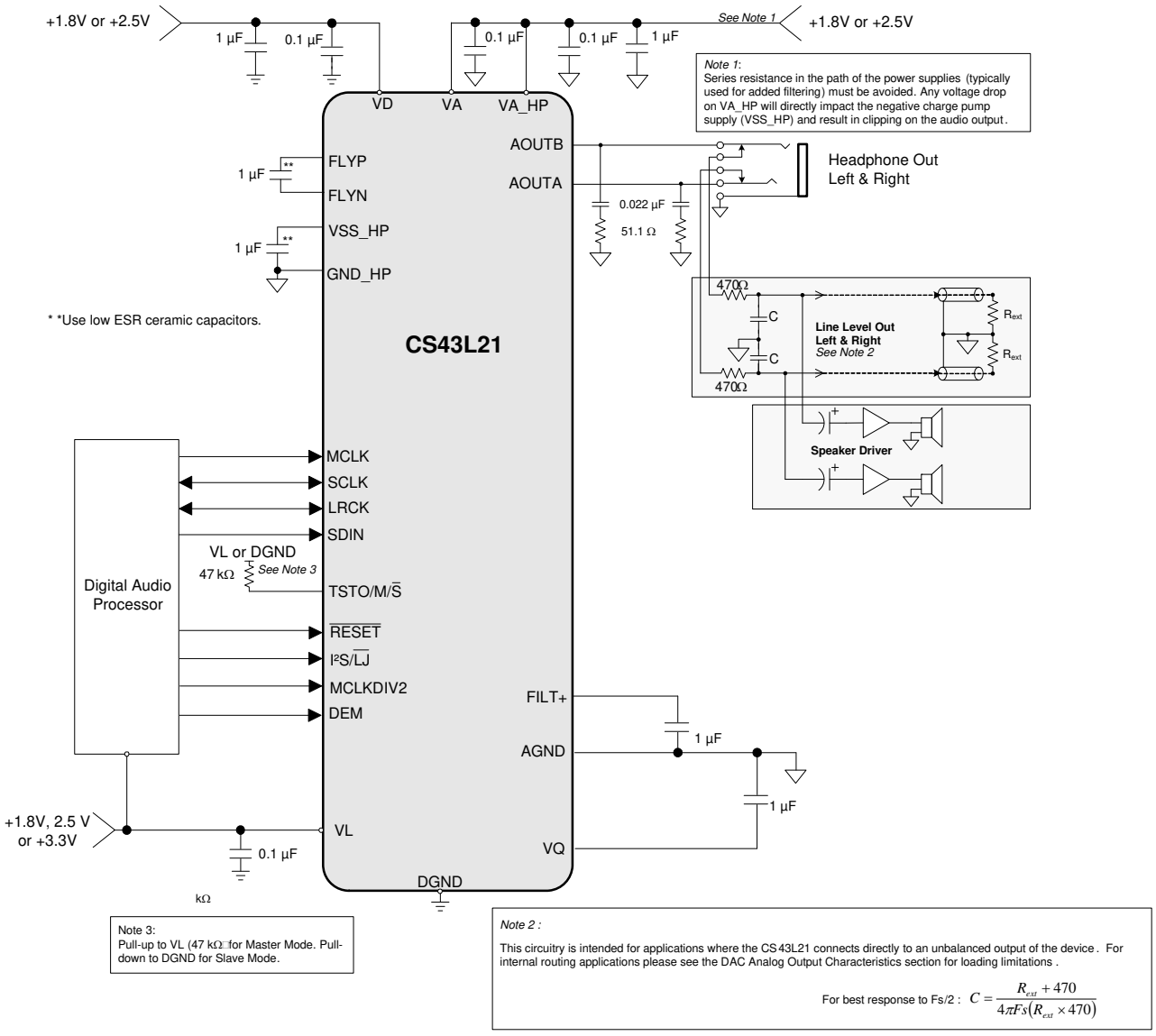


Figure 2. Typical Connection Diagram (Hardware Mode)

3. CHARACTERISTIC AND SPECIFICATION TABLES

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25° C.)

SPECIFIED OPERATING CONDITIONS

(AGND=DGND=0 V, all voltages with respect to ground.)

Parameters	Symbol	Min	Max	Units
DC Power Supply (Note 1)				
Analog Core	VA	1.65	2.63	V
Headphone Amplifier	VA_HP	1.65	2.63	V
Digital Core	VD	1.65	2.63	V
Serial/Control Port Interface	VL	1.65	3.47	V
Ambient Temperature Commercial - CNZ Automotive - DNZ	T_A	-10 -40	+70 +85	°C °C

ABSOLUTE MAXIMUM RATINGS

(AGND = DGND = 0 V; all voltages with respect to ground.)

Parameters	Symbol	Min	Max	Units
DC Power Supply Analog Digital Serial/Control Port Interface	VA, VA_HP VD VL	-0.3 -0.3 -0.3	3.0 3.0 4.0	V V V
Input Current (Note 2)	I_{in}	-	±10	mA
External Voltage Applied to Analog Output	V_{IN}	-VA_HP - 0.3	+VA_HP + 0.3	V
External Voltage Applied to Digital Input (Note 3)	V_{IND}	-0.3	VL+ 0.3	V
Ambient Operating Temperature (power applied)	T_A	-50	+115	°C
Storage Temperature	T_{stg}	-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:

1. The device will operate properly over the full range of the analog, headphone amplifier, digital core and serial/control port interface supplies.
2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.
3. The maximum over/under voltage is limited by the input current.

ANALOG OUTPUT CHARACTERISTICS (COMMERCIAL - CNZ)

(Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; Sample Frequency = 48 kHz; test load R_L = 10 kΩ, C_L = 10 pF for the line output (see Figure 3), and test load R_L = 16 Ω, C_L = 10 pF (see Figure 3) for the headphone output. HP_GAIN[2:0] = 011.)

Parameter (Note 4)		**VA = 2.5V** (nominal) Min	Typ	Max	**VA = 1.8V** (nominal) Min	Typ	Max	Unit
R_L = 10 kΩ								
Dynamic Range								
18 to 24-Bit	A-weighted	92	98	-	89	95	-	dB
	unweighted	89	95	-	86	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-86	-78	-	-88	-82	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-	-	-32	-	dB
16-Bit	0 dB	-	-86	-	-	-88	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
R_L = 16 Ω								
Dynamic Range								
18 to 24-Bit	A-weighted	92	98	-	89	95	-	dB
	unweighted	89	95	-	86	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-75	-69	-	-75	-69	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-	-	-32	-	dB
16-Bit	0 dB	-	-75	-	-	-75	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
Other Characteristics for R_L = 16 Ω or 10 kΩ								
Output Parameters (Note 5)	Modulation Index (MI)	-	0.6787	-	-	0.6787	-	
	Analog Gain Multiplier (G)		0.6047			0.6047		
Full-scale Output Voltage (2•G•MI•VA) (Note 5)		Refer to Table "Line Output Voltage Characteristics" on page 14						Vpp
Full-scale Output Power (Note 5)		Refer to Table "Headphone Output Power Characteristics" on page 15						mW
Interchannel Isolation (1 kHz)	16 Ω	-	80	-	-	80	-	dB
	10 kΩ	-	95	-	-	93	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
AC-Load Resistance (R_L)	(Note 6)	16	-	-	16	-	-	Ω
Load Capacitance (C_L)	(Note 6)	-	-	150	-	-	150	pF

ANALOG OUTPUT CHARACTERISTICS (AUTOMOTIVE - DNZ)

(Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; Sample Frequency = 48 kHz and 96 kHz; test load R_L = 10 kΩ, C_L = 10 pF for the line output (see Figure 3), and test load R_L = 16 Ω, C_L = 10 pF (see Figure 3) for the headphone output. HP_GAIN[2:0] = 011.)

Parameter (Note 4)		**VA = 2.5V** (nominal) Min	Typ	Max	**VA = 1.8V** (nominal) Min	Typ	Max	Unit
R_L = 10 kΩ								
Dynamic Range								
18 to 24-Bit	A-weighted	90	98	-	87	95	-	dB
	unweighted	87	95	-	84	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-86	-73	-	-88	-80	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-	-	-32	-	dB
16-Bit	0 dB	-	-86	-	-	-88	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
R_L = 16 Ω								
Dynamic Range								
18 to 24-Bit	A-weighted	90	98	-	87	95	-	dB
	unweighted	87	95	-	84	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-75	-67	-	-75	-67	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-	-	-32	-	dB
16-Bit	0 dB	-	-75	-	-	-75	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
Other Characteristics for R_L = 16 Ω or 10 kΩ								
Output Parameters (Note 5)	Modulation Index (MI)	-	0.6787	-	-	0.6787	-	
	Analog Gain Multiplier (G)		0.6047			0.6047		
Full-scale Output Voltage (2•G•MI•VA) (Note 5)		*Refer to Table* "Line Output Voltage Characteristics" on page 14						Vpp
Full-scale Output Power (Note 5)		*Refer to Table* "Headphone Output Power Characteristics" on page 15						mW
Interchannel Isolation (1 kHz)	16 Ω	-	80	-	-	80	-	dB
	10 kΩ	-	95	-	-	93	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
AC-Load Resistance (R_L)	(Note 6)	16	-	-	16	-	-	Ω
Load Capacitance (C_L)	(Note 6)	-	-	150	-	-	150	pF

LINE OUTPUT VOLTAGE CHARACTERISTICS

Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; Sample Frequency = 48 kHz; test load R_L = 10 kΩ, C_L = 10 pF (see Figure 3).

Parameter			VA = 2.5V (nominal)			VA = 1.8V (nominal)			Unit
			Min	Typ	Max	Min	Typ	Max	
AOUTx Voltage Into R_L = 10 kΩ									
HP_GAIN[2:0]	Analog Gain (G)	VA_HP							
000	0.3959	1.8 V	-	1.34	-	-	0.97	-	V_{pp}
		2.5 V	-	1.34	-	-	0.97	-	V_{pp}
001	0.4571	1.8 V	-	1.55	-	-	1.12	-	V_{pp}
		2.5 V	-	1.55	-	-	1.12	-	V_{pp}
010	0.5111	1.8 V	-	1.73	-	-	1.25	-	V_{pp}
		2.5 V	-	1.73	-	-	1.25	-	V_{pp}
011 (default)	0.6047	1.8 V	-	2.05	-	1.41	1.48	1.55	V_{pp}
		2.5 V	1.95	2.05	2.15	-	1.48	-	V_{pp}
100	0.7099	1.8 V	-	2.41	-	-	1.73	-	V_{pp}
		2.5 V	-	2.41	-	-	1.73	-	V_{pp}
101	0.8399	1.8 V	-	2.85	-		2.05		V_{pp}
		2.5 V	-	2.85	-	-	2.05	-	V_{pp}
110	1.0000	1.8 V	-	3.39	-	-	2.44	-	V_{pp}
		2.5 V	-	3.39	-	-	2.44	-	V_{pp}
111	1.1430	1.8 V	(See (Note 7)				2.79		V_{pp}
		2.5 V	-	3.88	-	-	2.79	-	V_{pp}

HEADPHONE OUTPUT POWER CHARACTERISTICS

Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; Sample Frequency = 48 kHz; test load R_L = 16 Ω, C_L = 10 pF (see Figure 3).

Parameter			VA = 2.5V (nominal)			VA = 1.8V (nominal)			Unit
			Min	Typ	Max	Min	Typ	Max	
AOUTx Power Into R_L = 16 Ω									
HP_GAIN[2:0]	Analog Gain (G)	VA_HP							
000	0.3959	1.8 V	-	14	-	-	7	-	mW_{rms}
		2.5 V	-	14	-	-	7	-	mW_{rms}
001	0.4571	1.8 V	-	19	-	-	10	-	mW_{rms}
		2.5 V	-	19	-	-	10	-	mW_{rms}
010	0.5111	1.8 V	-	23	-	-	12	-	mW_{rms}
		2.5 V	-	23	-	-	12	-	mW_{rms}
011 (default)	0.6047	1.8 V		(Note 7)		-	17	-	mW_{rms}
		2.5 V	-	32	-	-	17	-	mW_{rms}
100	0.7099	1.8 V		(Note 7)		-	23	-	mW_{rms}
		2.5 V	-	44	-	-	23	-	mW_{rms}
101	0.8399	1.8 V					(Note 5)		mW_{rms}
		2.5 V				-	32	-	mW_{rms}
110	1.0000	1.8 V							mW_{rms}
		2.5 V							mW_{rms}
111	1.1430	1.8 V							mW_{rms}
		2.5 V							mW_{rms}

(Note 5, 7)

4. One LSB of triangular PDF dither is added to data.
5. Full-scale output voltage and power is determined by the gain setting, G, in register "Headphone Analog Gain (HP_GAIN[2:0])" on page 42. High gain settings at certain VA and VA_HP supply levels may cause clipping when the audio signal approaches full-scale, maximum power output, as shown in Figures 21 - 24 on page 56.
6. See Figure 3. R_L and C_L reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. In this circuit topology, C_L will effectively move the band-limiting pole of the amp in the output stage. Increasing this value beyond the recommended 150 pF can cause the internal op-amp to become unstable.
7. VA_HP settings lower than VA reduces the headroom of the headphone amplifier. As a result, the DAC may not achieve the full THD+N performance at full-scale output voltage and power.

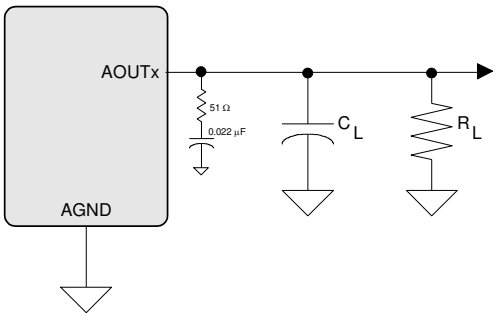


Figure 3. Headphone Output Test Load

COMBINED DAC INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

Parameter (Note 8)		Min	Typ	Max	Unit
Frequency Response 10 Hz to 20 kHz		-0.01	-	+0.08	dB
Passband	to -0.05 dB corner to -3 dB corner	0 0	- -	0.4780 0.4996	Fs Fs
StopBand		0.5465	-	-	Fs
StopBand Attenuation (Note 9)		50	-	-	dB
Group Delay		-	10.4/Fs	-	s
De-emphasis Error	Fs = 32 kHz Fs = 44.1 kHz Fs = 48 kHz	- - -	- - -	+1.5/+0 +0.05/-0.25 -0.2/-0.4	dB dB dB

Notes:

8. Response is clock dependent and will scale with Fs. Note that the response plots (Figure 27 to Figure 30 on page 61) have been normalized to Fs and can be denormalized by multiplying the X-axis scale by Fs.
9. Measurement Bandwidth is from Stopband to 3 Fs.

SWITCHING SPECIFICATIONS - SERIAL PORT

(Inputs: Logic 0 = DGND, Logic 1 = VL.)

Parameters		Symbol	Min	Max	Units
$\overline{\text{RESET}}$ pin Low Pulse Width (Note 10)			1	-	ms
MCLK Frequency			1.024	38.4	MHz
MCLK Duty Cycle (Note 11)			45	55	%
Slave Mode					
Input Sample Rate (LRCK)	Quarter-Speed Mode Half-Speed Mode Single-Speed Mode Double-Speed Mode	F_s F_s F_s F_s	4 8 4 50	12.5 25 50 100	kHz kHz kHz kHz
LRCK Duty Cycle			45	55	%
SCLK Frequency		$1/t_P$	-	$64 \cdot F_s$	Hz
SCLK Duty Cycle			45	55	%
LRCK Setup Time Before SCLK Rising Edge		$t_{s(LK-SK)}$	40	-	ns
SDIN Setup Time Before SCLK Rising Edge		$t_{s(SD-SK)}$	20	-	ns
SDIN Hold Time After SCLK Rising Edge		t_h	20	-	ns

Parameters		Symbol	Min	Max	Units
Master Mode (Note 12)					
Output Sample Rate (LRCK)	All Speed Modes (Note 13)	F_s	-	$\frac{MCLK}{128}$	Hz
LRCK Duty Cycle			45	55	%
SCLK Frequency		$1/t_P$	-	$64 \cdot F_s$	Hz
SCLK Duty Cycle			45	55	%
LRCK Edge to SDIN MSB Rising Edge		$t_{d(MSB)}$		52	ns
SDIN Setup Time Before SCLK Rising Edge		$t_{s(SD-SK)}$	20	-	ns
SDIN Hold Time After SCLK Rising Edge		t_h	20	-	ns

10. After powering up the CS43L21, $\overline{\text{RESET}}$ should be held low after the power supplies and clocks are settled.
11. See "Example System Clock Frequencies" on page 58 for typical MCLK frequencies.
12. See"Master" on page 29.
13. "MCLK" refers to the external master clock applied.

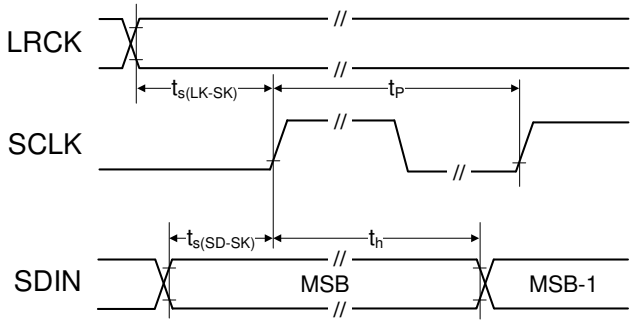


Figure 4. Serial Audio Interface Slave Mode Timing

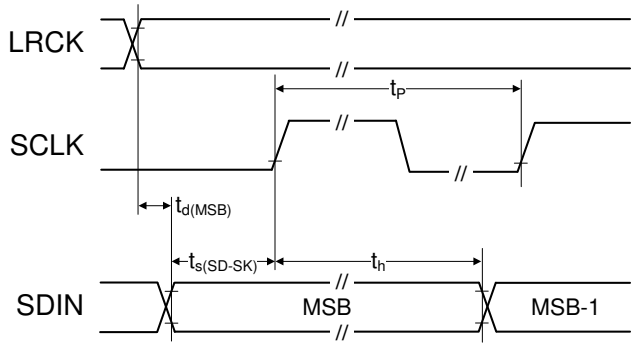


Figure 5. Serial Audio Interface Master Mode Timing

SWITCHING SPECIFICATIONS - I²C CONTROL PORT

(Inputs: Logic 0 = DGND, Logic 1 = VL, SDA C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{\text{RESET}}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 14)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}	-	1	µs
Fall Time SCL and SDA	t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	3450	ns

14. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

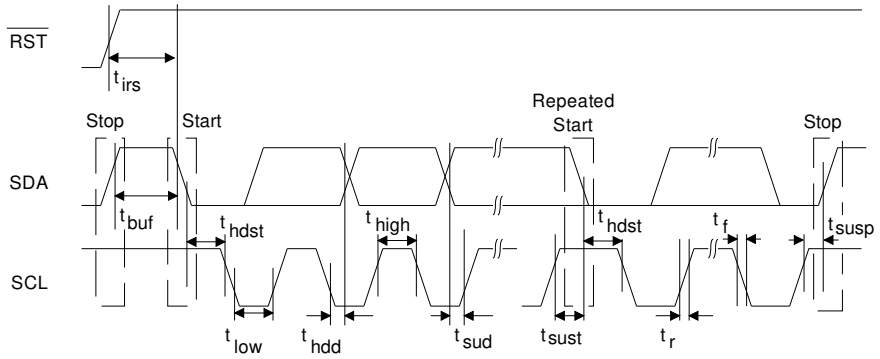


Figure 6. Control Port Timing - I²C

SWITCHING CHARACTERISTICS - SPI CONTROL PORT

(Inputs: Logic 0 = DGND, Logic 1 = VL)

Parameter		Symbol	Min	Max	Units
CCLK Clock Frequency		f_{sck}	0	6.0	MHz
$\overline{\text{RESET}}$ Rising Edge to $\overline{\text{CS}}$ Falling		t_{srs}	20	-	ns
$\overline{\text{CS}}$ Falling to CCLK Edge		t_{css}	20	-	ns
$\overline{\text{CS}}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 15)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN	(Note 16)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 16)	t_{f2}	-	100	ns

15. Data must be held for sufficient time to bridge the transition time of CCLK.
16. For f_{sck} <1 MHz.

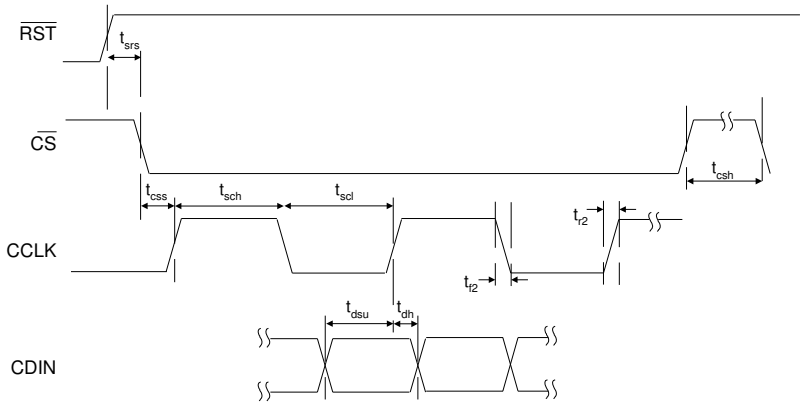


Figure 7. Control Port Timing - SPI Format

DC ELECTRICAL CHARACTERISTICS

(AGND = 0 V; all voltages with respect to ground.)

Parameters		Min	Typ	Max	Units
VQ Characteristics					
Nominal Voltage		-	0.5•VA	-	V
Output Impedance		-	23	-	kΩ
DC Current Source/Sink (Note 17)		-	-	10	µA
FILT+		-	VA	-	V
VSS_HP Characteristics					
Nominal Voltage		-	-0.8•(VA_HP)	-	V
DC Current Source		-		10	µA
Power Supply Rejection Ratio (PSRR) (Note 18)	1 kHz	-	60	-	dB

17. The DC current draw represents the allowed current draw from the VQ pin due to typical leakage through electrolytic de-coupling capacitors.
18. Valid with the recommended capacitor values on FILT+ and VQ. Increasing the capacitance will also increase the PSRR.

DIGITAL INTERFACE SPECIFICATIONS & CHARACTERISTICS

Parameters (Note 19)	Symbol	Min	Max	Units
Input Leakage Current	I_{in}	-	±10	µA
Input Capacitance		-	10	pF
1.8 V - 3.3 V Logic				
High-Level Output Voltage (I_{OH} = -100 µA)	V_{OH}	VL - 0.2	-	V
Low-Level Output Voltage (I_{OL} = 100 µA)	V_{OL}	-	0.2	V
High-Level Input Voltage	V_{IH}	0.68•VL	-	V
Low-Level Input Voltage	V_{IL}	-	0.32•VL	V

19. See “Digital I/O Pin Characteristics” on page 8 for serial and control port power rails.

POWER CONSUMPTION

See (Note 20)

	Operation	Power Control Registers										Typical Current (mA)				
		02h							03h							
		PDN_DACB	PDN_DACA	BIT 4	BIT 3	BIT 2	BIT 1	PDN	BIT 3	BIT 2	BIT 1	V	i_{VA_HP}	i_{VA}	i_{VD}	i_{VL} (Note 23)	**Total Power (mW_{rms})**
1	Off (Note 21)	x	x	x	x	x	x	x	x	x	x	1.8	0	0	0	0	0
												2.5	0	0	0	0	0
2	Standby (Note 22)	x	x	x	x	x	x	1	x	x	x	1.8	0	0.01	0.02	0	0.05
												2.5	0	0.01	0.03	0	0.10
5	Mono Playback	1	0	1	1	1	1	0	1	1	1	1.8	1.66	1.40	2.35	0.01	9.74
												2.5	2.03	1.71	3.48	0.02	18.08
6	Stereo Playback	0	0	1	1	1	1	0	1	1	1	1.8	2.77	2.05	2.35	0.01	12.93
												2.5	3.21	2.50	3.49	0.02	23.02

20. Unless otherwise noted, test conditions are as follows: All zeros input, slave mode, sample rate = 48 kHz; No load. Digital (VD) and logic (VL) supply current will vary depending on speed mode and master/slave operation.
21. $\overline{\text{RESET}}$ pin 25 held LO, all clocks and data lines are held LO.
22. $\overline{\text{RESET}}$ pin 25 held HI, all clocks and data lines are held HI.
23. VL current will slightly increase in master mode.

4. APPLICATIONS

4.1 Overview

4.1.1 Architecture

The CS43L21 is a highly integrated, low power, 24-bit audio D/A comprised of stereo digital-to-analog converters (DAC) designed using multi-bit delta-sigma techniques. The DAC operates at an oversampling ratio of 128 Fs. The D/A operates in one of four sample rate speed modes: Quarter, Half, Single and Double. It accepts and is capable of generating serial port clocks (SCLK, LRCK) derived from an input Master Clock (MCLK).

4.1.2 Line & Headphone Outputs

The analog output portion of the D/A includes a headphone amplifier capable of driving headphone and line-level loads. An on-chip charge pump creates a negative headphone supply allowing a full-scale output swing centered around ground. This eliminates the need for large DC-Blocking capacitors and allows the amplifier to deliver more power to headphone loads at lower supply voltages. Eight gain settings for the headphone amplifier are available.

4.1.3 Signal Processing Engine

A signal processing engine is available to process serial input D/A data before output to the DAC. The D/A data has independent volume controls and mixing functions such as mono mixes and left/right channel swaps. A Tone Control provides bass and treble at four selectable corner frequencies. An automatic level control provides limiting capabilities at programmable attack and release rates, maximum thresholds and soft ramping. A 15/50 μs de-emphasis filter is also available at a 44.1 kHz sample rate.

4.1.4 Beep Generator

A beep may be generated internally at select frequencies across approximately two octave major scales and configured to occur continuously, periodically or at single time intervals controlled by the user. Volume may be controlled independently.

4.1.5 Device Control (Hardware or Software Mode)

In Software Mode, all functions and features may be controlled via a two-wire I²C or three-wire SPI control port interface. In Hardware Mode, a limited feature set may be controlled via stand-alone control pins.

4.1.6 Power Management

Two Software Mode control registers provide independent power-down control of the DAC, allowing operation in select applications with minimal power consumption.

4.2 Hardware Mode

A limited feature-set is available when the D/A powers up in Hardware Mode (see "Recommended Power-Up Sequence" section on page 31) and may be controlled via stand-alone control pins. Table 2 shows a list of functions/features, the default configuration and the associated stand-alone control available.

Hardware Mode Feature/Function Summary				
Feature/Function		**Default Configuration**	**Stand-Alone Control**	**Note**
Power Control	Device DACx	Powered Up Powered Up	-	-
Auto-Detect		Enabled	-	-
Speed Mode	Serial Port Slave Serial Port Master	Auto-Detect Speed Mode Single-Speed Mode	-	-
MCLK Divide		(Selectable)	"MCLKDIV2" pin 2	see Section 4.4 on page 28
Serial Port Master / Slave Selection		(Selectable)	"M/$\overline{S}$" pin 29	see Section 4.4 on page 28
Interface Control	DAC	(Selectable)	"I²S/$\overline{LJ}$" pin 3	see Section 4.5 on page 30
DAC Volume & Gain	HP Gain AOUTx Volume Invert Soft Ramp Zero Cross	G = 0.6047 0 dB Disabled Enabled Disabled	-	-
DAC De-Emphasis		(Selectable)	"DEM" pin 4	see Section on page 24
Signal Processing Engine (SPE)	Mix Beep Tone Control Peak Detect and Limiter	Disabled Disabled Disabled Disabled	-	-
Data Selection		Data Input (PCM) to DAC	-	-
Channel Mix	DAC	PCMA = L; PCMB = R	-	-
Charge Pump Frequency		(64xFs)/7	-	-

Table 2. Hardware Mode Feature Summary

4.3 Analog Outputs

AOUTA and AOUTB are the ground-centered line or headphone outputs. Various signal processing options are available, including an internal Beep Generator. The desired path to the DAC must be selected using the DATA_SEL[1:0] bits.

Software Controls:	"DAC Control (Address 09h)" on page 43.

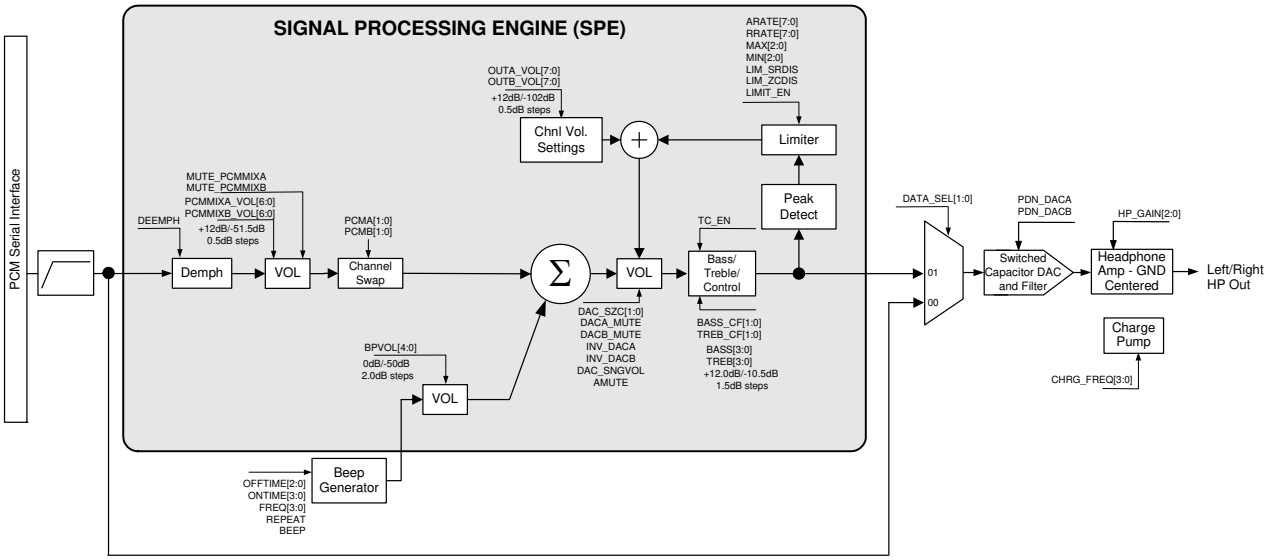


Figure 8. Output Architecture

4.3.1 *De-Emphasis Filter*

The device includes on-chip digital de-emphasis optimized for a sample rate of 44.1 kHz. The filter response is shown in Figure 9. The de-emphasis feature is included to accommodate audio recordings that utilize 50/15 µs pre-emphasis equalization as a means of noise reduction. De-emphasis is only available in Single-Speed Mode.

Software Controls:	"DAC Control (Address 09h)" on page 43.		
Hardware Control:	Pin	Setting	Selection
	"DEM" pin 4.	LO	No De-Emphasis
		HI	De-Emphasis Applied

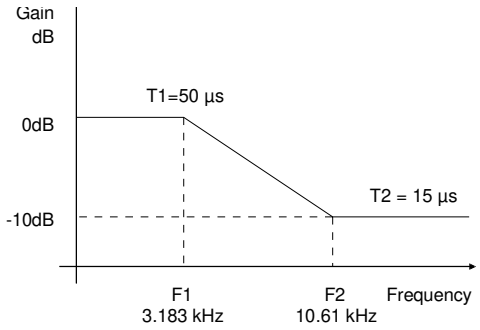


Figure 9. De-Emphasis Curve

4.3.2 Volume Controls

Two digital volume control functions offer independent control of the SDIN signal path into the mixer as well as a combined control of the mixed signals. The volume controls are programmable to ramp in increments of 0.125 dB at a rate controlled by the soft ramp/zero cross settings.

The signal paths may also be muted via mute control bits. When enabled, each bit attenuates the signal to its maximum value. When the mute bit is disabled, the signal returns to the attenuation level set in the respective volume control register. The attenuation is ramped up and down at the rate specified by the DAC_SZC[1:0] bits.

Software Controls:	“PCMX Mixer Volume Control: PCMA (Address 10h) & PCMB (Address 11h)” on page 45“AOUTx Volume Control: AOUTA (Address 16h) & AOUTB (Address 17h)” on page 49“DAC Output Control (Address 08h)” on page 42

4.3.3 Mono Channel Mixer

A channel mixer may be used to create a mix of the left and right channels for the SDIN data. This mix allows the user to produce a MONO signal from a stereo source. The mixer may also be used to implement a left/right channel swap.

Software Controls:	“PCM Channel Mixer (Address 18h)” on page 50.

4.3.4 Beep Generator

The Beep Generator generates audio frequencies across approximately two octave major scales. It offers three modes of operation: Continuous, multiple and single (one-shot) beeps. Sixteen on and eight off times are available.

Note: The Beep is generated before the limiter and may affect desired limiting performance. If the limiter function is used, it may be required to set the Beep volume sufficiently below the threshold to prevent the peak detect from triggering. Since the master volume control, AOUTx_VOL[7:0], will affect the Beep volume, DAC volume may alternatively be controlled using the PCMMIXx_VOL[6:0] bits.

Software Controls:	“Beep Frequency & Timing Configuration (Address 12h)” on page 46, “Beep Off Time & Volume (Address 13h)” on page 46, “Beep Configuration & Tone Configuration (Address 14h)” on page 48