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CS43L22

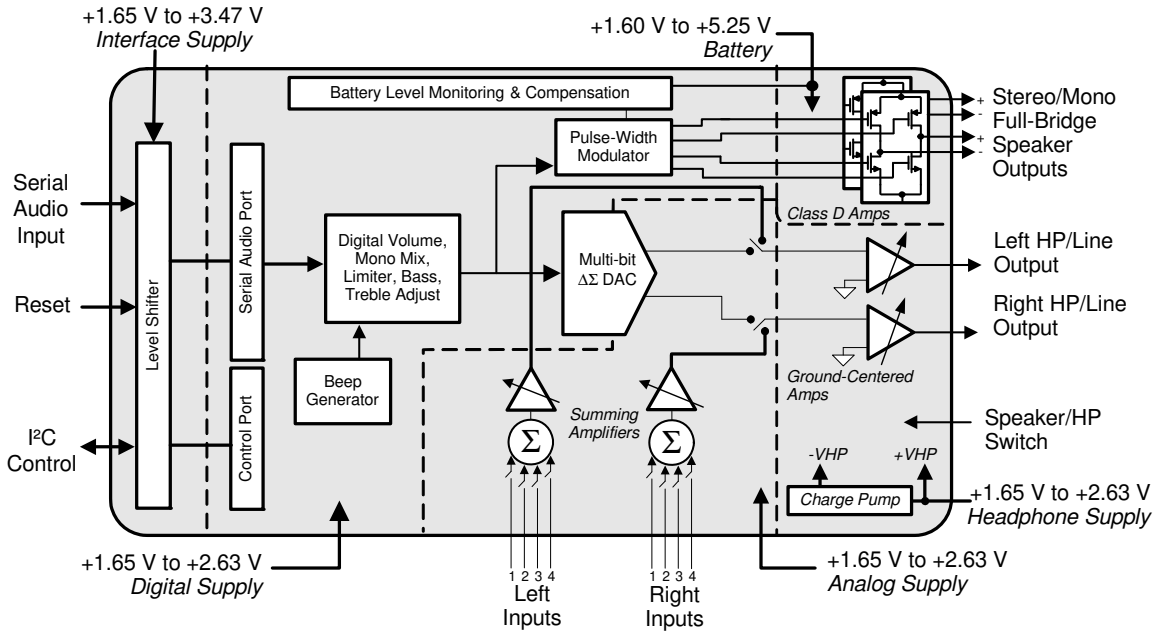
Low Power, Stereo DAC w/Headphone & Speaker Amps

FEATURES

- 98 dB Dynamic Range (A-wtd)
- 88 dB THD+N
- Headphone Amplifier - GND Centered
  - No DC-Blocking Capacitors Required
  - Integrated Negative Voltage Regulator
  - 2 x 23 mW into Stereo 16 Ω @ 1.8 V
  - 2 x 44 mW into Stereo 16 Ω @ 2.5V
- Stereo Analog Input Passthrough Architecture
  - Analog Input Mixing
  - Analog Passthrough with Volume Control
- Digital Signal Processing Engine
  - Bass & Treble Tone Control, De-Emphasis
  - PCM Input w/Independent Vol Control
  - Master Digital Volume Control and Limiter
  - Soft-Ramp & Zero-Cross Transitions
- Programmable Peak-Detect and Limiter
- Beep Generator w/Full Tone Control
  - Tone Selections Across Two Octaves
  - Separate Volume Control
  - Programmable On and Off Time Intervals
  - Continuous, Periodic, One-Shot Beep Selections

Class D Stereo/Mono Speaker Amplifier

- No External Filter Required
- High Stereo Output Power at 10% THD+N
  - 2 x 1.00 W into 8 Ω @ 5.0 V
  - 2 x 550 mW into 8 Ω @ 3.7 V
  - 2 x 230 mW into 8 Ω @ 2.5 V
- High Mono Output Power at 10% THD+N
  - 1 x 1.90 W into 4 Ω @ 5.0 V
  - 1 x 1.00 W into 4 Ω @ 3.7 V
  - 1 x 350 mW into 4 Ω @ 2.5 V
- Direct Battery Powered Operation
  - Battery Level Monitoring & Compensation
- 81% Efficiency at 800 mW
- Phase-Aligned PWM Output Reduces Idle Channel Current
- Spread Spectrum Modulation
- Low Quiescent Current



System Features

- 12, 24, and 27 MHz Master Clock Support in Addition to Typical Audio Clock Rates
- High Performance 24-bit Converters
  - Multi-bit Delta–Sigma Architecture
  - Very Low 64Fs Oversampling Clock Reduces Power Consumption
- Low Power Operation
  - Stereo Analog Passthrough: 10 mW @ 1.8 V
  - Stereo Playback: 14 mW @ 1.8 V
- Variable Power Supplies
  - 1.8 V to 2.5 V Digital & Analog
  - 1.6 V to 5 V Class D Amplifier
  - 1.8 V to 2.5 V Headphone Amplifier
  - 1.8 V to 3.3 V Interface Logic
- Power Down Management
  - DAC, Passthrough Amplifier, Headphone Amplifier, Speaker Amplifier
- Flexible Clocking Options
  - Master or Slave Operation
  - Quarter-Speed Mode - (i.e. allows 8 kHz Fs while maintaining a flat noise floor up to 16 kHz)
  - 4 kHz to 96 kHz Sample Rates
- I^2C^{TM} Control Port Operation
- Headphone/Speaker Detection Input
- Pop and Click Suppression
- Pin-Compatible w/CS42L52

Applications

- PDA's
- Personal Media Players
- Portable Game Consoles

General Description

The CS43L22 is a highly integrated, low power stereo DAC with headphone and Class D speaker amplifiers. The CS43L22 offers many features suitable for low power, portable system applications.

The **DAC output path** includes a digital signal processing engine with various fixed function controls. Tone Control provides bass and treble adjustment of four selectable corner frequencies. Digital Volume controls may be configured to change on soft ramp transitions while the analog controls can be configured to occur on every zero crossing. The DAC also includes de-emphasis, limiting functions and a BEEP generator delivering tones selectable across a range of two full octaves.

The **stereo headphone amplifier** is powered from a separate positive supply and the integrated **charge pump** provides a negative supply. This allows a ground-centered analog output with a wide signal swing and eliminates the need for external DC-blocking capacitors.

The **Class D stereo speaker amplifier** does not require an external filter and provides the high efficiency amplification required by power sensitive portable applications. The speaker amplifier may be powered directly from a battery while the internal DC supply monitoring and compensation provides a constant gain level as the battery's voltage decays.

The CS43L22 accommodates analog routing of the analog input signal directly to the headphone amplifier. This feature is useful in applications that utilize an FM tuner where audio recovered over-the-air must be transmitted to the headphone amplifier directly.

In addition to its many features, the CS43L22 operates from a low voltage analog and digital core making it ideal for portable systems that require extremely low power consumption in a minimal amount of space.

The CS43L22 is available in a 40-pin QFN package in Commercial (-40 to +85 °C) grade. The CS43L22 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please refer to "Ordering Information" on page 66 for complete ordering information.

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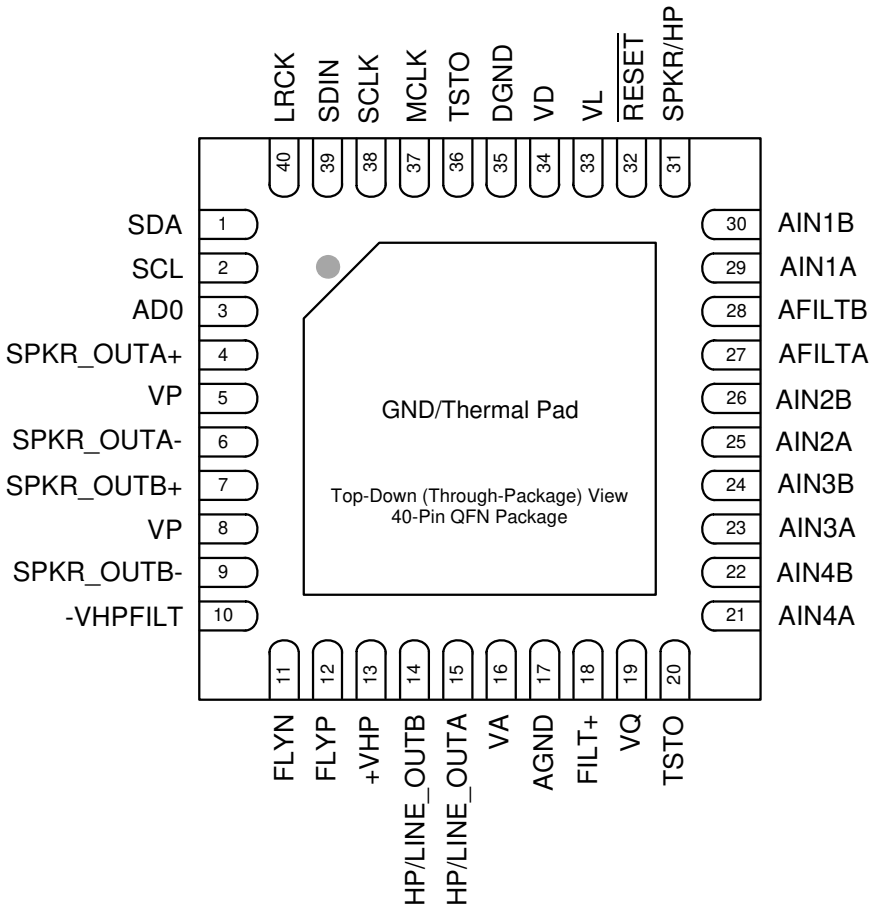
LIST OF FIGURES

1. PIN DESCRIPTIONS



Pin Name	#	Pin Description
SDA	1	**Serial Control Data** (*Input*/*Output*) - SDA is a data I/O in I²C Mode.
SCL	2	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port.
AD0	3	**Address Bit 0 (I²C)** (*Input*) - AD0 is a chip address pin in I²C Mode.
SPKR_OUTA+ SPKR_OUTA- SPKR_OUTB+ SPKR_OUTB-	4 6 7 9	**PWM Speaker Output** (*Output*) - Full-bridge amplified PWM speaker outputs.
VP	5 8	**Power for PWM Drivers** (*Input*) - Power supply for the PWM output driver stages.
-VHPFILT	10	**Inverting Charge Pump Filter Connection** *(Output)* - Power supply from the inverting charge pump that provides the negative rail for the headphone/line amplifiers.
FLYN	11	**Charge Pump Cap Negative Node** *(Output)* - Negative node for the inverting charge pump's flying capacitor.
FLYP	12	**Charge Pump Cap Positive Node** *(Output)* - Positive node for the inverting charge pump's flying capacitor.
+VHP	13	**Positive Analog Power for Headphone** (*Input*) - Positive voltage rail and power for the internal headphone amplifiers and inverting charge pump.
HP/LINE_OUTB, A	14,15	**Headphone/Line Audio Output** (*Output*) - Stereo headphone or line level analog outputs.
VA	16	**Analog Power** (*Input*) - Positive power for the internal analog section.

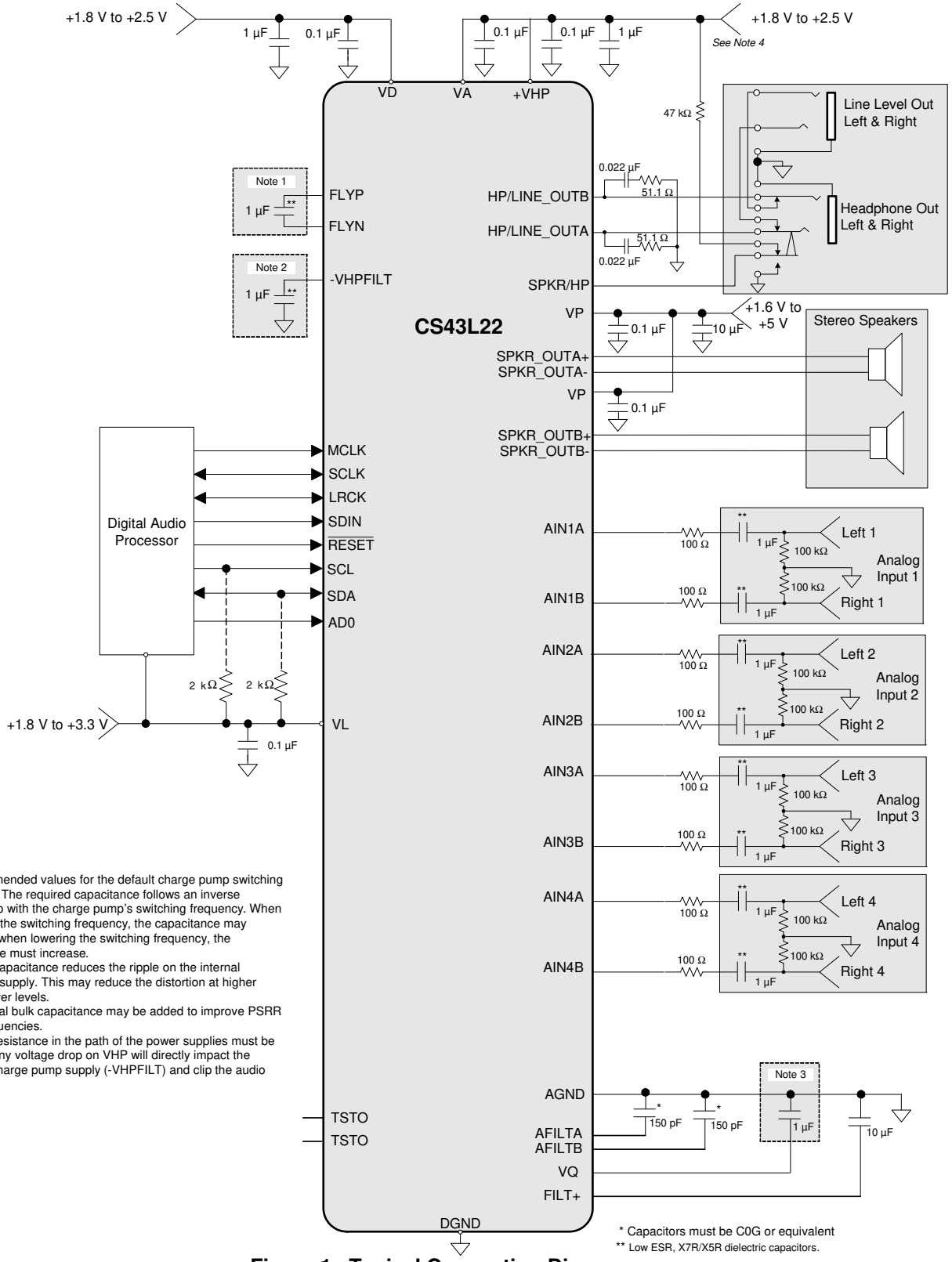
AGND	17	**Analog Ground** (*Input*) - Ground reference for the internal analog section.
FILT+	18	**Positive Voltage Reference** (Output) - Filter connection for the internal sampling circuits.
VQ	19	**Quiescent Voltage** (*Output*) - Filter connection for the internal quiescent voltage.
TSTO	20,36	**Test Out** (*Output*) - This pin is an output used for test purposes only and must be left "floating" (no connection external to the pin).
AIN4A,B AIN3A,B AIN2A,B AIN1A,B	21,22 23,24 25,26 29,30	**Line-Level Analog Inputs** (*Input*) - Single-ended stereo line-level analog inputs.
AFILTA,AFILTB	27,28	**Anti-alias Filter Connection** (Output) - Anti-alias filter connection for analog passthrough mode.
SPKR/HP	31	**Speaker/Headphone Switch** (*Input*) - Powers down the left and/or right channel of the speaker and/or headphone outputs.
$\overline{\text{RESET}}$	32	**Reset** (*Input*) - The device enters a low power mode when this pin is driven low.
VL	33	**Digital Interface Power** (*Input*) - Determines the required signal level for the serial audio interface and host control port.
VD	34	**Digital Power** (*Input*) - Positive power for the internal digital section.
DGND	35	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
MCLK	37	**Master Clock** (*Input*) - Clock source for the delta-sigma modulators.
SCLK	38	**Serial Clock** (*Input/Output*) - Serial clock for the serial audio interface.
SDIN	39	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
LRCK	40	**Left Right Clock** (*Input/Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
GND/Thermal Pad	-	Ground reference for PWM power FETs and charge pump; thermal relief pad for optimized heat dissipation.

1.1 I/O Pin Characteristics

Input and output levels and associated power supply voltage are shown in the table below. Logic levels should not exceed the corresponding power supply voltage.

Power Supply	Pin Name	I/O	Internal Connections	Driver	Receiver
VL	$\overline{\text{RESET}}$	Input	-	-	1.65 V - 3.47 V, with Hysteresis
	AD0	Input	-	-	1.65 V - 3.47 V, with Hysteresis
	SCL	Input	-	-	1.65 V - 3.47 V, with Hysteresis
	SDA	Input/ Output	-	1.65 V - 3.47 V, CMOS/Open Drain	1.65 V - 3.47 V, with Hysteresis
	MCLK	Input	-	-	1.65 V - 3.47 V
	LRCK	Input/ Output	Weak Pull-up (~1 MΩ)	1.65 V - 3.47 V, CMOS	1.65 V - 3.47 V
	SCLK	Input/ Output	Weak Pull-up (~1 MΩ)	1.65 V - 3.47 V, CMOS	1.65 V - 3.47 V
	SDIN	Input	-	-	1.65 V - 3.47 V
VA	SPKR/HP	Input	-	-	1.65 V - 2.63 V
VP	SPKR_OUTA+	Output	-	1.6 V - 5.25 V Power MOSFET	-
	SPKR_OUTA-	Output	-	1.6 V - 5.25 V Power MOSFET	-
	SPKR_OUTB+	Output	-	1.6 V - 5.25 V Power MOSFET	-
	SPKR_OUTB-	Output	-	1.6 V - 5.25 V Power MOSFET	-

2. TYPICAL CONNECTION DIAGRAM



Notes:
1. Recommended values for the default charge pump switching frequency. The required capacitance follows an inverse relationship with the charge pump's switching frequency. When increasing the switching frequency, the capacitance may decrease; when lowering the switching frequency, the capacitance must increase.
2. Larger capacitance reduces the ripple on the internal amplifier's supply. This may reduce the distortion at higher output power levels.
3. Additional bulk capacitance may be added to improve PSRR at low frequencies.
4. Series resistance in the path of the power supplies must be avoided. Any voltage drop on VHP will directly impact the negative charge pump supply (-VHPFILT) and clip the audio output.

* Capacitors must be C0G or equivalent
** Low ESR, X7R/X5R dielectric capacitors.

Figure 1. Typical Connection Diagram

3. CHARACTERISTIC AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

AGND=DGND=0 V, all voltages with respect to ground.

Parameters		Symbol	Min	Max	Units
DC Power Supply					
Analog		VA	1.65	2.63	V
Headphone Amplifier		+VHP	1.65	2.63	V
Speaker Amplifier		VP	1.60	5.25	V
Digital		VD	1.65	2.63	V
Serial/Control Port Interface		VL	1.65	3.47	V
Ambient Temperature	Commercial	T_A	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS

AGND = DGND = 0 V; all voltages with respect to ground.

Parameters		Symbol	Min	Max	Units
DC Power Supply	Analog	VA, VHP	-0.3	3.0	V
	Speaker	VP	-0.3	5.5	V
	Digital	VD	-0.3	3.0	V
	Serial/Control Port Interface	VL	-0.3	4.0	V
Input Current	(Note 1)	I_{in}	-	±10	mA
Analog Input Voltage	(Note 2)	V_{IN}	AGND-0.7	VA+0.7	V
External Voltage Applied to Analog Input	(Note 2)	V_{IN}	AGND-0.3	VA+0.3	V
External Voltage Applied to Analog Output		V_{IN}	-VHP - 0.3	+VHP + 0.3	V
External Voltage Applied to Digital Input	(Note 2)	V_{IND}	-0.3	VL+ 0.3	V
Ambient Operating Temperature (power applied)		T_A	-50	+115	°C
Storage Temperature		T_{stg}	-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:

1. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.
2. The maximum over/under voltage is limited by the input current.

ANALOG OUTPUT CHARACTERISTICS

Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; All Supplies = VA; T_A = +25°C; Sample Frequency = 48 kHz; Measurement bandwidth is 20 Hz to 20 kHz; Test load R_L = 10 kΩ, C_L = 10 pF for the line output (see Figure 2); Test load R_L = 16 Ω, C_L = 10 pF (see Figure 2) for the headphone output; HP_GAIN[2:0] = 011.

Parameters (Note 3)		VA = 2.5 V Min	VA = 2.5 V Typ	VA = 2.5 V Max	VA = 1.8 V Min	VA = 1.8 V Typ	VA = 1.8 V Max	Unit
R_L = 10 kΩ								
Dynamic Range								
18 to 24-Bit	A-weighted	92	98	-	89	95	-	dB
	unweighted	89	95	-	86	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-86	-80	-	-88	-82	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-29	-	-32	-26	dB
16-Bit	0 dB	-	-86	-	-	-88	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
R_L = 16 Ω								
Dynamic Range								
18 to 24-Bit	A-weighted	92	98	-	89	95	-	dB
	unweighted	89	95	-	86	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-75	-69	-	-75	-69	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-29	-	-32	-26	dB
16-Bit	0 dB	-	-75	-	-	-75	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
Other Characteristics for R_L = 16 Ω or 10 kΩ								
Output Parameters (Note 4)	Modulation Index (MI)	-	0.6787	-	-	0.6787	-	V/V
	Analog Gain Multiplier (G)	-	0.6047	-	-	0.6047	-	V/V
Full-scale Output Voltage (2•G•MI•VA) (Note 4)		Refer to Table "Headphone Output Power Characteristics" on page 14						Vpp
Full-scale Output Power (Note 4)		Refer to Table "Headphone Output Power Characteristics" on page 14						
Interchannel Isolation (1 kHz)	16 Ω	-	80	-	-	80	-	dB
	10 kΩ	-	95	-	-	93	-	dB
Speaker Amp to HP Amp Isolation		-	80	-	-	80	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
AC-Load Resistance (R_L)	(Note 5)	16	-	-	16	-	-	Ω
Load Capacitance (C_L)	(Note 5)	-	-	150	-	-	150	pF

3. One (least-significant bit) LSB of triangular PDF dither is added to data.
4. Full-scale output voltage and power is determined by the gain setting, G, in register "Headphone Analog Gain" on page 43. High gain settings at certain VA and VHP supply levels may cause clipping when the audio signal approaches full-scale, maximum power output, as shown in Figures 18 - 21 on page 60.

5. See Figure 2. R_L and C_L reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. In this circuit topology, C_L will effectively move the band-limiting pole of the amp in the output stage. Increasing this value beyond the recommended 150 pF can cause the internal op-amp to become unstable.

ANALOG PASSTHROUGH CHARACTERISTICS

Test Conditions (unless otherwise specified): Input sine wave (relative to full-scale): 1 kHz through passive input filter; Passthrough Amplifier and HP/Line Gain = 0 dB; All Supplies = VA; T_A = +25°C; Sample Frequency = 48 kHz; Measurement Bandwidth is 20 Hz to 20 kHz.

Parameters		VA = 2.5 V Min	VA = 2.5 V Typ	VA = 2.5 V Max	VA = 1.8 V Min	VA = 1.8 V Typ	VA = 1.8 V Max	Unit
Analog In to HP/Line Amp								
R_L = 10 kΩ								
Dynamic Range	A-weighted	-	-96	-	-	-94	-	dB
	unweighted	-	-93	-	-	-91	-	dB
Total Harmonic Distortion + Noise	-1 dBFS	-	-70	-	-	-70	-	dB
	-20 dBFS	-	-73	-	-	-71	-	dB
	-60 dBFS	-	-33	-	-	-31	-	dB
Full-scale Input Voltage		-	0.91•VA	-	-	0.91•VA	-	Vpp
Full-scale Output Voltage		-	0.84•VA	-	-	0.84•VA	-	Vpp
Passband Ripple		-	0/-0.3	-	-	0/-0.3	-	dB
R_L = 16 Ω								
Dynamic Range	A-weighted	-	-96	-	-	-94	-	dB
	unweighted	-	-93	-	-	-91	-	dB
Total Harmonic Distortion + Noise	-1 dBFS	-	-70	-	-	-70	-	dB
	-20 dBFS	-	-73	-	-	-71	-	dB
	-60 dBFS	-	-33	-	-	-31	-	dB
Full-scale Input Voltage		-	0.91•VA	-	-	0.91•VA	-	Vpp
Full-scale Output Voltage		-	0.84•VA	-	-	0.84•VA	-	Vpp
Output Power		-	32	-	-	17	-	mW
Passband Ripple		-	0/-0.3	-	-	0/-0.3	-	dB

PWM OUTPUT CHARACTERISTICS

Test conditions (unless otherwise specified): Input test signal is a full scale 997 Hz signal; MCLK = 12.2880 MHz; Measurement Bandwidth is 20 Hz to 20 kHz; Sample Frequency = 48 kHz; Test load R_L = 8 Ω for stereo full-bridge, R_L = 4 Ω for mono parallel full-bridge; VD = VL = VA = VHP = 1.8V; PWM Modulation Index of 0.85; PWM Switch Rate = 384 kHz.

Parameters (Note 7)	Symbol	Conditions	Min	Typ	Max	Units
VP = 5.0 V						
Power Output per Channel	P_O					
Stereo Full-Bridge		THD+N < 10% THD+N < 1%	- -	1.00 0.80	- -	W_{rms} W_{rms}
Mono Parallel Full-Bridge		THD+N < 10% THD+N < 1%	- -	1.90 1.50	- -	W_{rms} W_{rms}
Total Harmonic Distortion + Noise	THD+N					
Stereo Full-Bridge		P_O = 0 dBFS = 0.8W	-	0.52	-	%
Mono Parallel Full-Bridge		P_O = -3 dBFS = 0.75 W P_O = 0 dBFS = 1.5 W	- -	0.10 0.50	- -	% %
Dynamic Range	DR					
Stereo Full-Bridge		P_O = -60 dBFS, A-Weighted P_O = -60 dBFS, Unweighted	- -	91 88	- -	dB dB
Mono Parallel Full-Bridge		P_O = -60 dBFS, A-Weighted P_O = -60 dBFS, Unweighted	- -	91 88	- -	dB dB
VP = 3.7 V						
Power Output per Channel	P_O					
Stereo Full-Bridge		THD+N < 10% THD+N < 1%	- -	0.55 0.45	- -	W_{rms} W_{rms}
Mono Parallel Full-Bridge		THD+N < 10% THD+N < 1%	- -	1.00 0.84	- -	W_{rms} W_{rms}
Total Harmonic Distortion + Noise	THD+N					
Stereo Full-Bridge		P_O = 0 dBFS = 0.43 W	-	0.54	-	%
Mono Parallel Full-Bridge		P_O = -3 dBFS = 0.41 W P_O = 0 dBFS = 0.81 W	- -	0.09 0.45	- -	% %
Dynamic Range	DR					
Stereo Full-Bridge		P_O = -60 dBFS, A-Weighted P_O = -60 dBFS, Unweighted	- -	91 88	- -	dB dB
Mono Parallel Full-Bridge		P_O = -60 dBFS, A-Weighted P_O = -60 dBFS, Unweighted	- -	95 92	- -	dB dB
VP =2.5 V						
Power Output per Channel	P_O					
Stereo Full-Bridge		THD+N < 10% THD+N < 1%	- -	0.23 0.19	- -	W_{rms} W_{rms}
Mono Parallel Full-Bridge		THD+N < 10% THD+N < 1%	- -	0.44 0.35	- -	W_{rms} W_{rms}
Total Harmonic Distortion + Noise	THD+N					
Stereo Full-Bridge		P_O = 0 dBFS = 0.18 W	-	0.50	-	%
Mono Parallel Full-Bridge		P_O = -3 dBFS = 0.17 W P_O = 0 dBFS = 0.35 W	- -	0.08 0.43	- -	% %
Dynamic Range	DR					
Stereo Full-Bridge		P_O = -60 dBFS, A-Weighted P_O = -60 dBFS, Unweighted	- -	91 88	- -	dB dB
Mono Parallel Full-Bridge		P_O = -60 dBFS, A-Weighted P_O = -60 dBFS, Unweighted	- -	94 91	- -	dB dB
MOSFET On Resistance	$R_{DS(ON)}$	VP = 5.0V, I_d = 0.5 A	-	600	-	mΩ
MOSFET On Resistance	$R_{DS(ON)}$	VP = 3.7V, I_d = 0.5 A	-	640	-	mΩ

Parameters (Note 7)	Symbol	Conditions	Min	Typ	Max	Units
MOSFET On Resistance	$R_{DS(ON)}$	VP = 2.5V, I_d = 0.5 A	-	760	-	mΩ
Efficiency	η	VP = 5.0 V, P_O = 2 x 0.8 W, R_L = 8 Ω	-	81	-	%
Output Operating Peak Current	I_{PC}		-	-	1.5	A
VP Input Current During Reset	I_{VP}	$\overline{RESET}$, pin 32, is held low	-	0.8	5.0	µA

6. The PWM driver should be used in captive speaker systems only.
7. Optimal PWM performance is achieved when MCLK > 12 MHz.

HEADPHONE OUTPUT POWER CHARACTERISTICS

Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; Sample Frequency = 48 kHz; Measurement Bandwidth is 20 Hz to 20 kHz; Test load R_L = 16 Ω, C_L = 10 pF (see Figure 2); "Required Initialization Settings" on page 32 written on power up.

Parameters			VA = 2.5V Min	VA = 2.5V Typ	VA = 2.5V Max	VA = 1.8V Min	VA = 1.8V Typ	VA = 1.8V Max	Unit
AOUTx Power Into R_L = 16 Ω									
HP_GAIN[2:0]	Analog Gain (G)	VHP							
000	0.3959	1.8 V	-	14	-	-	7	-	mW_{rms}
		2.5 V	-	14	-	-	7	-	mW_{rms}
001	0.4571	1.8 V	-	19	-	-	10	-	mW_{rms}
		2.5 V	-	19	-	-	10	-	mW_{rms}
010	0.5111	1.8 V	-	23	-	-	12	-	mW_{rms}
		2.5 V	-	23	-	-	12	-	mW_{rms}
011 (default)	0.6047	1.8 V	(Note 8)			-	17	-	mW_{rms}
		2.5 V	-	32	-	-	17	-	mW_{rms}
100	0.7099	1.8 V	(Note 8)			-	23	-	mW_{rms}
		2.5 V	-	44	-	-	23	-	mW_{rms}
101	0.8399	1.8 V				(Note 4) See Figure 18 on page 59			mW_{rms}
		2.5 V				-	32	-	mW_{rms}
110	1.0000	1.8 V	(Note 4, 8) See Figures 18 and 19 on page 59						mW_{rms}
		2.5 V							mW_{rms}
111	1.1430	1.8 V							mW_{rms}
		2.5 V							mW_{rms}

8. VHP settings lower than VA reduces the headroom of the headphone amplifier. As a result, the DAC may not achieve the full THD+N performance at full-scale output voltage and power.

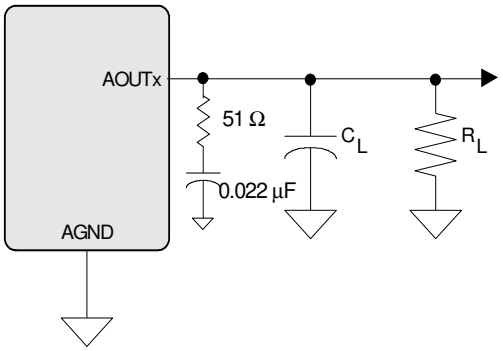


Figure 2. Headphone Output Test Load

LINE OUTPUT VOLTAGE LEVEL CHARACTERISTICS

Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; measurement bandwidth is 20 Hz to 20 kHz; Sample Frequency = 48 kHz; Test load R_L = 10 kΩ, C_L = 10 pF (see Figure 2); "Required Initialization Settings" on page 32 written on power up.

Parameters			VA = 2.5V			VA = 1.8V			Unit
			Min	Typ	Max	Min	Typ	Max	
AOUTx Voltage Into R_L = 10 kΩ									
HP_GAIN[2:0]	Analog Gain (G)	VHP							
000	0.3959	1.8 V	-	1.34	-	-	0.97	-	V_{pp}
		2.5 V	-	1.34	-	-	0.97	-	V_{pp}
001	0.4571	1.8 V	-	1.55	-	-	1.12	-	V_{pp}
		2.5 V	-	1.55	-	-	1.12	-	V_{pp}
010	0.5111	1.8 V	-	1.73	-	-	1.25	-	V_{pp}
		2.5 V	-	1.73	-	-	1.25	-	V_{pp}
011 (default)	0.6047	1.8 V	-	2.05	-	1.41	1.48	1.55	V_{pp}
		2.5 V	1.95	2.05	2.15	-	1.48	-	V_{pp}
100	0.7099	1.8 V	-	2.41	-	-	1.73	-	V_{pp}
		2.5 V	-	2.41	-	-	1.73	-	V_{pp}
101	0.8399	1.8 V	-	2.85	-		2.05		V_{pp}
		2.5 V	-	2.85	-	-	2.05	-	V_{pp}
110	1.0000	1.8 V	-	3.39	-	-	2.44	-	V_{pp}
		2.5 V	-	3.39	-	-	2.44	-	V_{pp}
111	1.1430	1.8 V	(See Note 8)				2.79		V_{pp}
		2.5 V	-	3.88	-	-	2.79	-	V_{pp}

COMBINED DAC INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

Parameters (Note 9)		Min	Typ	Max	Unit
Frequency Response 10 Hz to 20 kHz		-0.01	-	+0.08	dB
Passband	to -0.05 dB corner	0	-	0.4780	Fs
	to -3 dB corner	0	-	0.4996	Fs
StopBand		0.5465	-	-	Fs
StopBand Attenuation (Note 10)		50	-	-	dB
Group Delay		-	9/Fs	-	s
De-emphasis Error	Fs = 32 kHz	-	-	+1.5/+0	dB
	Fs = 44.1 kHz	-	-	+0.05/-0.25	dB
	Fs = 48 kHz	-	-	-0.2/-0.4	dB

9. Response is clock dependent and will scale with Fs. Note that the response plots (Figures 22 and 25 on page 63) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
10. Measurement Bandwidth is from Stopband to 3 Fs.

SWITCHING SPECIFICATIONS - SERIAL PORT

Inputs: Logic 0 = DGND; Logic 1 = VL.

Parameters		Symbol	Min	Max	Units
$\overline{\text{RESET}}$ pin Low Pulse Width (Note 11)			1	-	ms
MCLK Frequency (Note 12)			(See "Serial Port Clocking" on page 29)		MHz
MCLK Duty Cycle			45	55	%
Slave Mode					
Sample Rate (LRCK)		F_s	(See "Serial Port Clocking" on page 29)		kHz
LRCK Duty Cycle			45	55	%
SCLK Frequency		$1/t_P$	-	$64 \cdot F_s$	Hz
SCLK Duty Cycle			45	55	%
LRCK Setup Time Before SCLK Rising Edge		$t_{s(LK-SK)}$	40	-	ns
SDIN Setup Time Before SCLK Rising Edge		$t_{s(SD-SK)}$	20	-	ns
SDIN Hold Time After SCLK Rising Edge		t_h	20	-	ns
Master Mode					
Sample Rate (LRCK)		F_s	(See "Serial Port Clocking" on page 29)		Hz
LRCK Duty Cycle			45	55	%
SCLK Frequency	SCLK=MCLK mode	$1/t_P$	-	12.0000	MHz
	MCLK=12.0000 MHz	$1/t_P$	-	$68 \cdot F_s$	Hz
	all other modes	$1/t_P$	-	$64 \cdot F_s$	Hz
SCLK Duty Cycle			45	55	%
SDIN Setup Time Before SCLK Rising Edge		$t_{s(SD-SK)}$	20	-	ns
SDIN Hold Time After SCLK Rising Edge		t_h	20	-	ns

11. After powering up the CS43L22, $\overline{\text{RESET}}$ should be held low after the power supplies and clocks are settled.
12. See "Example System Clock Frequencies" on page 61 for typical MCLK frequencies.

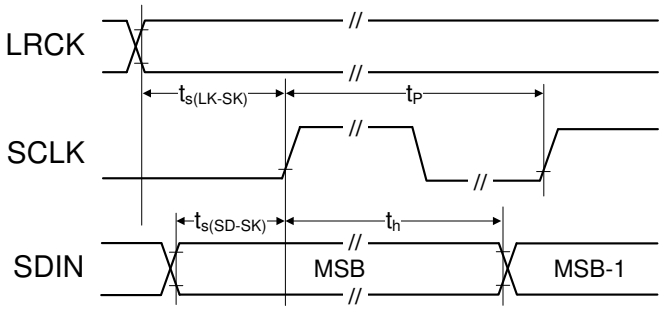


Figure 3. Serial Audio Interface Timing

SWITCHING SPECIFICATIONS - I²C CONTROL PORT

Inputs: Logic 0 = DGND; Logic 1 = V; SDA C_L = 30 pF.

Parameters	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{\text{RESET}}$ Rising Edge to Start	t_{irs}	550	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 13)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}	-	1	µs
Fall Time SCL and SDA	t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	1000	ns

13. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

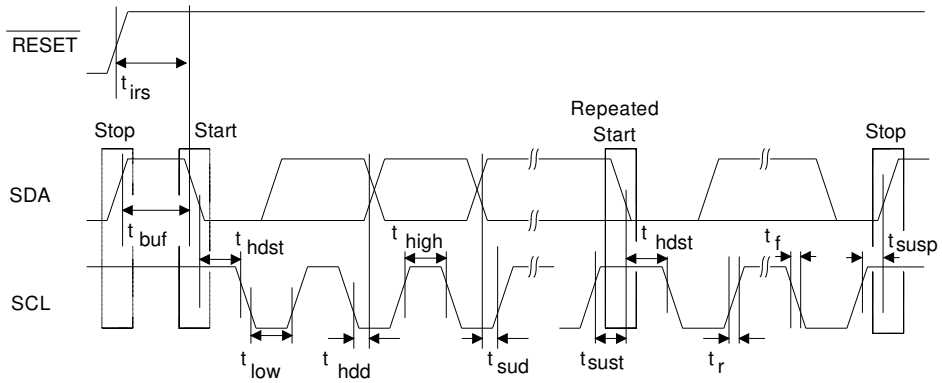


Figure 4. Control Port Timing - I²C

DC ELECTRICAL CHARACTERISTICS

AGND = 0 V; all voltages with respect to ground.

Parameters		Min	Typ	Max	Units
VQ Characteristics					
Nominal Voltage		-	0.5•VA	-	V
Output Impedance		-	23	-	kΩ
DC Current Source/Sink		-	-	1	µA
Power Supply Rejection Ratio Characteristics					
PSRR @ 1 kHz (Note 14)	DAC (HP & Line Amps)	-	60	-	dB
PSRR @ 60 Hz (Note 14)	DAC (HP & Line Amps)	-	60	-	dB
PSRR @ 217 Hz	Full-Bridge PWM Outputs	-	56	-	dB

14. Valid with the recommended capacitor values on FILT+ and VQ. Increasing the capacitance will also increase the PSRR.

DIGITAL INTERFACE SPECIFICATIONS & CHARACTERISTICS

Parameters (Note 15)		Symbol	Min	Max	Units
Input Leakage Current		I_{in}	-	±10	µA
Input Capacitance			-	10	pF
1.8 V - 3.3 V Logic					
High-Level Output Voltage (I_{OH} = -100 µA)		V_{OH}	VL - 0.2	-	V
Low-Level Output Voltage (I_{OL} = 100 µA)		V_{OL}	-	0.2	V
High-Level Input Voltage	VL = 1.65 V	V_{IH}	0.85•VL	-	V
	VL = 1.8 V		0.77•VL	-	V
	VL = 2.0 V		0.68•VL	-	V
	VL > 2.0 V		0.65•VL	-	V
Low-Level Input Voltage		V_{IL}	-	0.30•VL	V

15. See "I/O Pin Characteristics" on page 8 for serial and control port power rails.

POWER CONSUMPTION See (Note 16)

	Operation	Register Settings					V	Typical Current (mA)					Total Power (mW_{rms})
		02h	04h					i_{VHP}	i_{VA}	i_{VD}	i_{VL} VL=3.3V (Note 19)	i_{VP} VP=3.7V	
		PDN[7:0]	PDN_HPB[1:0]	PDN_HPA[1:0]	PDN_SPKB[1:0]	PDN_SPKA[1:0]							
1	Off (Note 17)	x	x	x	x	x	1.8 2.5	0.00 0.00	0.00 0.00	0.00 0.00	0.00	0.00	**0.00** **0.00**
2	Standby (Note 18)	0x9F	x	x	x	x	1.8 2.5	0.00 0.00	0.00 0.00	0.01 0.02	0.00	0.00	**0.02** **0.05**
3	Stereo Passthrough to Headphone	0x9E	10	10	11	11	1.8 2.5	2.79 3.18	1.91 2.14	1.06 1.81	0.01	0.00	**10.39** **17.85**
4	Mono Playback to Headphone	0x9E	10	11	11	11	1.8 2.5	1.59 2.07	1.99 2.62	2.72 4.27	0.01	0.00	**11.36** **22.43**
5	Stereo Playback to Headphone	0x9E	10	10	11	11	1.8 2.5	2.77 3.27	2.00 2.63	2.91 4.28	0.01	0.00	**13.84** **25.48**
6	Mono Playback to Speaker	0x9E	11	11	10	10	1.8 2.5	0.00 0.00	0.20 0.22	4.42 6.77	0.01	1.00	**12.05** **21.21**
7	Stereo Playback to Speaker	0x9E	11	11	10	10	1.8 2.5	0.00 0.00	0.20 0.22	4.38 6.80	0.01	1.00	**11.98** **21.28**

16. Unless otherwise noted, test conditions are as follows: All zeros input, Slave Mode, sample rate = 48 kHz; No load. Digital (VD) and logic (VL) supply current will vary depending on speed mode and master/slave operation."Required Initialization Settings" on page 32 written on power up.
17. $\overline{\text{RESET}}$ pin 25 held LO, all clocks and data lines are held LO.
18. $\overline{\text{RESET}}$ pin 25 held HI, all clocks and data lines are held HI.
19. VL current will slightly increase in Master Mode.

4. APPLICATIONS

4.1 Overview

4.1.1 Basic Architecture

The CS43L22 is a highly integrated, low power, 24-bit audio DAC comprised of a Digital Signal Processing Engine, headphone amplifiers, a digital PWM modulator and two full-bridge power back-ends. Other features include battery level monitoring and compensation and temperature monitoring. The DAC is designed using multi-bit delta-sigma techniques and operates at an oversampling ratio of 128Fs, where Fs is equal to the system sample rate.

The PWM modulator operates at a fixed frequency of 384 kHz. The power MOSFETs are configured for either stereo full-bridge or mono parallel full bridge output. The DAC operates in one of four sample rate speed modes: Quarter, Half, Single and Double. It accepts and is capable of generating serial port clocks (SCLK, LRCK) derived from an input Master Clock (MCLK).

4.1.2 Line Inputs

4 pairs of stereo analog inputs are provided for applications that require analog passthrough directly to the HP/Line amplifiers. This analog input portion allows selection from and configuration of multiple combinations of these stereo sources.

4.1.3 Line & Headphone Outputs

The analog output portion of the CS43L22 includes a headphone amplifier capable of driving headphone and line-level loads. An on-chip charge pump creates a negative headphone supply allowing a full-scale output swing centered around ground. This eliminates the need for large DC-Blocking capacitors and allows the amplifier to deliver more power to headphone loads at lower supply voltages.

4.1.4 Speaker Driver Outputs

The Class D power amplifiers drive 8 Ω (stereo) and 4 Ω (mono) speakers directly, without the need for an external filter. The power MOSFETS are powered directly from a battery eliminating the efficiency loss associated with an external regulator. Battery level monitoring and compensation maintains a steady output as battery levels fall. A temperature monitor continually measures the die temperature and registers when predefined thresholds are exceeded. **NOTE**: The CS43L22 should only be used in captive speaker systems where the outputs are permanently tied to the speaker terminals.

4.1.5 Fixed Function DSP Engine

The fixed-function digital signal processing engine processes the PCM serial input data. Independent volume control, left/right channel swaps, mono mixes, tone control and limiting functions also comprise the DSP engine.

4.1.6 Beep Generator

The beep generator delivers tones at select frequencies across approximately two octave major scales. With independent volume control, beeps may be configured to occur continuously, periodically, or at single time intervals.

4.1.7 Power Management

Two control registers provide independent power-down control of the DAC, Headphone and Speaker output blocks in the CS43L22 allowing operation in select applications with minimal power consumption.

4.2 DSP Engine

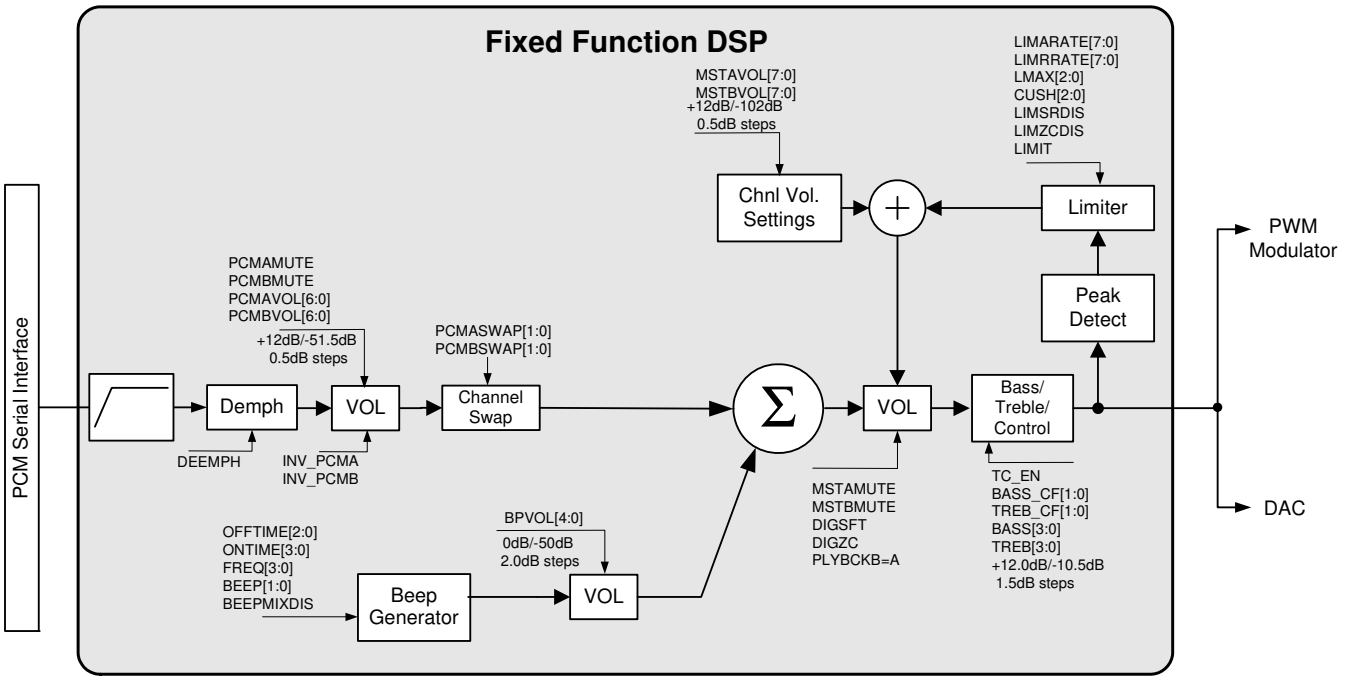


Figure 5. DSP Engine Signal Flow

Referenced Control	Register Location
DSP	
DEEMPH	"HP/Speaker De-Emphasis" on page 44
PCMxMUTE	"PCM Channel x Mute" on page 47
PCMxVOL[6:0]	"PCM Channel x Volume" on page 47
INV_PCMx	"Invert PCM Signal Polarity" on page 43
PCMxSWAP[1:0]	"PCM Channel Swap" on page 52
MSTxVOL[7:0]	"Master Volume Control" on page 51
MSTxMUTE	"Master Playback Mute" on page 43
DIGSFT	"Digital Soft Ramp" on page 44
DIGZC	"Digital Zero Cross" on page 45
PLYBCKB=A	"Playback Volume Setting B=A" on page 43
TC_EN	"Tone Control Enable" on page 50
BASS_CF[1:0]	"Bass Corner Frequency" on page 50
TREB_CF[1:0]	"Treble Corner Frequency" on page 50
BASS[3:0]	"Bass Gain" on page 51
TREB[3:0]	"Treble Gain" on page 50
LIMIT	"Peak Detect and Limiter" on page 54
LIMSRDIS	"Limiter Soft Ramp Disable" on page 53
LIMZCDIS	"Limiter Zero Cross Disable" on page 54
LMAX[2:0]	"Limiter Maximum Threshold" on page 53
CUSH[2:0]	"Limiter Cushion Threshold" on page 53
LIMARATE[7:0]	"Limiter Attack Rate" on page 55
LIMRRATE[7:0]	"Limiter Release Rate" on page 54

4.2.1 Beep Generator

The Beep Generator generates audio frequencies across approximately two octave major scales. It offers three modes of operation: Continuous, multiple and single (one-shot) beeps. Sixteen on and eight off times are available.

Note: The Beep is generated before the limiter and may affect desired limiting performance. If the limiter function is used, it may be required to set the beep volume sufficiently below the threshold to prevent the peak detect from triggering. Since the master volume control, MSTxVOL[7:0], will affect the beep volume, DAC volume may alternatively be controlled using the PCMxVOL[6:0] bits.

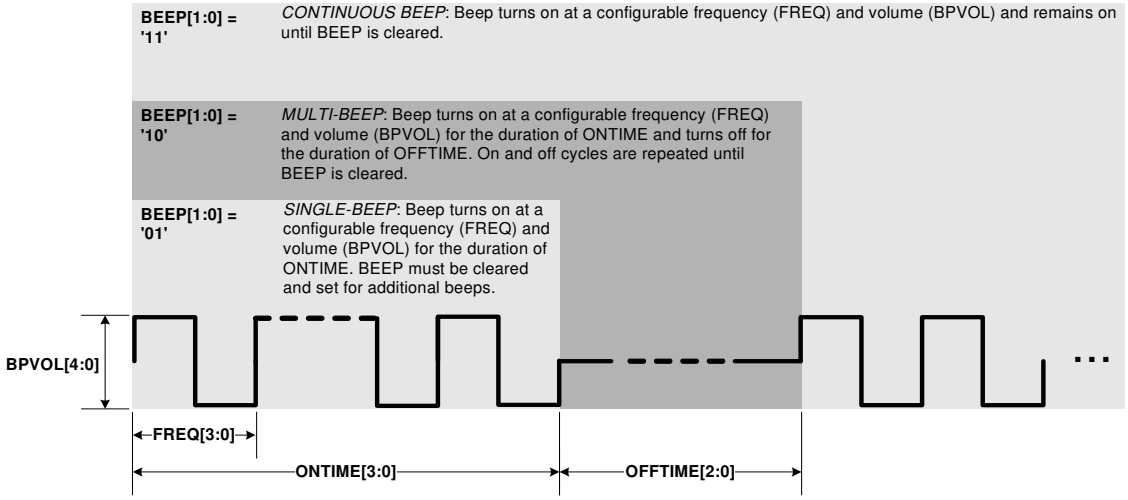


Figure 6. Beep Configuration Options

Referenced Control	Register Location
MSTxVOL[7:0]	"Master Volume Control: MSTA (Address 20h) & MSTB (Address 21h)" on page 51
PCMxVOL[6:0]	"PCMx Volume: PCMA (Address 1Ah) & PCMB (Address 1Bh)" on page 47
OFFTIME[2:0]	"Beep Off Time" on page 48
ONTIME[3:0]	"Beep On Time" on page 48
FREQ[3:0]	"Beep Frequency" on page 47
BEEP[1:0]	"Beep Configuration" on page 49
BEEPMIXDIS	"Beep Mix Disable" on page 49
BPVOL[4:0]	"Beep Volume" on page 49

4.2.2 Limiter

When enabled, the limiter monitors the digital input signal before the DAC and PWM modulators, detects when levels exceed the maximum threshold settings and lowers the master volume at a programmable attack rate below the maximum threshold. When the input signal level falls below the maximum threshold, the AOUT volume returns to its original level set in the Master Volume Control register at a programmable release rate. Attack and release rates are affected by the DAC soft ramp/zero cross settings and sample rate, Fs. Limiter soft ramp and zero cross dependency may be independently enabled/disabled.

Notes:

1. *Recommended settings*: Best limiting performance may be realized with the fastest attack and slowest release setting with soft ramp enabled in the control registers. The MIN bits allow the user to set a threshold slightly below the maximum threshold for hysteresis control - this cushions the sound as the limiter attacks and releases.
2. The Limiter maintains the output signal between the CUSH and MAX thresholds. As the digital input signal level changes, the level-controlled output may not always be the same but will always fall within

the thresholds.

Referenced Control	Register Location
Limiter Controls.....	"Limiter Control 2, Release Rate (Address 28h)" on page 54, "Limiter Attack Rate (Address 29h)" on page 55
Master Volume Control.....	"Master Volume Control: MSTA (Address 20h) & MSTB (Address 21h)" on page 51

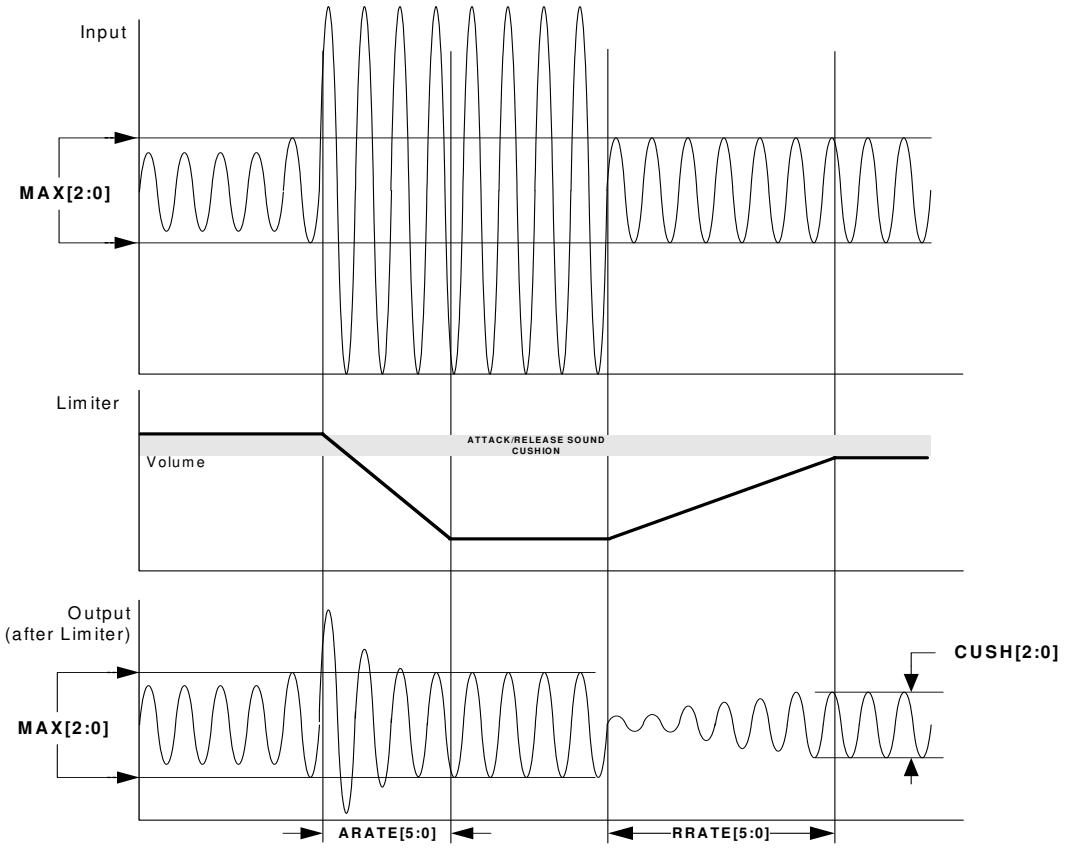


Figure 7. Peak Detect & Limiter

4.3 Analog Passthrough

The CS43L22 accommodates analog routing of the analog input signal directly to the headphone amplifiers by using the PASSTHRUx mux. This feature is useful in applications that utilize an FM tuner where audio recovered over-the-air must be transmitted to the headphone amplifier directly. This analog passthrough path reduces power consumption and is immune to modulator switching noise that could interfere with some tuners.

Four analog input channels can be chosen or summed by using the PASSxSEL bits as shown in Figure 8 to provide input to the CS43L22 when in analog passthrough mode. A pair of passthrough amplifiers can be used to mute and apply gain to the input signals.

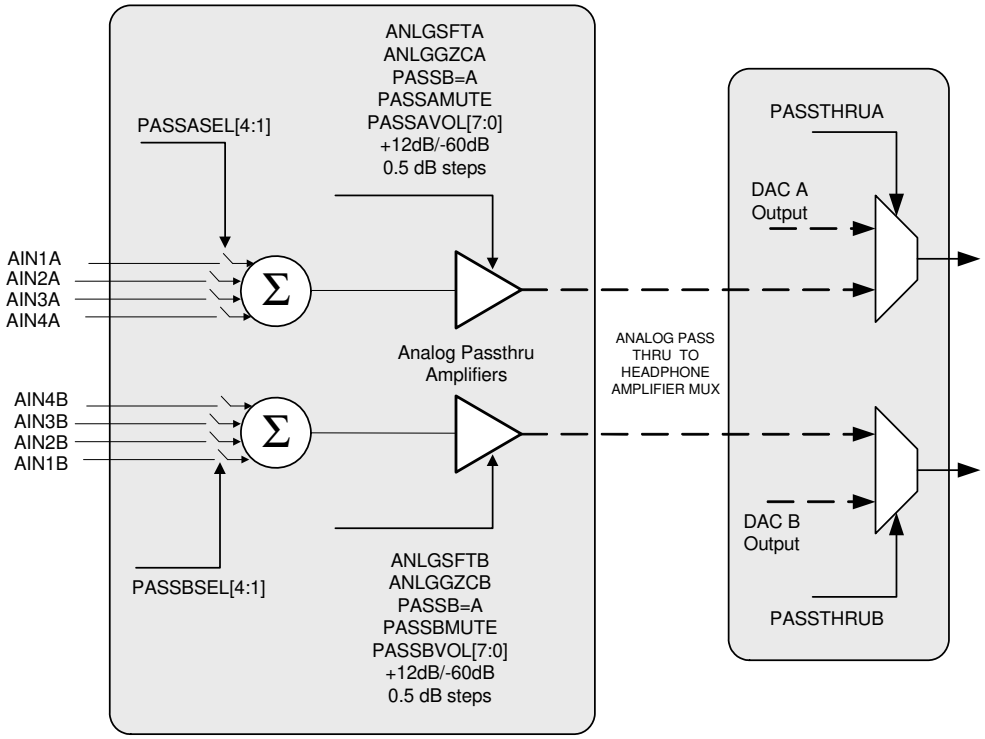


Figure 8. Analog Passthrough Signal Flow

Referenced Control	Register Location
Analog Front End	
PASSB=A	"Passthrough Channel B=A Gang Control" on page 42
ANLGSFTx	"Ch. x Analog Soft Ramp" on page 42
ANLGZCx	"Ch. x Analog Zero Cross" on page 42
PASSxSEL4,3,2,1	"Passthrough Input Channel Mapping" on page 42
PASSxMUTE	"Passthrough Mute" on page 44
PASSxVOL[7:0]	"Passthrough x Volume" on page 46
PASSTHRUx	"Passthrough Analog" on page 44

4.4 Analog Outputs

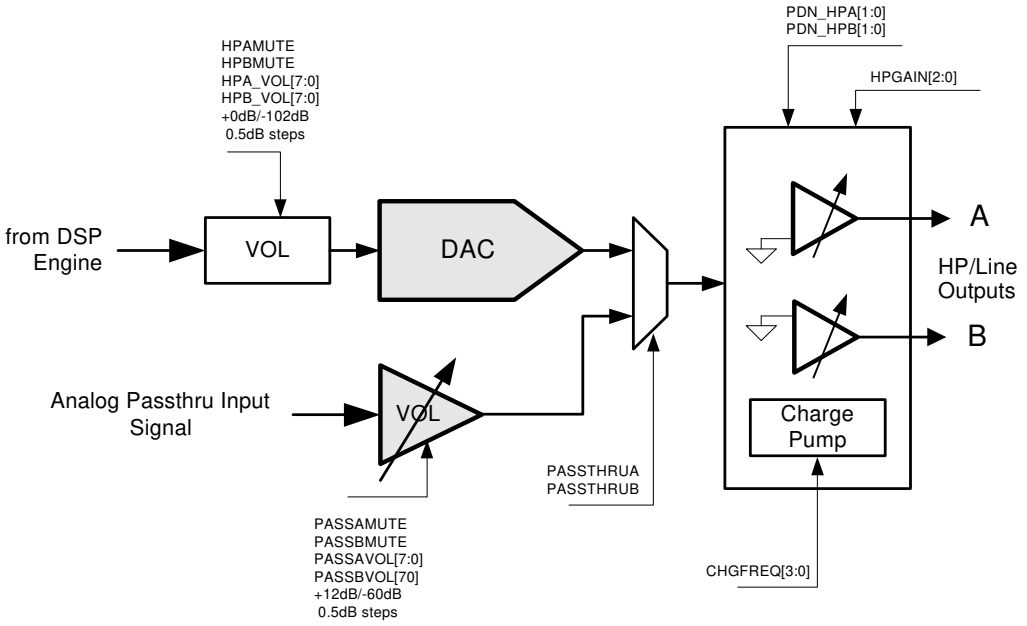


Figure 9. Analog Outputs

Referenced Control	Register Location
Analog Output	
HPxMUTE	"Headphone Mute" on page 45
HPxVOL[7:0]	"Headphone Volume Control" on page 51
PDN_HPx[1:0]	"Headphone Power Control" on page 38
HPGAIN[2:0]	"Headphone Analog Gain" on page 43
PASSTHRUx	"Passthrough Analog" on page 44
PASSxMUTE	"Passthrough Mute" on page 44
PASSxVOL[7:0]	"Passthrough x Volume" on page 46
CHGFREQ	"Charge Pump Frequency" on page 58