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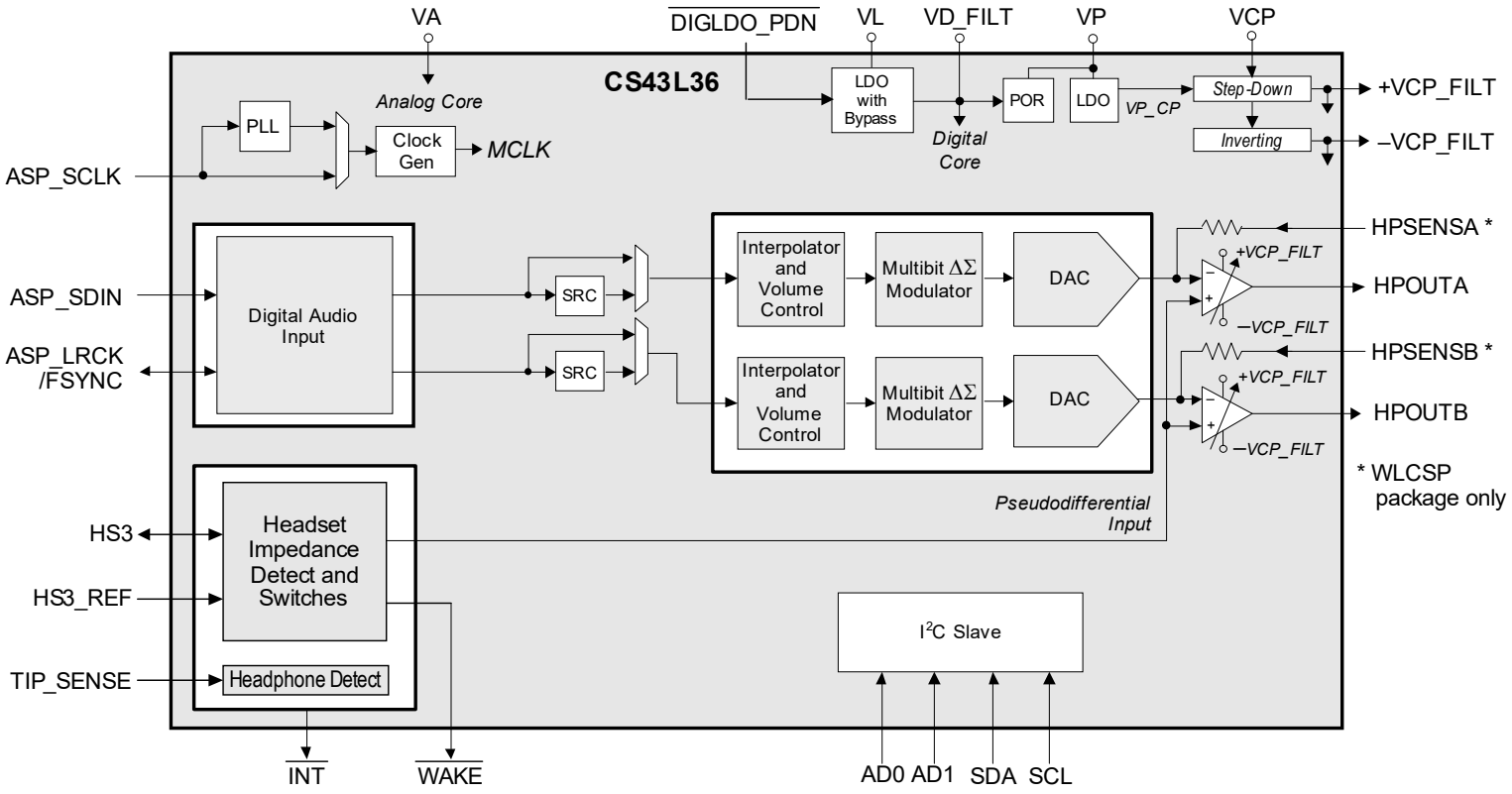
Low-Power, High-Performance Audio DAC with Class H Headphone Drivers

System Features

- Stereo headphone (HP) output with 114-dB dynamic range
  - Class H HP amplifier with four-level automatic or manual supply adjust
  - –98-dB THD+N into 30 Ω with 10-mW output power
  - 2 x 35 mW output power into 30 Ω with 0.018% THD+N
- Load detection
  - Headphone load detection of 15 or 30 Ω
  - Line-level load (3 kΩ) with capacitance detection
- Headphone insertion/removal detection with WAKE
- Audio serial port (ASP)
  - I²S (two channels) or TDM (up to four channels)
  - Slave or Hybrid-Master Mode (bit-clock slave and LRCK/FSYNC derived from bit clock)
  - Supports up to 32-bit audio
  - Sample rate support for 8 to 192 kHz
  - I²C control with interrupt output
- Integrated fractional-N PLL
  - Increases system-clock flexibility for audio processing
  - Reference clock sourced from I²S/TDM bit clock
- Bypassable SRCs for maximum flexibility
- Attenuation, mute, and volume controls for each output
- Integrated power management
  - Digital core operates from either an external 1.2-V supply or LDO from a 1.8-V supply.
  - Step-down charge pump improves HP efficiency
  - Independent peripheral power-down controls
  - Standby operation from VP with all other supplies powered off
  - VP monitor to detect and report brownout conditions
  - Low-impedance switching suppresses ground-noise

Applications

- Ultrabooks, tablets, and smartphones
- Digital headsets



General Description

The CS43L36 is a low-power, high dynamic-range, stereo audio DAC with integrated I²S/I²C/TDM interfaces designed for portable applications. The CS43L36 features support for up to 32-bit audio inputs and includes bypassable SRCs.

The bypassable fractional-N PLL sourced from the ASP SCLK allows for maximum flexibility in any system.

There is independent attenuation on each input along with volume adjustment and mute control.

The CS43L36 is available in 49-ball WLCSP package and a 40-pin QFN package, both supporting an extended commercial operational temperature range of –40°C to +85°C.

Table of Contents

1 Pin Assignments and Descriptions

This section shows pin assignments and describes pin functions.

1.1 WLCSP Pin Out (Through-Package View)

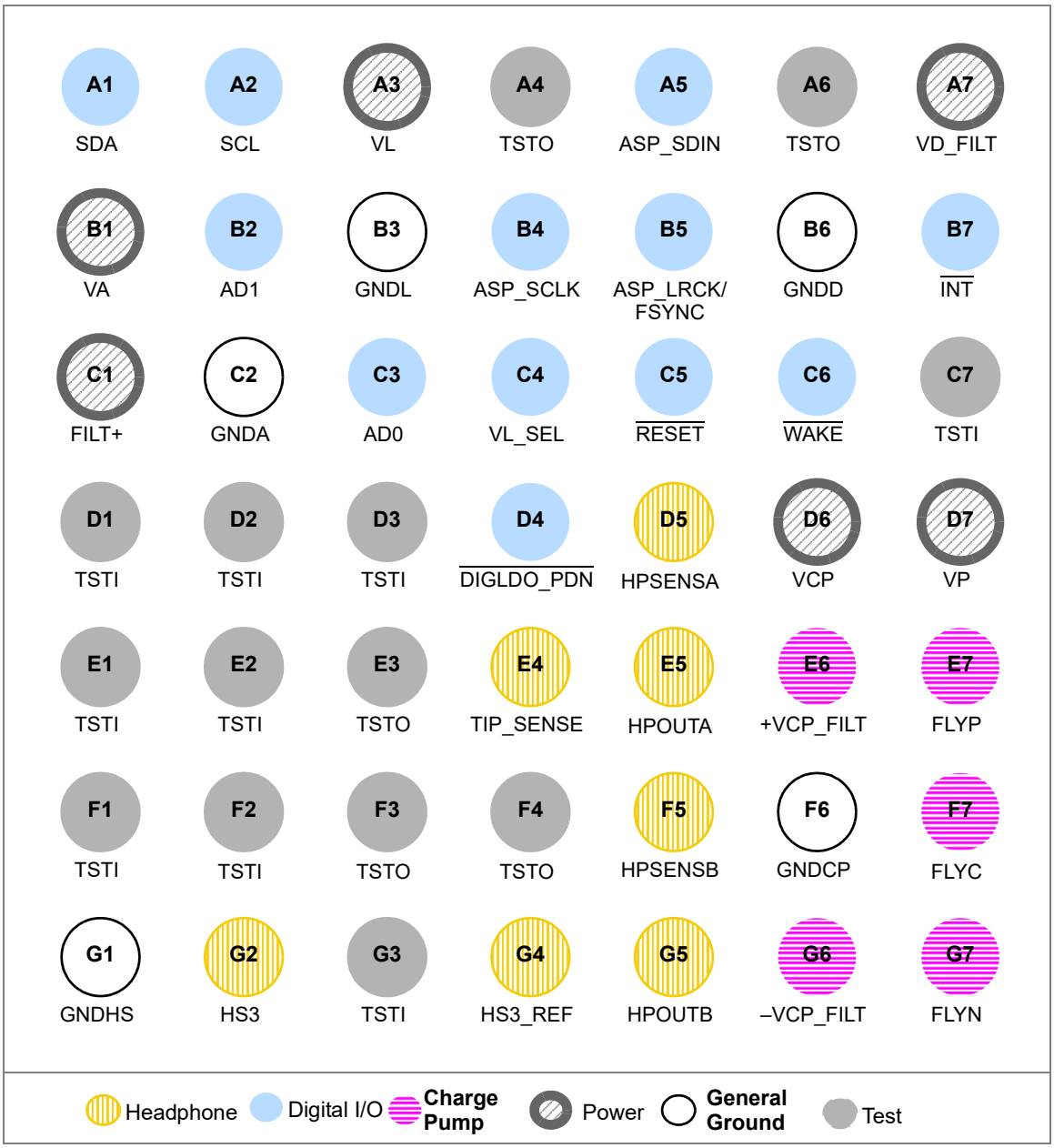


Figure 1-1. WLCSP Pin Diagram (Through-Package View)

1.2 QFN Pin Out (Through-Package View)

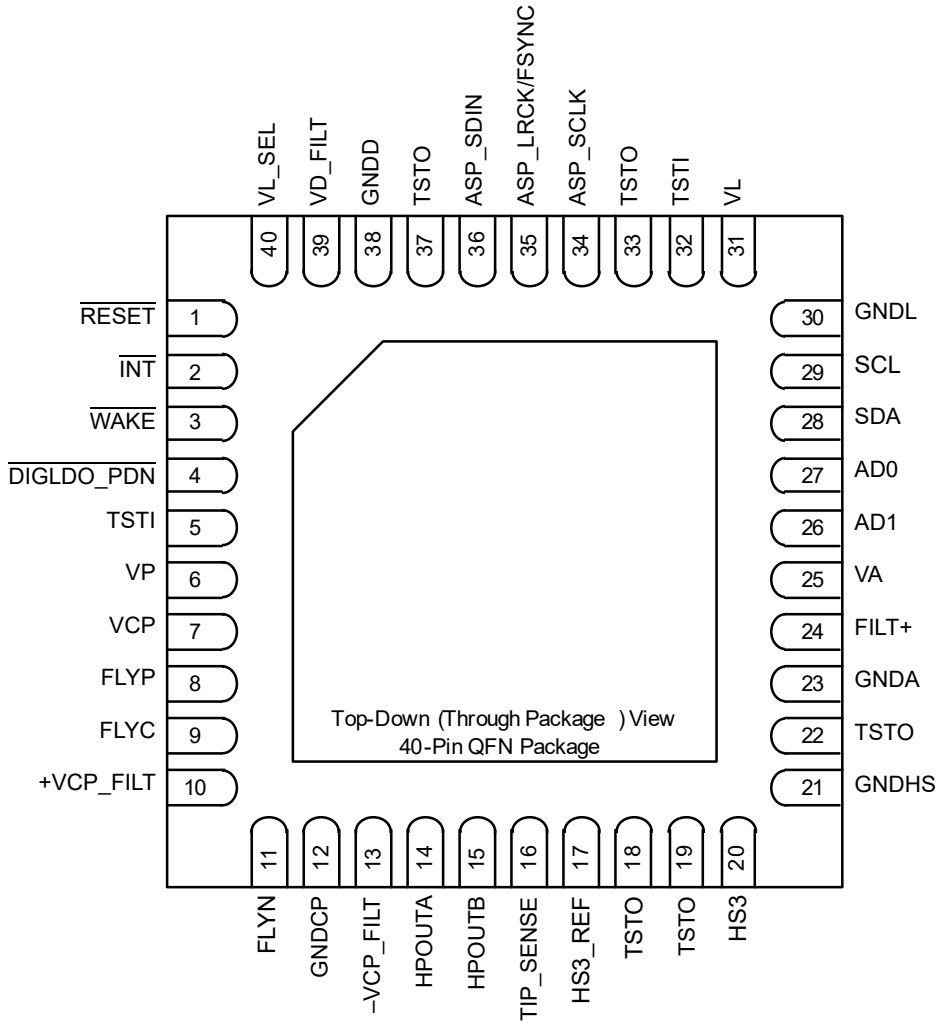


Figure 1-2. QFN Pin Diagram

1.3 Pin Descriptions

Table 1-1. Pin Descriptions

Pin Name	CSP Pin #	QFN Pin #	Power Supply	I/O	Pin Description	Internal Connection[1]	Driver	Receiver	State at Reset
					Headphone				
HS3_REF	G4	17	VP	I	**Headset Connection Reference**. Input to pseudodifferential HP output reference	—	—	—	Input
HS3	G2	20	VP	I	**Headset Connections**. Input to headset and mic-button detection functions	—	—	—	Input
HPOUTA HPOUTB	E5 G5	14 15	±VCP_FILT	O	**Headphone Audio Output.** Ground-centered audio output.	—	—	—	—
HPSENSA HPSENSB	D5 F5	— —	±VCP_FILT	I	**Headphone Audio Sense Input.** Audio sense input. WLCSP package only	—	—	—	Input
TIP_SENSE	E4	16	VP	I	**Tip Sense.** Output can be set to wake the system. Independently configurable to be debounced on plug and unplug events.	—	Hi-Z	—	—

Table 1-1. Pin Descriptions *(Cont.)*

Pin Name	CSP Pin #	QFN Pin #	Power Supply	I/O	Pin Description	Internal Connection[1]	Driver	Receiver	State at Reset
					Digital I/O				
AD0 AD1	C3 B2	27 26	VL	I	**I²C Address Input.** Address pins for I²C Instance ID [1:0] input.	—	—	Hysteresis on CMOS input	Input
ASP_LRCK/ FSYNC	B5	35	VL	I/O	**ASP Left/Right Clock or Frame Sync.** Left or right word select, or frame start sync for the ASP interface.	—	CMOS output	Hysteresis on CMOS input	Input
ASP_SCLK	B4	34	VL	I	**ASP/ Serial Data Clock.** Serial data-shift clock for the ASP interface in I²S/TDM Mode. Source clock used for internal master clock generation.	—	—	Hysteresis on CMOS input	Input
ASP_SDIN	A5	36	VL	I/O	**ASP Serial Data Input.** Serial data input and output in serial data input for the ASP interface in I²S/TDM mode.	—	CMOS output	Hysteresis on CMOS input	Input
$\overline{\text{DIGLDO\_PDN}}$	D4	4	VP	I	**Digital LDO Power Down.** Digital core logic LDO power down.	—	—	Hysteresis on CMOS input	Input
$\overline{\text{INT}}$	B7	2	VP	O	**Interrupt output.** Programmable, open-drain, active-low programmable interrupt output.	—	CMOS open-drain output	—	Output
$\overline{\text{RESET}}$	C5	1	VP	I	**Reset.** Hardware reset.	—	—	Hysteresis on CMOS input	Input
SCL	A2	29	VL	I	**I²C Clock.** Clock input for the I²C interface.	—	—	Hysteresis on CMOS input	Input
SDA	A1	28	VL	I/O	**I²C Input/Output.** I²C input and output.	—	CMOS open-drain output	Hysteresis on CMOS input	Input
VL_SEL	C4	40	VP	I	**VL Supply Voltage Select.** Select for VL power supply voltage level. Connect to VP for 1.8-V VL supply, connect to GNDD for 1.2-V VL supply	—	—	Hysteresis on CMOS input	Input
$\overline{\text{WAKE}}$	C6	3	VP	O	**Wake up.** Programmable, open-drain, active-low output. This outputs the state of the Mic S0 or HP wake detect.	—	Hi-Z, CMOS open-drain output	—	Output
					Charge Pump				
–VCP_FILT	G6	13	VCP/ VP[2]	O	**Inverting Charge Pump Filter Connection.** Power supply for the inverting charge pump that provides the negative rail for the HP amplifier.	—	—	—	—
+VCP_FILT	E6	10	VCP/ VP[2]	O	**Step Down Charge Pump Filter Connection.** Power supply for the step down charge pump that provides the positive rail for the HP amplifier.	—	—	—	—
FLYC	F7	9	VCP/ VP[2]	O	**Charge Pump Cap Common Node.** Common positive node for the HP amplifiers' step-down and inverting charge pumps' flying capacitors.	—	—	—	—
FLYN	G7	11	VCP/ VP[2]	O	**Charge Pump Cap Negative Node.** Negative node for the inverting charge pump's flying capacitor.	—	—	—	—
FLYP	E7	8	VCP/ VP[2]	O	**Charge Pump Cap Positive Node.** Positive node for HP amps' step-down charge pump's flying capacitor.	—	—	—	—
					Power				
FILT+	C1	24	VA	I	**Positive Voltage Reference.** Positive reference voltage for internal sampling circuits.	—	—	—	—
VA	B1	25	N/A	I	**Analog Power Supply.** Power supply for the internal analog section.	—	—	—	—
VCP	D6	7	N/A	I	**Charge Pump Power.** Power supply for the internal HP amplifiers charge pump.	—	—	—	—
VD_FILT	A7	39	N/A	I	**1.2-V Digital Core Power Supply.** Power supply for internal digital logic.	—	—	—	—
VL	A3	31	N/A	I	**I/O Power Supply.** Power supply for external interface and internal digital logic.	—	—	—	—

Table 1-1. Pin Descriptions *(Cont.)*

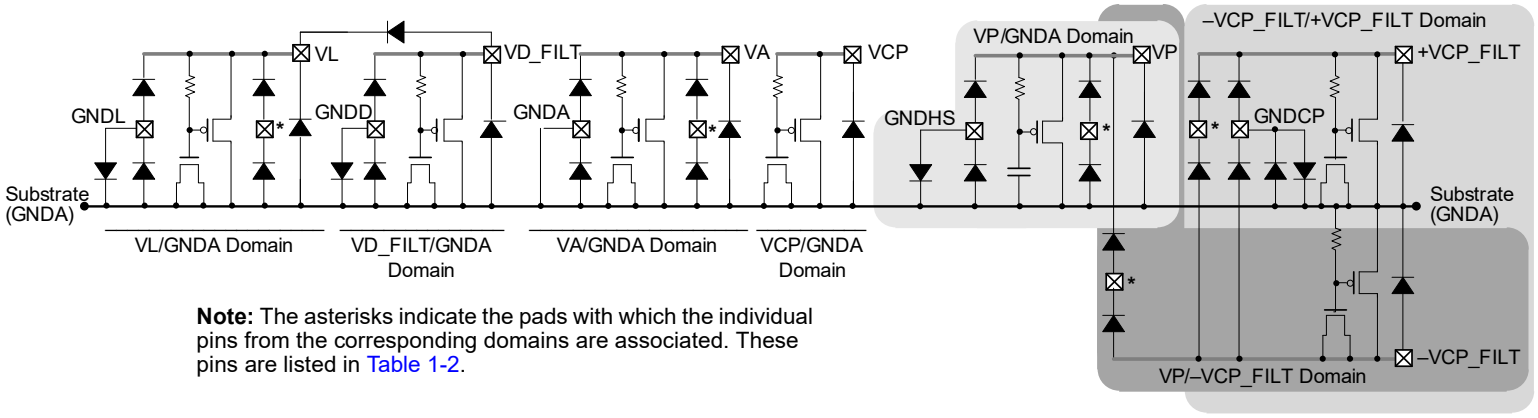
Pin Name	CSP Pin #	QFN Pin #	Power Supply	I/O	Pin Description	Internal Connection[1]	Driver	Receiver	State at Reset
VP	D7	6	N/A	I	**High Voltage Interface Supply.** Power supply for high voltage interface.	—	—	—	—
					Ground				
GNDA	C2	23	N/A	I	**Analog Ground.** Ground reference for the internal analog section.	—	—	—	—
GNDL	B3	30	N/A	I	**Digital Ground.** Ground reference for interface section.	—	—	—	—
GNDHS	G1	21	N/A	I	**Headset Ground.** Ground reference for the internal analog section.	—	—	—	—
GNDCP	F6	12	N/A	I	**Charge Pump Ground.** Ground reference for the internal HP amplifiers charge pump.	—	—	—	—
GNDD	B6	38	N/A	I	**Digital Ground.** Ground reference for the internal digital circuits.	—	—	—	—
					Test				
TSTI	C7	5	N/A	I	**Test input.** Connect to GNDD	—	—	—	—
TSTI	D3	32	VL	I	**Test input.** Connect to GNDD.	—	—	—	—
TSTI	D1, E1, E2, F1, F2, G3	—	VP	I	**Test input.** Connect to GNDA.	—	—	—	—
TSTI	D2	—	VA	I	**Test input.** Connect to GNDA.	—	—	—	—
TSTO	A4, A6	33,37	VL	O	**Test output.** No connection	—	—	—	—
TSTO	E3, F3, F4	18,19, 22	VP	O	**Test output.** No connection	—	—	—	—

1. There are no internal connections for the CS43L36.
2. The power supply is determined by ADPTPWR setting (see Section 7.10.1). VP is used if ADPTPWR = 001 (VP_CP Mode) or when necessary for ADPTPWR = 111 (Adapt-to-Signal Mode).

1.4 Electrostatic Discharge (ESD) Protection Circuitry

ESD-sensitive device. The CS43L36 is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to current JEDEC ESD standards.

Fig. 1-3 provides a composite view of the ESD domains showing the ESD protection paths between each pad and the substrate (GNDA) and the interrelations between some domains. Note that this figure represents the structure for the internal protection devices and that additional protections can be implemented as part of the integration into the board.



Note: The asterisks indicate the pads with which the individual pins from the corresponding domains are associated. These pins are listed in Table 1-2.

Figure 1-3. Composite ESD Topology

Table 1-2 shows the individual ESD domains and lists the pins associated with each domain.

Table 1-2. ESD Domains

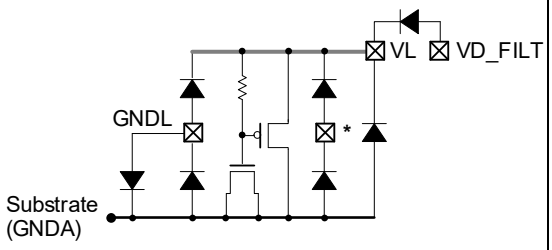
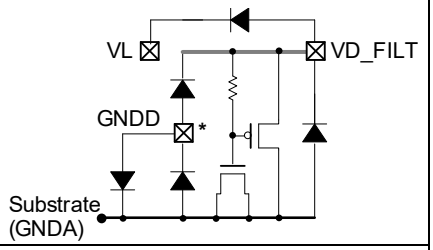
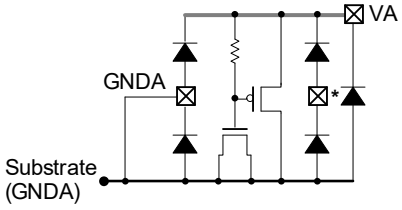
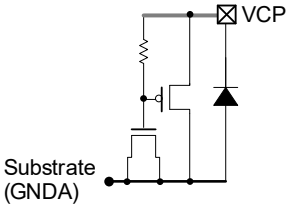
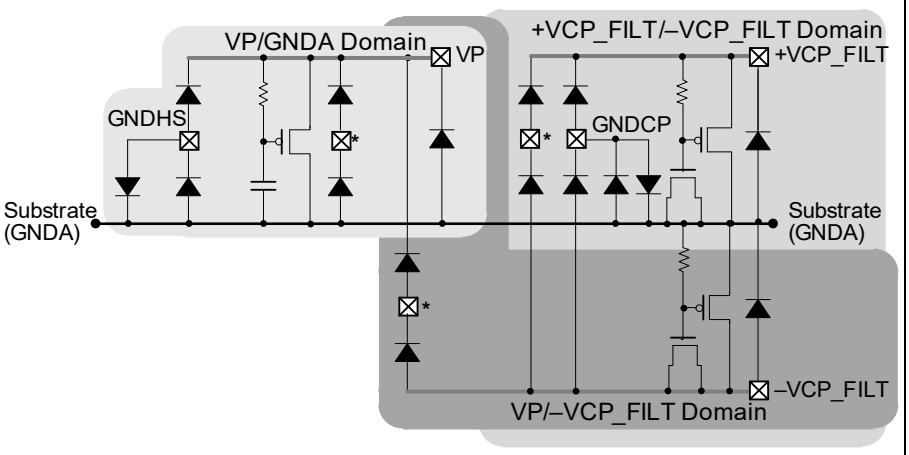
ESD Domain	Signal Name (See * in Topology Figures for Pad)	Topology
VL/ GNDA [1]	AD0 AD1 ASP_LRCK/FSYNC GNDL SCL SDA TSTO TSTO TSTI ASP_SCLK ASP_SDIN VD_FILT VL	
VD_FILT/ GNDA	VD_FILT GNDD TSTI	
VA/ GNDA	FILT+ GNDA TSTI VA	
VCP/ GNDA	VCP	

Table 1-2. ESD Domains *(Cont.)*

ESD Domain	Signal Name (See * in Topology Figures for Pad)	Topology
VP/ GNDA	GNDHS HS3 TSTO TSTI TSTI TSTO TSTO TSTI VP VL_SEL INT WAKE RESET DIGLDO_PDN	
+VCP_ FILT/ –VCP_ FILT	+VCP_FILT –VCP_FILT FLYN HPSENSA HPSENSB HPOUTA HPOUTB GNDCP	
VP/ –VCP_ FILT	FLYC FLYP HS3_REF TSTO TSTI TIP_SENSE	

1. See Section 5.5 for additional information regarding VD_FILT andVL.

2 Typical Connections

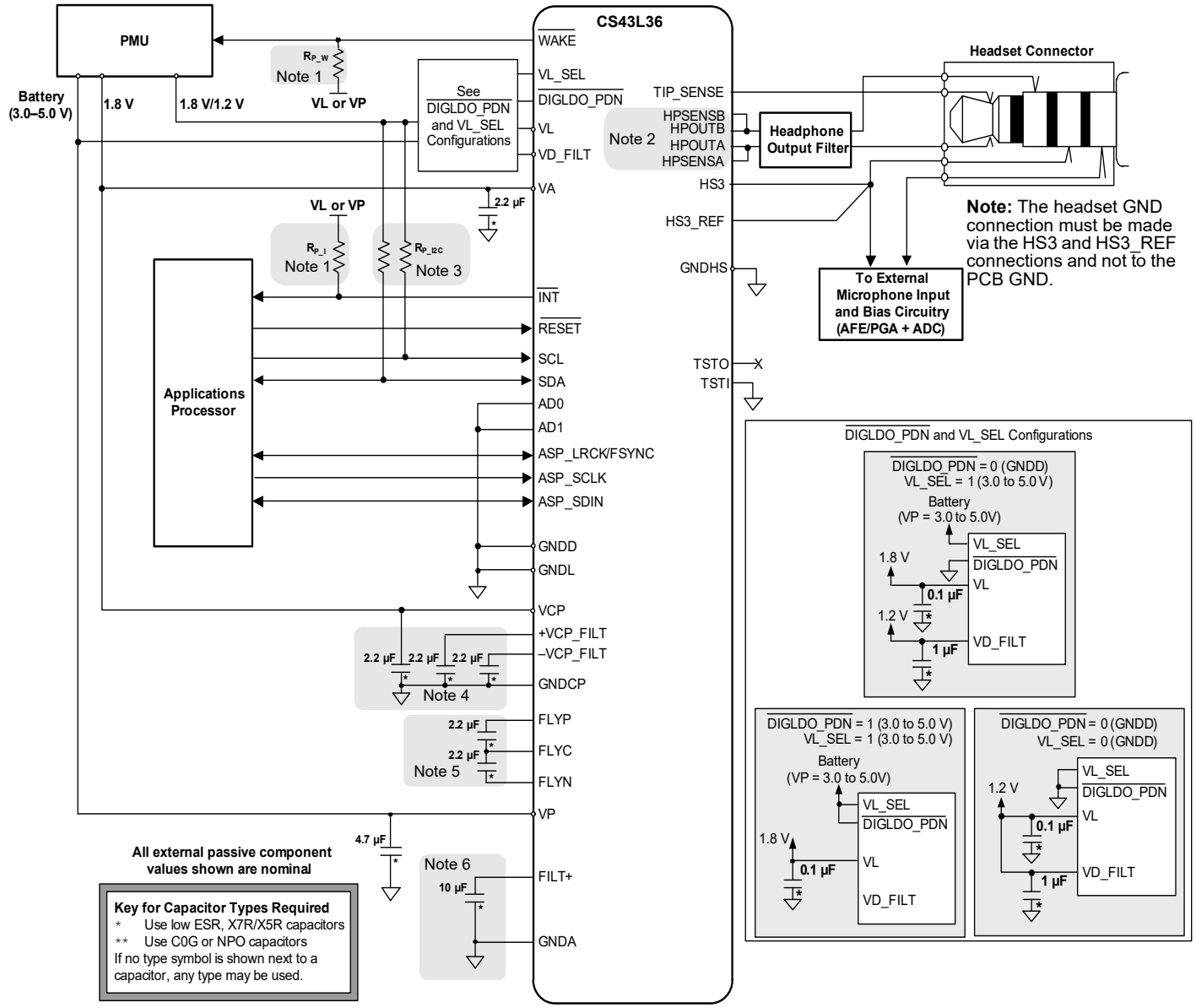


Figure 2-1. Typical Connection Diagram

Notes:

1. R_{P_I} and R_{P_W} values can be determined by the $\overline{INT}$ and $\overline{WAKE}$ pin specifications in Table 3-14.
2. HPSENSA and HPSENSB are supported only on the WLCSP package.
3. R_{P_I2C} values can be determined by the I^2C pull-up resistance specification in Table 3-13.
4. The headphone amplifier's output power and distortion ratings use the nominal capacitances shown. Larger capacitance reduces ripple on the internal amplifiers' supplies and, in turn, reduces distortion at high-output power levels. Smaller capacitance may not reduce ripple enough to achieve output power and distortion ratings. Because actual values of typical X7R/X5R ceramic capacitors deviate from nominal values by a percentage specified in the manufacturer's data sheet, capacitors must be selected for minimum output power and maximum distortion required. Higher value capacitors than those shown may be used, however lower value capacitors must not (values can vary from the nominal by ±20%). See Section 2.1.2 for additional details.
5. Series resistance in the path of the power supplies must be avoided. Any voltage drop on VCP directly affects the negative charge-pump supply (–VCP_FILT) and clips the audio output.
6. Lowering capacitance below the value shown affects PSRR, THD+N performance, and interchannel isolation and intermodulation.

2.1 Electromagnetic Compatibility (EMC) Circuitry

The circuit in Fig. 2-2 may be applied to signals not local to the CS43L36 (i.e., that traverse significant distances) for EMC.

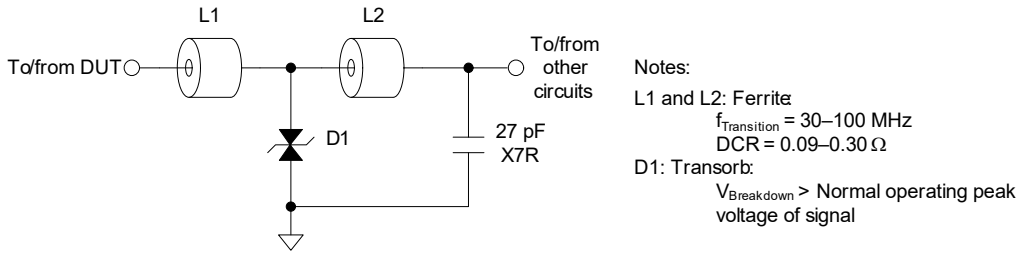


Figure 2-2. Optional EMC Circuit

2.1.1 Low-Profile Charge-Pump Capacitors

In the typical connection for analog mics (Fig. 2-1), the recommended capacitor values for the charge-pump circuitry are 2.2 µF, rated as X7R/X5R or better. The following low-profile versions of these capacitors are suitable for the application:

- Description: 2.2 µF ±20%, 6.3 V, X5R, 0201
- Manufacturer, Part Number: Murata, GRM033R60J225ME47, nominal height = 0.3 mm
- Manufacturer, Part Number: AVX, 02016D225MAT2A, nominal height = 0.33 mm

Note: Although the 0201 capacitors described are suitable, larger capacitors such as 0402 or larger may provide acceptable performance.

2.1.2 Ceramic Capacitor Derating

Note 4 in Fig. 2-1 highlights that ceramic capacitor derating factors can significantly affect in-circuit capacitance values and, in turn, CS43L36 performance. Under typical conditions, numerous types and brands of large-value ceramic capacitors in small packages exhibit effective capacitances well below their ±20% tolerance, with some being derated by as much as –50%. These same capacitors, when tested by a multimeter, read much closer to their rated value. A similar derating effect has not been observed with tantalum capacitors.

The derating observed varied with manufacturer and physical size: Larger capacitors performed better, as did ones from Kemet Electronics Corp. and TDK Corp. of any size. This derating effect is described in data sheets and in applications notes from capacitor manufacturers. For instance, as DC and AC voltages are varied from the standard test points (applied DC and AC voltages for standard test points versus PSRR test are 0 and 1 V_{RMS} @ 1 kHz versus 0.9 V and ~1 mV_{RMS} @ 20 Hz–20 kHz), it is documented that the capacitances vary significantly.

3 Characteristics and Specifications

Table 3-1 defines parameters as they are characterized in this section.

Table 3-1. Parameter Definitions

Parameter	Definition
Dynamic range	The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. A signal-to-noise ratio measurement over the specified bandwidth made with a –60 dB signal; 60 dB is added to resulting measurement to refer the measurement to full scale. This technique ensures that distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17–1991, and the Electronic Industries Association of Japan, EIAJ CP–307. Dynamic range is expressed in decibel units.
Idle channel noise	The rms value of the signal with no input applied (properly back-terminated analog input, digital zero, or zero modulation input). Measured over the specified bandwidth.
Interchannel isolation	A measure of cross talk between the left and right channel pairs. Interchannel isolation is measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Interchannel isolation is expressed in decibel units.
Load resistance and capacitance	The recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. The load capacitance effectively moves the band-limiting pole of the amp in the output stage. Increasing load capacitance beyond the recommended value can cause the internal op-amp to become unstable.
Offset error	The deviation of the midscale transition (111…111 to 000…000) from the ideal.
Output offset voltage	The DC offset voltage present at the amplifier's output when its input signal is in a mute state. The offset exists due to CMOS process limitations and is proportional to analog volume settings. When measuring the offset out the headphone amplifier, the headphone amplifier is ON.
Total harmonic distortion + noise (THD+N)	The ratio of the rms sum of distortion and noise spectral components across the specified bandwidth (typically 20 Hz–20 kHz) relative to the rms value of the signal. THD+N is measured at –1 and –20 dBFS for the analog input and at 0 and –20 dB for the analog output, as suggested in AES17–1991 Annex A. THD+N is expressed in decibel units.

Table 3-2. Recommended Operating Conditions

Test conditions: GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground.

Parameters		Symbol	Minimum [1]	Maximum [1]	Unit
DC power supply	Charge pump	VCP	1.66	1.94	V
	LDO regulator for digital [2] $\overline{\text{DIGLDO\_PDN}}$ = 0 and VL_SEL = 0	VD_FILT	1.10	1.30	V
	Serial interface control port $\overline{\text{DIGLDO\_PDN}}$ = 0 and VL_SEL = 0 VL_SEL = 1	VL VL	1.10 1.66	1.30 1.94	V V
	Analog	VA	1.66	1.94	V
	Battery supply	VP	2.50 [3]	5.25	V
External voltage applied to pin [4,5]	TIP_SENSE pin	V_{INHI}	–VCP_FILT – 0.3	VP + 0.3	V
	±VCP_FILT domain pins [6]	V_{VCPF}	–VCP_FILT – 0.3	+VCP_FILT + 0.3	V
	VL domain pins	V_{VL}	–0.3	VL + 0.3	V
	VA domain pins	V_{VA}	–0.3	VA + 0.3	V
	VP domain pins	V_{VP}	–0.3	VP + 0.3	V
Ambient temperature		T_A	–40	+85	°C

1. Device functional operation is guaranteed within these limits; operation outside them is not guaranteed or implied and may reduce device reliability.
2. If $\overline{\text{DIGLDO\_PDN}}$ is deasserted, no external voltage must be applied to VD_FILT.
3. Although device operation is guaranteed down to 2.5 V, device performance is guaranteed only down to 3.0 V. The following are affected when VP < 3.0 V: charge pump LDO, TIP_SENSE threshold.
4. The maximum over/undervoltage is limited by the input current.
5. Table 1-1 lists the power supply domain in which each CS43L36 pin resides.
6. ±VCP_FILT is specified in Table 3-8.

Table 3-3. Absolute Maximum Ratings

Test conditions: GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground.

Parameters		Symbol	Minimum	Maximum	Unit
DC power supply	Charge pump, LDO, serial/control, analog (see Section 4.9)	VL, VA, VCP	–0.3	2.33	V
	Digital core	VD_FILT	–0.3	1.55	V
	Battery	VP	–0.3	6.3	V
Input current [1]		I_{in}	—	±10	mA
Ambient operating temperature (power applied)		T_A	–50	+115	°C
Storage temperature		T_{stg}	–65	+150	°C

Caution: Stresses beyond "Absolute Maximum Ratings" levels may cause permanent damage to the device. These levels are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Table 3-2, "Recommended Operating Conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. Any pin except supply pins. Transient currents of up to ±100 mA on analog input pins do not cause SCR latch-up.

Table 3-4. Combined DAC Digital, On-Chip Analog, and HPOUTx Filter Characteristics

Test conditions (unless specified otherwise): T_A = +25°C; MCLK = 12 MHz, MCLK_SRC_SEL = 0, Fs_{INT} = 48 kHz; path is internal routing engine to HPOUTx, analog and digital gains are all set to 0 dB; HPF disabled.

Parameter [1]	Minimum	Typical	Maximum	Unit
Passband –0.05-dB corner	—	0.48	—	Fs_{INT}
Passband –3.0-dB corner	—	0.50	—	Fs_{INT}
Passband ripple ($0.417x10^{-3}$ Fs_{INT} to 0.417 Fs_{INT}; normalized to $0.417x10^{-3}$ Fs_{INT})	–0.04	—	0.063	dB
Stopband attenuation (0.545 Fs_{INT} to Fs_{INT})	60	—	—	dB
Total group delay [2]	—	$5.35/Fs_{INT}$	—	s

1. Response scales with Fs_{INT} (based on internal MCLK). Specifications are normalized to Fs_{INT} and denormalized by multiplying by Fs_{INT}.
2. Informational only; group delay cannot be measured for this block by itself. An additional $5.5/Fs_{int}$ group delay may be present through the serial ports and internal audio bus.

Table 3-5. DAC High-Pass Filter (HPF) Characteristics

Test conditions (unless specified otherwise) Analog and digital gains are all set to 0 dB; T_A = +25°C.

Parameter [1]	Minimum	Typical	Maximum	Unit
Passband –0.05-dB corner	—	$0.180x10^{-3}$	—	Fs_{INT}
Passband –3.0-dB corner	—	$19.5x10^{-6}$	—	Fs_{INT}
Passband ripple ($0.417x10^{-3}$ Fs_{INT} to 0.417 Fs_{INT}; normalized to 0.417 Fs_{INT})	—	—	0.01	dB
Phase deviation @ $0.453x10^{-3}$ Fs_{INT}	—	2.45	—	°
Filter settling time [2]	—	$24.5x10^3/Fs_{INT}$	—	s

1. Response scales with Fs_{INT} (internal sample rate, based on MCLK). Specifications are normalized to Fs_{INT} and are denormalized by multiplying by Fs_{INT}.
2. Required time for the magnitude of the DC component present at the output of the HPF to reach 5% of the applied DC signal.

Table 3-6. SDIN to HPOUTx with SRC-Enabled Datapath Characteristics

Test conditions (unless specified otherwise): LRCK = Fs_{INT} = Fs_{EXT} = 48 kHz; MCLK = 12 MHz; HPF disabled; passband/stopband levels normalized to $0.417x10^{-3}$ Fs_{EXT}; entire path characteristics including serial port + SRC + DAC + HPOUT.

Parameters [1]	Minimum	Typical	Maximum	Unit
Passband –0.2-dB corner	—	0.463	—	Fs_{EXT}
Passband –3.0-dB corner	—	0.466	—	Fs_{EXT}
Passband ripple ($0.417x10^{-3}$ Fs_{EXT} to 0.417 Fs_{EXT}; normalized to $0.417x10^{-3}$ Fs_{EXT})	–0.16	—	0.02	dB
Response at 0.5 Fs_{EXT}	—	—	–54.9	dB
Stopband rejection from 0.480 Fs_{EXT} to 0.524 Fs_{EXT}	55	—	—	dB
Stopband rejection from 0.524 Fs_{EXT} to 0.545 Fs_{EXT}	39	—	—	dB
Stopband rejection from 0.545 Fs_{EXT} to 3 Fs_{EXT}	60	—	—	dB
Square wave overshoot	—	—	3.1	dB
Group delay, bark-weighted average	—	—	$34/Fs_{EXT}$	s
Group delay $Fs_{EXT} \le$ 48 kHz	—	$(15.8 \pm 1.5)/Fs_{EXT} + 10.3/Fs_{INT}$	—	s
$Fs_{EXT} \ge$ 88.2 kHz)	—	$(20.1 \pm 1)/Fs_{EXT} + (11.6 \pm 0.5)/Fs_{INT}$	—	s
SRC disabled group delay [2]	—	(15±1)/Fs	—	s

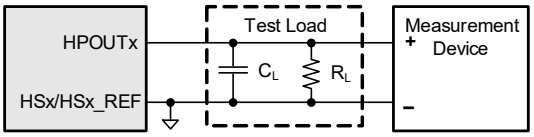
1. Fs_{EXT} is the external sample rate (LRCK/FSYNC frequency). Response scales with Fs_{EXT}.
2. This value varies by up to 1 Fs. If SRC is disabled, Fs = Fs_{OUT} = Fs_{IN}.

Table 3-7. Serial Data In-to-HPOUTx Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43L36 connections; input test signal is a 24-bit full-scale 997-Hz sine wave with 1 LSB of triangular PDF dither applied; GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground; parameters can vary with VA; typical performance data taken with VL = VA = 1.8 V, VP = 3.6 V; min/max performance data taken with VA = 1.66–1.94 V; VL = 1.8 V, VP = 3.6 V; VCP Mode; T_A = +25°C; measurement bandwidth is 20 Hz–20 kHz; ASP_LRCK = Fs_{INT} = 48-kHz mode; MCLK = 12 MHz, MCLK_SRC_SEL = 0; volume = 0 dB; FULL_SCALE_VOL = 0 (0dB); HP load: R_L = 30 Ω, C_L = 1 nF (HPOUT_LOAD = 0) and R_L = 3 kΩ, C_L = 10 nF (HPOUT_LOAD = 1)SRC bypassed.

Parameter [1]				Minimum	Typical	Maximum	Unit
R_L = 3 kΩ VP_CP Mode	Dynamic range (defined in Table 3-1)	18–24 bit	A-weighted	108	114	—	dB
			unweighted	105	111	—	dB
	THD+N [2] (defined in Table 3-1)	18–24 bit	0 dB	—	–90	–84	dB
			–20 dB	—	–83	—	dB
			–60 dB	—	–51	–48	dB
		16 bit	0 dB	—	–88	–82	dB
			–20 dB	—	–73	—	dB
			–60 dB	—	–33	–27	dB
	Idle channel noise (A-weighted)			—	2.0	—	µV
	Full-scale output voltage [3]			1.50•VA	1.58•VA	1.66•VA	V_{PP}
R_L = 30 Ω VP_CP Mode	Dynamic range (defined in Table 3-1)	18–24 bit	A-weighted	108	114	—	dB
			unweighted	105	111	—	dB
	THD+N [2] (defined in Table 3-1)		Pout = 10 mW	—	–98	—	dB
			Pout = 35 mW	—	–75	–69	dB
	Full-scale output voltage [3]			1.50•VA	1.58•VA	1.66•VA	V_{PP}
	Output power [2]			—	35.0	—	mW
R_L = 15 Ω VCP Mode (FULL_SCALE_ VOL = 1 [–6 dB])	Dynamic range (defined in Table 3-1)	18–24 bit	A-weighted	102	108	—	dB
			unweighted	99	105	—	dB
	THD+N [2] (defined in Table 3-1)		Pout = 17.3 mW	—	–75	–69	dB
	Full-scale output voltage [3]			0.71•VA	0.79•VA	0.86•VA	V_{PP}
	Output power [2]			—	17.3	—	mW
R_L = 15 Ω VP_CP Mode	Dynamic range	18–24 bit	A-weighted	102	108	—	dB
			unweighted	99	105	—	dB
Other characteristics (Table 3-1 gives parameter definitions.)	Interchannel isolation [3] (3 kΩ)		217 Hz	—	90	—	dB
			1 kHz	—	90	—	dB
			20 kHz	—	80	—	dB
	Interchannel isolation [3] (30 Ω)		217 Hz	—	90	—	dB
			1 kHz	—	90	—	dB
			20 kHz	—	70	—	dB
	Output offset voltage: mute [3,4] (ANA_MUTE_x = 1, see p. 76)		HPOUTx	—	±0.5	±1.0	mV
	Output offset voltage [3,4]		HPOUTx	—	±0.5	±2.5	mV
	Load resistance (R_L)		Normal operation [3]	15	—	—	Ω
	Load capacitance (C_L) [3,5]		HPOUT_LOAD = 0	—	—	1	nF
			HPOUT_LOAD = 1	—	—	10	nF
	Turn-on time [6]		SLOW_START_EN = 000	—	—	25	ms

1. One LSB of triangular PDF dither is added to data.
2. Because VCP settings lower than VA reduce the HP amplifier headroom, the specified THD+N performance at full-scale output voltage and power may not be achieved.
3. HP output test configuration. Symbolized component values are specified in the test conditions above.



4. Assumes no external impedance on HSx/HSx_REF. External impedance on HSx/HSx_REF affects the offset and step deviation. See Section 4.2.1.
5. Amplifier is guaranteed to be stable with either headphone load setting.
6. Turn-on time is measured from when the HP_PDN = 0 ACK signal is received to when the signal appears on the HP output. In most cases, enabling the SRC increases the turn-on time and may exceed the maximum specified value.

Table 3-8. DC Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43L36 connections; GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground; VL = VCP = VA = 1.8 V, VP = 3.6 V; T_A = +25°C.

Parameters			Minimum	Typical	Maximum	Unit
VCP_FILT (No load connected to HPOUTx.)	VP_CP Mode (ADPTPWR = 001)	+VCP_FILT	—	2.6	—	V
		–VCP_FILT	—	–2.6	—	V
	VCP Mode (ADPTPWR = 010)	+VCP_FILT	—	VCP	—	V
		–VCP_FILT	—	–VCP	—	V
	VCP/2 Mode (ADPTPWR = 011)	+VCP_FILT	—	VCP/2	—	V
		–VCP_FILT	—	–VCP/2	—	V
	VCP/3 Mode (ADPTPWR = 100)	+VCP_FILT	—	VCP/3	—	V
		–VCP_FILT	—	–VCP/3	—	V
HS3 ground switch resistance (Typical values have ±25% tolerance.)			—	0.5	—	Ω
Other DC filter	FILT+ voltage		—	VA	—	V
	HP output current limiter on threshold. See Section 4.3.4. [1]		80	115	160	mA
	VD_FILT and VL power-on reset threshold (V_{POR})	Up	—	0.777	—	V
		Down	—	0.628	—	V
HPOUT pull-down resistance [2,3]	HPOUT_PULLDOWN = 0000–0111, 1100		—	0.9	—	kΩ
	HPOUT_PULLDOWN = 1001		—	9.3	—	kΩ
	HPOUT_PULLDOWN = 1010		—	5.8	—	kΩ

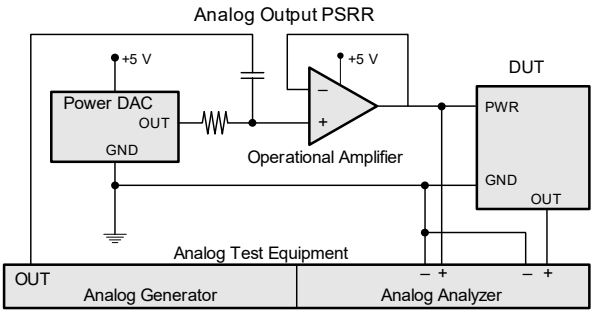
1. The HP output current limiter threshold spec is valid only while the Class H rails are in VCP Mode.
2. Typical values have ±20% tolerance.
3. Clamp is disabled (HPOUT_CLAMP = 1) and channel is powered down (HPOUT_PDN = 1).

Table 3-9. Power-Supply Rejection Ratio (PSRR) Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43L36 connections; input test signal held low (all zero data); GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground; VL = VA = 1.8 V, VP = 3.6 V; T_A = +25°C.

Parameters [1]		Minimum	Typical	Maximum	Unit
HPOUTx (–6-dB analog gain) PSRR with 100-mVpp signal AC coupled to VA supply [2]	217 Hz	—	75	—	dB
	1 kHz	—	75	—	dB
	20 kHz	—	70	—	dB
HPOUTx (–6-dB analog gain) PSRR with 100-mVpp signal AC-coupled to VCP supply [2]	217 Hz	—	85	—	dB
	1 kHz	—	85	—	dB
	20 kHz	—	65	—	dB
HPOUTx (0-dB analog gain) PSRR with 100-mVpp signal AC coupled to VP supply	217 Hz	—	80	—	dB
	1 kHz	—	80	—	dB
	20 kHz	—	60	—	dB

1. PSRR test configuration: Typical PSRR can vary by approximately 6 dB below the indicated values.



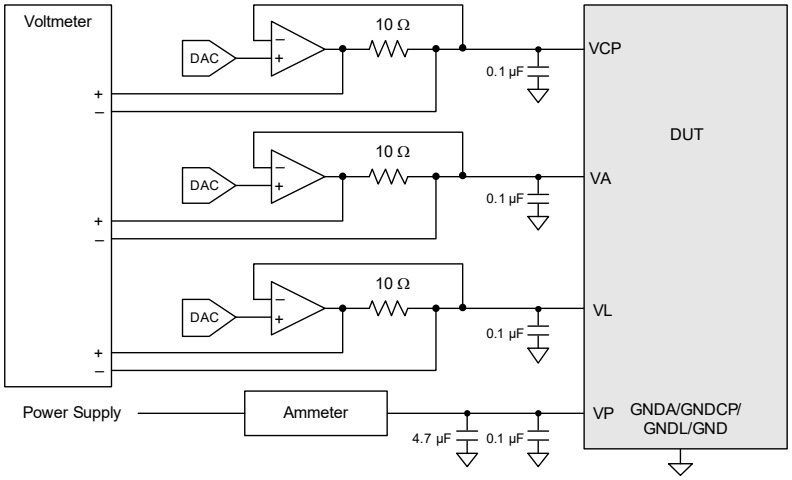
2. No load connected to any analog outputs.

Table 3-10. Power Consumption

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43L36 connections; GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground; performance data taken with VA = VCP = VL = 1.8 V; DIGLDO_PDN is deasserted; VP = 3.6 V; T_A = +25°C; ASP_LRCK = 48-kHz Mode; Fs_{INT} = 48 kHz; SCLK = 12 MHz, MCLK_SRC_SEL = 0; volume= 0 dB; FULL_SCALE_VOL = 1 (–6 dB) for HPOUTx, TIP_SENSE_CTRL = 11, all other fields are set to defaults; no signal on any input; control port inactive; input clock/data are held low when not required; test load is R_L = 30 Ω and C_L = 1 nF for HPOUTx; measured values include currents consumed by the DAC and do not include current delivered to external loads unless specified otherwise (e.g., HPOUTx); see Fig. 3-1.

Use Cases			Class H Mode	Typical Current (µA)				Total Power (µW)
				i_{VA}	i_{VCP}	i_{VL}	i_{VP}	
1	A	Off [1]	—	0	0	0	3.1	11.16
2	A	Standby [2,3]	—	0	0	0	20	72.0
3	A	Standby (RCO Mode) [4,5]	—	0	0	343	31	729
4	A	Playback — Stereo HPOUT (no signal, HPOUT_LOAD = 0)	VCP/3	1413	1204	858	58	6464
	B	Stereo HPOUT (0.1 mW, HPOUT_LOAD = 0)	VCP/3	1441	2336	965	58	8744

1. Off configuration: Clock/data lines held low; $\overline{\text{RESET}}$ = LOW; VA = VL = VCP = 0 V; VP = 3.6 V.
2. Standby configuration: Clock/data lines held low; VA = VL = VCP = 0 V; VP = 3.6 V; M_HP_WAKE = 0 (unmasked).
3. SCLK_PRESENT = 1.
4. SCLK_PRESENT = 0 (RCO clocking).
5. Standby configuration (RCO clocking): Clock/data lines held low; VA = 0 V; VL = 1.8 V, VCP = 0 V, VP = 3.6 V; M_HP_WAKE = 0 (unmasked).



Note: The current draw on the VA, VCP, and VL power supply pins is derived from the measured voltage drop across a 10-Ω series resistor between the associated supply source and each voltage supply pin. Given the larger currents that are possible on the VP supply, an ammeter is used for the measurement.

Figure 3-1. Power Consumption Test Configuration

Table 3-11. Register Field Settings

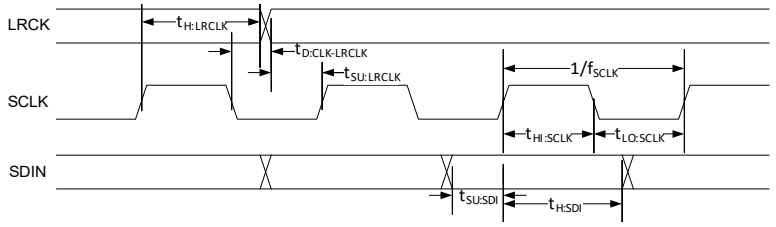
Use Cases		Register Fields and Settings				
		PDN_ALL	ASP_DAI_PDN	HP_PDN		Class H Mode p. 23
1	A	—	—	—		—
2	A	1	—	—		—
3	A	1	—	—		—
4	A	0	0	0		VCP/3
	B	0	0	0		VCP/3

Table 3-12. Digital Audio Interface Timing Characteristics

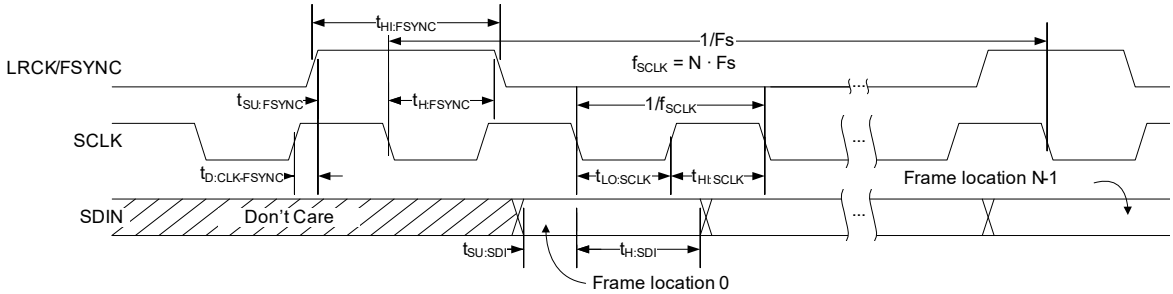
Test conditions (unless specified otherwise): GNDA = GNDL = GNDCP = 0 V; all voltages with respect to ground; values are for both VL = 1.2 and 1.8 V; inputs: Logic 0 = GNDL = 0 V, Logic 1 = VL; T_A = +25°C; C_{LOAD} = 30 pF (for VL = 1.2 V) and 60 pF (for VL = 1.8 V); input timings are measured at V_{IL} and V_{IH} thresholds; output timings are measured at V_{OL} and V_{OH} thresholds (see Table 3-14); ASP_TX_HIZ_DLY = 00.

Parameters [1,2,3]			Symbol	Minimum	Typical	Maximum	Unit
ASP_SCLK frequency [4]			f_{SCLK}	0.973 [5]	—	25.81	MHz
SCLK high period [4]			$t_{HI:SCLK}$	18.5	—	—	ns
SCLK low period [4]			$t_{LO:SCLK}$	18.5	—	—	ns
SCLK duty cycle [4]			—	45	—	55	%
Hybrid-Master Mode	FSYNC/LRCK frame rate		—	0.99	—	1.01	Fs
	LRCK duty cycle		—	45	—	55	%
	FSYNC high period [6]		$t_{HI:FSYNC}$	1/f_{SCLK}	—	(n–1)/f_{SCLK}	s
	FSYNC/LRCK delay time after SCLK launching edge [7]	VL = 1.8 V VL = 1.2 V	$t_{D:CLK–LRCK}$	0 0	— —	15 17	ns ns
	SDIN setup time before SCLK latching edge [7]		$t_{SU:SDI}$	10	—	—	ns
	SDIN hold time after SCLK latching edge [7]		$t_{H:SDI}$	5	—	—	ns
Slave Mode	FSYNC/LRCK frame rate		—	0.99	—	1.01	Fs
	FSYNC/LRCK duty cycle		—	45	—	55	%
	FSYNC/LRCK setup time before SCLK latching edge [7]		$t_{SU:LRCK}$	10	—	—	ns
	FSYNC/LRCK hold time after SCLK latching edge [7]		$t_{H:LRCK}$	5	—	—	ns
	SDIN hold time after SCLK latching edge [7]		$t_{H:SDI}$	5	—	—	ns
	FSYNC/LRCK duty cycle		—	45	—	55	%

1. Output clock frequencies follow SCLK frequency proportionally. Deviation of the bit-clock source from nominal supported rates is directly imparted to the output clock rate by the same factor (e.g., +100-ppm offset in the frequency of SCLK becomes a +100-ppm offset in MCLK and LRCK).
2. I²S interface timing



3. TDM interface timing



4. SCLK is mastered from an external device. The external device is expected to maintain SCLK timing specifications.
5. SCLK operation below 2.8224 MHz may result in degraded performance.
6. Maximum LRCK duty cycle is equal to frame length, in SCLK periods, minus 1. Maximum duty cycle occurs when LRCK_HI is set to 511 SCLK periods and LRCK period is set to 512 SCLK periods.
7. Data is latched on the rising or falling edge of SCLK, as determined by ASP_SCPOL_IN_x and ASP_FSD (See Section 7.3.6 and Section 7.3.7).

Table 3-13. I²C Slave Port Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows typical connections; Inputs: GNDA = GNDL = GNDCP = 0 V; all voltages with respect to ground; min/max performance data taken with VL = 1.66–1.94 V (VL_SEL = VP) or VL = 1.1–1.3 V (VL_SEL = GNDD); inputs: Logic 0 = GNDA = 0 V, Logic 1 = VL; T_A = +25°C; SDA load capacitance equal to maximum value of C_B = 400 pF; minimum SDA pull-up resistance, $R_{P(min)}$.[1] Table 3-1 describes some parameters in detail. All specifications are valid for the signals at the pins of the CS43L36 with the specified load capacitance.

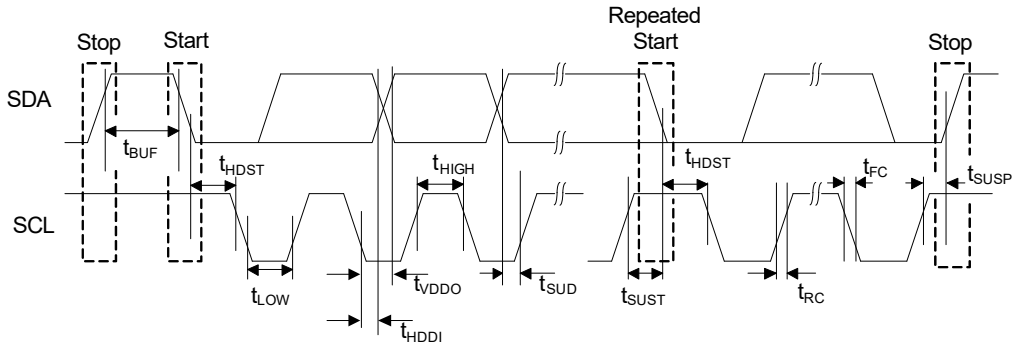
Parameter [2]		Symbol [3]	Minimum	Maximum	Unit
SCL clock frequency		f_{SCL}	—	1000	kHz
Clock low time		t_{LOW}	500	—	ns
Clock high time		t_{HIGH}	260	—	ns
Start condition hold time (before first clock pulse)		t_{HDST}	260	—	ns
Setup time for repeated start		t_{SUST}	260	—	ns
Rise time of SCL and SDA	Standard Mode Fast Mode Fast Mode Plus	t_{RC}	— — —	1000 300 120	ns ns ns

Table 3-13. I²C Slave Port Characteristics *(Cont.)*

Test conditions (unless specified otherwise): Fig. 2-1 shows typical connections; Inputs: GNDA = GNDL = GNDCP = 0 V; all voltages with respect to ground; min/max performance data taken with VL = 1.66–1.94 V (VL_SEL = VP) or VL = 1.1–1.3 V (VL_SEL = GNDD); inputs: Logic 0 = GNDA = 0 V, Logic 1 = VL; T_A = +25°C; SDA load capacitance equal to maximum value of C_B = 400 pF; minimum SDA pull-up resistance, $R_{P(min)}$.[1] Table 3-1 describes some parameters in detail. All specifications are valid for the signals at the pins of the CS43L36 with the specified load capacitance.

Parameter [2]		Symbol [3]	Minimum	Maximum	Unit
Fall time of SCL and SDA	Standard Mode Fast Mode Fast Mode Plus	t_{FC}	— — —	300 300 120	ns ns ns
Setup time for stop condition		t_{SUSP}	260	—	ns
SDA setup time to SCL rising		t_{SUD}	50	—	ns
SDA input hold time from SCL falling [4]		t_{HDDI}	0	—	ns
Output data valid (Data/Ack) [5]	Standard Mode Fast Mode Fast Mode Plus	t_{VDDO}	— — —	3450 900 450	ns ns ns
Bus free time between transmissions		t_{BUF}	500	—	ns
SDA bus capacitance	Fast Mode Plus Standard Mode, Fast Mode	C_B	— —	550 400	pF pF
SCL/SDA pull-up resistance [1]	VL = 1.2 V VL = 1.8 V	R_P	200 250	— —	Ω Ω
Switching time between RCO and PLL or SCLK [6]		—	150	—	µs

1. The minimum R_P value (see Fig. 2-1) is determined by using the maximum VL level, the minimum sink current strength of its respective output, and the maximum low-level output voltage, V_{OL}. The maximum R_P value may be determined by how fast its associated signal must transition (e.g., the lower the R_P value, the faster the I²C bus can operate for a given bus load capacitance). See the I²C bus specification referenced in Section 13.
2. All timing is relative to thresholds specified in Table 3-14, V_{IL} and V_{IH} for input signals, and V_{OL} and V_{OH} for output signals.
3. I²C control-port timing



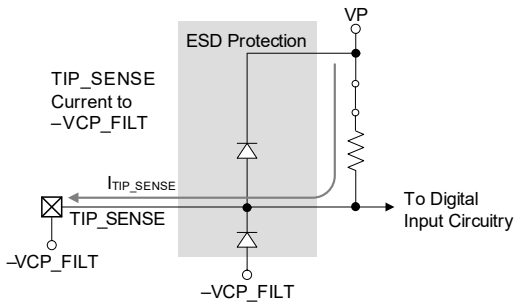
4. Data must be held long enough to bridge the SCL transition time, t_F.
5. Time from falling edge of SCL until data output is valid.
6. The switch between RCO and either SCLK or PLL occurs upon setting/clearing SCLK_PRESENT (see p. 63) and sending the I²C stop condition. An SCLK_PRESENT transition (0 to 1 or 1 to 0) starts a switch between RCO and the selected SCLK or PLL. An I²C stop condition is sent, after which a wait time of at least 150 µs is required before the next I²C transaction can begin using the newly selected clock.

Table 3-14. Digital Interface Specifications and Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows CS43L36 connections; GNDD = GNDCP = GNDA = 0 V; voltages are with respect to ground; parameters can vary with VL and VP; min/max performance data taken with VCP = VA = 1.8 V, VD_FILT = 1.2 V; VP = 3.0–5.25 V; VL = 1.66–1.94 V (VL_SEL = VP) or VL = 1.1–1.3 V (VL_SEL = GNDD); T_A = +25°C; C_L = 60 pF.

Parameters [1]		Symbol	Min	Max	Unit
Input leakage current [2,3]	ASP_LRCK/FSYNC	I_{in}	—	±4	µA
	ASP_SCLK,ASP_SDIN		—	±3	µA
	TIP_SENSE		—	±100	nA
	SDA, SCL		—	±100	nA
	INT, WAKE, RESET		—	±100	nA
Internal weak pull-down		—	550	2450	kΩ
Input capacitance [2]		—	—	10	pF
INT or WAKE current sink (V_{OL} = 0.3 V maximum)		—	825	—	µA
VL Logic (non-I²C)	High-level output voltage (I_{OH} = –100 µA)	V_{OH}	0.9*VL	—	V
	Low-level output voltage	V_{OL}	—	0.1*VL	V
	High-level input voltage	V_{IH}	0.7*VL	—	V
	Low-level input voltage	V_{IL}	—	0.3*VL	V
VL Logic (I²C only)	Low-level output voltage	V_{OL}	—	0.2*VL	V
	High-level input voltage	V_{IH}	0.7*VL	—	V
	Low-level input voltage	V_{IL}	—	0.3*VL	V
	Hysteresis voltage	V_{HYS}	0.05*VL	—	V
VP Logic (excluding TIP_SENSE)	Low-level output voltage	V_{OL}	—	0.2	V
	High-level input voltage	V_{IH}	0.9	—	V
	Low-level input voltage	V_{IL}	—	0.2	V
TIP_SENSE [4]	High-level input voltage	V_{IH}	0.87*VP	—	V
	Low-level input voltage	V_{IL}	—	2.0	V
TIP_SENSE current to –VCP_FILT [4]	TIP_SENSE_CTRL = 11 (Short-Detect Mode)	I_{TIP_SENSE}	1.00	2.91	µA

1. See Table 1-1 for serial and control-port power rails.
2. Specification is per pin. The CS43L36 is not a low-leakage device, per the *MIPI Specification*. See Section 13.
3. Includes current through internal pull-up or pull-down resistors on pin.
4. TIP_SENSE input circuit. This circuit allows the TIP_SENSE signal to go as low as –VCP_FILT and as high as VP. Section 4.8.2 provides configuration details.



4 Functional Description

This section provides a general description of the CS43L36 architecture and detailed functional descriptions of the various blocks that make up the CS43L36. Fig. 4-1 shows the flow of signals through the CS43L36 and gives links to detailed descriptions of the respective sections.

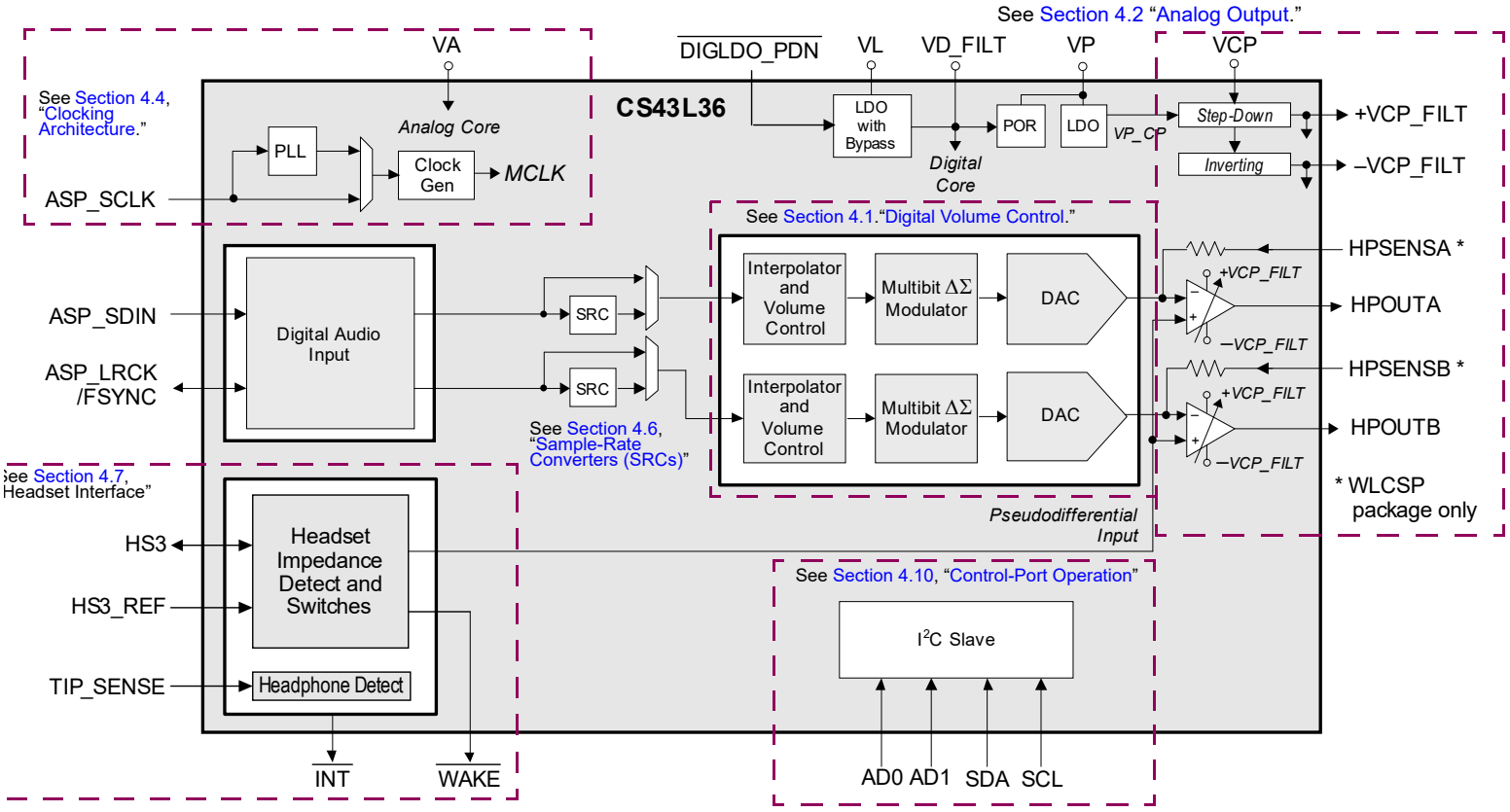


Figure 4-1. Overview of Signal Flow

The CS43L36 is an ultralow-power stereo DAC. The DAC feeds a stereo pseudodifferential output amplifier. The converters operate at a low oversampling ratio, maximizing power savings while maintaining high performance.

The serial data interface ports operate either at standard audio-sample rates as timing slaves or in Hybrid-Master Mode as a bit-clock slave generating LRCK internally. An onboard fractional-N PLL can be used to generate the internal-core timing ($MCLK_{INT}$) if the SCLK source is not one of the following rates (where N = 2 or 4):

- N x 5.6448 or 6.1440 MHz
- USB rates (N x 6 MHz)

The CS43L36 significantly reduces overall power consumption, with a very low-voltage digital core and with low-voltage Class H amplifiers (powered from an integrated LDO regulator and a step-down/inverting charge pump, respectively). The CS43L36 comprises the following subblocks:

- Volume control, described in Section 4.1, uses selectable attenuation to provide relative volume control and to avoid clipping.
- Analog outputs. The analog output block, described in Section 4.2, includes separate pseudodifferential headphone Class H amplifiers. An on-chip step-down/inverting charge pump creates a positive and negative voltage equal to the input or to either one-half or one-third of the input supply for the amplifiers, allowing an adaptable, full-scale output swing centered around ground. The resulting internal amplifier supply can be ±VCP/3, ±VCP/2, ±VCP, or ±2.5 V.

  The inverting architecture eliminates the need for large DC-blocking capacitors and allows the amplifier to deliver more power to HP loads at lower supply voltages. The step-down architecture allows the amplifier's power supply to adapt to the required output signal. This adaptive power-supply scheme converts traditional Class AB amplifiers into more power-efficient Class H amplifiers.

- Class H amplifier. The HP output amplifiers, described in Section 4.3, use a patented Cirrus Logic four-mode Class H technology that maintains high performance and maximizes operating efficiency of a typical Class AB amplifier.
- Clocking architecture. Described in Section 4.4, the clock for the device can be supplied internally from an integrated fractional-N PLL using ASP_SCLK/ as the source clock or the internal PLL can be bypassed and derived directly from the input pin.
- Serial port. The CS43L36 TDM/I²S (ASP) port is a highly configurable serial port. See Section 4.5.

  The ASP can operate in TDM Mode, which includes full-duplex communication, flexible data structuring via control port registers, clock slave mode, and higher bandwidth, enabling more data to be transferred to and from the device.
- Sample-rate converters (SRCs). SRCs, described in Section 4.6, are used to bridge different sample rates at the serial ports within the digital-processing core. SRCs can be bypassed.
- Headset interface. This interface is described in Section 4.7.
- Power management. Several control registers provide independent power-down control of the analog and digital sections of the CS43L36, allowing operation in select applications with minimal power consumption. Power management considerations are described in Section 4.9.
- Control-port operation. The control port, described in Section 4.10, provides access to the registers for configuring the DAC. The control port operation may be completely asynchronous with respect to the audio sample rates. To avoid potential interference problems, control-port data pins must remain static if no operation is required.
- Resets. Section 4.11 describes the reset options—power-on reset (POR), asserting and $\overline{\text{RESET}}$.
- Interrupts. The CS43L36 includes an open-drain interrupt output, $\overline{\text{INT}}$. Interrupt mask registers control whether an event associated with an interrupt status/mask bit pair triggers the assertion of $\overline{\text{INT}}$. See Section 4.12.

4.1 Digital Volume Control

The internal stereo volume control is shown in Fig. 4-2. Each input can be attenuated via CHx_VOLy. Outputs are available as a source for the DACs.

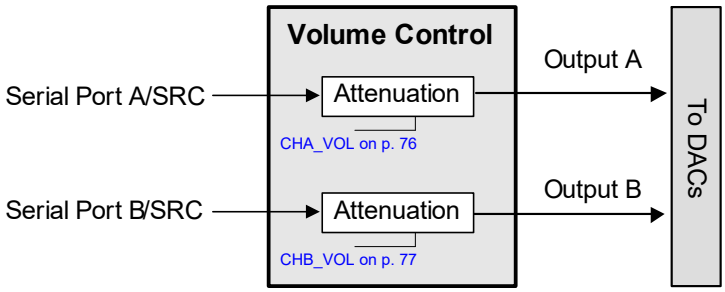


Figure 4-2. Digital Volume Control Subblocks

4.1.1 Attenuation Values

The volume control contains programmable attenuation blocks that are configured as described in the CHx_VOLy field descriptions in Section 7.11.1—Section 7.11.2. For all settings except 0 dB, attenuation on the mixer input includes an offset that increases as attenuation increases, as follows:

- For commonly used –6*n* dB (*n* = {1, 2, etc.}) attenuation settings, the offset rounds the attenuation exactly to the desired $1/2^n$ factor (e.g., 20Log(1/2) = 6.021 dB, not 6.000 dB).
- For attenuation settings other than –6*n* dB, the always positive offset provides slightly more attenuation, giving enough margin to avoid mixer clipping.

4.2 Analog Output

This section describes the headphone (HP) outputs. The CS43L36 provides an analog output that is fed from the mixer. Fig. 4-3 shows the general flow of the analog outputs.

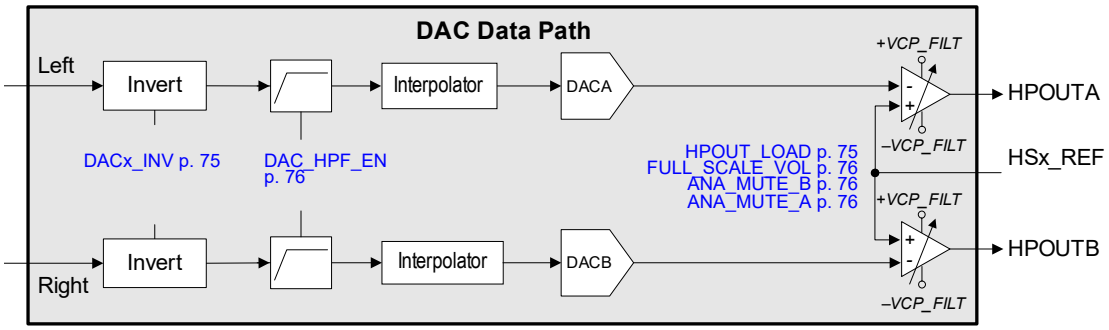


Figure 4-3. Analog-Output Signal Flow

The output path is sourced directly from the digital volume control output. The playback path uses advanced analog and digital signal-processing techniques to adapt to the input signal content and enhance dynamic range and power consumption of the playback path. The HP output must be muted before changing the state of FULL_SCALE_VOL (see p. 76), which sets the maximum HPOUT output voltage. See Table 3-7. HP outputs are muted by ANA_MUTE_B and ANA_MUTE_A (see p. 76).

Fig. 4-4 is an op-amp–level schematic for the analog output flow.

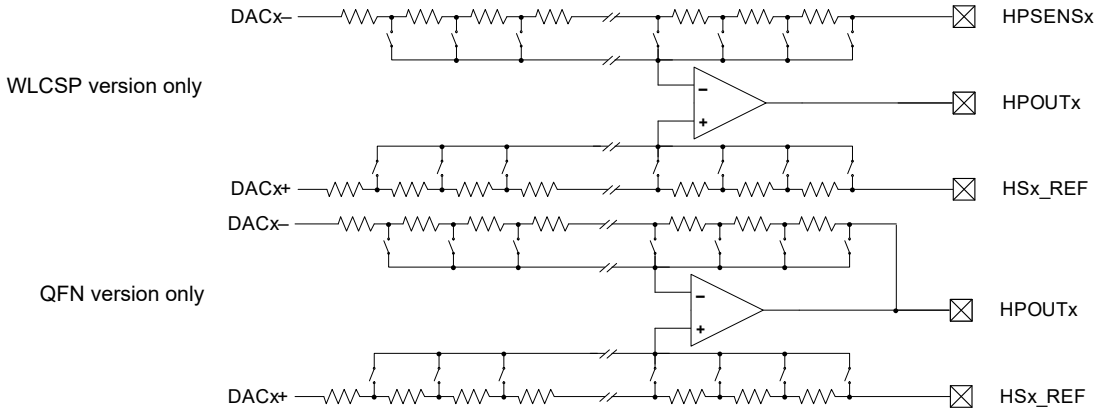


Figure 4-4. Op-Amp-Level Schematic—Analog Outputs

4.2.1 Pseudodifferential Outputs

The analog output amplifiers use a pseudodifferential output topology that allows the amplifier to monitor the ground potential at the load through the reference pins (HSx_REF). Minimize the impedance from the CS43L36 reference pin to the load ground (typically the connector ground). Impedance in this path affects analog output attenuation as well as the common-mode rejection of the output amplifier, which affects output offset and step deviation.

4.2.2 Output Load Detection

The CS43L36 can distinguish between the following output loads:

- R_L = 15, 30, or 3 kΩ
- C_L < ~2 nF (low capacitance); C_L > ~2 nF (high capacitance)

Note: Channels A and B must have matching loads, although load detection is performed using Channel A.

Before output load detection is initiated, the following steps must be performed:

1. HS-type information must be determined to run a headset load-detection sequence, as described in Section 4.8.

2. Power down the HP block: HP_PDN = 1 (see p. 62).
3. Mute the analog outputs: ANA_MUTE_B = ANA_MUTE_A = 1 (see p. 76).
4. Disable the DAC high-pass filter: DAC_HPF_EN = 0 (see p. 76).
   Note: Restore the previous setup after detection completes.
5. Set LATCH_TO_VP (see p. 74).
6. Set ADPTPWR = 100 (see p. 76).
7. Set the analog soft-ramp rate (ASR_RATE = 0111; see p. 60).
8. Set the digital soft-ramp rate (DSR_RATE; see p. 60) = 0001.
9. After load detection completes, ASR_RATE, DSR_RATE, ADPTPWR, and DAC_HPF_EN must be restored to their previous values. See Section 4.3 for details.

After an HP-detect event, if HP_LD_EN is set (see p. 73), the CS43L36 proceeds to detect the resistance and capacitance of the output load. A 24-kHz tone is output on HPOUTA, and HS3 is measured using an internal resistor bank as a reference.

RLA_STAT (see p. 73) reports resistance-detection results for Channel A as follows:

- 00: 15 Ω
- 01: 30 Ω
- 10: 3 kΩ
- 11: Reserved

If the typical output resistance of less than ~300 Ω is indicated, a low-capacitance load is assumed. If the resistance is greater than 300 Ω, capacitance detection proceeds. After the detection sequence completes, HPLOAD_DET_DONE (see p. 73) is set. The results of capacitor detection is reported in CLA_STAT (see p. 73). This result can be used to program the value in HPOUT_LOAD(see p. 75), which determines the compensation of the headphone amplifier.

Notes:

- The HP path must be powered down before updating the HPOUT_LOAD setting and repowered afterwards.
- Low capacitance results were determined with C_L = 1 nF; high capacitance results were determined with C_L = 10 nF.

4.2.3 Slow Start Control

Volume control, DAC, and HP soft ramping is enabled through SLOW_START_EN (p. 61). If SLOW_START_EN = 111, changes to DAC/HP volumes are applied slowly by stepping through each volume-control setting with a delay between steps equal to an integer number of Fs periods. The delay between steps, which can vary from 1/Fs to 72/Fs periods, is set via DSR_RATE and ASR_RATE (see p. 60).

If ramping is disabled, changes occur immediately with the clock edge.

4.3 Class H Amplifier

Fig. 4-5 shows the Class H operation.

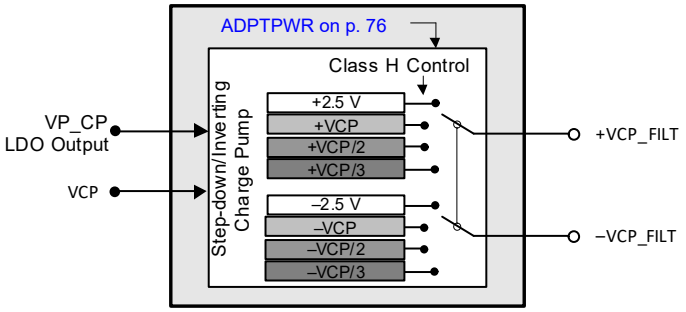


Figure 4-5. Class H Operation

The CS43L36 HP output amplifiers use a Cirrus Logic four-mode Class H technology, which maximizes operating efficiency of the typical Class AB amplifier while maintaining high performance. In a Class H amplifier design, the rail voltages supplied to the amplifier vary with the needs of the music passage being amplified. This conserves energy during low-power passages and when the program material is played back at low volume.

The internal charge pump, which creates the rail voltages for the HP amplifiers, is the central component of the four-mode Class H technology. The charge pump receives its input voltage from the voltage present on either the VCP or VP pin. From this voltage, the charge pump generates the differential rail voltages supplied to the amplifier output stages. The charge pump can supply four sets of differential rail voltages: ±2.5, ±VCP, ±VCP/2, and ±VCP/3.

Table 4-1 shows the nominal signal- and volume-level ranges if the amplifier is set to the adapt-to-signal mode explained in Section 4.3.1. In addition to adapting to the input signal, the Class H control is capable of monitoring the internal headphone amplifier supply to allow more efficient, load-dependent, automatic Smart Class H Mode selection. In fixed modes, if the signal level exceeds the maximum value of the indicated range, clipping can occur.

Table 4-1. Class H Supply Modes

Load		Mode	Class-H Supply Voltage	Signal-Level Range [1,2,3,4]
Resistance	Capacitance			
15 Ω	1 nF	0	±2.5 V	≥ –8 dB
		1	± VCP	–9 to –14 dB
		2	± VCP/2	–15 to –20 dB
		3	± VCP/3	≤ –21 dB
	10 nF	0	±2.5 V	≥ –9 dB
		1	± VCP	–10 to –14 dB
		2	± VCP/2	–15 to –19 dB
		3	± VCP/3	≤ –20 dB
30 Ω	1 or 10 nF	0	±2.5 V	≥ –4 dB
		1	± VCP	–5 to –11 dB
		2	± VCP/2	–12 to –16 dB
		3	± VCP/3	≤ –17 dB
3 kΩ	1 or 10 nF	0	±2.5 V	≥ –1 dB
		1	± VCP	–2 to –8 dB
		2	± VCP/2	–9 to –13 dB
		3	± VCP/3	≤ –14 dB

1. In Adapt-to-Signal Mode, volume level ranges are approximations but are within –0.5 dB from the values shown.
2. Relative to digital full scale with FULL_SCALE_VOL set to 0 dB.
3. In fixed modes, clipping occurs if the signal level exceeds the maximum of this range due to setting the amplifier's supply too low.
4. To optimize efficiency, smart Class H thresholds automatically vary based on load conditions.

4.3.1 Power Control Options

This section describes the supported types of operation: standard Class AB and adapt to signal. The set of rail voltages supplied to the amplifier output stages depends on the ADPTPWR setting, as described in Section 7.10.1.

4.3.1.1 Standard Class AB Operation (ADPTPWR = 001, 010, 011, or 100)

If ADPTPWR is set to 001, 010, 011, or 100, the rail voltages supplied to the amplifiers are held to ±2.5, ±VCP, ±VCP/2, or ±VCP/3, respectively. For these settings, the rail voltages supplied to the output stages are held constant, regardless of the signal level. In these settings, the CS43L36 amplifiers operate in a traditional Class AB configuration.

4.3.1.2 Adapt-to-Output Signal (ADPTPWR = 111)

If ADPTPWR = 111, the rail voltage sent to the amplifiers is based only on whether the signal sent to the amplifiers would cause the amplifiers to clip when operating on the lower set of rail voltages at certain threshold values.

- If clipping can occur, the control logic instructs the charge pump to provide the next higher set of rail voltages.
- If clipping could not occur, the control logic instructs the charge pump to provide the lower set of rail voltages, eliminating the need to advise the CS43L36 of volume settings external to the device.

4.3.2 Power-Supply Transitions

Charge-pump transitions from the lower to the higher set of rail voltages occur on the next FLYN/FLYP clock cycle. Despite the system's fast response time, the VCP_FILT pin's capacitive elements prevent rail voltages from changing instantly. Instead, the rail voltages ramp from the lower to the higher supply, based on the time constant created by the output impedance of the charge pump and the capacitor on the VCP_FILT pin (the transition time is approximately 20 µs).

Fig. 4-6 shows Class H supply switching. During this transition, a high dV/dt transient on the inputs may briefly clip the outputs before the rail voltages charge to the full higher supply level. This transitory clipping has been found to be inaudible in listening tests.

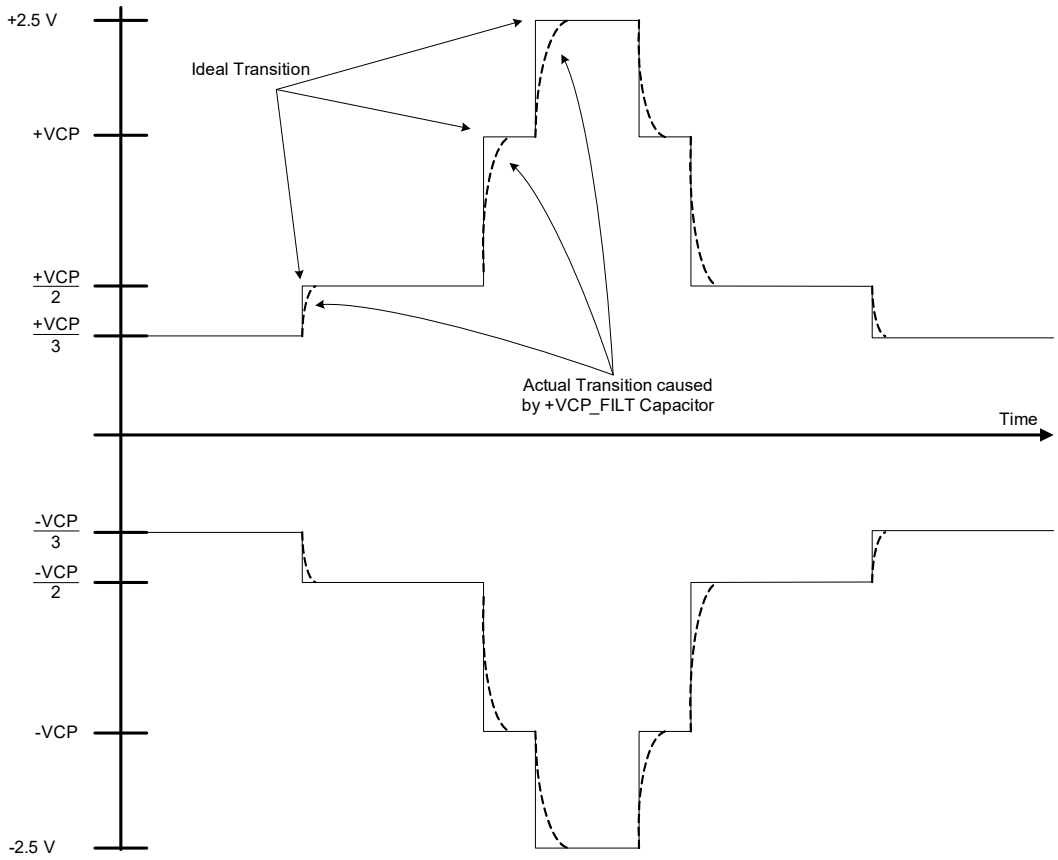


Figure 4-6. VCP_FILT Transitions—Headphone Output

When the charge pump transitions from the higher to the lower set of rail voltages, there is a 5.5-s delay before the charge pump supplies the lower rail voltages to the amplifiers. This hysteresis ensures that the charge pump does not toggle between the two rail voltages as signals approach the clip threshold. It also prevents clipping in the instance of repetitive high-level transients in the input signal. Fig. 4-7 shows this transitional behavior.