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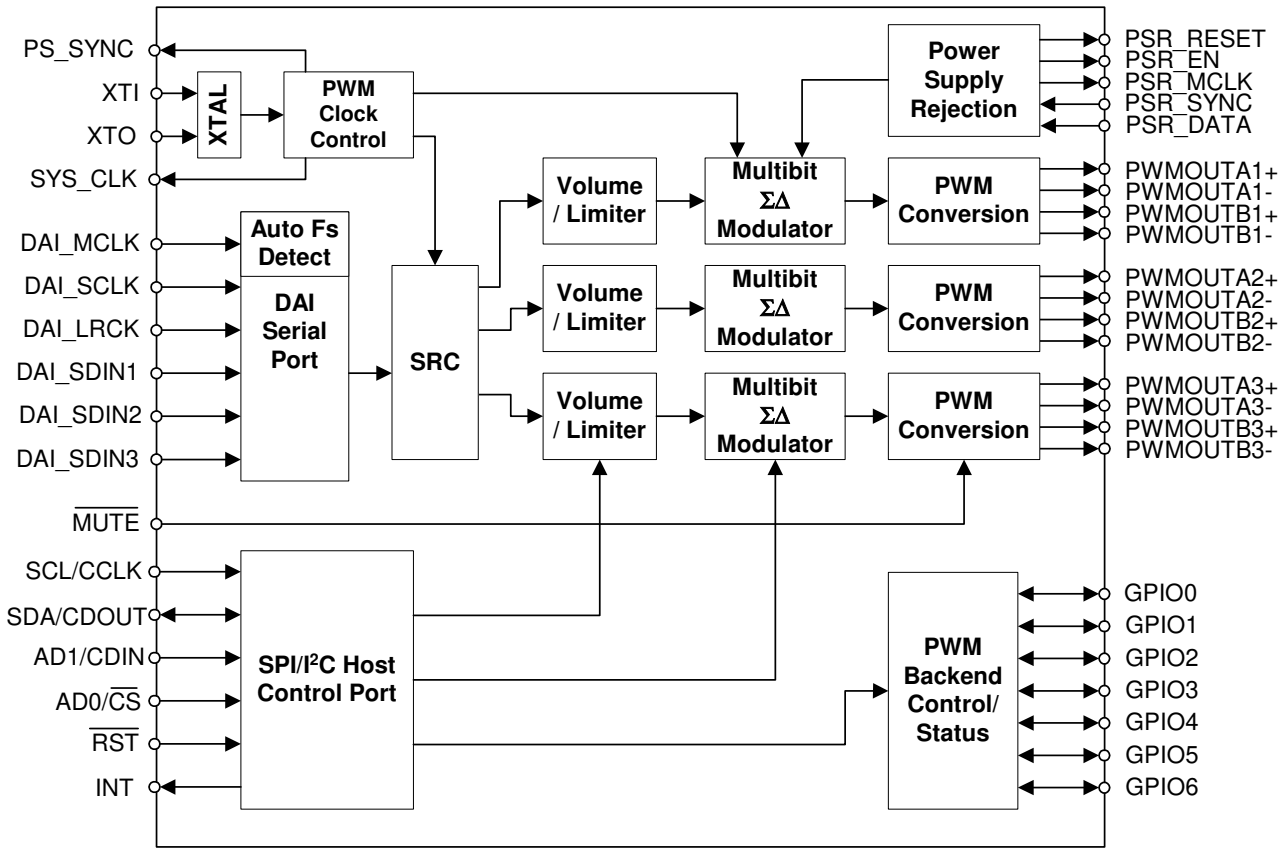
CS44600

6-Channel Digital Amplifier Controller

Features

- > 100 dB Dynamic Range - System Level
- < 0.03% THD+N @ 1 W - System Level
- 32 kHz to 192 kHz Sample Rates
- Internal Oscillator Circuit Supports 24.576 MHz to 54 MHz Crystals
- Integrated Sample Rate Converter (SRC)
  - Eliminates Clock Jitter Effects
  - Input Sample Rate Independent Operation
- Power Supply Rejection Realtime Feedback
- Spread Spectrum Modulation - Reduces EMI
- PWM Popguard® for Single-Ended Mode
- Eliminates AM Frequency Interference
- Programmable Load Compensation Filters
- Support for up to 40 kHz Audio Bandwidth
- Digital Volume Control with Soft Ramp
  - +24 to -127 dB in 0.25 dB Steps
- Per Channel Programmable Peak Detect and Limiter
- SPI™ and I²C® Host Control Interfaces
- Separate 2.5 V to 5.0 V Serial Port and Host Control Port Supplies



General Description

The CS44600 is a multi-channel digital-to-PWM Class D audio system controller including interpolation, sample rate conversion, half- and full-bridge PWM driver outputs, and power supply rejection feedback in a 64-pin LQFP package.The architecture uses a direct-to-digital approach that maintains digital signal integrity to the final output filter, minimizing analog interference effects which negatively affect system performance.

The CS44600 integrates on-chip digital volume control, peak detect with limiter, de-emphasis, and 7 GPIO's, allowing easy interfacing to many commonly available power stages. The PWM amplifier can achieve greater than 90% efficiency. This efficiency provides for smaller device package, less heat sink requirements, and smaller power supplies.

The CS44600 is ideal for audio systems requiring wide dynamic range, negligible distortion and low noise, such as A/V receivers, DVD receivers, digital speaker and automotive audio systems.

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1. CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25°C.)

SPECIFIED OPERATING CONDITIONS

(GND = 0 V, all voltages with respect to ground)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supply						
Digital	2.5 V	VD	2.37	2.5	2.63	V
XTAL (Note 1)	2.5 V	VDX	2.37	2.5	2.63	V
	3.3 V		3.14	3.3	3.47	V
	5.0 V		4.75	5.0	5.25	V
PWM Interface	3.3 V	VDP	3.14	3.3	3.47	V
	5.0 V		4.75	5.0	5.25	V
Serial Audio Interface	2.5 V	VLS	2.37	2.5	2.63	V
	3.3 V		3.14	3.3	3.47	V
	5.0 V		4.75	5.0	5.25	V
Control Interface	2.5 V	VLC	2.37	2.5	2.63	V
	3.3 V		3.14	3.3	3.47	V
	5.0 V		4.75	5.0	5.25	V
Ambient Operating Temperature						
Commercial	-CQZ	T_A	-10	-	+70	°C
Automotive	-DQZ		-40	-	+85	°C

Notes:

1. When using external crystal, VDX = 3.14 V(min). When using clock signal input, VDX = 2.37 V(min).

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Max	Units
DC Power Supply	Digital	VD	-0.3	3.5	V
	XTAL	VDX	-0.3	6.0	V
	PWM Interface	VDP	-0.3	6.0	V
	Serial Audio Interface	VLS	-0.3	6.0	V
	Control Interface	VLC	-0.3	6.0	V
Input Current	(Note 2)	I_{in}	-	±10	mA
Digital Input Voltage	PWM Interface	$V_{IND-PWM}$	-0.3	VDP+0.4	V
(Note 3)	Serial Audio Interface	V_{IND-S}	-0.3	VLS+0.4	V
	Control Interface	V_{IND-C}	-0.3	VLC+0.4	V
Ambient Operating Temperature	-CQ	T_A	-20	+85	°C
(power applied)	-DQ		-50	+95	°C
Storage Temperature		T_{stg}	-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

2. Any pin except supplies. Transient currents of up to ±100 mA on the input pins will not cause SCR latch-up.
3. The maximum over/under voltage is limited by the input current.

DC ELECTRICAL CHARACTERISTICS

(GND = 0 V, all voltages with respect to ground; DAI_MCLK = 12.288 MHz, XTAL = 24.576 MHz, PWM Switch Rate = 384 kHz unless otherwise specified.)

Parameter		Symbol	Min	Typ	Max	Units
Normal Operation (Note 4)						
Power Supply Current (Note 5)	VD = 2.5 V	I_D	-	150	-	mA
	VDX = 3.3 V	I_{DX}	-	2	-	mA
	VDP = 3.3 V	I_{DP}	-	1.2	-	mA
	VLS = 3.3 V	I_{LS}	-	150	-	µA
	VLC = 3.3 V (Note 6)	I_{LC}	-	250	-	µA
Power Dissipation	VD=2.5 V, VDX = VDP = VLS = VLC = 3.3 V		-	387	500	mW
Power Supply Rejection Ratio (Note 7)	(1 kHz)	PSRR	-	15	-	dB
	(60 Hz)		-	40	-	dB
Power-Down Mode (Note 8)						
Power Supply Current	All Supplies except VDX (Note 9)	I_{pd}	-	80	-	µA

4. Normal operation is defined as $\overline{RST}$ = HI with a 997 Hz, 0 dBFS input.
5. Current consumption increases with increasing XTAL clock rates and PWM switch rates. Variance between DAI clock rates is negligible.
6. I_{LC} measured with no external loading on the SDA pin.
7. Valid with PSRR function enabled and the recommended external ADC (CS4461) and filtering.
8. Power down mode is defined as $\overline{RST}$ pin = LOW with all clock and data lines held static.
9. When $\overline{RST}$ pin = LOW, the internal oscillator is active to provide a valid clock for the SYS_CLK output.

DIGITAL INTERFACE CHARACTERISTICS

(GND = 0 V, all voltages with respect to ground)

Parameters (Note 10)		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	XTAL	V_{IH}	0.7xVDX	-	-	V
	PWM Interface		0.7xVDP	-	-	V
	Serial Audio Interface		0.7xVLS	-	-	V
	Control Interface		0.7xVLC	-	-	V
Low-Level Input Voltage	XTAL	V_{IL}	-	-	0.2xVDX	V
	PWM Interface		-	-	0.2xVDP	V
	Serial Audio Interface		-	-	0.2xVLS	V
	Control Interface		-	-	0.2xVLC	V
High-Level Output Voltage at I_o = -2 mA	PWM Interface	V_{OH}	VDP-1.0	-	-	V
	Serial Audio Interface		VLS-1.0	-	-	V
	Control Interface		VLC-1.0	-	-	V
Low-Level Output Voltage at I_o = 2 mA	PWM Interface	V_{OL}	-	-	0.45	V
	Serial Audio Interface		-	-	0.45	V
	Control Interface		-	-	0.45	V
Input Leakage Current		I_{in}	-	-	±10	µA
Input Capacitance			-	-	8	pF

10. Serial Port signals include: SYS_CLK, DAI_MCLK, DAI_SCLK, DAI_LRCK, DAI_SDIN1-3
Control Port signals include: SCL/CCLK, SDA/CDOUT, AD0/$\overline{CS}$, AD1/CDIN, INT, $\overline{RST}$, MUTE
PWM signals include: PWMOUTA1-B3, PSR_MCLK, PSR_SYNC, PSR_DATA, PS_SYNC, GPIO[6:0]

PWM OUTPUT PERFORMANCE CHARACTERISTICS

(Logic “0” = GND = 0 V; Logic “1” = VLS = VLC; VD = 2.5 V; DAI_MCLK = 12.288 MHz; XTAL= 24.576 MHz; PWM Switch Rate = 384 kHz; Fs = 32 kHz to 192 kHz; Measurement bandwidth is 10 Hz to 20 kHz unless otherwise specified; Performance measurements taken with a full-scale 997 Hz.)

Parameter		Symbol	Min	Typ	Max	Unit
Dynamic Performance (Note 11)						
24-Bits	A-Weighted		102	108	-	dB
	unweighted		99	105	-	dB
16-Bits	unweighted		-	96	-	dB
Total Harmonic Distortion + Noise (Note 11)						
24-Bits	0 dB	THD+N	-	-90	-85	dB
	-20 dB		-	-77	-	dB
	-60 dB		-	-45	-	dB
Idle Channel Noise / Signal-to-Noise Ratio			-	110	-	dB
Interchannel Isolation	(1 kHz)		-	100	-	dB

11. Performance characteristics measured using filter shown in Figure 1.

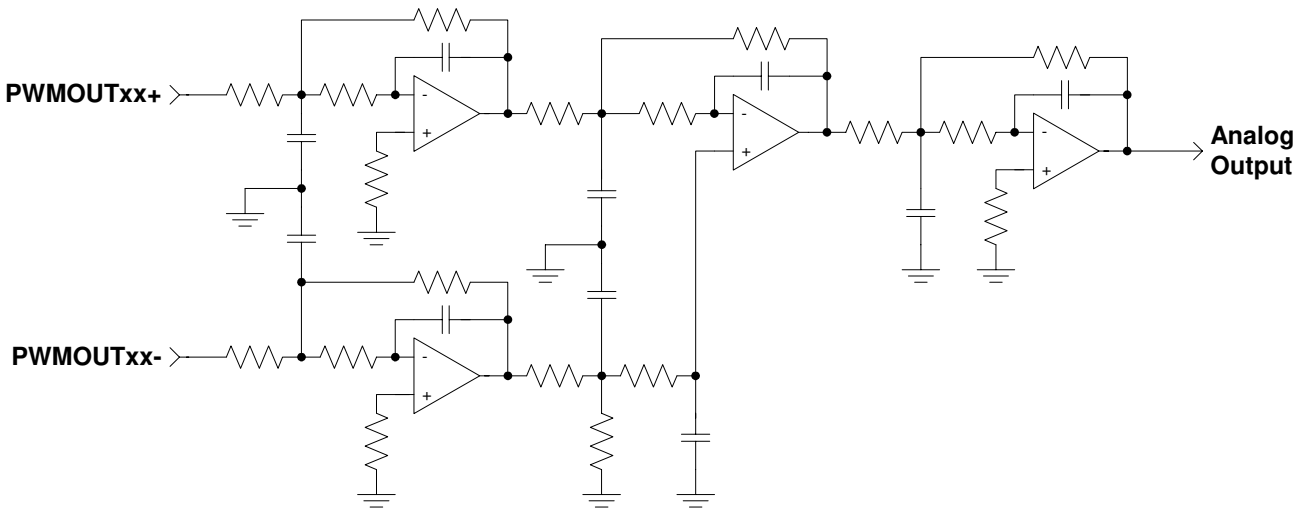

Figure 1. Performance Characteristics Evaluation Active Filter Circuit

PWM FILTER CHARACTERISTICS

(Logic “0” = GND = 0 V; Logic “1” = VLS = VLC; VD = 2.5 V; DAI_MCLK = 12.288 MHz; XTAL = 24.576 MHz; PWM Switch Rate = 384 kHz; Fs = 32 kHz to 192 kHz; Measurement bandwidth is 10 Hz to 20 kHz unless otherwise specified.)

Parameter		Min	Typ	Max	Unit
Digital Filter Response (Note 12)					
Passband					
OSRATE = 0b	to -0.01 dB corner	0	-	1.6	kHz
	to -3 dB corner	0	-	24.0	kHz
OSRATE = 1b (Note 13)	to -0.01 dB corner	0	-	3.3	kHz
	to -3 dB corner	0	-	44.5	kHz
	Frequency Response				
OSRATE = 0b	10 Hz to 20 kHz	-0.8	-	+0.02	dB
OSRATE = 1b (Note 13)	10 Hz to 40 kHz	-1.2	-	+0.02	dB
Group Delay			(Note 14)		ms
De-emphasis Error	Fs = 32 kHz	-	-	±0.23	dB
(Relative to 1 kHz)	Fs = 44.1 kHz	-	-	±0.14	dB
	Fs = 48 kHz	-	-	±0.09	dB

12. Filter response is not production tested but is characterized and guaranteed by design.
13. XTAL = 49.152 MHz; PWM Switch Rate = 768 kHz; Fs = 96 kHz to 192 kHz.
14. The equation for the group delay through the sample rate converter with OSRATE = 0b is (8.5 / Fsi) + (10 / Fso) ± (4.5 / Fsi). The equation for the group delay through the sample rate converter with OSRATE = 1b is (8.5 / Fsi) + (20 / Fso) ± (4.5 / Fsi).

SWITCHING CHARACTERISTICS - XTI

(VD = 2.5 V, VDP = VLC = VLS = 3.3 V, VDX = 2.5 V to 5.0 V; Inputs: Logic 0 = GND, Logic 1 = VDX)

Parameter	Symbol	Min	Typ	Max	Unit
XTI period	t_{clki}	18.518	---	40.69	ns
XTI high time	t_{clkih}	8.34	---	22.38	ns
XTI low time	t_{clkil}	8.34	---	22.38	ns
XTI Duty Cycle		45	50	55	%
External Crystal operating frequency		24.576	---	54	MHz

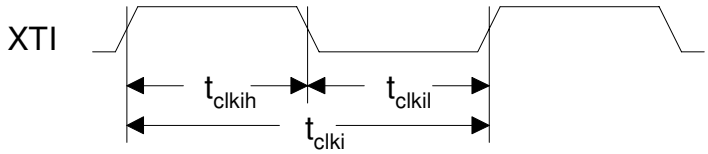

Figure 2. XTI Timings

SWITCHING CHARACTERISTICS - SYS_CLK

(VD = 2.5 V, VDP = VLC = VDX = 3.3 V, VLS = 2.5 V to 5.0 V, Cload = 50 pF)

Parameter	Symbol	Min	Typ	Max	Unit
SYS_CLK Period	t_{sclki}	18.518	---	---	ns
SYS_CLK Duty Cycle		45	50	55	%

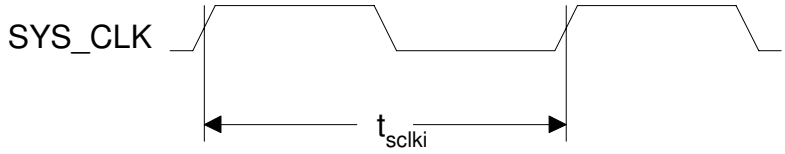

Figure 3. SYS_CLK Timings

SWITCHING CHARACTERISTICS - PWMOUTA1-B3

(VD = 2.5 V, VLS = VLC = VDX = 3.3 V, VDP = 3.3 V to 5.0 V unless otherwise specified, Cload = 10 pF)

Parameter		Symbol	Min	Typ	Max	Unit
PWMOUTxx Period		t_{pwm}	2.60	-	1.18	µs
Rise Time of PWMOUTxx	VDP = 5.0 V	t_r	-	1.6	-	ns
	VDP = 3.3 V		-	2.1	-	ns
Fall Time of PWMOUTxx	VDP = 5.0 V	t_f	-	1.1	-	ns
	VDP = 3.3 V		-	1.4	-	ns

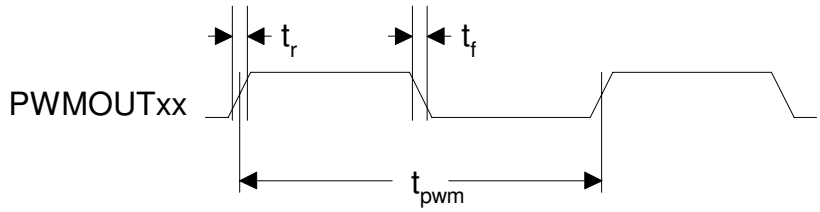

Figure 4. PWMOUTxx Timings

SWITCHING CHARACTERISTICS - PS_SYNC

(VD = 2.5 V, VLS = VLC = VDX = 3.3 V, VDP = 3.3 V to 5.0 V, Cload = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
PS_SYNC Period	t_{psclki}	592.576	---	---	ns
PS_SYNC Duty Cycle		45	50	55	%

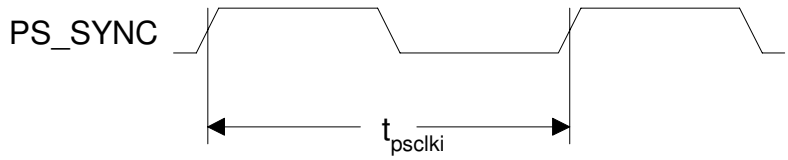

Figure 5. PS_SYNC Timings

SWITCHING CHARACTERISTICS - DAI INTERFACE

(VD = 2.5 V, VDX = VDP = VLC = 3.3 V, VLS = 2.5 V to 5.0 V; Inputs: Logic 0 = GND, Logic 1 = VLS.)

Parameters	Symbol	Min	Max	Units
$\overline{\text{RST}}$ pin Low Pulse Width (Note 15)		1	-	ms
DAI_MCLK Duty Cycle (Note 16)		40	60	%
DAI_SCLK Duty Cycle		45	55	%
DAI_LRCK Duty Cycle		45	55	%
DAI Sample Rate (Note 17)	F_s	32	192	kHz
DAI_SDIN Setup Time Before DAI_SCLK Rising Edge	t_{ds}	10	-	ns
DAI_SDIN Hold Time After DAI_SCLK Rising Edge	t_{dh}	10	-	ns
DAI_SCLK High Time	t_{sckh}	20	-	ns
DAI_SCLK Low Time	t_{sckl}	20	-	ns
DAI_LRCK Setup Time Before DAI_SCLK Rising Edge	t_{lrcks}	25	-	ns
DAI_SCLK Rising Edge Before DAI_LRCK Edge	t_{lrckd}	25	-	ns

15. After powering up, the CS44600, $\overline{\text{RST}}$ should be held low until after the power supplies and clocks are settled.
16. See Table 1 on page 26 for suggested MCLK frequencies.
17. Max DAI sample rate is 96 kHz for One Line and TDM modes of operation.

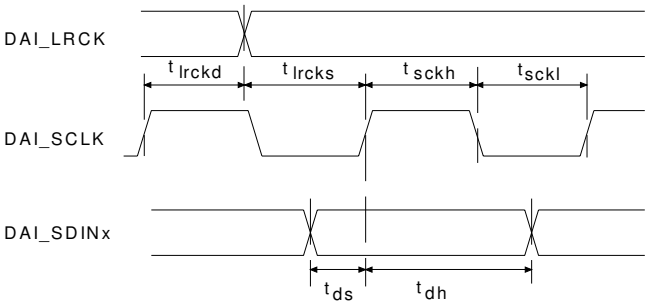

Figure 6. Serial Audio Interface Timing

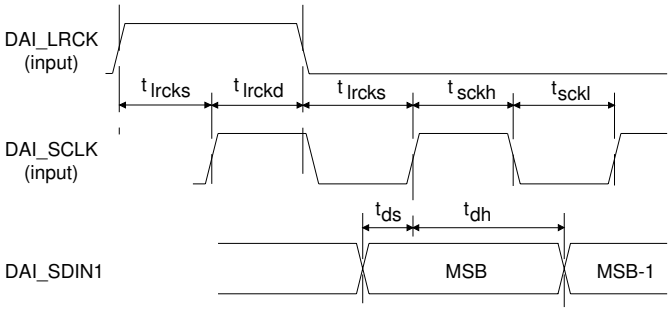

Figure 7. Serial Audio Interface Timing - TDM Mode

SWITCHING CHARACTERISTICS - CONTROL PORT - I²C FORMAT

(VD = 2.5 V, VDX = VDP = VLS = 3.3 V; VLC = 2.5 V to 5.0 V; Inputs: Logic 0 = GND, Logic 1 = VLC, C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
Bus Free Time between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 18)	t_{hdd}	10	-	ns
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_r	-	1000	ns
Fall Time SCL and SDA	t_f	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs

18. Data must be held for sufficient time to bridge the transition time, t_f, of SCL.

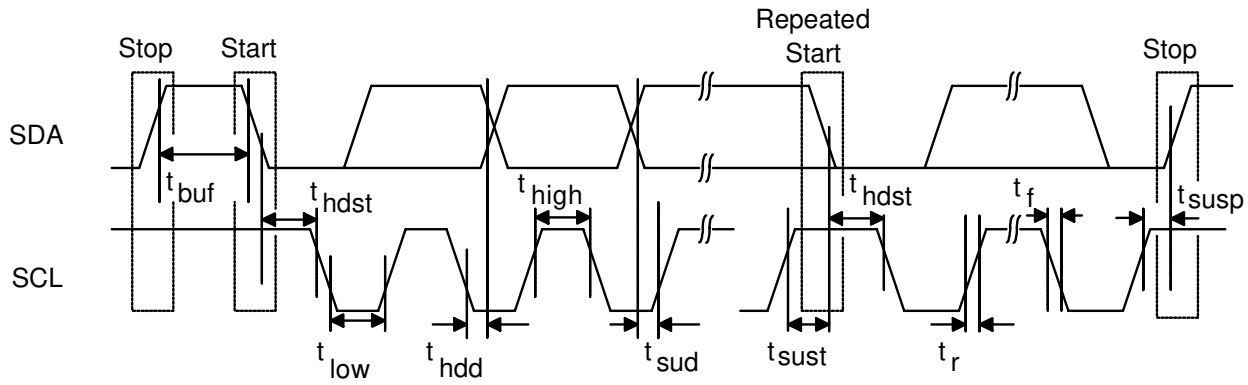

Figure 8. Control Port Timing - I²C Format

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI FORMAT

(VD = 2.5 V, VDP = VLS = 3.3 V; VLC = 2.5 V to 5.0 V; Inputs: Logic 0 = GND, Logic 1 = VLC, C_L = 30 pF)

Parameter		Symbol	Min	Typ	Max	Units
CCLK Clock Frequency		f_{sck}	0	-	6.0	MHz
$\overline{CS}$ High Time between Transmissions		t_{csh}	1.0	-	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	-	ns
CCLK Low Time		t_{scl}	66	-	-	ns
CCLK High Time		t_{sch}	66	-	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	-	ns
CCLK Rising to DATA Hold Time	(Note 19)	t_{dh}	15	-	-	ns
CCLK Falling to CDOUT Stable		t_{pd}	-	-	50	ns
Rise Time of CDOUT		t_{r1}	-	-	25	ns
Fall Time of CDOUT		t_{f1}	-	-	25	ns
Rise Time of CCLK and CDIN	(Note 20)	t_{r2}	-	-	100	ns
Fall Time of CCLK and CDIN	(Note 20)	t_{f2}	-	-	100	ns

19. Data must be held for sufficient time to bridge the transition time of CCLK.
20. For f_{sck} <1 MHz.

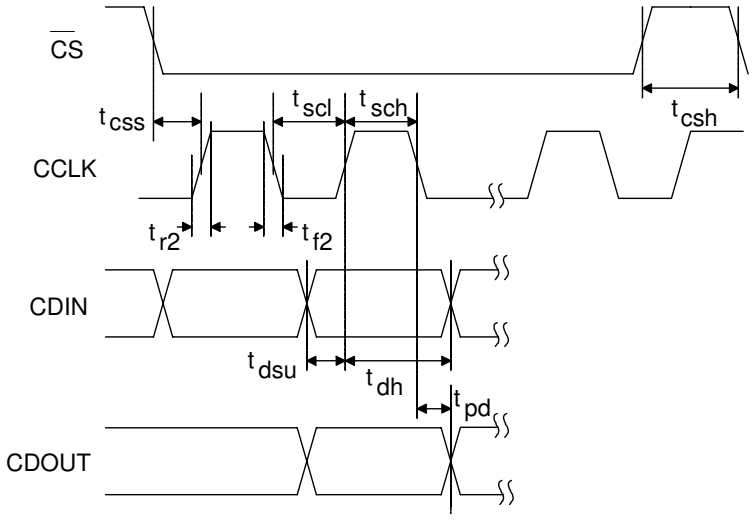

Figure 9. Control Port Timing - SPI Format

2. PIN DESCRIPTIONS

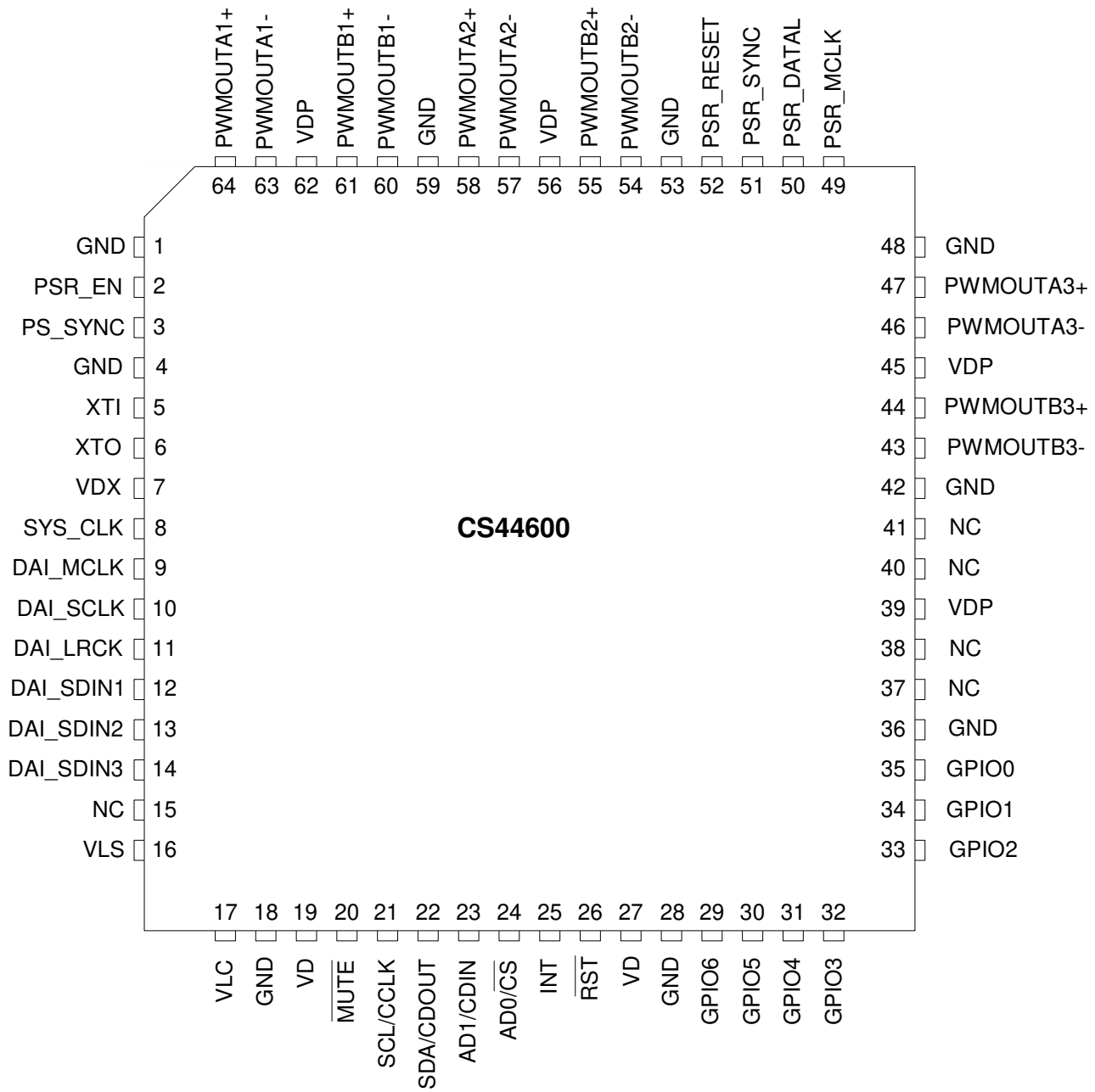

Figure 10. CS44600 Pinout Diagram

Pin Name	Pin #	Pin Description
PS_SYNC	3	**Power Supply Synchronization Clock** *(Output)* - The PWM synchronized clock to the switch mode power supply.
XTI	5	**Crystal Oscillator Input** (*Input*) - Crystal Oscillator input or accepts an external clock input signal that is used to drive the internal PWM core logic.
XTO	6	**Crystal Oscillator Output** *(Output)* - Crystal Oscillator output.
SYS_CLK	8	**External System Clock** (*Output*) - Clock output. This pin provides a divided down clock derived from the XTI input.
DAI_MCLK	9	**Digital Audio Input Master Clock** (Input) - Master audio clock.
DAI_SCLK	10	**Digital Audio Input Serial Clock** *(Input)* - Serial clock for the Digital Audio Input Interface. The clock frequency is a multiple of the Left/Right Clock running at Fs.
DAI_LRCK	11	**Digital Audio Input Left/Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line. The rate is determined by the sampling frequency Fs.
DAI_SDIN1 DAI_SDIN2 DAI_SDIN3	12 13 14	**Digital Audio Input Serial Data** (*Input*) - Input for two's complement serial audio data.
MUTE	20	**Mute** (*Input*) - The device will perform a hard mute on all channels. All internal registers are not reset to their default settings.
SCL/CCLK	21	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port. Requires an external pull-up resistor to the logic interface voltage in I²C mode as shown in the Typical Connection Diagram.
SDA/CDOUT	22	**Serial Control Data** (*Input/Output*) **-** SDA is a data I/O line in I²C mode and requires an external pull-up resistor to the logic interface voltage, as shown in the Typical Connection Diagram.; CDOUT is the output data line for the control port interface in SPI mode.
AD1/CDIN	23	**Address Bit 1 (I²C)/Serial Control Data (SPI)** (*Input*) - AD1 is a chip address pin in I²C mode.;CDIN is the input data line for the control port interface in SPI mode.
AD0/$\overline{CS}$	24	**Address Bit 0 (I²C)/Control Port Chip Select (SPI)** *(Input*) - AD0 is a chip address pin in I²C mode; $\overline{CS}$ is the chip select signal in SPI mode.
INT	25	**Interrupt Request** *(Output*) - CMOS or open-drain interrupt request output. This pin is driven to the configured active state to indicate that the PWM Controller has status data that should be read by the host.
RST	26	**Reset** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings when low.
GPIO6	29	**General Purpose Input, Output** *(Input/Output*) - This pin is configured as an input following a $\overline{RST}$ condition. It can be configured as a general purpose input or output which can be individually controlled by the Host Controller.
GPIO5	30	**General Purpose Input, Output** *(Input/Output*) - This pin is configured as an input following a $\overline{RST}$ condition. It can be configured as a general purpose input or output which can be individually controlled by the Host Controller.
GPIO4	31	**General Purpose Input, Output** *(Input/Output*) - This pin is configured as an input following a $\overline{RST}$ condition. It can be configured as a general purpose input or output which can be individually controlled by the Host Controller.

GPIO3	32	**General Purpose Input, Output** *(Input/Output)* - This pin is configured as an input following a $\overline{\text{RST}}$ condition. It can be configured as a general purpose input or output which can be individually controlled by the Host Controller.
GPIO2	33	**General Purpose Input, Output** *(Input/Output)* - This pin is configured as an input following a $\overline{\text{RST}}$ condition. It can be configured as a general purpose input or output which can be individually controlled by the Host Controller.
GPIO1	34	**General Purpose Input, Output** *(Input/Output)* - This pin is configured as an input following a $\overline{\text{RST}}$ condition. It can be configured as a general purpose input or output which can be individually controlled by the Host Controller.
GPIO0	35	**General Purpose Input, Output** *(Input/Output)* - This pin is configured as an input following a $\overline{\text{RST}}$ condition. It can be configured as a general purpose input or output which can be individually controlled by the Host Controller.
PSR_MCLK	49	**Power Supply Rejection Master Clock** (*Output*) - Master audio clock for external PSR ADC (CS4461).
PSR_DATAL	50	**Power Supply Rejection Input Serial Data** (*Input*) - Input for serial audio data from external PSR ADC (CS4461).
PSR_SYNC	51	**Power Supply Rejection Sync Clock** *(Input)* - Synchronization signal for external PSR ADC (CS4461).
PSR_RESET	52	**Power Supply Rejection Reset** *(Output)* - The reset pin for the external Power Supply Rejection circuitry.
PSR_EN	2	**Power Supply Rejection Enable** *(Output)* - The enable pin for the external Power Supply Rejection circuitry.
PWMOUTA1+ PWMOUTA1- PWMOUTB1+ PWMOUTB1- PWMOUTA2+ PWMOUTA2- PWMOUTB2+ PWMOUTB2- PWMOUTA3+ PWMOUTA3- PWMOUTB3+ PWMOUTB3-	64 63 61 60 58 57 55 54 47 46 44 43	**PWM Output** (*Output*) - PWM control signals for the Class D amplifier backend.
VDX	7	**Crystal Power** (*Input*) - Positive power supply for the Crystal section.
VD	19, 27	**Digital Power** (*Input*) - Positive power supply for the digital section.
VLC	17	**Host Interface Power** (*Input*) **-** Determines the required signal level for the digital input/output signals for the host interface.
VLS	16	**Digital Audio Interface Power** (*Input*) **-** Determines the required signal level for the digital input signals for the digital audio interface.
VDP	39, 45, 56, 62	**PWM Interface Power** (*Input*) - Determines the required signal level for the digital input/output signals for the PWM and GPIO interface.
GND	1, 4, 18, 28, 36, 42, 48, 53, 59	**Digital Ground** (*Input*) - Ground reference for digital circuits.

2.1 I/O Pin Characteristics

Signal Name	Power Rail	I/O	Driver	Receiver
RST	VLC	Input	-	2.5 V and 3.3/5.0 V TTL Compatible.
SCL/CCLK	VLC	Input	-	2.5 V and 3.3/5.0 V TTL Compatible, with Hysteresis.
SDA/CDOUT	VLC	Input / Output	2.5-5.0 V, CMOS/Open Drain	2.5 V and 3.3/5.0 V TTL Compatible, with Hysteresis.
AD0/$\overline{CS}$	VLC	Input	-	2.5 V and 3.3/5.0 V TTL Compatible, Internal pull-up.
AD1/CDIN	VLC	Input	-	2.5 V and 3.3/5.0 V TTL Compatible, Internal pull-up.
INT	VLC	Output	2.5-5.0 V, CMOS/Open Drain	-
MUTE	VLC	Input	-	2.5 V and 3.3/5.0 V TTL Compatible.
DAI_SDINx	VLS	Input	-	2.5 V and 3.3/5.0 V TTL Compatible.
DAI_SCLK	VLS	Input	-	2.5 V and 3.3/5.0 V TTL Compatible.
DAI_LRCK	VLS	Input	-	2.5 V and 3.3/5.0 V TTL Compatible.
DAI_MCLK	VLS	Input	-	2.5 V and 3.3/5.0 V TTL Compatible.
SYS_CLK	VLS	Output	2.5-5.0 V, CMOS	-
XTI	VDX	Input	-	2.5 V and 3.3/5.0 V TTL Compatible, Internal pull-down.
XTO	VDX	Output	-	-
GPIOx	VDP	Input / Output	3.3/5.0 V, CMOS/Open Drain	3.3/5.0 V TTL Compatible.
PWMOUTAx+/-	VDP	Output	3.3/5.0 V, CMOS	-
PWMOUTBx+/-	VDP	Output	3.3/5.0 V, CMOS	-
PSR_MCLK	VDP	Output	3.3/5.0 V, CMOS	-
PSR_SYNC	VDP	Input	-	3.3/5.0 V TTL Compatible, Internal pull-up.
PSR_DATA	VDP	Input	-	3.3/5.0 V TTL Compatible, Internal pull-up.
PSR_EN	VDP	Output	3.3/5.0 V, CMOS	-
PSR_RESET	VDP	Output	3.3/5.0 V, CMOS	-
PS_SYNC	VDP	Output	3.3/5.0 V, CMOS	-

3. TYPICAL CONNECTION DIAGRAMS

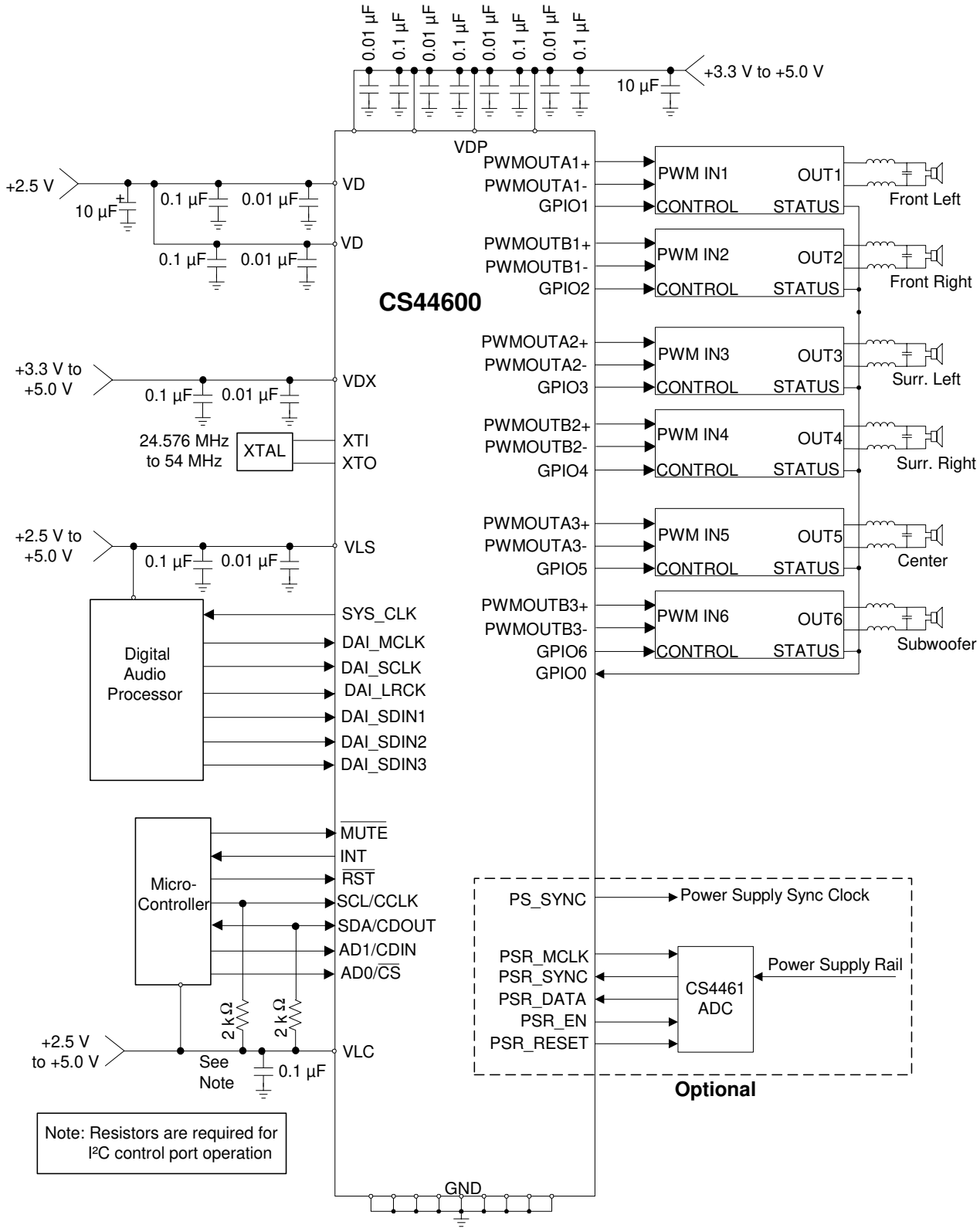

Figure 11. Typical Full-Bridge Connection Diagram

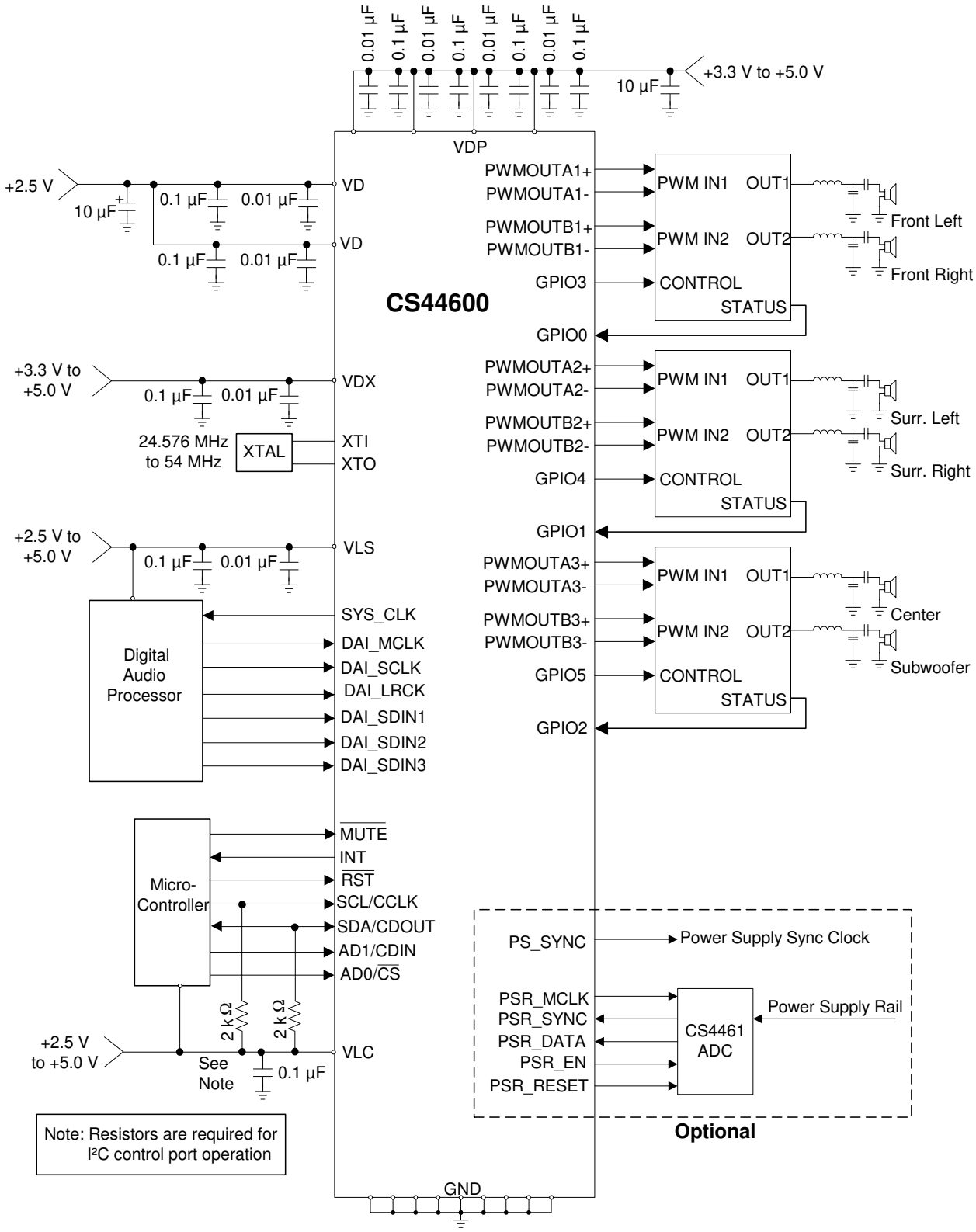

Figure 12. Typical Half-Bridge Connection Diagram

4. APPLICATIONS

4.1 Overview

The CS44600 is a multi-channel digital-to-PWM Class D audio system controller including interpolation, sample rate conversion, half- and full-bridge PWM driver outputs, and power supply rejection feedback in a 64-pin LQFP package. The architecture uses a direct-to-digital approach that maintains digital signal integrity to the final output filter, minimizing analog interference effects which negatively affect system performance.

The CS44600 integrates on-chip sample rate conversion, digital volume control, peak detect with volume limiter, de-emphasis, programmable interrupt conditions, and the ability to change the PWM switch rate to eliminate AM frequency interference. The CS44600 also has a programmable load compensation filter, which allows the speaker load to vary while the output filter remains fixed, maintaining a flat frequency response. For single-ended half-bridge applications PWM Popguard® reduces the transient pops and clicks and realtime power supply feedback reduces noise coupling from the power supply. The PWM amplifier can achieve greater than 90% efficiency. This efficiency provides for a smaller device package, less heat sink requirements, and smaller power supplies.

The CS44600 is ideal for audio systems requiring wide dynamic range, negligible distortion, and low noise such as A/V receivers, DVD receivers, digital speaker, and automotive audio systems.

4.2 Feature Set Summary

Core Features

- 2.5 V digital core voltage, VD.
- VLC voltage pin for host interface logic levels between 2.5 V and 5.0 V.
- VLS voltage pin for digital audio interface logic levels between 2.5 V and 5.0 V.
- VDP voltage pin for PWM backend interface logic levels between 3.3 V and 5.0 V.
- VDX voltage pin for clock input signals between 2.5 V and 5.0 V.

Clocking

- Minimum of 128Fs DAI_MCLK for DAI serial interface.
- DAI interface uses automatic detection of LRCK/MCLK ratio to configure internal DAI/SRC clocks.
- All PWM Processing clocks generated internally via:
  - An external crystal - 24.576 MHz to 54 MHz, or
  - XTI input pin capable of supporting a clock signal at the VDX voltage level.
- Programmable divide of XTI by 1, 2, 4, 8 for SYS_CLK output.
- Programmable divide of XTI by 32, 64, 128, 256 for PS_SYNC (power supply synchronization signal).

Digital Audio Playback

- Supports 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz and 192 kHz sample frequencies.
- High performance sample rate converter.
- 16, 20 and 24 bit audio sample lengths.
- De-emphasis for 32 kHz, 44.1 kHz, 48 kHz.

- Digital volume control with soft ramp.
- Individual channel volume gain, attenuation and mute capability; +24 to -127 dB in 0.25 dB steps.
- Master volume attenuation; +24 to -127 dB in 0.25 dB steps.
- Peak Detect and Volume Limiter with programmable attack and release rates.
- Signal-clipping interrupt indicator.

Additional Features

- Contains a two-stage digital output filter for speaker impedance compensation.
- Provides 7 programmable GPIO pins with interrupt generation for easily interfacing to a variety of commonly available power state parts. Interrupts can be masked.
- Selectable over-sample rate for increased audio bandwidth.
- Power supply clock output, PS_SYNC, with programmable divider

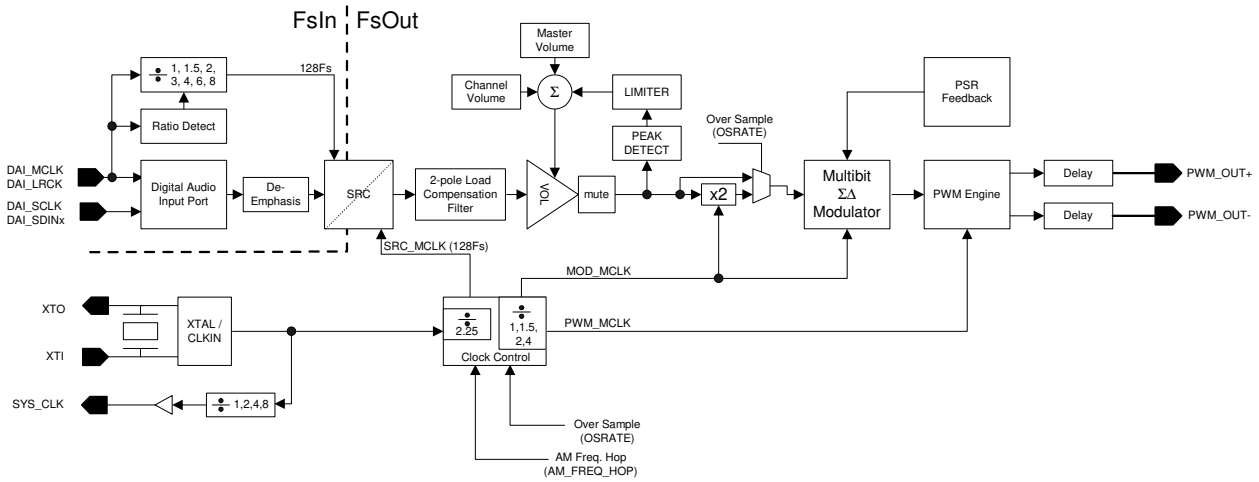

Figure 13. CS44600 Data Flow Diagram (Single Channel Shown)

4.3 Clock Generation

The sources for internal clock generation for the PWM processing are as follows:

- FsIn Domain:
  - DAI_MCLK, minimum 128Fs
- FsOut Domain:
  - XTI/XTO (Fundamental or 3rd overtone crystal), or
  - Clock signal on XTI (VDX is used to set logic voltage level)

4.3.1 FsIn Domain Clocking

Common DAI_MCLK frequencies and sample rates are shown in Table 1.

Mode (sample-rate range)	Sample Rate (kHz)	DAI_MCLK (MHz)				
DAI_MCLK/LRCK Ratio –>		**256x**	**384x**	**512x**	**768x**	**1024x**
Single Speed (4 to 50 kHz)	32	8.1920	12.2880	16.3840	24.5760	32.7680
	44.1	11.2896	16.9344	22.5792	33.8688	45.1584
	48	12.2880	18.4320	24.5760	36.8640	49.1520
DAI_MCLK/LRCK Ratio –>		**128x**	**192x**	**256x**	**384x**	**512x**
Double Speed (50 to 100 kHz)	64	8.1920	12.2880	16.3840	24.5760	32.7680
	88.2	11.2896	16.9344	22.5792	33.8688	45.1584
	96	12.2880	18.4320	24.5760	36.8640	49.1520
DAI_MCLK/LRCK Ratio –>		**64x**	**96x**	**128x**	**192x**	**256x**
Quad Speed (100 to 200 kHz)	176.4	n/a	n/a	22.5792	33.8688	45.1584
	192	n/a	n/a	24.5760	36.8640	49.1520

Table 1. Common DAI_MCLK Frequencies

4.3.2 FsOut Domain Clocking

To ensure the highest quality conversion of PWM signals, the CS44600 is capable of operating from a fundamental mode or 3rd overtone crystal, or a clock signal attached to XTI, at a frequency of 24.576 MHz to 54 MHz. If XTI is being directly driven by a clock signal, XTO can be left floating or tied to ground through a pull-down resistor and the internal oscillator should be powered down using the PDN_XTAL bit in register 02h.

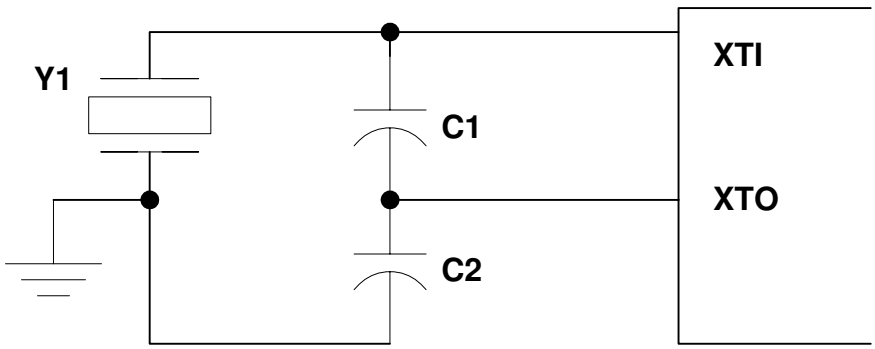

Figure 14. Fundamental Mode Crystal Configuration

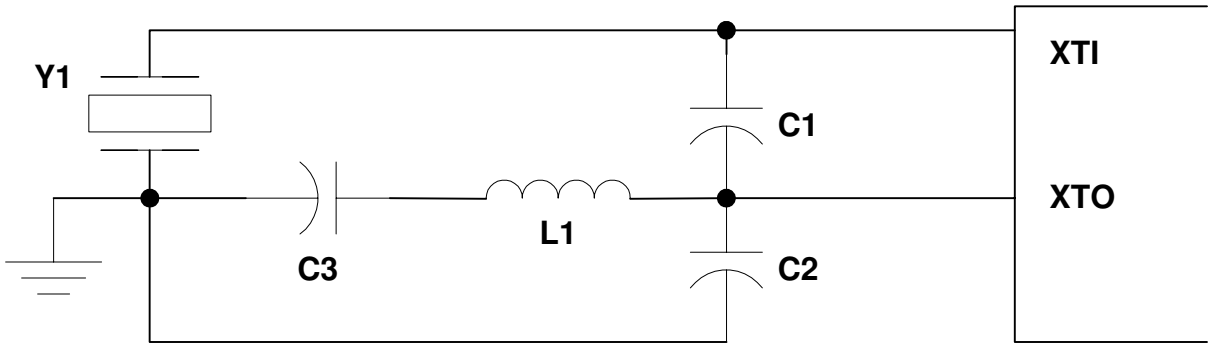

Figure 15. 3rd Overtone Crystal Configuration

Appropriate clock dividers for each functional block and a programmable divider to support an output for switched-mode power supply synchronization are provided. The clock generation for the CS44600 is shown in the Figure 16.

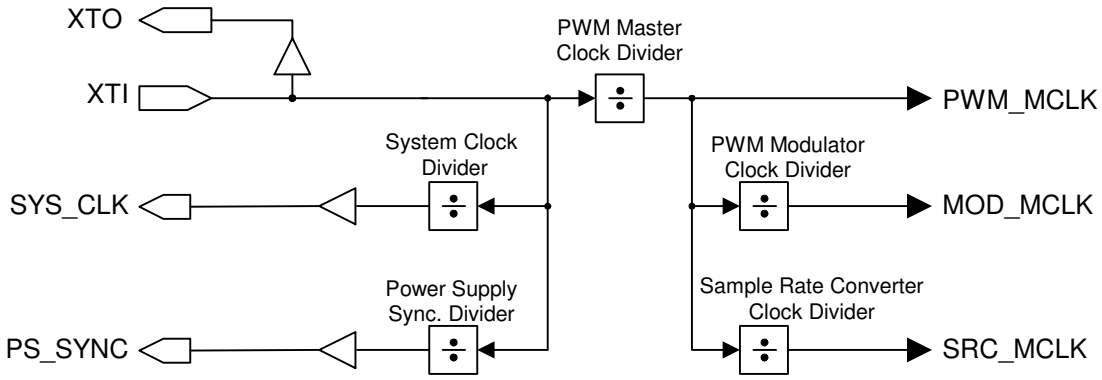

Figure 16. CS44600 Internal Clock Generation