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CS44L11

Low Voltage Class-D PWM Headphone Amplifier

Features

- Up to 95 dB Dynamic Range
- 1.8 V to 2.4 V Analog and Digital Supplies
- Sample Rates up to 96 kHz
- Digital Tone Control
  - 3 Selectable HPF and LPF Corner Frequencies
  - 12 dB Boost for Bass and Treble - 1 dB step size
- Programmable Digital Volume Control
  - +18 to -96 dB in 1 dB steps
- Peak Signal Soft Limiting
- De-emphasis for 32 kHz, 44.1 kHz, and 48 kHz
- Selectable Outputs for Each Channel, including
  - Channel A: R, L, mono (L + R) / 2, mute
  - Channel B: R, L, mono (L + R) / 2, mute
- PWM PopGuard®
- 23 mW/Channel into 16 Ω @ 2.4 V

Description

The CS44L11 is a complete stereo digital-to-PWM Class-D audio amplifier system controller including interpolation, volume control, and a headphone amplifier in a 16-pin TSSOP package.

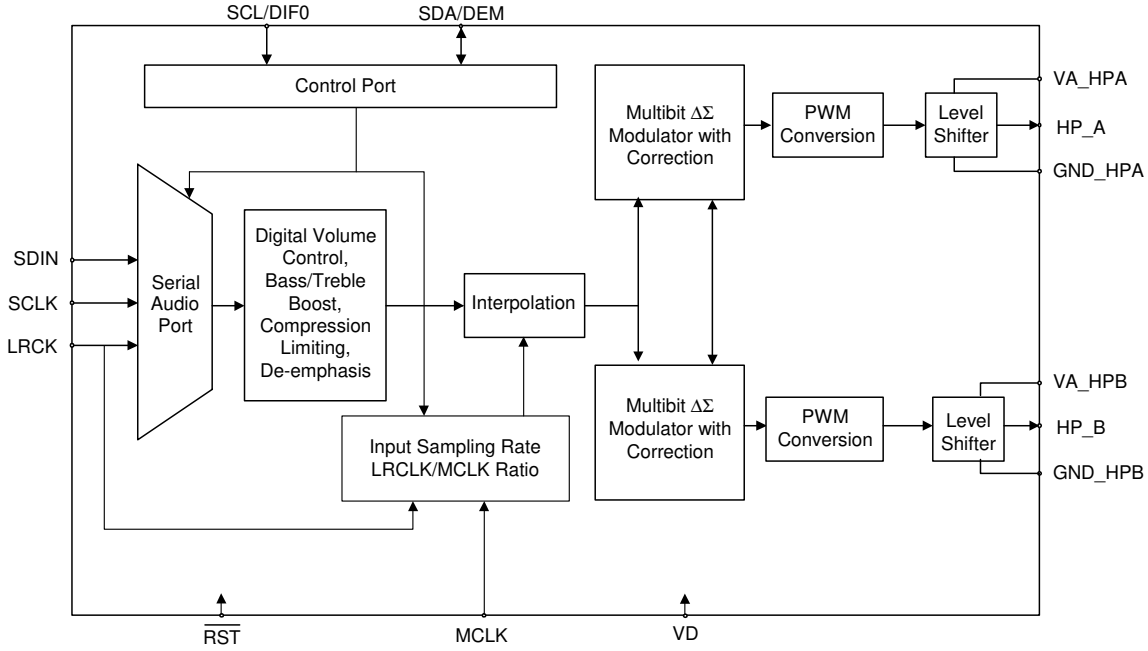
The CS44L11 architecture uses a direct-to-digital approach that maintains digital signal integrity to the final output filter. This minimizes analog interference effects that can negatively affect system performance.

The CS44L11 contains on-chip digital bass and treble boost, peak signal limiting, and de-emphasis. The PWM amplifier can achieve greater than 90% efficiency. This efficiency leads to longer battery life for portable systems, smaller device package, less heat sink requirements, and smaller power supplies.

The CS44L11 is ideal for portable audio, headphone amplifiers, and mobile phones.

ORDERING INFORMATION

CS44L11-CZZ, Lead Free -10 to 70 °C 16-pin TSSOP



Preliminary Product Information This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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1. CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and TA = 25°C.)

SPECIFIED OPERATING CONDITIONS

(GND = 0 V, all voltages with respect to 0 V)

Parameters		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Headphone	VA_HPx	1.7	-	2.5	V
	Digital	VD	1.7	-	2.5	V
Ambient Temperature		T_A	-10	-	70	°C

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V; all voltages with respect to 0 V. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.)

Parameters		Symbol	Min	Max	Units
DC Power Supplies:	Headphone	VA_HPx	-0.3	3.0	V
	Digital	VD	-0.3	3.0	V
Input Current, Any Pin Except Supplies		I_{in}		±10	mA
Digital Input Voltage		V_{IND}	-0.3	VD + 0.4	V
Ambient Operating Temperature (power applied)		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

PERFORMANCE SPECIFICATIONS

(Full-Scale Output Sine Wave, 997 Hz, MCLK = 12.288 MHz, Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified; Fs for Single-Speed Mode = 48 kHz, SCLK = 3.072 MHz; Fs for Double-Speed Mode = 96 kHz, SCLK = 6.144 MHz. Test load RL= 16 Ω, CL = 10 pF. Performance results are measured in production using a 4700 µF capacitor on the VA_HPx pins. Results will be degraded if smaller value capacitors are used.)

Parameter			Symbol	Min	Typ	Max	Unit
Headphone Output Dynamic Performance for VD = VA_HPx = 2.4 V							
Dynamic Range	18 to 24-Bit	A-Weighted		90	95	-	dB
		UnWeighted		88	93	-	dB
	16-Bit	A-Weighted		88	93	-	dB
		Unweighted		86	91	-	dB
Total Harmonic Distortion + Noise		0 dBFS	THD+N	-	-60	-55	dB
		-20 dBFS		-	-73	-	dB
		-60 dBFS		-	-33	-	dB
Interchannel Isolation		(1 kHz)		-	TBD	-	dB
Headphone Output Dynamic Performance for VD = VA_HPx = 1.8 V							
Dynamic Range	18 to 24-Bit	A-Weighted		87	92	-	dB
		UnWeighted		85	90	-	dB
	16-Bit	A-Weighted		85	90	-	dB
		Unweighted		83	88	-	dB
Total Harmonic Distortion + Noise		0 dB	THD+N	-	-55	-50	dB
		-20 dB		-	-70	-	dB
		-60 dB		-	-30	-	dB
Interchannel Isolation		(1 kHz)		-	60	-	dB
PWM Headphone Output							
Full-Scale Headphone Output Voltage				-	0.75 x VA_HP	-	Vpp
Headphone Output Quiescent Voltage				-	0.5 x VA_HP	-	VDC
Interchannel Gain Mismatch				-	0.1	-	dB
Modulation Index				-	-	85	%
Maximum Headphone Output		VA_HPx=2.4 V	I_{HP}	-	38	-	mA
RMS AC-Current		VA_HPx=1.8 V		-	28	-	mA

Parameter		Symbol	Single-Speed Mode			Double-Speed Mode			Unit
			Min	Typ	Max	Min	Typ	Max	
Digital Filter Response (Note 1)***)***									
Passband	to -0.05 dB corner		0	-	.4535	-	-	-	Fs
(Note 2)	to -0.1 dB corner		-	-	-	0	-	.4426	Fs
	to -3 dB corner		0	-	.4998	0	-	.4984	Fs
Frequency Response 10 Hz to 20 kHz (Note 3)			-.02	-	+.08	0	-	+0.11	dB
StopBand			.5465	-	-	.577	-	-	Fs
StopBand Attenuation (Note 4)			50	-	-	55	-	-	dB
Group Delay		tgd	-	9/Fs	-	-	4/Fs	-	s

Parameter		Symbol	Single-Speed Mode Min	Typ	Max	Double-Speed Mode Min	Typ	Max	Unit
Passband Group Delay Deviation	0 - 40 kHz		-	-	-	-	±1.39/Fs	-	s
	0 - 20 kHz		-	±0.36/Fs	-	-	±0.23/Fs	-	s
De-emphasis Error	Fs = 32 kHz		-	-	+.2/-.1		(Note 5)		dB
(Relative to 1 kHz)	Fs = 44.1 kHz		-	-	+.05/-.14				dB
	Fs = 48 kHz		-	-	+0/-.22				dB

Notes:

1. Filter response is not tested but is guaranteed by design.
2. Response is clock-dependent and will scale with Fs. Note that the response plots (Figures 8-15) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
3. Referenced to a 1 kHz, full-scale sine wave.
4. For Single-Speed Mode, the measurement bandwidth is 0.5465 Fs to 3 Fs.
   For Double-Speed Mode, the measurement bandwidth is 0.577 Fs to 1.4 Fs.
5. De-emphasis is not available in Double-Speed Mode.

DIGITAL CHARACTERISTICS

(GND = 0 V; all voltages with respect to 0 V.)

Parameters	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	0.7 x VD	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.3 x VD	V
Input Leakage Current	I_{in}	-	-	±10	µA
Input Capacitance		-	8	-	pF

POWER AND THERMAL CHARACTERISTICS

(GND = 0 V; all voltages with respect to 0 V. HP_x outputs unloaded.)

Parameters		Symbol	Min	Typ	Max	Units
Power Down (Note 6)						
Power Supply Current	VD = VA_HPx = 2.4 V		-	380	-	µA
	VD = VA_HPx = 1.8 V		-	110	-	µA
Normal Operation (Note 7)						
Power Supply Current	VD = VA_HPx = 2.4 V		-	14	-	mA
	VD = VA_HPx = 1.8 V		-	9	-	mA
Total Power Dissipation-	VD = VA_HPx = 2.4 V		-	34	-	mW
Normal Operation (Note 6)	VD = VA_HPx = 1.8 V		-	16	-	mW
Maximum Headphone Power Output						
(1 kHz full-scale sine wave	VA_HPx = 2.4 V		-	23	-	mW
into 16 Ω load)	VA_HPx = 1.8 V		-	13	-	mW
Power Supply Rejection Ratio		PSRR	-	0	-	dB
Package Thermal Resistance		θ_{JA}	-	75	-	°C/Watt

Notes:

6. Power Down Mode is defined as $\overline{RST}$ = LOW with all clocks and data lines held static.
7. Normal operation is defined as RST = HI.

SWITCHING CHARACTERISTICS

(GND = 0 V; all voltages with respect to 0 V.)

Parameters		Symbol	Min	Typ	Max	Units
Input Sample Rate	Single-Speed Mode	Fs	8	-	50	kHz
	Double-Speed Mode	Fs	50	-	100	kHz
MCLK Duty Cycle			40	50	60	%
LRCK Duty Cycle			40	50	60	%
SCLK Pulse Width Low		t_{sclkl}	20	-	-	ns
SCLK Pulse Width High		t_{sclkh}	20	-	-	ns
SCLK Period	Single-Speed Mode	t_{sclkw}	$\frac{1}{(128)Fs}$	-	-	ns
	Double-Speed Mode	t_{sclkw}	$\frac{1}{(64)Fs}$	-	-	ns
SCLK rising to LRCK edge delay		t_{slrd}	20	-	-	ns
SCLK rising to LRCK edge setup time		t_{slrs}	20	-	-	ns
SDIN valid to SCLK rising setup time		t_{sdlrs}	20	-	-	ns
SCLK rising to SDIN hold time		t_{sdh}	20	-	-	ns

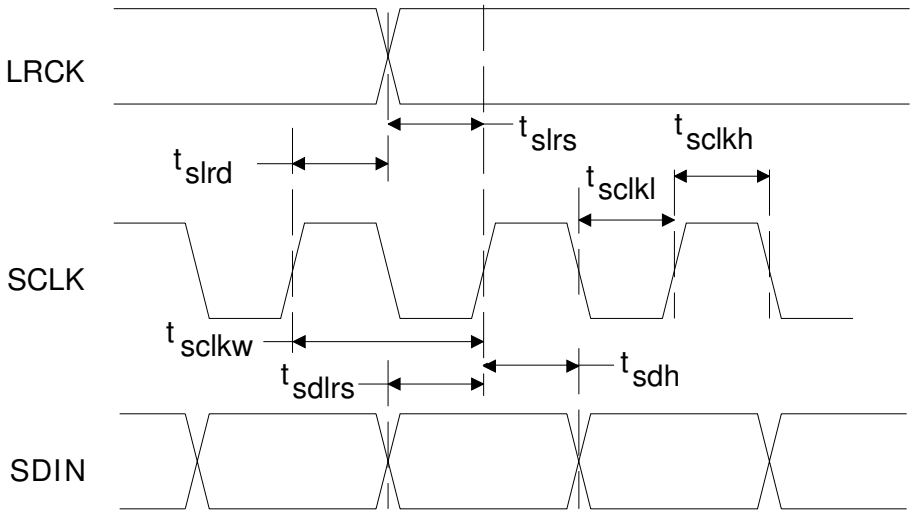


Figure 1. Serial Audio Data Interface Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - I²C FORMAT

(GND = 0 V; all voltages with respect to 0 V.)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{RST}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 8)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}, t_{rc}	-	1	µs
Fall Time SCL and SDA	t_{fc}, t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling (Note 9)	t_{ack}	-	(Note 10)	ns

Notes:

8. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.
9. The acknowledge delay is based on MCLK and can limit the maximum transaction speed.
10. $\frac{5}{256 \times Fs}$ for Single-Speed Mode and $\frac{5}{128 \times Fs}$ for Double-Speed Mode.

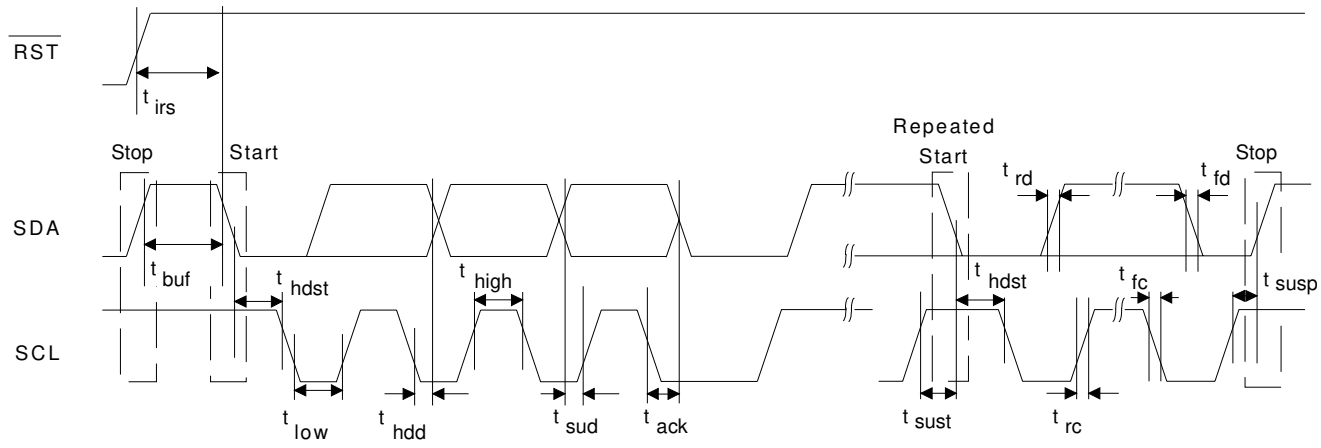
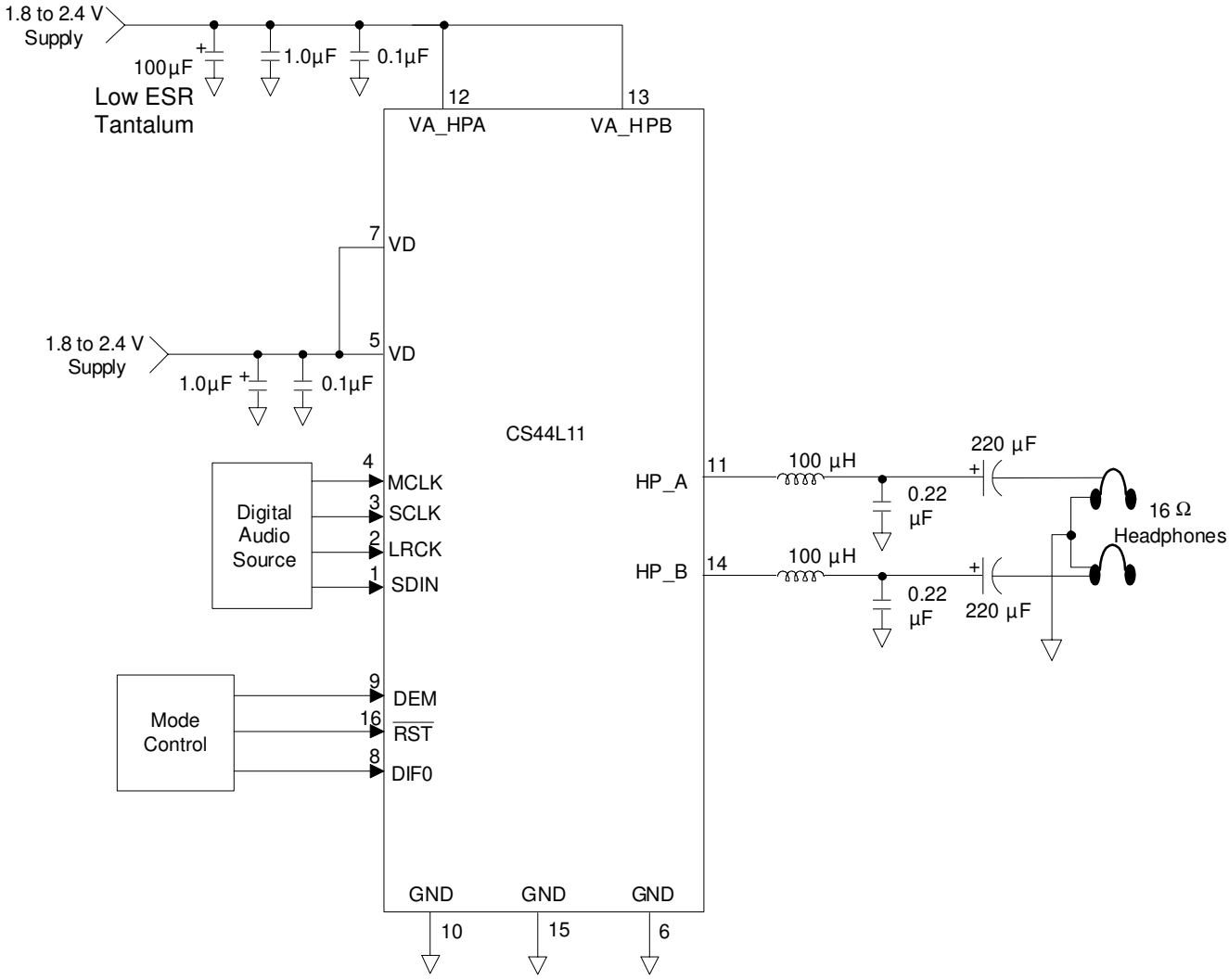


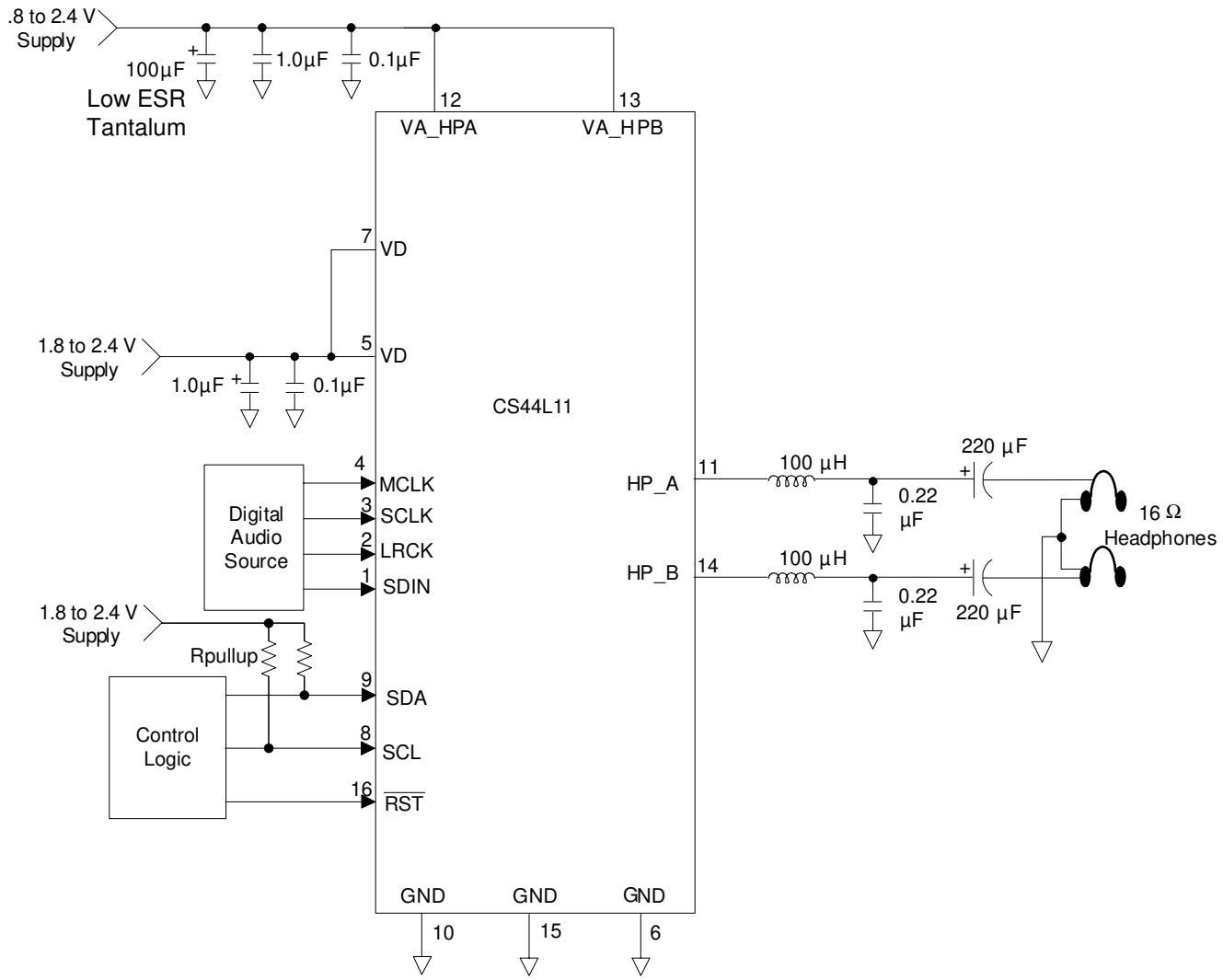
Figure 2. Control Port Timing - I²C Format

2. TYPICAL CONNECTION DIAGRAMS



* Filter component values shown are for a 16 Ω load. Please see the CDB44L11 datasheet for information on how to calculate filter values for other loads.

Figure 3. Typical CS44L11 Connection Diagram Stand-Alone Mode



* Filter component values shown are for a 16 Ω load. Please see the CDB44L11 datasheet for information on how to calculate filter values for other loads.

Figure 4. Typical CS44L11 Connection Diagram Control Port Mode

3. REGISTER QUICK REFERENCE

Addr	Function	7	6	5	4	3	2	1	0
2h	Power and Muting Control	SZC1	SZC0	PDN	FLT	RUPBYP	RDNBYP	Reserved	Reserved
	default	1	0	1	0	0	0	0	0
3h	Channel A Volume Control	VOLA7	VOLA6	VOLA5	VOLA4	VOLA3	VOLA2	VOLA1	VOLA0
	default	0	0	0	0	0	0	0	0
4h	Channel B Volume Control	VOLB7	VOLB6	VOLB5	VOLB4	VOLB3	VOLB2	VOLB1	VOLB0
	default	0	0	0	0	0	0	0	0
5h	Tone Control	BB3	BB2	BB1	BB0	TB3	TB2	TB1	TB0
	default	0	0	0	0	0	0	0	0
6h	Mode Control 1	BBCF1	BBCF0	TBCF1	TBCF0	TC1	TC0	TC_EN	LIM_EN
	default	0	0	0	0	0	0	0	0
7h	Limiter Attack Rate	ARATE7	ARATE6	ARATE5	ARATE4	ARATE3	ARATE2	ARATE1	ARATE0
	default	0	0	0	1	0	0	0	0
8h	Limiter Release Rate	RRATE7	RRATE6	RRATE5	RRATE4	RRATE3	RRATE2	RRATE1	RRATE0
	default	0	0	1	0	0	0	0	0
9h	Volume and Mixing Control	Reserved	Reserved	RMP_SP1	RMP_SP0	ATAPI3	ATAPI2	ATAPI1	ATAPI0
	default	0	0	0	1	1	0	0	1
Ah	Mode Control2	mclkdiv	CLKDV1	CLKDV0	DBS	FRQSFT1	FRQSFT0	DEM1	DEM0
	default	0	0	0	0	0	0	0	0
Bh	Mode Control 3	DIF1	DIF0	A=B	VCBYP	CP_EN	FREEZE	Reserved	Reserved
	default	0	0	0	0	0	0	0	0
Ch	Revision Indicator	Reserved	Reserved	Reserved	Reserved	REV3	REV2	REV1	REV0
	default	0	0	0	0	Read Only	Read Only	Read Only	Read Only

Table 1. Register Quick Reference

4. REGISTER DESCRIPTIONS

4.1 Power and Muting Control (address 02h)

7	6	5	4	3	2	1	0
SZC1	SZC0	PDN	FLT	RUPBYP	RDNBYP	Reserved	Reserved
1	0	1	0	0	0	0	0

4.1.1 Soft Ramp and Zero Cross Control (SZC)

Default = 10
00 - Immediate Change
01 - Zero Cross Control
10 - Ramped Control
11 - Reserved

Function:

Immediate Change

When Immediate Change is selected, all level changes will take effect immediately in one step.

Zero Cross Control

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a time-out period of 512 sample periods (10.7 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Ramped Control

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods.

Note: Ramped Control is not available in Double-Speed Mode.

4.1.2 Power Down (PDN)

Default = 1
0 - Disabled
1 - Enabled

Function:

The entire device will enter a low-power state when this function is enabled, and the contents of the control registers are retained in this mode. The power-down bit defaults to ‘enabled’ on power-up and must be disabled before normal operation in Control Port Mode can occur.

4.1.3 Float Output (FLT)

Default = 0
0 - Disabled
1 - Enabled

Function:

When enabled, this bit will cause the headphone output of the CS44L11 to float when in the power down state (PDN=1). The float function can be used in single-ended applications to maintain the charge on the

DC-blocking capacitor during power transients. On power transitions, the output will quickly change to the bias point; however, if the DC-blocking capacitor still has a full charge, as in short power cycles, the transition will be very small, often inaudible. Refer to Section 6.4.

4.1.4 Ramp-Up Bypass (RUPBYP)

Default = 0
0 - Normal
1 - Bypass

Function:

When in normal mode, the duty cycle of the output PWM signal is increased at a rate determined by the Ramp Speed variable (RMP_SPx). Normal mode is used in Single-Ended applications to reduce pops in the output caused by the DC-blocking capacitor. When the ramp-up function is bypassed in Single-Ended applications, there will be an abrupt change in the output signal. Refer to Section 6.4.

4.1.5 Ramp-Down Bypass (RDNBYP)

Default = 0
0 - Disabled
1 - Enabled

Function:

When in normal mode, the duty cycle of the output PWM signal is decreased at a rate determined by the Ramp Speed variable (RMP_SPx). Normal mode is used in Single-Ended applications to reduce pops in the output caused by the DC-blocking capacitor and changes in bias conditions. When the ramp-down function is bypassed in Single-Ended applications, there will be an abrupt change in the output signal. Refer to Section 6.4.

4.2 Channel A Volume Control (address 03h) (VOLA)

4.3 Channel B Volume Control (address 04h) (VOLB)

7	6	5	4	3	2	1	0
VOLx7	VOLx6	VOLx5	VOLx4	VOLx3	VOLx2	VOLx1	VOLx0
0	0	0	0	0	0	0	0

Default = 0 dB (No attenuation)

Function:

The Volume Control registers allow independent control of the signal levels in 1 dB increments from +18 to -96 dB. Volume settings are decoded using a 2's complement code, as shown in Table 2. The volume changes are implemented as dictated by the Soft and Zero Cross bits. All volume settings less than -96 dB are equivalent to muting the channel via the ATAPI bits (see Section 4.8.2).

Note: All volume settings greater than +18 dB are interpreted as +18 dB.

Binary Code	Decimal Value	Volume Setting
00001100	12	+12 dB
00000111	7	+7 dB
00000000	0	0 dB
11000100	-60	-60 dB
10100110	-90	-90 dB

Table 2. Example Volume Settings

4.4 Tone Control (address 05h)

7	6	5	4	3	2	1	0
BB3	BB2	BB1	BB0	TB3	TB2	TB1	TB0
0	0	0	0	0	0	0	0

4.4.1 Bass Boost Level (BB)

Default = 0 dB (No Bass Boost)

Function:

The level of the shelving Bass Boost filter is set by Bass Boost Level. The level can be adjusted in 1 dB increments from 0 to +12 dB of boost. Boost levels are decoded as shown in Table 3. Levels above +12 dB are interpreted as +12 dB.

Binary Code	Decimal Value	Boost Setting
0000 0000	0	0 dB
0000 0010	2	+2 dB
0000 0110	6	+6 dB
0000 1001	9	+9 dB
0000 1100	12	+12 dB

Table 3. Example Bass Boost Settings

4.4.2 Treble Boost Level (TB)

Default = 0 dB (No Treble Boost)

Function:

The level of the shelving Treble Boost filter is set by Treble Boost Level. The level can be adjusted in 1 dB increments from 0 to +12 dB of boost. Boost levels are decoded as shown in Table 4. Levels above +12 dB are interpreted as +12 dB.

Note: Treble Boost is not available in Double-Speed Mode.

Binary Code	Decimal Value	Boost Setting
0000 0000	0	0 dB
0000 0010	2	+2 dB
0000 0110	6	+6 dB
0000 1001	9	+9 dB
0000 1100	12	+12 dB

Table 4. Example Treble Boost Settings

4.5 Mode Control 1 (address 06h)

7	6	5	4	3	2	1	0
BBCF1	BBCF0	TBCF1	TBCF0	TC1	TC0	TC_EN	LIM_EN
0	0	0	0	0	0	0	0

4.5.1 Bass Boost Corner Frequency (BBCF)

Default = 00
00 - 50 Hz
01 - 100 Hz
10 - 200 Hz
11 - Reserved

Function:

The Bass Boost corner frequency is user-selectable. The corner frequency is a function of LRCK (sampling frequency), the DBS bit and the BBCF bits as shown in Table 5 and Table 6.

BBCF	LRCK in Single-Speed Mode (DBS=0)			
Fs	48 kHz	24 kHz	12 kHz	8 kHz
00	50 Hz	25 Hz	12.5 Hz	8.33 Hz
01	100 Hz	50 Hz	25 Hz	16.7 Hz
10	200 Hz	100 Hz	50 Hz	33.3 Hz
11	Reserved	Reserved	Reserved	Reserved

Table 5. Base Boost Corner Frequencies in Single-Speed Mode

BBCF	LRCK in Double-Speed Mode (DBS=1)			
Fs	96 kHz	48 kHz	24 kHz	16 kHz
00	50 Hz	25 Hz	12.5 Hz	8.33 Hz
01	100 Hz	50 Hz	25 Hz	16.7 Hz
10	200 Hz	100 Hz	50 Hz	33.3 Hz
11	Reserved	Reserved	Reserved	Reserved

Table 6. Base Boost Corner Frequencies in Double-Speed Mode

4.5.2 Treble Boost Corner Frequency (TBCF)

Default = 00
00 - 2 kHz
01 - 4 kHz
10 - 7 kHz
11 - Reserved

Function:

The Treble Boost corner frequency is user selectable. The corner frequency is a function of LRCK (sampling frequency) and the TBCF bits as shown in Table 7.

Note: Treble Boost is not available in Double-Speed Mode.

TBCF	LRCK in Single-Speed Mode (DBS=0)			
Fs	48 kHz	24 kHz	12 kHz	8 kHz
00	2 kHz	1 kHz	0.5 kHz	0.33 kHz
01	4 kHz	2 kHz	1 kHz	0.67 kHz
10	7 kHz	3.5 kHz	1.75 kHz	1.17 kHz
11	Reserved	Reserved	Reserved	Reserved

Table 7. Treble Boost Corner Frequencies in Single-Speed Mode

4.5.3 Tone Control Mode (TC)

Default = 00
00 - All settings are taken from user registers
01 - 12 dB of Bass Boost at 100 Hz and 6 dB of Treble Boost at 7 kHz (at LRCK = 48 kHz)
10 - 8 dB of Bass Boost at 100 Hz and 4 dB of Treble Boost at 7 kHz (at LRCK = 48 kHz)
11 - 4 dB of Bass Boost at 100 Hz and 2 dB of Treble Boost at 7 kHz (at LRCK = 48 kHz)

Function:

The Tone Control Mode bits determine how the Bass Boost and Treble Boost features are configured. The user-defined settings from the Bass and Treble Boost Level and Corner Frequency registers are used when these bits are set to '00'. Alternately, one of three pre-defined settings may be used (these settings are a function of LRCK - refer to Tables 5, 6, and 7).

Note: Treble Boost is not available in Double-Speed Mode.

4.5.4 Tone Control Enable (TC_EN)

Default = 0
0 - Disabled
1 - Enabled

Function:

The Bass Boost and Treble Boost features are active when this function is enabled.

4.5.5 Peak Signal Limiter Enable (LIM_EN)

Default = 0
0 - Disabled
1 - Enabled

Function:

The CS44L11 will limit the maximum signal amplitude to prevent clipping when this function is enabled. Peak Signal Limiting is performed by first decreasing the Bass and Treble Boost Levels. If the signal is still clipping, the digital attenuation is increased. The attack rate is determined by the Limiter Attack Rate register.

Once the signal has dropped below the clipping level, the attenuation is decreased back to the user-selected level, followed by the Bass Boost being increased back to the user-selected level. The release rate is determined by the Limiter Release Rate register.

Note: The A=B bit should be set to '1' for optimal limiter performance.

4.6 Limiter Attack Rate (address 07h) (ARATE)

7	6	5	4	3	2	1	0
ARATE7	ARATE6	ARATE5	ARATE4	ARATE3	ARATE2	ARATE1	ARATE0
0	0	0	1	0	0	0	0

Default = 10h - 2 LRCK's per 1/8 dB

Function:

The limiter attack rate is user-selectable. The rate is a function of sampling frequency, Fs, and the value in the Limiter Attack Rate register. Rates are calculated using the function RATE = 32/{value}, where {value} is the decimal value in the Limiter Attack Rate register and RATE is in LRCK's per 1/8 dB of change.

A value of zero in this register is not recommended, as it will induce erratic behavior of the limiter. Use the LIM_EN bit to disable the limiter function (see "Peak Signal Limiter Enable (LIM_EN)").

Binary Code	Decimal Value	LRCK's per 1/8 dB
00000001	1	32
00010100	20	1.6
00101000	40	0.8
00111100	60	0.53
01011010	90	0.356

Table 8. Example Limiter Attack Rate Settings

4.7 Limiter Release Rate (address 08h) (RRATE)

7	6	5	4	3	2	1	0
RRATE7	RRATE6	RRATE5	RRATE4	RRATE3	RRATE2	RRATE1	RRATE0
0	0	1	0	0	0	0	0

Default = 20h - 16 LRCK's per 1/8 dB

Function:

The limiter release rate is user-selectable. The rate is a function of sampling frequency, Fs, and the value in the Limiter Release Rate register. Rates are calculated using the function RATE = 512/{value}, where {value} is the decimal value in the Limiter Release Rate register and RATE is in LRCK's per 1/8 dB of change.

Note: A value of zero in this register is not recommended, as it will induce erratic behavior of the limiter. Use the LIM_EN bit to disable the limiter function (see "Peak Signal Limiter Enable (LIM_EN)").

Binary Code	Decimal Value	LRCK's per 1/8 dB
00000001	1	512
00010100	20	25
00101000	40	12
00111100	60	8
01011010	90	5

Table 9. Example Limiter Release Rate Settings

4.8 Volume and Mixing Control (address 09h)

7	6	5	4	3	2	1	0
Reserved	Reserved	RMP_SP1	RMP_SP0	ATAPI3	ATAPI2	ATAPI1	ATAPI0
0	0	0	0	1	0	0	1

4.8.1 Ramp Speed (RMP_SP)

Default = 01
00 - Ramp speed = approximately 0.1 seconds
01 - Ramp speed = approximately 0.2 seconds
10 - Ramp speed = approximately 0.3 seconds
11 - Ramp speed = approximately 0.65 seconds

Function:

This feature is used in Single-Ended applications to reduce pops in the output caused by the DC-blocking capacitor. When in Control Port Mode, the Ramp Speed sets the time for the PWM signal to linearly ramp up and down from the bias point (50% PWM duty cycle). Refer to Section 6.4.

4.8.2 ATAPI Channel Mixing and Muting (ATAPI)

Default = 1001 - HP_A = L, HP_B = R (Stereo)

Function:

The CS44L11 implements the channel mixing functions of the ATAPI CD-ROM specification. Refer to Table 10 and Figure 5 for additional information.

Note: All mixing functions occur prior to the digital volume control.

ATAPI3	ATAPI2	ATAPI1	ATAPI0	HP_A	HP_B
0	0	0	0	MUTE	MUTE
0	0	0	1	MUTE	R
0	0	1	0	MUTE	L
0	0	1	1	MUTE	[(L+R)/2]
0	1	0	0	R	MUTE
0	1	0	1	R	R
0	1	1	0	R	L
0	1	1	1	R	[(L+R)/2]
1	0	0	0	L	MUTE
1	0	0	1	L	R
1	0	1	0	L	L
1	0	1	1	L	[(L+R)/2]
1	1	0	0	[(L+R)/2]	MUTE
1	1	0	1	[(L+R)/2]	R
1	1	1	0	[(L+R)/2]	L
1	1	1	1	[(L+R)/2]	[(L+R)/2]

Table 10. ATAPI Decode

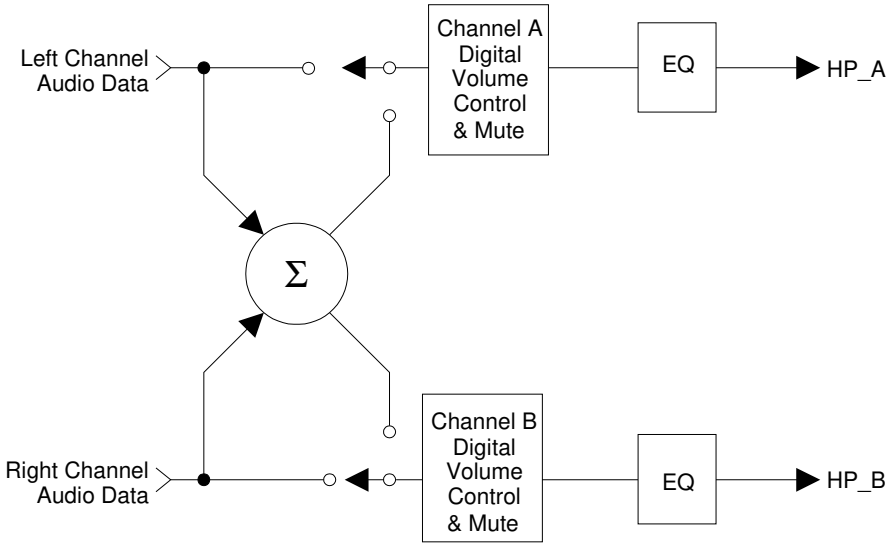


Figure 5. Dynamics Control Block Diagram

4.9 Mode Control 2 (address 0Ah)

7	6	5	4	3	2	1	0
mclkdiv	CLKDV1	CLKDV0	DBS	FRQSFT1	FRQSFT0	DEM1	DEM0
0	0	0	0	0	0	0	0

4.9.1 Master Clock Divide Enable (MCLKDIV)

Default = 0

Function:

The MCLKDIV bit enables a circuit which divides the externally applied MCLK signal by 2 prior to all other internal circuitry. MCLKDIV, DBS, CLKDIV and FRQSFT are set per the user's MCLK and LRCK requirements. Refer to Tables 11, 12, 13, and Section 6.2.

4.9.2 Clock Divide (CLKDIV)

Default = 00

Function:

MCLKDIV, DBS, CLKDIV and FRQSFT are set per the user's MCLK and LRCK requirements. Refer to Tables 11, 12, 13, and Section 6.2.

4.9.3 Double-Speed Mode (DBS)

Default = 0
0 - Single-Speed
1 - Double-Speed (DBS)

Function:

Single-Speed supports 8 kHz to 50 kHz sample rates and Double-Speed supports 50 kHz to 96 kHz sample rates. MCLKDIV, DBS, CLKDIV and FRQSFT are set per the user's MCLK and LRCK requirements. Refer to Tables 11, 12, 13, and Section 6.2.

Note: De-emphasis, ramp control, and treble control are not available in Double-Speed Mode.

4.9.4 Frequency Shift (FRQSFT)

Default = 00

Function:

MCLKDIV, DBS, CLKDIV and FRQSFT are set per the user's MCLK and LRCK requirements. Refer to Tables 11, 12, 13, and Section 6.2.

	DBS = 0 MCLKDIV = 0		DBS = 0 MCLKDIV = 1						
LRCK (kHz)	**MCLK/ LRCK**	**MCLK (MHz)**	**MCLK/ LRCK**	**MCLK (MHz)**	**FRQSFT1**	**FRQSFT0**	**CLKDIV1**	**CLKDIV0**	**PWM Switching Freq. (kHz)**
48	256	12.288	512	24.576	0	0	0	0	384
48	512	24.576	1024	49.152	0	0	1	0	
44.1	256	11.2896	512	22.5792	0	0	0	0	352.8
44.1	512	22.5792	1024	45.1584	0	0	1	0	
32	512	16.384	1024	32.768	0	1	0	0	512
32	1024	32.768	2048	65.536	0	1	1	0	
24	512	12.288	1024	24.576	0	1	0	0	384
24	1024	24.576	2048	49.152	0	1	1	0	
12	1024	12.288	2048	24.576	1	0	0	0	384
12	2048	24.576	4096	49.152	1	0	1	0	

Table 11. Single-Speed Clock Modes - Control Port Mode

LRCK (kHz)	MCLK/ LRCK	MCLK (MHz)	PWM Switching Freq. (kHz)
48	256	12.288	384
48	512	24.576	
44.1	256	11.2896	352.8
44.1	512	22.5792	
32	1024	32.768	512
24	1024	24.576	384
12	2048	24.576	

Table 12. Single-Speed Clock Modes - Stand-Alone Mode

	DBS = 1 MCLKDIV = 0		DBS = 1 MCLKDIV = 1						
LRCK (kHz)	MCLK/ LRCK	MCLK (MHz)	MCLK/ LRCK	MCLK (MHz)	FRQSFT1	FRQSFT0	CLKDIV1	CLKDIV0	PWM Switching Freq. (kHz)
96	128	12.288	256	24.576	0	0	0	0	384
96	256	24.576	512	49.152	0	0	1	0	
88.2	128	11.2896	256	22.5792	0	0	0	0	352.8
88.2	256	22.5792	512	45.1584	0	0	1	0	

Table 13. Double-Speed Clock Modes - Control Port Mode

4.9.5 De-Emphasis Control (DEM)

Default = 00
00 - Disabled
01 - 44.1 kHz
10 - 48 kHz
11 - 32 kHz

Function:

Selects the appropriate digital filter to maintain the standard 15 µs/50 µs digital de-emphasis filter response at 32, 44.1 or 48 kHz sample rates (see Figure 6).

Note: De-emphasis is not available in Double-Speed Mode**.**

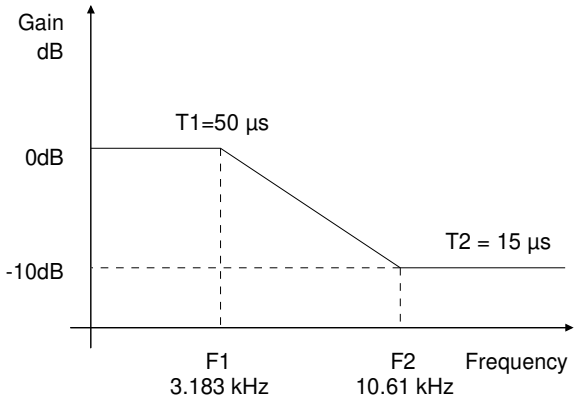


Figure 6. De-Emphasis Curve

4.10 Mode Control 3 (address 0Bh)

7	6	5	4	3	2	1	0
DIF1	DIF0	A=B	VCBYP	CP_EN	FREEZE	HPSEN	Reserved
0	0	0	0	0	0	0	0

4.10.1 Digital Interface Formats (DIF)

Default = 00
00 - I²S
01 - Right Justified, 16 bit
10 - Left Justified
11 - Right Justified, 24 bit

Function:

The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in Figures 16 through 19.

4.10.2 Channel A Volume = Channel B Volume (A=B)

Default = 0
0 - Disabled
1 - Enabled

Function:

The HP_A and HP_B volume levels are independently controlled by the A and the B Channel Volume Control Bytes when this function is disabled. The volume on both HP_A and HP_B are determined by the A Channel Volume Control Byte and the B Channel Byte is ignored when this function is enabled.

4.10.3 Volume Control Bypass (VCBYP)

Default = 0
0 - Disabled
1 - Enabled

Function:

The digital volume control section is bypassed when this function is enabled. This disables the digital volume control, muting, bass boost, treble boost, limiting, and ATAPI functions.

4.10.4 Control Port Enable (CP_EN)

Default = 0
0 - Disabled
1 - Enabled

Function:

This bit defaults to 0, allowing the device to power-up in Stand-Alone mode. The Control Port Mode can be accessed by setting this bit to 1. This will allow the operation of the device to be controlled by the registers and the pin definitions will conform to Control Port Mode. Refer to Section 6.5.2.

4.10.5 Freeze (FREEZE)

Default = 0
0 - Disabled
1 - Enabled

Function:

This function allows modifications to be made to the registers without the changes being taking effect until the FREEZE is disabled. To make multiple changes in the Control port registers take effect simultaneously, you will first enable the FREEZE Bit, then make all register changes, then Disable the FREEZE bit.

4.11 Revision Indicator (address 0Ch)[Read Only]

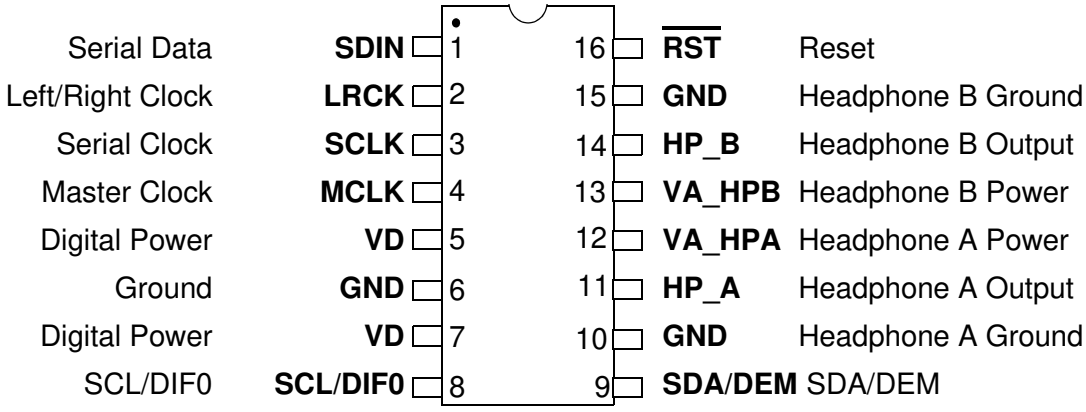
7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	REV3	REV2	REV1	REV0
0	0	0	0	0	0	0	0

Default = none
0001 - Revision A
0010 - Revision B
0011 - Revision C
etc.

Function:

This read-only register indicates the revision level of the device.

5. PIN DESCRIPTION



SDIN	1	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
LRCK	2	**Left Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line. The frequency of the left/right clock must be at the audio sample rate, Fs.
SCLK	3	**Serial Clock** (*Input*) - Serial clock for the serial audio interface.
MCLK	4	**Master Clock** (*Input*) - Clock source for the PWM modulator and digital filters. Tables 11, 12, 13 and 14 illustrate several standard audio sample rates and required master clock frequencies.
VD	5 7	**Digital Power** (*Input*) **-** Positive power supply for the digital section. Refer to "Specified Operating Conditions" for appropriate voltages.
GND	6, 10 & 15	**Ground** (*Input*) - Ground Reference.
HP_A HP_B	11 14	**Headphone Outputs** (*Output*) - PWM Headphone Outputs. An external LC filter should be added to suppress high frequency switching noise. A DC blocking capacitor is also required. Refer to Typical Connection Diagrams.
VA_HPA VA_HPB	12 13	**Headphone Amplifier Power** (*Input*) - Positive power supply for the headphone amplifier. Refer to "Specified Operating Conditions" for appropriate voltages.
RST	16	**Reset** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings when low. The control port cannot be accessed when Reset is low. See Section 6.5.
Control Port Definitions		
SCL	8	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port. Requires an external pull-up resistor to VD in I²C mode.
SDA	9	**Serial Control Data** (*Input/Output*) - SDA is a data I/O line in I²C mode and requires an external pull-up resistor to the logic interface voltage.
Stand-Alone Definitions		
DIF0	8	**Digital Interface Format** (I*nput*) - The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed below

DIF0	DESCRIPTION	FIGURE
0	I²S, up to 24-bit data	18
1	Right Justified, 16-bit Data	19

Table 14. Digital Interface Format (Stand-Alone Mode)

DEM	9	**De-emphasis Control** (*Input*) - Selects the standard 15 µs/50 µs digital de-emphasis filter response at 44.1 kHz sample rates. **NOTE:** De-emphasis is not available in Double- or Quad-Speed Modes. When DEM is grounded, de-emphasis is disabled.