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CS47L15

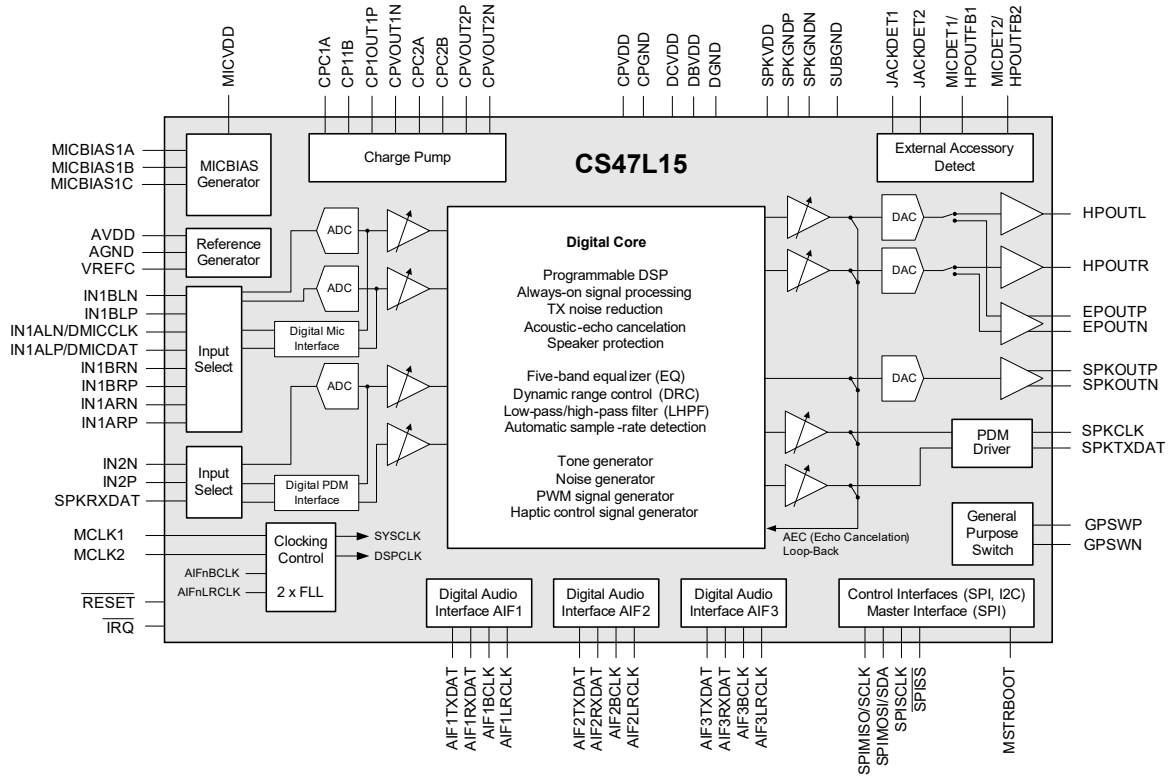
Smart Codec with Low-Power Audio DSP

Features

- 150 MIPS, 150 MMAC audio-signal processor
  - — Low-power, always-on voice trigger capability
  - — Speaker protection algorithm support
  - — Event loggers with time-stamp and interrupt functions
- Programmable wideband audio processing
  - — Transmit-path noise reduction and echo cancelation
- Integrated multichannel 24-bit hi-fi audio hub codec
  - — 98-dB signal-to-noise ratio (SNR) mic input (48 kHz)
  - — 127-dB SNR headphone playback (48 kHz)
  - — Low-power analog input modes
- Up to four analog or four digital microphone (DMIC) inputs
  - — Speaker-monitoring input path (analog or digital)
- Stereo headphone/earpiece/line output driver: 30 mW into 32-Ω load at 0.1% total harmonic distortion + noise (THD+N)
- Earpiece, speaker, and digital (pulse-density modulation, PDM) output interfaces
  - — Two-way stereo PDM interface
- Three full digital-audio interfaces
  - — Standard sample rates from 8 to 192 kHz
  - — Multichannel support on AIF1 and AIF2
- Self-boot capability from external non-volatile memory
- Flexible clocking, derived from MCLK*n* or AIF*n*
- Low-power frequency-locked loops (FLLs) support reference clocks down to 32 kHz
- Advanced accessory detection functions
- Configurable functions on up to 15 general-purpose input/output (GPIO) pins
- Small WLCSP package, 0.4-mm ball array

Applications

- Smartphones, tablets, and wearable technology
  - — Karaoke algorithm support



Description

The CS47L15 is a highly integrated, low-power audio hub for smartphones, tablets, and other portable audio devices including wearable technology. It combines an advanced DSP feature set with a flexible, high-performance audio hub codec. The CS47L15 combines a programmable DSP core with a variety of power-efficient fixed-function audio processors. An SPI master interface is provided, for autonomous boot-up and configuration using an external non-volatile memory—enabling the CS47L15 to be used independently of a host processor.

The DSP core supports advanced audio processing functions such as wideband noise reduction, acoustic-echo cancelation (AEC), speech enhancement, karaoke, and many more. Low-power analog and digital interfaces provide flexible support for always-on voice applications and speaker-protection algorithms implemented on the programmable DSP core. The DSP core is integrated within a fully flexible, all-digital mixing and routing engine with sample-rate converters, for wide use-case flexibility. Support for third-party DSP programming provides far-reaching opportunities for product differentiation.

Three digital audio interfaces are provided, each supporting a wide range of standard audio sample rates and serial interface formats. Automatic sample-rate detection enables seamless wideband/narrowband voice-call handover. The DACs and output paths provide full support for high definition audio throughout the entire signal chain.

The stereo headphone driver provides ground-referenced output, with noise levels as low as 0.45 μV_{RMS} for hi-fi quality line or headphone output. The CS47L15 also features a mono bridge-tied load (BTL) earpiece output, mono 2.5-W Class D speaker driver, two channels of stereo PDM output, and an IEC-60958-3–compatible S/PDIF transmitter. A signal generator for controlling haptics devices is included; vibe actuators can connect directly to the Class D speaker output, or via an external driver on the PDM output interface.

The CS47L15 supports up to five analog inputs, and up to four PDM digital inputs. As many as four analog microphone connections can be supported; a separate analog input channel is provided for use in speaker-protection applications. Microphone activity detection with interrupt is available. A smart accessory interface supports most standard 3.5-mm accessories. Impedance sensing and measurement is provided for external accessory and push-button detection (Android™ headset specification compliant).

The CS47L15 supports SPI™ and I^2C interface modes for control-register access. The CS47L15 can also be configured as SPI master, enabling autonomous boot-up and configuration without dependency on a host processor. Two integrated FLLs support a wide range of system-clock frequencies. The device is powered from 1.8- and 1.2-V supplies. Separate MICVDD input can be supported, for microphone operation above 1.8 V. An additional supply is required for the Class D speaker drivers (typically direct connection to 4.2-V battery). The power, clocking, and output driver architectures are designed to maximize battery life in voice, music, and standby modes. Low-power (25 μW) Sleep Mode is supported, with configurable wake-up events.

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1 Pin Descriptions

1.1 WLCSP Pinout

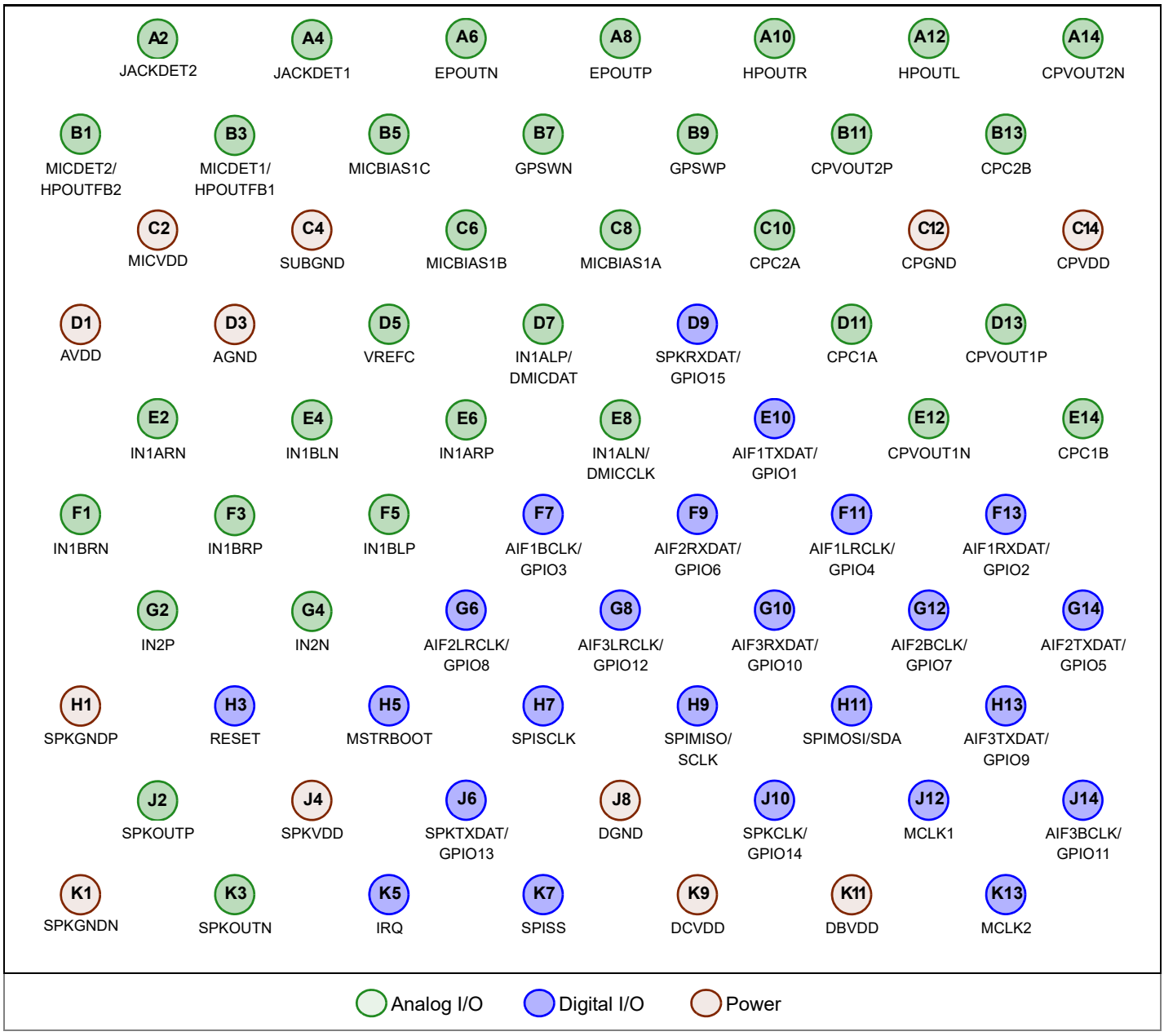


Figure 1-1. Top-Down (Through-Package) View—70-Ball WLCSP Package

1.2 Pin Descriptions

Table 1-1 describes each pin on the CS47L15. All digital output pins are CMOS outputs, unless otherwise stated.

Table 1-1. Pin Descriptions

PU = Pull-up, PD = Pull-down, K = Bus keeper, H = Hysteresis on CMOS input, Z = Hi-Z (High impedance), C = CMOS, OD = Open drain.

Pin Name	Pin #	Power Supply	I/O	Pin Description	Digital Pad Attributes	State at Reset [1]
				Analog I/O		
CPC1A	D11	—	O	Charge pump fly-back capacitor 1 pin	—	—
CPC1B	E14	—	O	Charge pump fly-back capacitor 1 pin	—	—
CPC2A	C10	—	O	Charge pump fly-back capacitor 2 pin	—	—
CPC2B	B13	—	O	Charge pump fly-back capacitor 2 pin	—	—
CPVOUT1N	E12	—	O	Charge pump negative output 1 decoupling pin	—	Output
CPVOUT1P	D13	—	O	Charge pump positive output 1 decoupling pin	—	Output
CPVOUT2N	A14	—	O	Charge pump negative output 2 decoupling pin	—	Output
CPVOUT2P	B11	—	O	Charge pump positive output 2 decoupling pin	—	Output
EPOUTN	A6	—	O	Earpiece negative output	—	Output
EPOUTP	A8	—	O	Earpiece positive output	—	Output
GPSWN	B7	—	I/O	General-purpose bidirectional switch contact	—	—
GPSWP	B9	—	I/O	General-purpose bidirectional switch contact	—	—
HPOUTL	A12	—	O	Left headphone output	—	Output
HPOUTR	A10	—	O	Right headphone output	—	Output
IN1ALN/ DMICCLK	E8	MICVDD or MICBIAS*nx* [2]	I/O	Left-channel negative differential mic/line input /DMIC clock output	PD/H	IN1ALN input
IN1ALP/ DMICDAT	D7	MICVDD or MICBIAS*nx* [2]	I	Left-channel single-ended mic/line input/left-channel positive differential mic/line input/DMIC data input	PD/H	IN1ALP input
IN1ARN	E2	MICVDD	I	Right-channel negative differential mic/line input	—	Input
IN1ARP	E6	MICVDD	I	Right-channel single-ended mic/line input/ right-channel positive differential mic/line input	—	Input
IN1BLN	E4	MICVDD	I	Left-channel negative differential mic/line input. Also suitable for connection to external accessory interfaces.	—	Input
IN1BLP	F5	MICVDD	I	Left-channel single-ended mic/line input/left-channel positive differential mic/line input. Also suitable for connection to external accessory interfaces.	—	Input
IN1BRN	F1	MICVDD	I	Right-channel negative differential mic/line input. Also suitable for connection to external accessory interfaces.	—	Input
IN1BRP	F3	MICVDD	I	Right-channel single-ended mic/line input/ right-channel positive differential mic/line input. Also suitable for connection to external accessory interfaces.	—	Input
IN2N	G4	MICVDD	I	Negative differential analog input	—	Input
IN2P	G2	MICVDD	I	Positive differential analog input	—	Input
JACKDET1	A4	AVDD	I	Jack detect input 1	—	Input
JACKDET2	A2	AVDD	I	Jack detect input 2	—	Input
MICBIAS1A	C8	—	O	Microphone bias 1A	—	Output
MICBIAS1B	C6	—	O	Microphone bias 1B	—	Output
MICBIAS1C	B5	—	O	Microphone bias 1C	—	Output
MICDET1/ HPOUTFB1	B3	—	I	Microphone and accessory sense input 1/HPOUTL and HPOUTR ground feedback pin 1	—	Input
MICDET2/ HPOUTFB2	B1	—	I	Microphone and accessory sense input 2/HPOUTL and HPOUTR ground feedback pin 2	—	Input

Table 1-1. Pin Descriptions *(Cont.)*

PU = Pull-up, PD = Pull-down, K = Bus keeper, H = Hysteresis on CMOS input, Z = Hi-Z (High impedance), C = CMOS, OD = Open drain.

Pin Name	Pin #	Power Supply	I/O	Pin Description	Digital Pad Attributes	State at Reset [1]
SPKOUTN	K3	—	O	Speaker negative output	—	Output
SPKOUTP	J2	—	O	Speaker positive output	—	Output
VREFC	D5	—	O	Band-gap reference external capacitor connection	—	Output
				Digital I/O		
AIF1BCLK/ GPIO3	F7	DBVDD	I/O	Audio interface 1 bit clock/GPIO	PU/PD/K/H/ Z/C/OD	GPIO3 input with bus-keeper
AIF1LRCLK/ GPIO4	F11	DBVDD	I/O	Audio interface 1 left/right clock/GPIO	PU/PD/K/H/ Z/C/OD	GPIO4 input with bus-keeper
AIF1RXDAT/ GPIO2	F13	DBVDD	I/O	Audio interface 1 RX digital audio data/GPIO	PU/PD/K/H/ C/OD	GPIO2 input with bus-keeper
AIF1TXDAT/ GPIO1	E10	DBVDD	I/O	Audio interface 1 TX digital audio data/GPIO	PU/PD/K/H/ Z/C/OD	GPIO1 input with bus-keeper
AIF2BCLK/ GPIO7	G12	DBVDD	I/O	Audio interface 2 bit clock/GPIO	PU/PD/K/H/ Z/C/OD	GPIO7 input with bus-keeper
AIF2LRCLK/ GPIO8	G6	DBVDD	I/O	Audio interface 2 left/right clock/GPIO	PU/PD/K/H/ Z/C/OD	GPIO8 input with bus-keeper
AIF2RXDAT/ GPIO6	F9	DBVDD	I/O	Audio interface 2 RX digital audio data/GPIO	PU/PD/K/H/ C/OD	GPIO6 input with bus-keeper
AIF2TXDAT/ GPIO5	G14	DBVDD	I/O	Audio interface 2 TX digital audio data/GPIO. If the JTAG interface is configured, this pin provides the TDI input connection.	PU/PD/K/H/ Z/C/OD	GPIO5 input with bus-keeper
AIF3BCLK/ GPIO11	J14	DBVDD	I/O	Audio interface 3 bit clock/GPIO. If the JTAG interface is configured, this pin provides the TCK input connection.	PU/PD/K/H/ Z/C/OD	GPIO11 input with bus-keeper
AIF3LRCLK/ GPIO12	G8	DBVDD	I/O	Audio interface 3 left/right clock/GPIO. If the JTAG interface is configured, this pin provides the TDO output connection.	PU/PD/K/H/ Z/C/OD	GPIO12 input with bus-keeper
AIF3RXDAT/ GPIO10	G10	DBVDD	I/O	Audio interface 3 RX digital audio data/GPIO. If the JTAG interface is configured, this pin provides the TMS input connection.	PU/PD/K/H/ C/OD	GPIO10 input with bus-keeper
AIF3TXDAT/ GPIO9	H13	DBVDD	I/O	Audio interface 3 TX digital audio data/GPIO. If the JTAG interface is configured, this pin provides the TRST input connection.	PU/PD/K/H/ Z/C/OD	GPIO9 input with bus-keeper
$\overline{\text{IRQ}}$	K5	DBVDD	O	Interrupt request output (default is active low). The pin configuration is selectable CMOS or open drain.	C/OD	Output
MCLK1	J12	DBVDD	I	Master clock 1	H	Input
MCLK2	K13	DBVDD	I	Master clock 2	H	Input
MSTRBOOT	H5	DBVDD	I	Master boot mode select	PD/H	Input
$\overline{\text{RESET}}$	H3	DBVDD	I	Digital reset input (active low)	PU/PD/K/H	Input with pull-up
SPIMISO/ SCLK	H9	DBVDD	I/O	Control interface (SPI) Master In Slave Out data/I²C clock input. SPIMISO is high impedance if $\overline{\text{SPISS}}$ is not asserted.	PD/H/C	Input
SPIMOSI/SDA	H11	DBVDD	I/O	Control interface (SPI) Master Out Slave In data/I²C data input and output.	H/C/OD	Input
SPISCLK	H7	DBVDD	I/O	Control interface (SPI) clock	H/C	Input
$\overline{\text{SPISS}}$	K7	DBVDD	I/O	Control interface (SPI) slave select (SS)	H/C	Input
SPKCLK/ GPIO14	J10	DBVDD	I/O	Digital speaker (PDM) clock output/GPIO/I²C clock input. GPIO output is selectable CMOS or open drain; SPKCLK output is CMOS.	PU/PD/K/H/ C/OD	GPIO14 input with bus-keeper
SPKRXDAT/ GPIO15	D9	DBVDD	I/O	Digital speaker (PDM) data input/GPIO. GPIO output is selectable CMOS or open drain.	PU/PD/K/H/ C/OD	GPIO15 input with bus-keeper

Table 1-1. Pin Descriptions *(Cont.)*

PU = Pull-up, PD = Pull-down, K = Bus keeper, H = Hysteresis on CMOS input, Z = Hi-Z (High impedance), C = CMOS, OD = Open drain.

Pin Name	Pin #	Power Supply	I/O	Pin Description	Digital Pad Attributes	State at Reset [1]
SPKTXDAT/ GPIO13	J6	DBVDD	I/O	Digital speaker (PDM) data output/GPIO/I²C data input and output. GPIO output is selectable CMOS or open drain; SPKTXDAT output is CMOS.	PU/PD/K/H/ C/OD	GPIO13 input with bus-keeper
				Supply		
AGND	D3	—	—	Analog ground (return path for AVDD and MICVDD)	—	—
AVDD	D1	—	—	Analog supply	—	—
CPGND	C12	—	—	Charge pump ground (return path for CPVDD)	—	—
CPVDD	C14	—	—	Supply for charge pump	—	—
DBVDD	K11	—	—	Digital buffer (I/O) supply	—	—
DCVDD	K9	—	—	Digital core supply	—	—
DGND	J8	—	—	Digital ground (return path for DCVDD and DBVDD)	—	—
MICVDD	C2	—	—	Microphone bias supply (input to MICBIAS regulator)	—	—
SPKGNDN	K1	—	—	Speaker driver ground (return path for SPKVDD) [3]	—	—
SPKGNDP	H1	—	—	Speaker driver ground (return path for SPKVDD) [3]	—	—
SPKVDD	J4	—	—	Speaker driver supply	—	—
SUBGND	C4	—	—	Substrate ground	—	—

1. Note that the default conditions described are not valid if modified by the boot sequence or by a wake-up control sequence.
2. The analog input functions on these pins are referenced to the MICVDD power domain. The digital input/output functions are referenced to the MICVDD or MICBIAS1 power domain, as selected by the IN1_DMIC_SUP field.
3. Separate P/N ground connections are provided for the Class D speaker output, which provides flexible support for current monitoring and output-protection circuits. If this option is not used, these ground connections should be tied together on the PCB.

2 Typical Connection Diagram

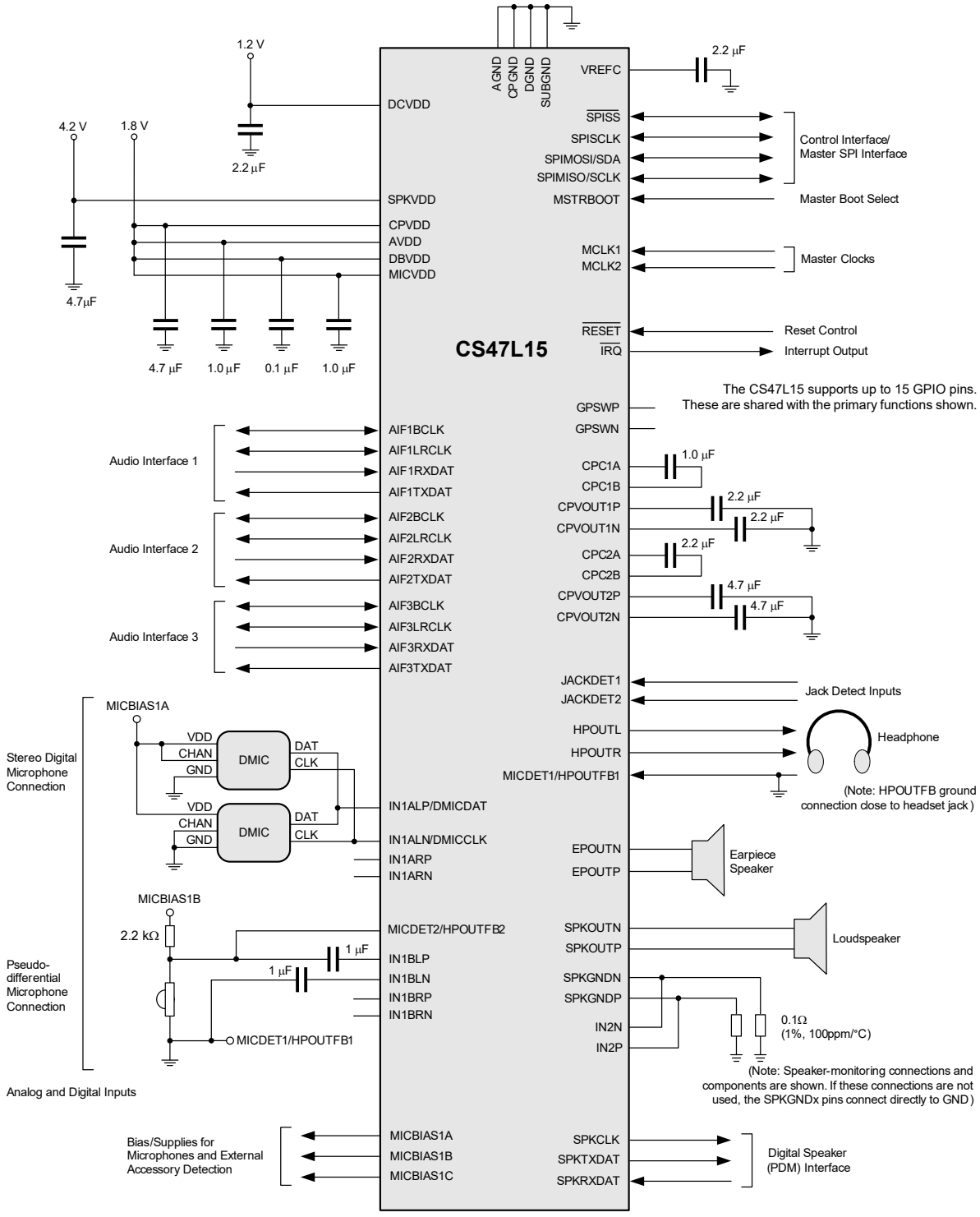


Figure 2-1. Typical Connection Diagram

3 Characteristics and Specifications

Table 3-1 defines parameters as they are characterized in this section.

Table 3-1. Parameter Definitions

Parameter	Definition
Channel separation	Left-to-right and right-to-left channel separation is the difference in level between the active channel (driven to maximum full scale output) and the measured signal level in the idle channel at the test signal frequency. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel.
Common-mode rejection ratio (CMRR)	The ratio of a specified input signal (applied to both sides of a differential input), relative to the output signal that results from it.
Dynamic range (DR)	A measure of the difference between the maximum full scale output signal and the sum of all harmonic distortion products plus noise, with a low-level input signal applied. Typically, an input signal level 60 dB below full scale is used.
Power-supply rejection ratio (PSRR)	The ratio of a specified power supply variation relative to the output signal that results from it. PSRR is measured under quiescent signal path conditions.
Signal-to-noise ratio (SNR)	A measure of the difference in level between the maximum full scale output signal and the output with no input signal applied.
Total harmonic distortion (THD)	The ratio of the RMS sum of the harmonic distortion products in the specified bandwidth [1] relative to the RMS amplitude of the fundamental (i.e., test frequency) output.
Total harmonic distortion plus noise (THD+N)	The ratio of the RMS sum of the harmonic distortion products plus noise in the specified bandwidth [1] relative to the RMS amplitude of the fundamental (i.e., test frequency) output.

1. All performance measurements are specified with a 20-kHz, low-pass brick-wall filter and, where noted, an A-weighted filter. The low-pass filter removes out-of-band noise.

Table 3-2. Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under electrical characteristics at the test conditions specified.

Parameter	Symbol	Minimum	Maximum
Supply voltages	DCVDD CPVDD DBVDD, AVDD, MICVDD SPKVDD	–0.3 V –0.3 V –0.3 V –0.3 V	1.6 V 2.5 V 5.0 V 6.0 V
Voltage range digital inputs	—	SUBGND – 0.3 V	DBVDD + 0.3 V
Voltage range analog inputs	IN1Axx, IN2xx IN1Bxx HPOUTFB*n* [1] MICDET*n* [1] JACKDET1 JACKDET2 [2], GPSWP, GPSWN	SUBGND – 0.3 V SUBGND – 0.9 V SUBGND – 0.3 V SUBGND – 0.3 V CPVOUT2N – 0.3 V [3] SUBGND – 0.3 V	MICVDD + 0.3 V MICVDD + 0.3 V SUBGND + 0.3 V MICVDD + 0.3 V AVDD + 0.3 V MICVDD + 0.3 V
Ground	AGND, DGND, CPGND, SPKGNDN, SPKGNDP	SUBGND – 0.3 V	SUBGND + 0.3 V
Operating temperature range	T_A	–40ºC	+85ºC
Operating junction temperature	T_J	–40ºC	+125ºC
Storage temperature after soldering	—	–65ºC	+150ºC

ESD-sensitive device. The CS47L15 is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device. This device is qualified to current JEDEC ESD standards.

1. The HPOUTFB*n* and MICDET*n* functions share common pins. The absolute maximum rating varies according to the applicable function of each pin.
2. If AVDD > MICVDD the maximum JACKDET2 voltage is AVDD + 0.3 V.
3. CPVOUT2N is an internal supply, generated by the CS47L15 charge pump (CP). Its voltage can vary between CPGND and –CPVDD.

Table 3-3. Recommended Operating Conditions

Parameter		Symbol	Minimum	Typical	Maximum	Units
Digital supply range [1,2]	Core and FLL	DCVDD [3]	1.14	1.2	1.26	V
	I/O	DBVDD	1.71	—	3.6	V
Charge pump supply range	CPVDD	CPVDD	1.71	1.8	1.89	V
Speaker supply range		SPKVDD	2.4	—	5.5	V
Analog supply range		AVDD	1.71	1.8	1.89	V
Mic bias supply		MICVDD	1.71	1.8	3.6	V
Ground [4]		DGND, AGND, CPGND, SPKGNDN, SPKGNDP, SUBGND	—	0	—	V
Power supply rise time [5,6]		DCVDD	100	—	2000	µs
		All other supplies	100	—	—	µs
Operating temperature range		T_A	–40	—	85	ºC

1. When powering-up the CS47L15, the DBVDD and AVDD supplies must be enabled before DCVDD. The DCVDD domain must not be powered if DBVDD or AVDD is not present. There are no power-down sequencing requirements; the supplies may be disabled in any order.
2. When powering-up the CS47L15, RESET must be deasserted (high) before DCVDD is applied. RESET must be held high until at least 10 ms after DCVDD is applied.
3. Sleep mode is supported for when DCVDD is below the limits noted, provided that AVDD and DBVDD are present.
4. The impedance between DGND, AGND, and SUBGND must not exceed 0.1 Ω.
   The impedance between SPKGNDN, SPKGNDP, and SUBGND must not exceed 0.2 Ω.
5. If the DCVDD rise time exceeds 2 ms, RESET must be asserted (low) during the rise and held asserted until after DCVDD is within the recommended operating limits. This requirement takes precedence over Note 2 above.
6. The specified minimum power supply rise times assume a minimum decoupling capacitance of 100 nF per pin. However, Cirrus Logic strongly advises that the recommended decoupling capacitors are present on the PCB and that appropriate layout guidelines are observed. The specified minimum power supply rise times also assume a maximum PCB inductance of 10 nH between decoupling capacitor and pin.

Table 3-4. Analog Input Signal Level—IN1Axx, IN1Bxx, IN2x

Test conditions (unless specified otherwise): AVDD = 1.8V, sinusoid input signal; with the exception of the conditions noted, the following electrical characteristics are valid across the full range of recommended operating conditions.

Parameter		Minimum	Typical	Maximum	Units
Maximum input signal level (IN1Axx, IN1Bxx) [1, 2]	Single-ended configuration, 0 dB PGA gain	—	0.5	—	V_{RMS}
		—	–6	—	dBV
	Differential configuration [3], 0 dB PGA gain	—	1	—	V_{RMS}
		—	0	—	dBV
Maximum input signal level (IN2x) [4]	Differential configuration	—	0.1	—	V_{RMS}
		—	–20	—	dBV

Note: The maximum and full-scale input signal levels change in proportion with AVDD.

1. The maximum input signal level (before clipping occurs) is also the full-scale input signal level (0 dBFS) at the IN1 ADC outputs.
2. If Low-Power Mode is enabled, the maximum input signal level is reduced by 6 dB. The maximum input signal level corresponds to –6 dBFS at the IN1 ADC output in this case.
3. A 1.0V_{RMS} differential signal equates to 0.5V_{RMS}/–6dBV per input.
4. The maximum input signal level (before clipping occurs) corresponds to –6 dBFS at the IN2 ADC output.

Table 3-5. Analog Input Pin Characteristics

Test conditions (unless specified otherwise): T_A = +25ºC; with the exception of the condition noted, the following electrical characteristics are valid across the full range of recommended operating conditions.

Parameter		Minimum	Typical	Maximum	Units
Input resistance (IN1x)	Single-ended PGA input, All PGA gain settings	9	10	—	kΩ
	Differential PGA input, All PGA gain settings	18	21	—	kΩ
Input resistance (IN2x)		—	17	—	kΩ
Input capacitance		—	—	5	pF

Table 3-6. Analog Input Gain—Programmable Gain Amplifiers (PGAs)

The following electrical characteristics are valid across the full range of recommended operating conditions.

Parameter[1]		Minimum	Typical	Maximum	Units
Minimum programmable gain		—	0	—	dB
Maximum programmable gain		—	31	—	dB
Programmable gain step size	Guaranteed monotonic	—	1	—	dB

1. Note that PGA control is provided for the IN1x analog input channels only.

Table 3-7. Digital Input Signal Level—DMICDAT, SPKRXDAT

The following electrical characteristics are valid across the full range of recommended operating conditions.

Parameter		Minimum	Typical	Max	Units
Full-scale input level [1]	0 dBFS digital core input, 0 dB gain	—	–6	—	dBFS

1. The digital input signal level is measured in dBFS, where 0 dBFS is a signal level equal to the full-scale range (FSR) of the PDM input. The FSR is defined as the amplitude of a 1-kHz sine wave whose positive and negative peaks are represented by the maximum and minimum digital codes respectively—this is the largest 1-kHz sine wave that can fit in the digital output range without clipping.

Table 3-8. Output Characteristics

The following electrical characteristics are valid across the full range of recommended operating conditions.

Parameter			Minimum	Typical	Max	Units
Line/headphone/earpiece output driver (HPOUTL, HPOUTR)	Load resistance	Normal operation, Single-Ended Mode	6	—	—	Ω
		Normal operation, Differential (BTL) Mode	15	—	—	Ω
		Device survival with load applied indefinitely	0	—	—	Ω
	Load capacitance	Single-Ended Mode	—	—	500	pF
		Differential (BTL) Mode	—	—	200	pF
Earpiece output driver (EPOUTP+EPOUTN)	Load resistance	Normal operation	15	—	—	Ω
		Device survival with load applied indefinitely	0	—	—	Ω
	Load capacitance		—	—	200	pF
Speaker output driver (SPKOUTP+SPKOUTN)	Load resistance	Normal operation	4	—	—	Ω
		Device survival with load applied indefinitely	0	—	—	Ω
	Load capacitance		—	—	200	pF
Digital speaker output (SPKTXDAT)	Full-scale output level [1]	0 dBFS digital core output, 0 dB gain	—	–6	—	dBFS

1. The digital output signal level is measured in dBFS, where 0 dBFS is a signal level equal to the full-scale range (FSR) of the PDM output. The FSR is defined as the amplitude of a 1-kHz sine wave whose positive and negative peaks are represented by the maximum and minimum digital codes respectively—this is the largest 1-kHz sine wave that can fit in the digital output range without clipping.

Table 3-9. Input/Output Path Characteristics

Test conditions (unless specified otherwise): DBVDD = CPVDD = AVDD = 1.8 V, DCVDD = 1.2 V; MICVDD = 2.5 V; SPKVDD = 4.2 V; T_A = +25ºC; 1 kHz sinusoid signal; Fs = 48 kHz; PGA gain = 0 dB, 24-bit audio data.

Parameter			Min	Typ	Max	Units
Line/headphone/earpiece output driver (HPOUTL, HPOUTR)	DC offset at Load	Single-ended mode	—	50	—	µV
		Differential (BTL) mode	—	75	—	µV
Earpiece output driver (EPOUTP+EPOUTN)	DC offset at Load		—	75	—	µV
Speaker output driver (SPKOUTP+SPKOUTN)	DC offset at Load		—	300	—	µV
	SPKVDD leakage current		—	1	—	µA
Analog input paths (IN1xL, IN1xR) to ADC (Differential Input Mode)	SNR (A-weighted), defined in Table 3-1	48 kHz sample rate	90	98	—	dB
		16 kHz sample rate (wideband voice)	—	104	—	dB
	THD, defined in Table 3-1	–1 dBV input	—	–87	—	dB
	THD+N, defined in Table 3-1	–1 dBV input	—	–88	–80	dB
	Channel separation (L/R), defined in Table 3-1	100 Hz to 10 kHz	—	109	—	dB
	Input-referred noise floor	A-weighted, PGA gain = +20 dB	—	2.7	—	μV_{RMS}
	CMRR, defined in Table 3-1	PGA gain = +30 dB	—	79	—	dB
		PGA gain = 0 dB	—	70	—	dB
	PSRR (DBVDD, CPVDD, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	93	—	dB
		100 mV (peak-peak) 10 kHz	—	77	—	dB
	PSRR (MICVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	98	—	dB
		100 mV (peak-peak) 10 kHz	—	90	—	dB
	PSRR (DCVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	98	—	dB
		100 mV (peak-peak) 10 kHz	—	83	—	dB
	PSRR (SPKVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	100	—	dB
		100 mV (peak-peak) 10 kHz	—	95	—	dB

Table 3-9. Input/Output Path Characteristics *(Cont.)*

Test conditions (unless specified otherwise): DBVDD = CPVDD = AVDD = 1.8 V, DCVDD = 1.2 V; MICVDD = 2.5 V; SPKVDD = 4.2 V; T_A = +25ºC; 1 kHz sinusoid signal; Fs = 48 kHz; PGA gain = 0 dB, 24-bit audio data.

Parameter			Min	Typ	Max	Units
Analog input paths (IN1xL, IN1xR) to ADC (Single-Ended Input Mode)	SNR (A-weighted), defined in Table 3-1	48-kHz sample rate	85	97	—	dB
		16-kHz sample rate (wideband voice)	—	102	—	dB
	THD, defined in Table 3-1	–7dBV input	—	–86	—	dB
	THD+N, defined in Table 3-1	–7dBV input	—	–85	–78	dB
	Channel separation (L/R), defined in Table 3-1	100 Hz to 10 kHz	—	107	—	dB
	Input-referred noise floor	A-weighted, PGA gain = +20 dB	—	4	—	μV_{RMS}
	PSRR (DBVDD, CPVDD, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	77	—	dB
		100 mV (peak-peak) 10 kHz	—	52	—	dB
	PSRR (MICVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	100	—	dB
		100 mV (peak-peak) 10 kHz	—	90	—	dB
	PSRR (DCVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	96	—	dB
		100 mV (peak-peak) 10 kHz	—	74	—	dB
	PSRR (SPKVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	100	—	dB
		100 mV (peak-peak) 10 kHz	—	80	—	dB
Analog input path (IN2) to ADC (Differential Input Mode)	SNR (A-weighted), defined in Table 3-1	48 kHz sample rate	—	70	—	dB
	THD, defined in Table 3-1	–21 dBV input	—	–65	—	dB
	THD+N, defined in Table 3-1	–21 dBV input	—	–63	—	dB
	Input-referred noise floor	A-weighted	—	28	—	μV_{RMS}
	CMRR, defined in Table 3-1		—	60	—	dB
			—	70	—	dB
	PSRR (DBVDD, CPVDD, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	50	—	dB
		100 mV (peak-peak) 10 kHz	—	50	—	dB
	PSRR (MICVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	71	—	dB
		100 mV (peak-peak) 10 kHz	—	83	—	dB
	PSRR (DCVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	50	—	dB
		100 mV (peak-peak) 10 kHz	—	50	—	dB
	PSRR (SPKVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	50	—	dB
		100 mV (peak-peak) 10 kHz	—	50	—	dB
DAC to line output (HPOUTL, HPOUTR; Load = 10 kΩ, 50 pF)	Full-scale output signal level	0 dBFS input	—	1	—	V_{RMS}
			—	0	—	dBV
	SNR, defined in Table 3-1	A-weighted, output signal = 1 V_{RMS}	—	127	—	dB
	Dynamic range, defined in Table 3-1	A-weighted, –60 dBFS input	105	114	—	dB
	THD, defined in Table 3-1	0 dBFS input	—	–94	—	dB
	THD+N, defined in Table 3-1	0 dBFS input	—	–92	–85	dB
	Channel separation (L/R), defined in Table 3-1	100 Hz to 10 kHz	—	105	—	dB
	Output noise floor	A-weighted	—	0.45	—	μV_{RMS}
	PSRR (DBVDD, CPVDD, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	124	—	dB
		100 mV (peak-peak) 10 kHz	—	80	—	dB
	PSRR (MICVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	110	—	dB
		100 mV (peak-peak) 10 kHz	—	105	—	dB
	PSRR (DCVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	126	—	dB
		100 mV (peak-peak) 10 kHz	—	90	—	dB
	PSRR (SPKVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	110	—	dB
		100 mV (peak-peak) 10 kHz	—	100	—	dB

Table 3-9. Input/Output Path Characteristics *(Cont.)*

Test conditions (unless specified otherwise): DBVDD = CPVDD = AVDD = 1.8 V, DCVDD = 1.2 V; MICVDD = 2.5 V; SPKVDD = 4.2 V; T_A = +25ºC; 1 kHz sinusoid signal; Fs = 48 kHz; PGA gain = 0 dB, 24-bit audio data.

Parameter			Min	Typ	Max	Units
DAC to headphone output (HPOUTL, HPOUTR; R_L = 32 Ω)	Maximum output power	0.1% THD+N	—	30	—	mW
	SNR, defined in Table 3-1	A-weighted, output signal = 1 V_{RMS}	—	127	—	dB
	Dynamic range, defined in Table 3-1	A-weighted, –60 dBFS input	105	115	—	dB
	THD, defined in Table 3-1	P_O = 25 mW	—	–94	—	dB
	THD+N, defined in Table 3-1	P_O = 25 mW	—	–92	—	dB
	THD, defined in Table 3-1	P_O = 20 mW	—	–92	—	dB
	THD+N, defined in Table 3-1	P_O = 20 mW	—	–90	–85	dB
	THD, defined in Table 3-1	P_O = 2 mW	—	–92	—	dB
	THD+N, defined in Table 3-1	P_O = 2 mW	—	–90	—	dB
	Channel separation (L/R), defined in Table 3-1	100 Hz to 10 kHz	—	102	—	dB
	Output noise floor	A-weighted	—	0.45	—	μV_{RMS}
	PSRR (DBVDD, CPVDD, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	124 80	— —	dB dB
	PSRR (MICVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	124 110	— —	dB dB
	PSRR (DCVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	126 90	— —	dB dB
	PSRR (SPKVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	110 100	— —	dB dB
DAC to headphone output (HPOUTL, HPOUTR; R_L = 16 Ω)	Maximum output power	0.1% THD+N	—	40	—	mW
	SNR, defined in Table 3-1	A-weighted, output signal = 1 V_{RMS}	—	127	—	dB
	Dynamic range, defined in Table 3-1	A-weighted, –60 dBFS input	105	114	—	dB
	THD, defined in Table 3-1	P_O = 25 mW	—	–90	—	dB
	THD+N, defined in Table 3-1	P_O = 25 mW	—	–88	—	dB
	THD, defined in Table 3-1	P_O = 20 mW	—	–90	—	dB
	THD+N, defined in Table 3-1	P_O = 20 mW	—	–88	–80	dB
	THD, defined in Table 3-1	P_O = 2 mW	—	–88	—	dB
	THD+N, defined in Table 3-1	P_O = 2 mW	—	–86	—	dB
	Channel separation (L/R), defined in Table 3-1	100 Hz to 10 kHz	—	100	—	dB
	Output noise floor	A-weighted	—	0.45	—	μV_{RMS}
	PSRR (DBVDD, CPVDD, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	124 80	— —	dB dB
	PSRR (MICVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	124 110	— —	dB dB
	PSRR (DCVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	126 90	— —	dB dB
	PSRR (SPKVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	110 100	— —	dB dB
DAC to earpiece output (EPOUTP+EPOUTN, R_L = 32 Ω BTL)	Maximum output power	0.1% THD+N	—	96	—	mW
	SNR, defined in Table 3-1	A-weighted, output signal = 1.41 V_{RMS}	—	128	—	dB
	Dynamic range, defined in Table 3-1	A-weighted, –60 dBFS input	105	118	—	dB
	THD, defined in Table 3-1	P_O = 75 mW	—	–92	—	dB
	THD+N, defined in Table 3-1	P_O = 75 mW	—	–88	—	dB
	THD, defined in Table 3-1	P_O = 5 mW	—	–88	—	dB
	THD+N, defined in Table 3-1	P_O = 5 mW	—	–86	—	dB
	Output noise floor	A-weighted	—	0.60	—	μV_{RMS}
	PSRR (DBVDD, CPVDD, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	85 85	— —	dB dB
	PSRR (MICVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	124 110	— —	dB dB
	PSRR (DCVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	126 86	— —	dB dB
	PSRR (SPKVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	110 105	— —	dB dB

Table 3-9. Input/Output Path Characteristics *(Cont.)*

Test conditions (unless specified otherwise): DBVDD = CPVDD = AVDD = 1.8 V, DCVDD = 1.2 V; MICVDD = 2.5 V; SPKVDD = 4.2 V; T_A = +25ºC; 1 kHz sinusoid signal; Fs = 48 kHz; PGA gain = 0 dB, 24-bit audio data.

Parameter			Min	Typ	Max	Units
DAC to earpiece output (EPOUTP+EPOUTN, R_L = 16 Ω BTL)	Maximum output power	0.1% THD+N	—	108	—	mW
	SNR, defined in Table 3-1	A-weighted, output signal = 1.41 V_{RMS}	—	128	—	dB
	Dynamic range, defined in Table 3-1	A-weighted, –60 dBFS input	105	118	—	dB
	THD, defined in Table 3-1	P_O = 75 mW	—	–89	—	dB
	THD+N, defined in Table 3-1	P_O = 75 mW	—	–87	—	dB
	THD, defined in Table 3-1	P_O = 5 mW	—	–90	—	dB
	THD+N, defined in Table 3-1	P_O = 5 mW	—	–88	—	dB
	Output noise floor	A-weighted	—	0.60	—	μV_{RMS}
	PSRR (DBVDD, CPVDD, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	85 85	— —	dB dB
	PSRR (MICVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	124 110	— —	dB dB
	PSRR (DCVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	126 86	— —	dB dB
	PSRR (SPKVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	108 110	— —	dB dB
DAC to speaker output (SPKOUTP+SPKOUTN, Load = 8 Ω, 22 μH, BTL)	Maximum output power	SPKVDD = 5.0 V, 1% THD+N SPKVDD = 4.2 V, 1% THD+N SPKVDD = 3.6 V, 1% THD+N	— — —	1.4 1.0 0.7	— — —	W W W
	SNR, defined in Table 3-1	A-weighted, output signal = 2.83 V_{RMS}	—	127	—	dB
	Dynamic range, defined in Table 3-1	A-weighted, –60 dBFS input	90	100	—	dB
	THD, defined in Table 3-1	P_O = 1.0 W	—	–40	—	dB
	THD+N, defined in Table 3-1	P_O = 1.0 W	—	–40	—	dB
	THD, defined in Table 3-1	P_O = 0.5 W	—	–61	—	dB
	THD+N, defined in Table 3-1	P_O = 0.5 W	—	–60	–50	dB
	Output noise floor	A-weighted	—	1.3	—	μV_{RMS}
	PSRR (DBVDD, CPVDD, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	110 90	— —	dB dB
	PSRR (MICVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	124 110	— —	dB dB
	PSRR (DCVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	125 105	— —	dB dB
	PSRR (SPKVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	125 105	— —	dB dB
DAC to speaker output (SPKOUTP+SPKOUTN, Load = 4 Ω, 15 μH, BTL)	Maximum output power	SPKVDD = 5.0 V, 1% THD+N SPKVDD = 4.2 V, 1% THD+N SPKVDD = 3.6 V, 1% THD+N	— — —	2.5 1.8 1.3	— — —	W W W
	SNR, defined in Table 3-1	A-weighted, output signal = 2.83 V_{RMS}	—	127	—	dB
	Dynamic range, defined in Table 3-1	A-weighted, –60 dBFS input	—	100	—	dB
	THD, defined in Table 3-1	P_O = 1.0 W	—	–40	—	dB
	THD+N, defined in Table 3-1	P_O = 1.0 W	—	–40	—	dB
	THD, defined in Table 3-1	P_O = 0.5 W	—	–61	—	dB
	THD+N, defined in Table 3-1	P_O = 0.5 W	—	–60	—	dB
	Output noise floor	A-weighted	—	1.3	—	μV_{RMS}
	PSRR (DBVDD, CPVDD, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	110 90	— —	dB dB
	PSRR (MICVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	124 110	— —	dB dB
	PSRR (DCVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	125 105	— —	dB dB
	PSRR (SPKVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	125 105	— —	dB dB

Table 3-10. Digital Input/Output

The following electrical characteristics are valid across the full range of recommended operating conditions.

Parameter			Minimum	Typical	Maximum	Units
Digital I/O (except DMICDAT and DMICCLK) [1,3]	Input HIGH level	V_{DBVDD} = 1.71–1.98 V	0.75 × DBVDD	—	—	V
		V_{DBVDD} = 2.5 V ±10%	0.8 × DBVDD	—	—	V
		V_{DBVDD} = 3.3 V ±10%	0.7 × DBVDD	—	—	V
	Input LOW level	V_{DBVDD} = 1.71–1.98 V	—	—	0.3 × DBVDD	V
		V_{DBVDD} = 2.5 V ±10%	—	—	0.25 × DBVDD	V
		V_{DBVDD} = 3.3 V ±10%	—	—	0.2 × DBVDD	V
	Output HIGH level (I_{OH} = 1 mA)	V_{DBVDD} = 1.71–1.98 V	0.75 × DBVDD	—	—	V
		V_{DBVDD} = 2.5 V ±10%	0.65 × DBVDD	—	—	V
		V_{DBVDD} = 3.3 V ±10%	0.7 × DBVDD	—	—	V
	Output LOW level (I_{OL} = 1mA)	V_{DBVDD} = 1.71–1.98 V	—	—	0.25 × DBVDD	V
		V_{DBVDD} = 2.5 V ±10%	—	—	0.3 × DBVDD	V
		V_{DBVDD} = 3.3 V ±10%	—	—	0.15 × DBVDD	V
	Input capacitance		—	—	5	pF
	Input leakage		–1	—	1	µA
	Pull-up/pull-down resistance (where applicable)	RESET pin	35	—	55	kΩ
		All other pins	25	—	50	kΩ
DMIC I/O (DMICDAT and DMICCLK) [2,3]	DMICDAT input HIGH Level		0.65 × V_{SUP}	—	—	V
	DMICDAT input LOW Level		—	—	0.35 × V_{SUP}	V
	DMICCLK output HIGH Level	I_{OH} = 1 mA	0.8 × V_{SUP}	—	—	V
	DMICCLK output LOW Level	I_{OL} = –1 mA	—		0.2 × V_{SUP}	V
	Input capacitance		—	25		pF
	Input leakage		–1	—	1	µA
GPIO*n*	Clock output frequency	GPIO pin as OPCLK or FLL output	—	—	50	MHz

1. Digital I/O is referenced to DBVDD.
2. DMICDAT and DMICCLK are referenced to a selectable supply, V_{SUP}, according to the IN1_DMIC_SUP field.
3. Note that digital input pins should not be left unconnected or floating.

Table 3-11. Miscellaneous Characteristics

Test conditions (unless specified otherwise): DBVDD = CPVDD = AVDD = 1.8 V, DCVDD = 1.2 V; MICVDD = 2.5 V; SPKVDD = 4.2 V; T_A = +25ºC; 1 kHz sinusoid signal; Fs = 48 kHz; PGA gain = 0 dB, 24-bit audio data.

Parameter			Min	Typ	Max	Units
Microphone bias (MICBIAS1A, MICBIAS1B, MICBIAS1C) [1]	Minimum Bias Voltage [2]		—	1.5	—	V
	Maximum Bias Voltage		—	2.8	—	V
	Bias Voltage output step size		—	0.1	—	V
	Bias Voltage accuracy		–5%	—	+5%	V
	Bias Current [3]	Regulator Mode (MICB1_BYPASS = 0), $V_{MICVDD} - V_{MICBIAS}$ >200 mV	—	—	2.4	mA
		Bypass Mode (MICBn_BYPASS = 1)	—	—	5.0	mA
	Output Noise Density	Regulator Mode (MICB1_BYPASS = 0), MICB1_LVL = 0x4, Load current = 1 mA, Measured at 1 kHz	—	50	—	nV/√Hz
	Integrated noise voltage	Regulator Mode (MICB1_BYPASS = 0), MICB1_LVL = 0x4, Load current = 1 mA, 100 Hz to 7 kHz, A-weighted	—	5	—	μV_{RMS}
	PSRR (DBVDD, CPVDD, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	100	—	dB
		100 mV (peak-peak) 10 kHz	—	80	—	dB
	PSRR (MICVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	82	—	dB
		100 mV (peak-peak) 10 kHz	—	44	—	dB
	PSRR (DCVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	100	—	dB
		100 mV (peak-peak) 10 kHz	—	80	—	dB
	PSRR (SPKVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	100	—	dB
		100 mV (peak-peak) 10 kHz	—	80	—	dB
	Load capacitance [3]	Regulator Mode (MICB1_BYPASS = 0), MICB1_EXT_CAP = 0	—	—	50	pF
		Regulator Mode (MICB1_BYPASS = 0), MICB1_EXT_CAP = 1	0.1	1.0	10	µF
	Output discharge resistance	MICB*nx*_ENA = 0, MICB*nx*_DISCH = 1	—	2	—	kΩ
General-purpose switch [4]	Switch resistance	Switch closed, I = 1 mA	—	25	40	Ω
		Switch open	—	100	—	MΩ
External Accessory Detect	Headphone detection load impedance range: Detection via HPOUTL (HPD_SENSE_SEL = 100) or HPOUTR (HPD_SENSE_SEL = 101)	HPD_IMPEDANCE_RANGE = 01	0	—	90	Ω
		HPD_IMPEDANCE_RANGE = 10	90	—	1000	Ω
		HPD_IMPEDANCE_RANGE = 11	1	—	10	kΩ
	Headphone detection load impedance range: Detection via MICDET*n* or JACKDET*n* pins		400	—	6000	Ω
	Headphone detection accuracy: (HPD_DACVAL, HPD_SENSE_SEL = 100 or 101)	HPD_IMPEDANCE_RANGE = 01	–10	—	+10	%
		HPD_IMPEDANCE_RANGE = 10	–5	—	+5	%
		HPD_IMPEDANCE_RANGE = 11	–10	—	+10	%
	Headphone detection accuracy (HPD_LVL, HPD_SENSE_SEL = 0XX or 11X)		–20	—	+20	%
	Microphone impedance detection range: (MICD1_ADC_MODE = 0, 2.2 kΩ ±2% MICBIAS resistor. [5]	for MICD1_LVL[0] = 1	0	—	70	Ω
		for MICD1_LVL[1] = 1	110	—	180	Ω
		for MICD1_LVL[2] = 1	210	—	290	Ω
		for MICD1_LVL[3] = 1	360	—	680	Ω
		for MICD1_LVL[8] = 1	1	—	30	kΩ
	Jack-detection input threshold voltage (JACKDET*n*)	Detection on JACKDET1, Jack insertion	—	0.9	—	V
		Detection on JACKDET1, Jack removal	—	1.65	—	V
		Detection on JACKDET2, Jack insertion	—	0.27	—	V
		Detection on JACKDET2, Jack removal	—	0.9	—	V
	Pull-up resistance (JACKDET*n*)		—	1	—	MΩ
Frequency-Locked Loop (FLL1)	Output frequency	FLL output as SYSCLK source	90	—	98.3	MHz
		FLL output as DSPCLK source	135	—	150	MHz
	Lock Time	F_{REF} = 32 kHz, F_{OUT} (DSPCLK source) = 147.456 MHz	—	10	—	ms
		F_{REF} = 12 MHz, F_{OUT} (DSPCLK source) = 147.456 MHz	—	1	—	ms
$\overline{\text{RESET}}$ pin input	$\overline{\text{RESET}}$ input pulse width [6]		1	—	—	µs

1. No capacitor on MICBIAS1x. In Regulator Mode, it is required that $V_{MICVDD} - V_{MICBIAS}$ > 200 mV.
2. Regulator Mode (MICB1_BYPASS = 0), Load current ≤ 1.0 mA.
3. Bias current and load capacitance specifications are for the sum of all enabled MICBIAS1*x* outputs.
4. The GPSWN pin voltage must not exceed GPSWP + 0.3 V. See Table 3-2 for voltage limits applicable to the GPSWP and GPSWN pins.
5. These characteristics assume no other component is connected to MICDET*n*.
6. To trigger a hardware reset, the $\overline{\text{RESET}}$ input must be asserted for longer than this duration.

Table 3-12. Device Reset Thresholds

The following electrical characteristics are valid across the full range of recommended operating conditions.

Parameter		Symbol	Minimum	Typical	Maximum	Units
AVDD reset threshold	V_{AVDD} rising	V_{AVDD}	—	—	1.66	V
	V_{AVDD} falling		1.06	—	1.44	V
DCVDD reset threshold	V_{DCVDD} rising	V_{DCVDD}	—	—	1.04	V
	V_{DCVDD} falling		0.40	—	0.72	V
DBVDD reset threshold	V_{DBVDD} rising	V_{DBVDD}	—	—	1.66	V
	V_{DBVDD} falling		1.06	—	1.44	V

Note: The reset thresholds are derived from simulations only, across all operational and process corners. Device performance is not assured outside the voltage ranges defined in Table 3-3.

Table 3-13. System Clock and Frequency-Locked Loop (FLL)

The following timing information is valid across the full range of recommended operating conditions.

Parameter			Minimum	Typical	Maximum	Units
Master clock timing (MCLK1, MCLK2) [1]	MCLK cycle time	MCLK as input to FLL, FLL1_REFCLK_DIV = 00	74	—	—	ns
		MCLK as input to FLL, FLL1_REFCLK_DIV = 01	37	—	—	ns
		MCLK as input to FLL, FLL1_REFCLK_DIV = 10	18	—	—	ns
		MCLK as input to FLL, FLL1_REFCLK_DIV = 11	12.5	—	—	ns
		MCLK as direct SYSCLK source	40	—	—	ns
	MCLK duty cycle	MCLK as input to FLL	80:20	—	20:80	%
		MCLK as direct SYSCLK source	60:40	—	40:60	%
Frequency-locked loop (FLL1)	FLL input frequency	FLL1_REFCLK_DIV = 00	0.032	—	13.5	MHz
		FLL1_REFCLK_DIV = 01	0.064	—	27	MHz
		FLL1_REFCLK_DIV = 11	0.128	—	54	MHz
		FLL1_REFCLK_DIV = 11	0.256	—	80	MHz
	FLL synchronizer input frequency	FLL1_SYNCCLK_DIV = 00	0.032	—	13.5	MHz
		FLL1_SYNCCLK_DIV = 01	0.064	—	27	MHz
		FLL1_SYNCCLK_DIV = 10	0.128	—	54	MHz
		FLL1_SYNCCLK_DIV = 11	0.256	—	80	MHz
Internal clocking	SYSCLK frequency	SYSCLK_FREQ = 000, SYSCLK_FRAC = 0	–1%	6.144	+1%	MHz
		SYSCLK_FREQ = 000, SYSCLK_FRAC = 1	–1%	5.6448	+1%	MHz
		SYSCLK_FREQ = 001, SYSCLK_FRAC = 0	–1%	12.288	+1%	MHz
		SYSCLK_FREQ = 001, SYSCLK_FRAC = 1	–1%	11.2896	+1%	MHz
		SYSCLK_FREQ = 010, SYSCLK_FRAC = 0	–1%	24.576	+1%	MHz
		SYSCLK_FREQ = 010, SYSCLK_FRAC = 1	–1%	22.5792	+1%	MHz
		SYSCLK_FREQ = 011, SYSCLK_FRAC = 0	–1%	49.152	+1%	MHz
		SYSCLK_FREQ = 011, SYSCLK_FRAC = 1	–1%	45.1584	+1%	MHz
		SYSCLK_FREQ = 100, SYSCLK_FRAC = 0	–1%	98.304	+1%	MHz
		SYSCLK_FREQ = 100, SYSCLK_FRAC = 1	–1%	90.3168	+1%	MHz
	DSPCLK frequency		5	—	150	MHz

1. If MCLK1 or MCLK2 is selected as a source for SYSCLK (either directly or via the FLL), the frequency must be within 1% of the SYSCLK_FREQ setting.

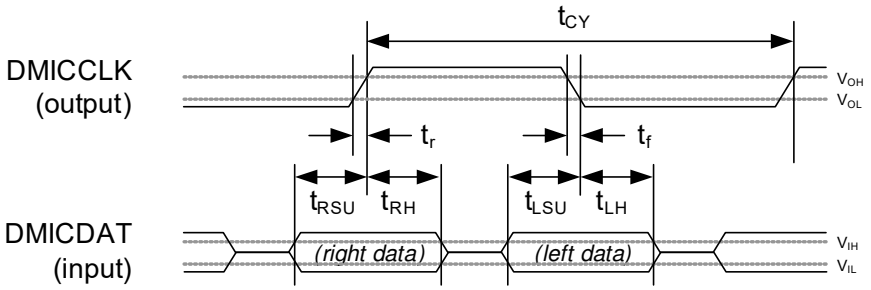
Table 3-14. Digital Microphone (DMIC) Interface Timing

The following timing information is valid across the full range of recommended operating conditions.

Parameter [1,2]	Symbol	Minimum	Typical	Maximum	Units
DMICCLK cycle time	t_{CY}	160	163	1432	ns
DMICCLK duty cycle	—	45	—	55	%
DMICCLK rise/fall time (25-pF load, 1.8-V supply)	t_r, t_f	5	—	30	ns
DMICDAT (Left) setup time to falling DMICCLK edge	t_{LSU}	15	—	—	ns
DMICDAT (Left) hold time from falling DMICCLK edge	t_{LH}	0	—	—	ns
DMICDAT (Right) setup time to rising DMICCLK edge	t_{RSU}	15	—	—	ns
DMICDAT (Right) hold time from rising DMICCLK edge	t_{RH}	0	—	—	ns

Note: The voltage reference for the IN1 interface is selectable, using the IN1_DMIC_SUP field—the interface is referenced to MICVDD or MICBIAS1.

1. DMIC interface timing



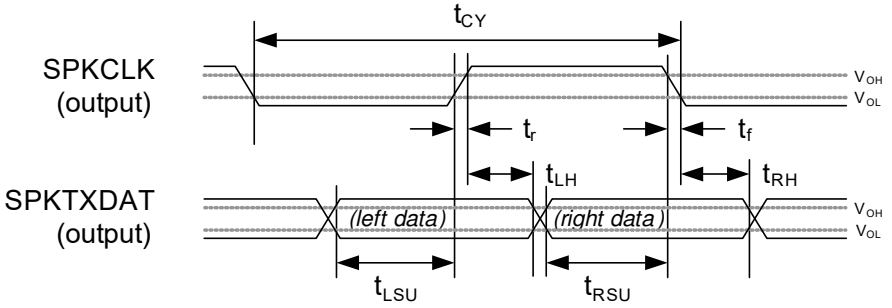
2. If the SPKRXDAT pin is configured for digital input, the SPKRXDAT timing requirements (with respect to SPKCLK) are the same as the DMICDAT timing requirements (with respect to DMICCLK).

Table 3-15. Digital Speaker (PDM) Interface Timing

The following timing information is valid across the full range of recommended operating conditions.

Parameter		Symbol	Minimum	Typical	Maximum	Units
Mode A [1]	SPKCLK cycle time	t_{CY}	160	163	358	ns
	SPKCLK duty cycle	—	45	—	55	%
	SPKCLK rise/fall time (25-pF load)	t_r, t_f	2	—	8	ns
	SPKTXDAT set-up time to SPKCLK rising edge (left channel)	t_{LSU}	30	—	—	ns
	SPKTXDAT hold time from SPKCLK rising edge (left channel)	t_{LH}	30	—	—	ns
	SPKTXDAT set-up time to SPKCLK falling edge (right channel)	t_{RSU}	30	—	—	ns
	SPKTXDAT hold time from SPKCLK falling edge (right channel)	t_{RH}	30	—	—	ns
Mode B [2]	SPKCLK cycle time	t_{CY}	160	163	358	ns
	SPKCLK duty cycle	—	45	—	55	%
	SPKCLK rise/fall time (25-pF load)	t_r, t_f	2	—	8	ns
	SPKTXDAT enable from SPKCLK rising edge (right channel)	t_{REN}	—	—	15	ns
	SPKTXDAT disable to SPKCLK falling edge (right channel)	t_{RDIS}	—	—	5	ns
	SPKTXDAT enable from SPKCLK falling edge (left channel)	t_{LEN}	—	—	15	ns
	SPKTXDAT disable to SPKCLK rising edge (left channel)	t_{LDIS}	—	—	5	ns

1. Digital speaker (PDM) interface timing—Mode A



2. Digital speaker (PDM) interface timing—Mode B

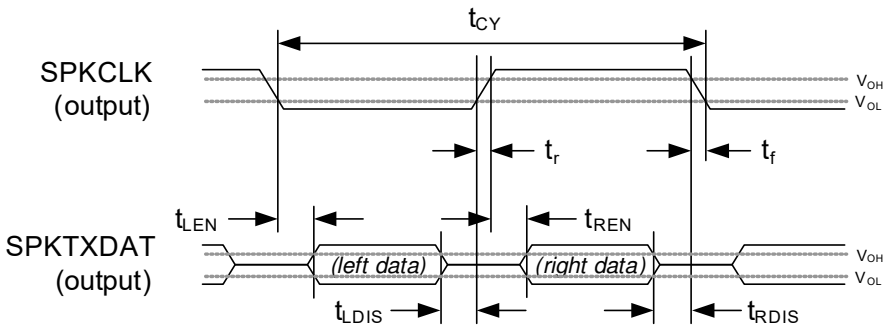


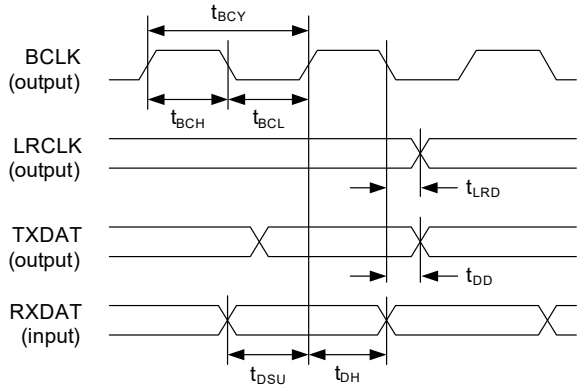
Table 3-16. Digital Audio Interface—Master Mode

Test conditions (unless specified otherwise): C_{LOAD} = 25 pF (output pins); BCLK slew (10% to 90%) = 3.7–5.6 ns; with the exception of the conditions noted, the following electrical characteristics are valid across the full range of recommended operating conditions.

Parameter [1]		Symbol	Minimum	Typical	Maximum	Units
Master Mode	AIF*n*BCLK cycle time	t_{BCY}	40	—	—	ns
	AIF*n*BCLK pulse width high	t_{BCH}	18	—	—	ns
	AIF*n*BCLK pulse width low	t_{BCL}	18	—	—	ns
	AIF*n*LRCLK propagation delay from BCLK falling edge [2]	t_{LRD}	0	—	8.3	ns
	AIF*n*TXDAT propagation delay from BCLK falling edge	t_{DD}	0	—	5	ns
	AIF*n*RXDAT setup time to BCLK rising edge	t_{DSU}	11	—	—	ns
	AIF*n*RXDAT hold time from BCLK rising edge	t_{DH}	0	—	—	ns
Master Mode, Slave LRCLK	AIF*n*LRCLK setup time to BCLK rising edge	t_{LRSU}	14	—	—	ns
	AIF*n*LRCLK hold time from BCLK rising edge	t_{LRH}	0	—	—	ns

Note: The descriptions above assume noninverted polarity of AIF*n*BCLK.

1. Digital audio interface timing—Master Mode. Note that BCLK and LRCLK outputs can be inverted if required; the figure shows the default, noninverted polarity.



2. The timing of the AIF*n*LRCLK signal is selectable. If the LRCLK advance option is enabled, the LRCLK transition is timed relative to the preceding BCLK edge. Under the required condition that BCLK is inverted in this case, the LRCLK transition is still timed relative to the falling BCLK edge.

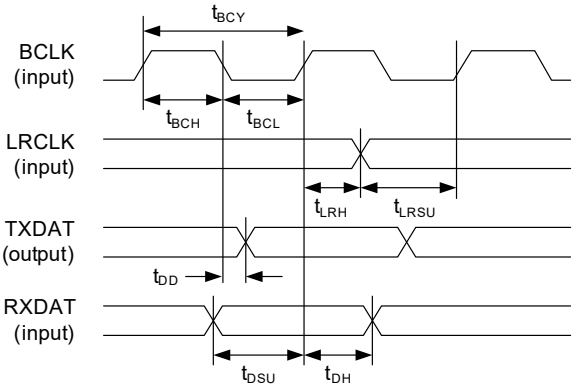
Table 3-17. Digital Audio Interface—Slave Mode

The following timing information is valid across the full range of recommended operating conditions, unless otherwise noted.

Parameter [1,2]		Symbol	Min	Typ	Max	Units
AIF*n*BCLK cycle time		t_{BCY}	40	—	—	ns
AIF*n*BCLK pulse width high	BCLK as direct SYSCLK source	t_{BCH}	16	—	—	ns
	All other conditions	t_{BCH}	14	—	—	ns
AIF*n*BCLK pulse width low	BCLK as direct SYSCLK source	t_{BCL}	16	—	—	ns
	All other conditions	t_{BCL}	14	—	—	ns
C_{LOAD} = 15 pF (output pins), BCLK slew (10%–90%) = 3 ns	AIF*n*LRCLK set-up time to BCLK rising edge	t_{LRSU}	7	—	—	ns
	AIF*n*LRCLK hold time from BCLK rising edge	t_{LRH}	0	—	—	ns
	AIF*n*TXDAT propagation delay from BCLK falling edge	t_{DD}	0	—	12.2	ns
	AIF*n*RXDAT set-up time to BCLK rising edge	t_{DSU}	2	—		ns
	AIF*n*RXDAT hold time from BCLK rising edge	t_{DH}	0	—		ns
	Master LRCLK, AIF*n*LRCLK propagation delay from BCLK falling edge	t_{LRD}	—	—	14.8	ns
C_{LOAD} = 25 pF (output pins), BCLK slew (10%–90%) = 6 ns	AIF*n*LRCLK set-up time to BCLK rising edge	t_{LRSU}	7	—		ns
	AIF*n*LRCLK hold time from BCLK rising edge	t_{LRH}	0	—		ns
	AIF*n*TXDAT propagation delay from BCLK falling edge	t_{DD}	0	—	14.2	ns
	AIF*n*RXDAT set-up time to BCLK rising edge	t_{DSU}	2	—		ns
	AIF*n*RXDAT hold time from BCLK rising edge	t_{DH}	0	—		ns
	Master LRCLK, AIF*n*LRCLK propagation delay from BCLK falling edge	t_{LRD}	—	—	15.9	ns

Note: The descriptions above assume noninverted polarity of AIF*n*BCLK.

1. Digital audio interface timing—Slave Mode. Note that BCLK and LRCLK inputs can be inverted if required; the figure shows the default, noninverted polarity.



2. If AIF*n*BCLK or AIF*n*LRCLK is selected as a source for SYSCLK (either directly or via the FLL), the frequency must be within 1% of the SYSCLK_FREQ setting.

Table 3-18. Digital Audio Interface Timing—TDM Mode

The following timing information is valid across the full range of recommended operating conditions, unless otherwise noted.

Parameter [1]		Min	Typ	Max	Units
Master Mode—C_{LOAD} (AIF*n*TXDAT) = 15 to 25 pF. BCLK slew (10%–90%) = 3.7ns to 5.6 ns.	AIF*n*TXDAT enable time from BCLK falling edge	0	—	—	ns
	AIF*n*TXDAT disable time from BCLK falling edge	—	—	6	ns
Slave Mode—C_{LOAD} (AIF*n*TXDAT) = 15 pF). BCLK slew (10%–90%) = 3 ns	AIF*n*TXDAT enable time from BCLK falling edge	2	—	—	ns
	AIF*n*TXDAT disable time from BCLK falling edge	—	—	12.2	ns
Slave Mode—C_{LOAD} (AIF*n*TXDAT) = 25 pF). BCLK slew (10%–90%) = 6 ns	AIF*n*TXDAT enable time from BCLK falling edge	2	—	—	ns
	AIF*n*TXDAT disable time from BCLK falling edge	—	—	14.2	ns

Note: If TDM operation is used on the AIF*n*TXDAT pins, it is important that two devices do not attempt to drive the AIF*n*TXDAT pin simultaneously. To support this requirement, the AIF*n*TXDAT pins can be configured to be tristated when not outputting data.

1. Digital audio interface timing—TDM Mode. The timing of the AIF*n*TXDAT tristating at the start and end of the data transmission is shown.

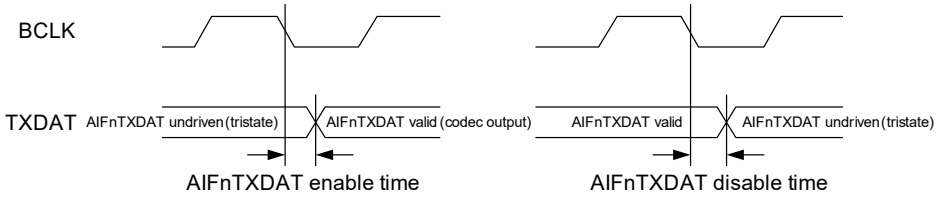


Table 3-19. Control Interface Timing—Two-Wire (I²C) Mode

The following timing information is valid across the full range of recommended operating conditions.

Parameter [1]		Symbol	Min	Typ	Max	Units
SCLK Frequency		—	—	—	3400	kHz
SCLK Low Pulse-Width		t_1	160	—	—	ns
SCLK High Pulse-Width		t_2	100	—	—	ns
Hold Time (Start Condition)		t_3	160	—	—	ns
Setup Time (Start Condition)		t_4	160	—	—	ns
SDA, SCLK Rise Time (10%–90%)	SCLK frequency > 1.7MHz	t_6	—	—	80	ns
	SCLK frequency > 1MHz	t_6	—	—	160	ns
	SCLK frequency ≤ 1MHz	t_6	—	—	2000	ns
SDA, SCLK Fall Time (90%–10%)	SCLK frequency > 1.7MHz	t_7	—	—	60	ns
	SCLK frequency > 1MHz	t_7	—	—	160	ns
	SCLK frequency ≤ 1MHz	t_7	—	—	200	ns
Setup Time (Stop Condition)		t_8	160	—	—	ns
SDA Setup Time (data input)		t_5	40	—	—	ns
SDA Hold Time (data input)		t_9	0	—	—	ns
SDA Valid Time (data/ACK output)	SCLK slew (90%–10%) = 20ns, C_{LOAD} (SDA) = 15 pF	t_{10}	—	—	40	ns
	SCLK slew (90%–10%) = 60ns, C_{LOAD} (SDA) = 100 pF	t_{10}	—	—	130	ns
	SCLK slew (90%–10%) = 160ns, C_{LOAD} (SDA) = 400 pF	t_{10}	—	—	190	ns
	SCLK slew (90%–10%) = 200ns, C_{LOAD} (SDA) = 550 pF	t_{10}	—	—	220	ns
Pulse width of spikes that are suppressed		t_{ps}	0	—	25	ns

1. Control interface timing—I²C Mode

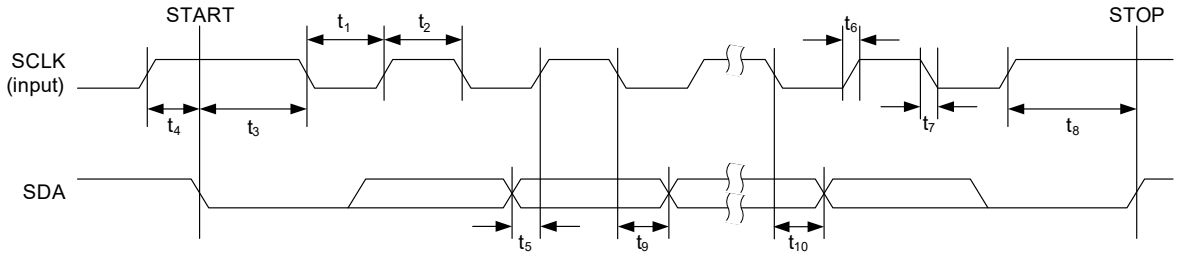
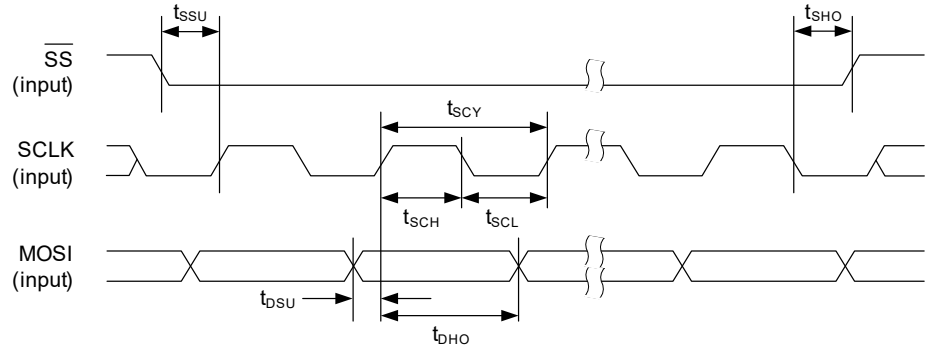


Table 3-20. Control Interface Timing—Four-Wire (SPI) Mode

The following timing information is valid across the full range of recommended operating conditions.

Parameter [1, 2]		Symbol	Min	Typ	Max	Units
$\overline{SS}$ falling edge to SCLK rising edge		t_{SSU}	2.6	—	—	ns
SCLK falling edge to $\overline{SS}$ rising edge		t_{SHO}	0	—	—	ns
SCLK pulse cycle time	SYSCLK disabled (SYSCLK_ENA = 0)	t_{SCY}	38.4	—	—	ns
	SYSCLK_ENA = 1, SYSCLK_FREQ = 000	t_{SCY}	76.8	—	—	ns
	SYSCLK_ENA = 1, SYSCLK_FREQ > 000	t_{SCY}	38.4	—	—	ns
SCLK pulse width low		t_{SCL}	15.3	—	—	ns
SCLK pulse width high		t_{SCH}	15.3	—	—	ns
MOSI to SCLK set-up time		t_{DSU}	1.5	—	—	ns
MOSI to SCLK hold time		t_{DHO}	1.7	—	—	ns
SCLK falling edge to MISO transition	SCLK slew (90%–10%) = 5 ns, C_{LOAD} (MISO) = 25 pF	t_{DL}	0	—	12.6	ns

1. Control interface timing—SPI Mode (write cycle)



2. Control interface timing—SPI Mode (read cycle)

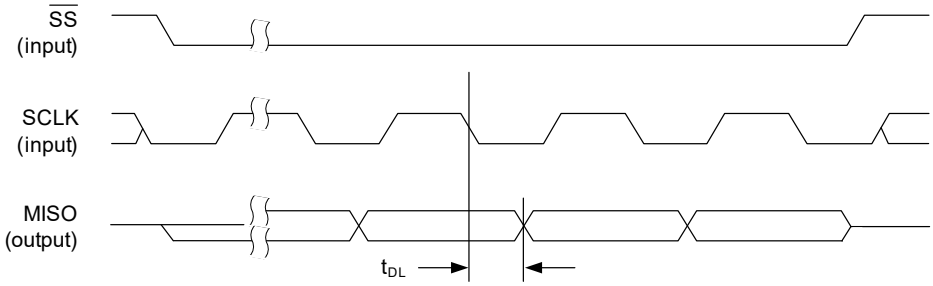


Table 3-21. Master Interface Timing—SPI Master

The following timing information is valid across the full range of recommended operating conditions.

Parameter [1]		Symbol	Min	Typ	Max	Units
$\overline{SS}$ falling edge to SCLK rising edge		t_{SSU}	13.88	—	—	ns
SCLK falling edge to $\overline{SS}$ rising edge		t_{SHO}	0	—	—	ns
SCLK pulse cycle time		t_{SCY}	27.77	—	—	ns
SCLK pulse width low		t_{SCL}	13.88	—	—	ns
SCLK pulse width high		t_{SCH}	13.88	—	—	ns
SCLK falling edge to MOSI transition	SCLK slew (90%–10%) = 5 ns, C_{LOAD} (MOSI) = 25 pF	t_{DL}	0	—	8.88	ns
MISO to SCLK set-up time		t_{DSU}	5	—	—	ns
MISO to SCLK hold time		t_{DHO}	5	—	—	ns

1.Master interface timing—SPI read cycle

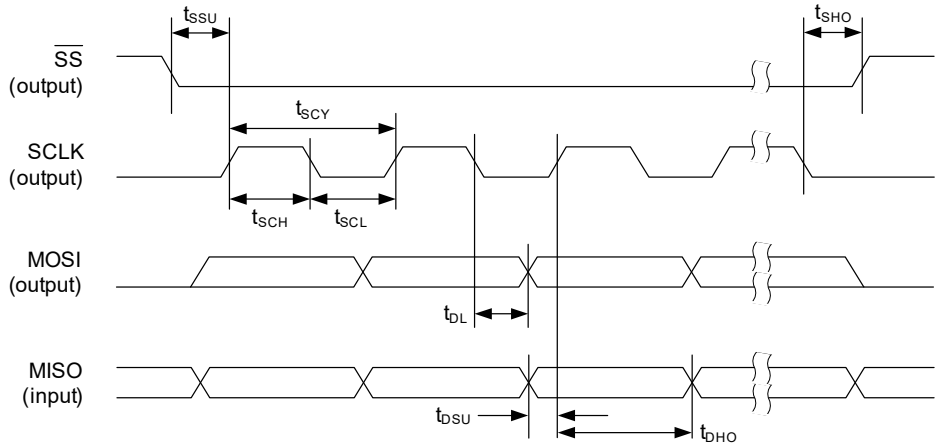


Table 3-22. JTAG Interface Timing

Test conditions (unless specified otherwise): C_{LOAD} = 25 pF (output pins); TCK slew (20%–80%) = 5 ns; with the exception of the conditions noted, the following electrical characteristics are valid across the full range of recommended operating conditions.

Parameter [1]	Symbol	Minimum	Typical	Maximum	Units
TCK cycle time	T_{CCY}	50	—	—	ns
TCK pulse width high	T_{CCH}	20	—	—	ns
TCK pulse width low	T_{CCL}	20	—	—	ns
TMS setup time to TCK rising edge	T_{MSU}	1	—	—	ns
TMS hold time from TCK rising edge	T_{MH}	2	—	—	ns
TDI setup time to TCK rising edge	T_{DSU}	1	—	—	ns
TDI hold time from TCK rising edge	T_{DH}	2	—	—	ns
TDO propagation delay from TCK falling edge	T_{DD}	0	—	17	ns
TRST setup time to TCK rising edge	T_{RSU}	3	—	—	ns
TRST hold time from TCK rising edge	T_{RH}	3	—	—	ns
TRST pulse width low	—	20	—	—	ns

1.JTAG Interface timing

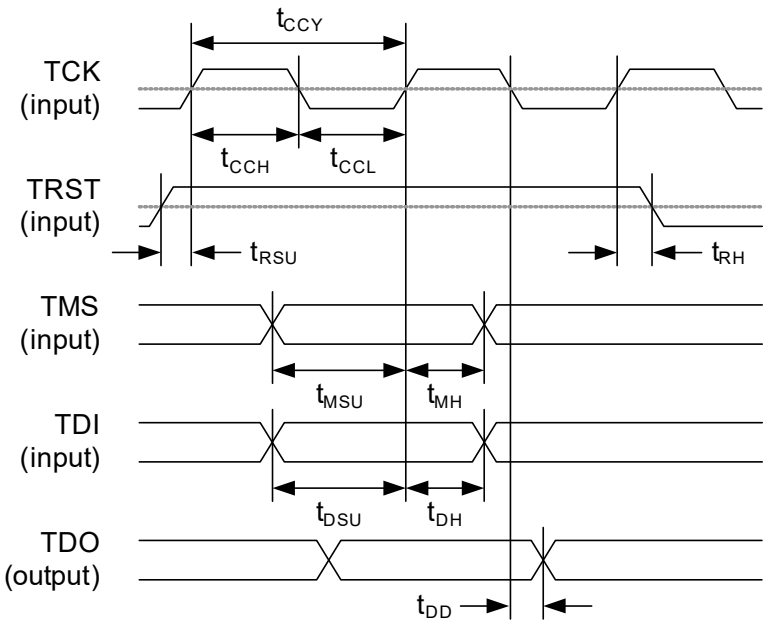


Table 3-23. Typical Power Consumption

Test conditions (unless specified otherwise): DBVDD = CPVDD = AVDD = 1.8 V, DCVDD = 1.2 V; MICVDD = 2.5 V; SPKVDD = 4.2 V; T_A = +25ºC; Fs = 48 kHz; 24-bit audio data, I²S Slave Mode; SYSCLK = 24.576 MHz (direct MCLK1 input).

Operating Configuration		Typical $I_{1.2V}$ (mA)	Typical $I_{1.8V}$ (mA)	Typical $I_{2.5V}$ (mA)	Typical $I_{4.2V}$ (mA)	P_{TOT} (mW)
Headphone playback—AIF1 to DAC to HPOUT (stereo), 32-Ω load.	Quiescent	0.78	0.92	0.001	0.00	2.59
	1-kHz sine wave, P_O = 0.1 mW	0.87	3.6	0.001	0.00	7.6
Earpiece playback—AIF1 to DAC to EPOUT, 32-Ω load (BTL).	Quiescent	0.59	0.94	0.001	0.00	2.40
	1-kHz sine wave, P_O = 30 mW	0.62	61.68	0.001	0.00	112
Speaker playback—AIF1 to DAC to SPKOUT, 8-Ω, 22-µH load.	Quiescent	0.61	1.18	0.001	0.13	3.40
	1-kHz sine wave, P_O = 700 mW	0.66	1.18	0.001	187	790
Stereo line record—Analog line to ADC to AIF1	1-kHz sine wave, –1 dBFS output	1.11	2.22	0.001	0.00	5.33
Sleep Mode	Accessory detect enabled (JD1_ENA = 1)	0.000	0.014	0.000	0.000	0.025

Table 3-24. Typical Signal Latency

Test conditions (unless specified otherwise): DBVDD = CPVDD = AVDD = 1.8 V, DCVDD = 1.2 V; MICVDD = 2.5 V; SPKVDD = 4.2 V; T_A = +25ºC; Fs = 48 kHz; 24-bit audio data, I²S Slave Mode; SYSCLK = 24.576 MHz (direct MCLK1 input).

Operating Configuration			Latency (µs)
AIF to DAC path	Digital input (AIFn) to analog output (HPOUT).	48 kHz input, 48 kHz output, Synchronous	332
		44.1 kHz input, 44.1 kHz output, Synchronous	358
		16 kHz input, 16 kHz output, Synchronous	550
		8 kHz input, 8 kHz output, Synchronous	1076
		8 kHz input, 48 kHz output, Isochronous [1]	1717
		16 kHz input, 48 kHz output, Isochronous [1]	1041
ADC to AIF path	Analog input (INn) to digital output (AIFn).[2]	48 kHz input, 48 kHz output, Synchronous	219
		44.1 kHz input, 44.1 kHz output, Synchronous	234
		16 kHz input, 16 kHz output, Synchronous	654
		8 kHz input, 8 kHz output, Synchronous	1323
		8 kHz input, 48 kHz output, Isochronous [1]	1802
		16 kHz input, 48 kHz output, Isochronous [1]	994

1. Signal is routed via the ISRC function in the isochronous cases only.
2. Digital core high-pass filter is included in the signal path