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CS47L24

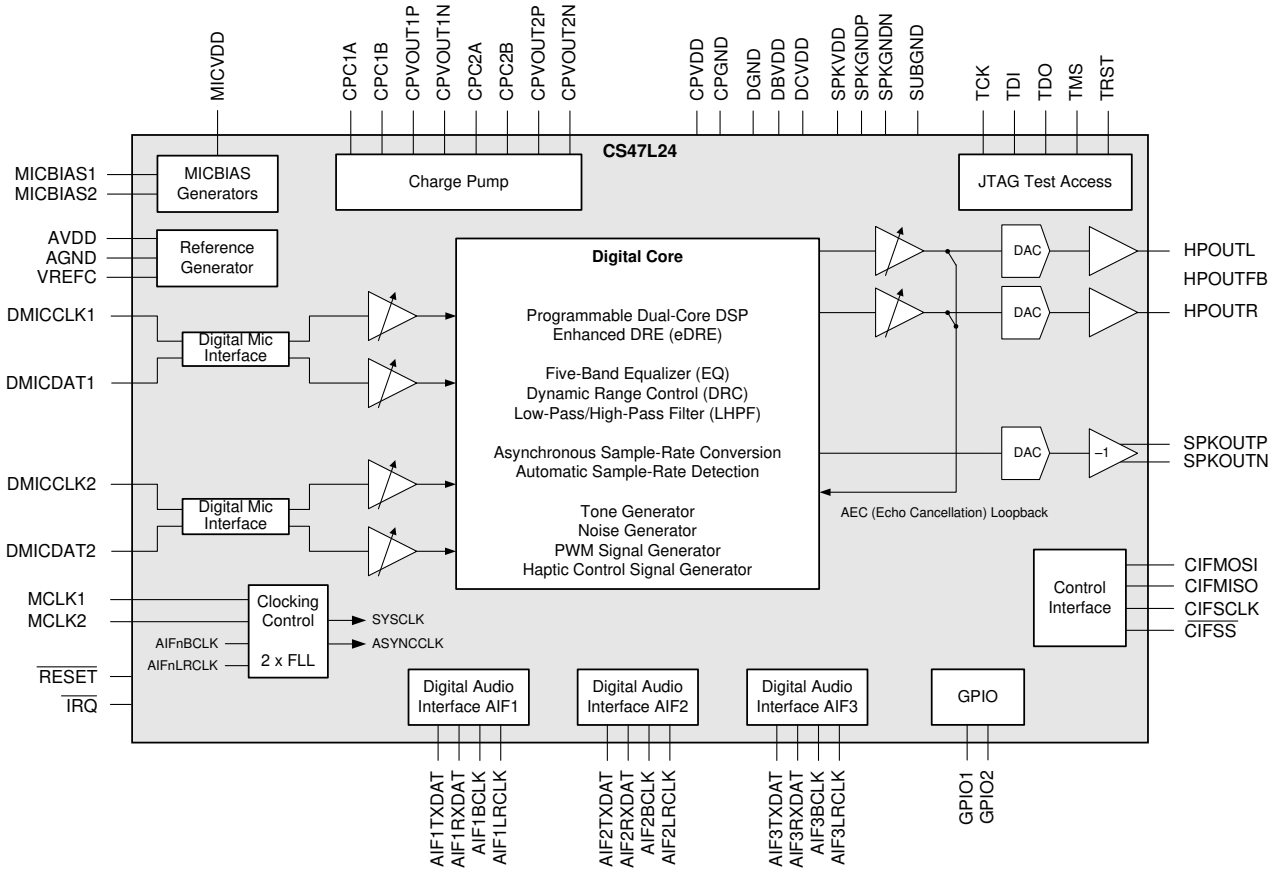
Low Power Audio Hub for Wearable Technology

Features

- 300 MIPS, 300MMAC dual-core audio-signal processor
- Enhanced DRE processing (eDRE) for 121dB SNR
- Fixed function signal-processing functions
  - — Dynamic range control, fully parametric EQs
  - — Tone, noise, PWM, haptic control signal generators
- Multichannel asynchronous sample-rate conversion
- Integrated multichannel 24-bit hi-fi audio hub codec
  - — 121-dB SNR headphone playback (48 kHz)
- Four digital microphone inputs (two stereo interfaces)
- Stereo headphone/earpiece/line output driver
  - — 33 mW into 32-Ω load at 1% THD+N
- Mono 2W Class D speaker output driver
- Three full digital audio interfaces
  - — Standard sample rates from 8kHz up to 192kHz
  - — TDM support on all AIFs
- Flexible clocking, derived from MCLKn or AIFn
- Two low-power frequency-locked loops (FLLs) support reference clocks down to 32 kHz
- Configurable functions on two GPIO pins
- Integrated regulators and charge pumps
- Small W-CSP package, 0.4-mm ball array

Applications

- Portable accessories and wearable technology
- Smartphones and multimedia handsets
- Speech-recognition applications



Description

The CS47L24 is a highly integrated, low-power audio hub for wearable technology and other portable audio devices. It combines an advanced DSP feature set with a flexible, high-performance audio hub codec.

The CS47L24 digital core combines a dual-core, 300MMAC DSP system, with a variety of power-efficient fixed-function audio-processing blocks. These are supported by a fully flexible, all-digital mixing and routing engine with sample rate converters for wide use-case flexibility. The programmable DSP cores support a range of advanced audio processing features, including multimic noise suppression, acoustic-echo cancellation (AEC), and voice recognition functions. The Enhanced DRE (eDRE) software is included with the CS47L24; additional software packages can be chosen according to the requirements of the target application.

Three digital audio interfaces are provided, each supporting a wide range of standard audio sample rates and serial interface formats. Automatic sample-rate detection enables seamless wideband/narrowband voice-call handover.

The headphone/line output driver provides stereo ground-referenced or mono BTL output. 121dB SNR, and noise levels as low as 0.8 µVRMS, offer hi-fi quality line or headphone output. A mono Class D output driver is incorporated; supporting up to 2-W audio output. A signal generator for controlling haptics devices is included; vibe actuators can connect directly to the Class D speaker output or via an external driver connected to a GPIO output. All inputs, outputs, and system interfaces can function concurrently.

The CS47L24 supports up to four digital microphone inputs. Microphone activity detection with interrupt is available.

The CS47L24 power, clocking and output driver architectures are all designed to maximize battery life in voice, music, and standby modes. The CS47L24 is powered from 1.8- and 1.2-V external supplies. Separate MICVDD input can be supported, for microphone operation above 1.8 V. An additional supply is required for the Class D speaker drivers (typically direct connection to 4.2-V battery).

Two integrated FLLs provide support for a wide range of system clock frequencies. The CS47L24 is configured using an SPI™ control interface. The fully CS47L24 differential internal analog architecture, minimal analog signal paths, and on-chip RF noise filters ensure a very high degree of noise immunity.

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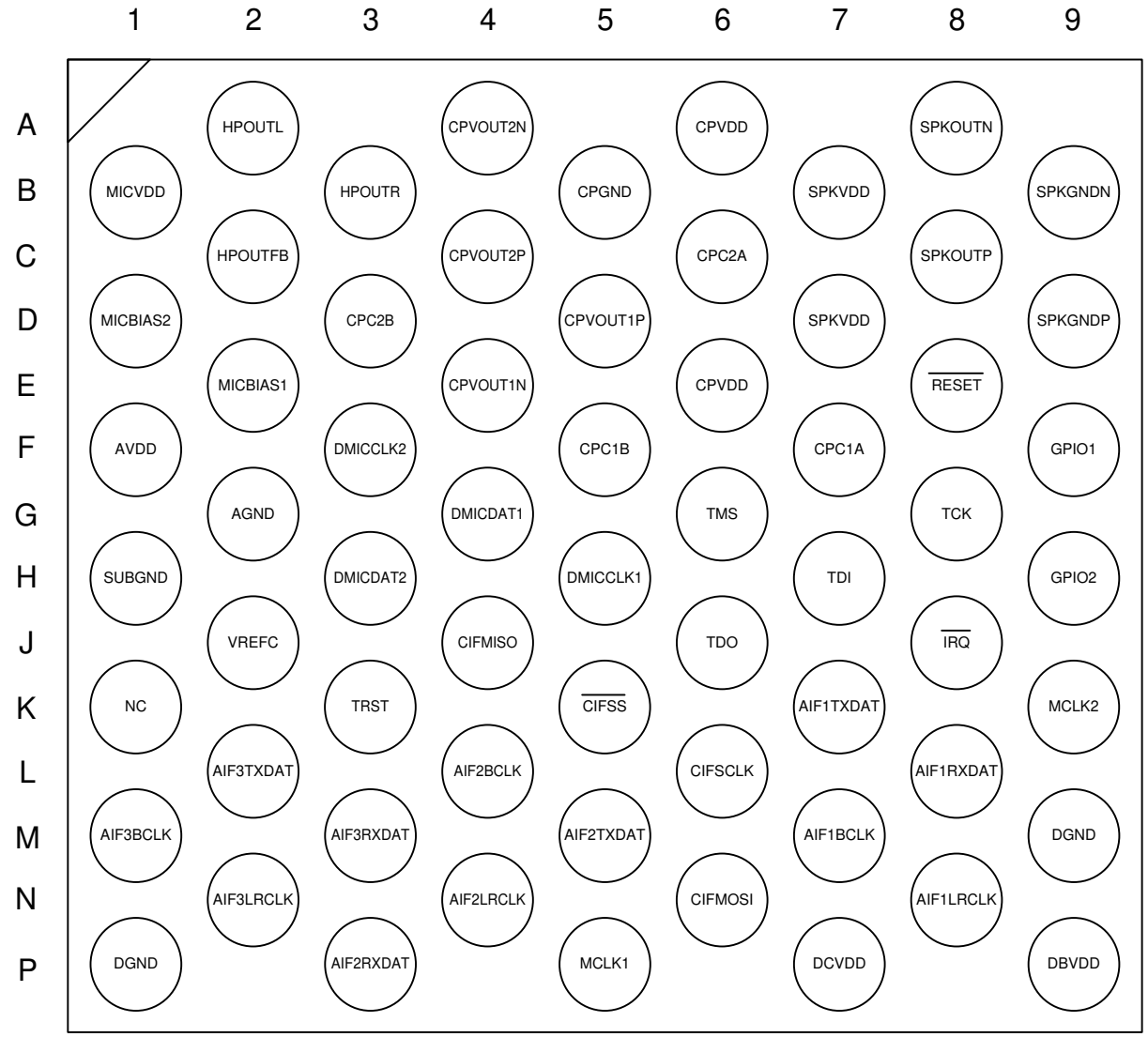
PIN CONFIGURATION



TOP VIEW – CS47L24

ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
CS47L24-CWZ	-40°C to +85°C	W-CSP (Pb-free)	MSL1	260°C
CS47L24-CWZR	-40°C to +85°C	W-CSP (Pb-free, Tape and reel)	MSL1	260°C

Note:
Reel quantity = 7000

PIN DESCRIPTION

A description of each pin on the CS47L24 is provided below.

Note that a table detailing the associated power domain for every input and output pin is provided on the following page.

Note that, where multiple pins share a common name, these pins should be tied together on the PCB.

All Digital Output pins are CMOS outputs, unless otherwise stated.

PIN NO	NAME	TYPE	DESCRIPTION
G2	AGND	Supply	Analogue ground (Return path for AVDD and MICVDD)
M7	AIF1BCLK	Digital Input / Output	Audio interface 1 bit clock
N8	AIF1LRCLK	Digital Input / Output	Audio interface 1 left / right clock
L8	AIF1RXDAT	Digital Input	Audio interface 1 RX digital audio data
K7	AIF1TXDAT	Digital Output	Audio interface 1 TX digital audio data
L4	AIF2BCLK	Digital Input / Output	Audio interface 2 bit clock
N4	AIF2LRCLK	Digital Input / Output	Audio interface 2 left / right clock
P3	AIF2RXDAT	Digital Input	Audio interface 2 RX digital audio data
M5	AIF2TXDAT	Digital Output	Audio interface 2 TX digital audio data
M1	AIF3BCLK	Digital Input / Output	Audio interface 3 bit clock
N2	AIF3LRCLK	Digital Input / Output	Audio interface 3 left / right clock
M3	AIF3RXDAT	Digital Input	Audio interface 3 RX digital audio data
L2	AIF3TXDAT	Digital Output	Audio interface 3 TX digital audio data
F1	AVDD	Supply	Analogue supply
J4	CIFMISO	Digital Output	Control interface Master In Slave Out. The pin configuration is selectable CMOS or 'Wired OR'.
N6	CIFMOSI	Digital Input	Control interface Master Out Slave In data.
L6	CIFSCLK	Digital Input	Control interface clock input
K5	$\overline{\text{CIFSS}}$	Digital Input	Control interface Slave Select (SS)
F7	CPC1A	Analogue Output	Charge pump fly-back capacitor 1 pin
F5	CPC1B	Analogue Output	Charge pump fly-back capacitor 1 pin
C6	CPC2A	Analogue Output	Charge pump fly-back capacitor 2 pin
D3	CPC2B	Analogue Output	Charge pump fly-back capacitor 2 pin
B5	CPGND	Supply	Charge pump ground (Return path for CPVDD)
A6, E6	CPVDD	Supply	Supply for Charge Pump
E4	CPVOUT1N	Analogue Output	Charge pump negative output 1 decoupling pin
D5	CPVOUT1P	Analogue Output	Charge pump positive output 1 decoupling pin
A4	CPVOUT2N	Analogue Output	Charge pump negative output 2 decoupling pin
C4	CPVOUT2P	Analogue Output	Charge pump positive output 2 decoupling pin
P9	DBVDD	Supply	Digital buffer (I/O) supply
P7	DCVDD	Supply	Digital core supply
M9, P1	DGND	Supply	Digital ground (Return path for DCVDD and DBVDD)
H5	DMICCLK1	Digital Output	Digital MIC clock output 1
F3	DMICCLK2	Digital Output	Digital MIC clock output 2
G4	DMICDAT1	Digital Input	Digital MIC data input 1
H3	DMICDAT2	Digital Input	Digital MIC data input 2
F9	GPIO1	Digital Input / Output	General Purpose pin GPIO1. The output configuration is selectable CMOS or Open Drain.
H9	GPIO2	Digital Input / Output	General Purpose pin GPIO2. The output configuration is selectable CMOS or Open Drain.
C2	HPOUTFB	Analogue Input	HPOUTL and HPOUTR ground feedback pin
A2	HPOUTL	Analogue Output	Left headphone output
B3	HPOUTR	Analogue Output	Right headphone output
J8	$\overline{\text{IRQ}}$	Digital Output	Interrupt Request (IRQ) output (default is active low). The pin configuration is selectable CMOS or Open Drain.
P5	MCLK1	Digital Input	Master clock 1
K9	MCLK2	Digital Input	Master clock 2

PIN NO	NAME	TYPE	DESCRIPTION
E2	MICBIAS1	Analogue Output	Microphone bias 1
D1	MICBIAS2	Analogue Output	Microphone bias 2
B1	MICVDD	Supply	Microphone bias supply (input to MICBIASn regulators).
E8	RESET	Digital Input	Digital Reset input (active low)
B9	SPKGNDN	Supply	Speaker driver ground (Return path for SPKVDD). See note.
D9	SPKGNDP	Supply	Speaker driver ground (Return path for SPKVDD). See note.
A8	SPKOUTN	Analogue Output	Speaker negative output
C8	SPKOUTP	Analogue Output	Speaker positive output
B7, D7	SPKVDD	Supply	Speaker driver supply
H1	SUBGND	Supply	Substrate ground
G8	TCK	Digital Input	JTAG clock input. Internal pull-down holds this pin at logic 0 for normal operation.
H7	TDI	Digital Input	JTAG data input. Internal pull-down holds this pin at logic 0 for normal operation.
J6	TDO	Digital Output	JTAG data output
G6	TMS	Digital Input	JTAG mode select input. Internal pull-down holds this pin at logic 0 for normal operation.
K3	TRST	Digital Input	JTAG Test Access Port reset (active low). Internal pull-down holds this pin at logic 0 for normal operation.
J2	VREFC	Analogue Output	Bandgap reference decoupling capacitor connection
K1	NC		No Connection

Note:

Separate P/N ground connections are provided for each speaker driver channel; this provides flexible support for current monitoring and output protection circuits. If this option is not used, then the respective ground connections should be tied together on the PCB.

The following table identifies the power domain and ground reference associated with each of the input / output pins.

PIN NO	NAME	POWER DOMAIN	GROUND DOMAIN
M7	AIF1BCLK	DBVDD	DGND
N8	AIF1LRCLK	DBVDD	DGND
L8	AIF1RXDAT	DBVDD	DGND
K7	AIF1TXDAT	DBVDD	DGND
L4	AIF2BCLK	DBVDD	DGND
N4	AIF2LRCLK	DBVDD	DGND
P3	AIF2RXDAT	DBVDD	DGND
M5	AIF2TXDAT	DBVDD	DGND
M1	AIF3BCLK	DBVDD	DGND
N2	AIF3LRCLK	DBVDD	DGND
M3	AIF3RXDAT	DBVDD	DGND
L2	AIF3TXDAT	DBVDD	DGND
J4	CIFMISO	DBVDD	DGND
N6	CIFMOSI	DBVDD	DGND
L6	CIFSCLK	DBVDD	DGND
K5	$\overline{\text{CIFSS}}$	DBVDD	DGND
H5	DMICCLK1	MICVDD, MICBIAS1, MICBIAS2 The DMICCLK1 power domain is selectable using IN1_DMIC_SUP	AGND
F3	DMICCLK2	MICVDD, MICBIAS1, MICBIAS2 The DMICCLK2 power domain is selectable using IN2_DMIC_SUP	AGND
G4	DMICDAT1	MICVDD, MICBIAS1, MICBIAS2 The DMICDAT1 power domain is selectable using IN1_DMIC_SUP	AGND
H3	DMICDAT2	MICVDD, MICBIAS1, MICBIAS2 The DMICDAT2 power domain is selectable using IN2_DMIC_SUP	AGND
F9	GPIO1	DBVDD	DGND
H9	GPIO2	DBVDD	DGND
C2	HPOUTFB	CPVDD (Ground noise rejection)	CPGND
A2	HPOUTL	CPVDD	CPGND
B3	HPOUTR	CPVDD	CPGND
J8	$\overline{\text{IRQ}}$	DBVDD	DGND
P5	MCLK1	DBVDD	DGND
K9	MCLK2	DBVDD	DGND
E2	MICBIAS1	MICVDD	AGND
D1	MICBIAS2	MICVDD	AGND
E8	$\overline{\text{RESET}}$	DBVDD	DGND
A8	SPKOUTN	SPKVDD	SPKGNDN
C8	SPKOUTP	SPKVDD	SPKGNDP
G8	TCK	DBVDD	DGND
H7	TDI	DBVDD	DGND
J6	TDO	DBVDD	DGND
G6	TMS	DBVDD	DGND
K3	TRST	DBVDD	DGND

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Cirrus Logic tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages (DCVDD)	-0.3V	MIN (1.6V, AVDD+0.6V)
Supply voltages (CPVDD)	-0.3V	2.5V
Supply voltages (DBVDD, AVDD, MICVDD)	-0.3V	5.0V
Supply voltages (SPKVDD)	-0.3V	6.0V
Voltage range digital inputs	SUBGND - 0.3V	DBVDD + 0.3V
Voltage range digital inputs (DMICDATn)	SUBGND - 0.3V	MICVDD + 0.3V
Voltage range analogue inputs (HPOUTFB)	SUBGND - 0.3V	SUBGND + 0.3V
Ground (AGND, DGND, CPGND, SPKGND)	SUBGND - 0.3V	SUBGND + 0.3V
Operating temperature range, T_A	-40ºC	+85ºC
Operating junction temperature, T_J	-40ºC	+125ºC
Storage temperature after soldering	-65ºC	+150ºC

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core) See note 2	DCVDD	1.14	1.2	1.26	V
Digital supply range (I/O)	DBVDD	1.71	1.8	2.75	V
Charge Pump supply range	CPVDD	1.71	1.8	1.89	V
Analogue supply range See note 2	AVDD	1.71	1.8	1.89	V
Microphone Bias supply	MICVDD	1.71		3.6	V
Speaker supply range	SPKVDD	2.4		5.5	V
Ground See note 1	DGND, AGND, CPGND, SPKGNDN, SPKGNDP, SUBGND		0		V
Power supply rise time See notes 3, 4, 5	DCVDD	10		2000	µs
	All other supplies	10			
Operating temperature range	T_A	-40		85	°C

Notes:

1. The impedance between DGND, AGND, CPGND and SUBGND should be less than 0.1Ω.The impedance between SPKGND and SUBGND should be less than 0.2Ω.
2. AVDD must be supplied before or simultaneously to DCVDD. DCVDD must not be powered if AVDD is not present. There are no other power sequencing requirements.
3. If the DCVDD rise time exceeds 2ms, then $\overline{\text{RESET}}$ must be asserted (low) during the rise, and held asserted until after DCVDD is within the recommended operating limits.
4. The specified minimum power supply rise times assume a minimum decoupling capacitance of 100nF per pin. However, Cirrus Logic strongly advises that the recommended decoupling capacitors are present on the PCB and that appropriate layout guidelines are observed.
5. The specified minimum power supply rise times also assume a maximum PCB inductance of 10nH between decoupling capacitor and pin.

ELECTRICAL CHARACTERISTICS

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Microphone Input Signal Level (DMICDAT1, DMICDAT2)						
Full-scale input signal level (0dBFS signal to digital core)		0dB gain		-6		dBFS

Note:

The digital microphone input signal level is measured in dBFS, where 0dBFS is a signal level equal to the full-scale range (FSR) of the PDM input. The FSR is defined as the amplitude of a 1kHz sine wave whose positive and negative peaks are represented by the maximum and minimum digital codes respectively - this is the largest 1kHz sine wave that will fit in the digital output range without clipping.

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Line / Headphone / Earpiece Output Driver (HPOUTL, HPOUTR)						
Load resistance		Normal operation, Single-ended mode	6			Ω
		Normal operation, Differential (BTL) mode	15			
		Device survival with load applied indefinitely	0			
Load capacitance		Direct connection, Normal Mode			500	pF
		Direct connection, Mono Mode (BTL)			200	
		Connection via 16Ω series resistor			2	nF
Speaker Output Driver (SPKOUTP+SPKOUTN)						
Load resistance		Normal operation	4			Ω
		Device survival with load applied indefinitely	0			
Load capacitance					200	pF
Digital Speaker Output (SPKDAT)						
Full-scale output level (0dBFS digital core output)		0dB gain		-6		dBFS

Note:

The digital output signal level is measured in dBFS, where 0dBFS is a signal level equal to the full-scale range (FSR) of the PDM output. The FSR is defined as the amplitude of a 1kHz sine wave whose positive and negative peaks are represented by the maximum and minimum digital codes respectively - this is the largest 1kHz sine wave that will fit in the digital output range without clipping.

Test Conditions

DBVDD = CPVDD = AVDD = 1.8V, MICVDD = 2.2V, DCVDD = 1.2V, SPKVDD = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Line / Headphone / Earpiece Output Driver (HPOUTL, HPOUTR)						
DC offset at Load		Single-ended mode		0.1		mV
		Differential (BTL) mode		0.2		
Speaker Output Driver (SPKOUTP+SPKOUTN)						
DC offset at Load				10		mV
SPKVDD leakage current				1		µA
DAC to Line Output (HPOUTL, HPOUTR; Load = 10kΩ, 50pF)						
Full-scale output signal level	V_{OUT}	0dBFS input	1 0			Vrms dBV
Signal to Noise Ratio (A-weighted)	SNR	Output signal = 1Vrms	106	115		dB
		Output signal = 1Vrms, eDRE software enabled		121		
Dynamic Range (A-weighted)	DR	-60dBFS input		115		dB
Total Harmonic Distortion	THD	0dBFS input		-93	-84	dB
Total Harmonic Distortion + Noise	THD+N	0dBFS input		-92		dB
Channel separation (Left/Right)				110		dB
Output noise floor (A-weighted)		eDRE software enabled		0.9		μV_{RMS}
PSRR (DBVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		105		dB
		100mV (peak-peak) 10kHz		75		
PSRR (MICVDD)	PSRR	100mV (peak-peak) 217Hz		112		dB
		100mV (peak-peak) 10kHz		102		
PSRR (DCVDD)	PSRR	100mV (peak-peak) 217Hz		110		dB
		100mV (peak-peak) 10kHz		114		
PSRR (SPKVDD)	PSRR	100mV (peak-peak) 217Hz		111		dB
		100mV (peak-peak) 10kHz		103		

Test Conditions

DBVDD = CPVDD = AVDD = 1.8V, MICVDD = 2.2V, DCVDD = 1.2V, SPKVDD = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Headphone Output (HPOUTL, HPOUTR, R_L = 32Ω, Short Circuit Protection disabled)						
Maximum output power	P_O	0.1% THD+N		30		mW
Signal to Noise Ratio (A-weighted)	SNR	Output signal = 1Vrms	106	115		dB
		Output signal = 1Vrms, eDRE software enabled		121		
Dynamic Range (A-weighted)	DR	-60dBFS input		115		dB
Total Harmonic Distortion	THD	P_O = 20mW		-92	-82	dB
Total Harmonic Distortion + Noise	THD+N	P_O = 20mW		-90		dB
Total Harmonic Distortion	THD	P_O = 5mW		-91		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 5mW		-88		dB
Channel separation (Left/Right)				94		dB
Output noise floor (A-weighted)		eDRE software enabled		0.9		μV_{RMS}
PSRR (DBVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		105		dB
		100mV (peak-peak) 10kHz		75		
PSRR (MICVDD)	PSRR	100mV (peak-peak) 217Hz		112		dB
		100mV (peak-peak) 10kHz		102		
PSRR (DCVDD)	PSRR	100mV (peak-peak) 217Hz		110		dB
		100mV (peak-peak) 10kHz		114		
PSRR (SPKVDD)	PSRR	100mV (peak-peak) 217Hz		111		dB
		100mV (peak-peak) 10kHz		103		
DAC to Headphone Output (HPOUTL, HPOUTR, R_L = 16Ω, Short Circuit Protection disabled; eDRE enabled)						
Maximum output power	P_O	0.1% THD+N		39		mW
Signal to Noise Ratio (A-weighted)	SNR	Output signal = 1Vrms	106	115		dB
		Output signal = 1Vrms, eDRE software enabled		121		
Dynamic Range (A-weighted)	DR	-60dBFS input		115		dB
Total Harmonic Distortion	THD	P_O = 20mW		-88	-78	dB
Total Harmonic Distortion + Noise	THD+N	P_O = 20mW		-87		dB
Total Harmonic Distortion	THD	P_O = 5mW		-88		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 5mW		-86		dB
Channel separation (Left/Right)				92		dB
Output noise floor (A-weighted)		eDRE software enabled		0.9		μV_{RMS}
PSRR (DBVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		105		dB
		100mV (peak-peak) 10kHz		75		
PSRR (MICVDD)	PSRR	100mV (peak-peak) 217Hz		112		dB
		100mV (peak-peak) 10kHz		102		
PSRR (DCVDD)	PSRR	100mV (peak-peak) 217Hz		110		dB
		100mV (peak-peak) 10kHz		114		
PSRR (SPKVDD)	PSRR	100mV (peak-peak) 217Hz		111		dB
		100mV (peak-peak) 10kHz		103		

Test Conditions

DBVDD = CPVDD = AVDD = 1.8V, MICVDD = 2.2V, DCVDD = 1.2V, SPKVDD = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Earpiece Output (HPOUTL, HPOUTR, Mono Mode, R_L = 32Ω BTL, Short Circuit Protection disabled)						
Maximum output power	P_O	0.1% THD+N		97		mW
Signal to Noise Ratio (A-weighted)	SNR	Output signal = 1.41Vrms		115		dB
		Output signal = 1.41Vrms, eDRE software enabled		126		
Dynamic Range (A-weighted)	DR	-60dBFS input		115		dB
Total Harmonic Distortion	THD	P_O = 75mW		-88		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 75mW		-86		dB
Total Harmonic Distortion	THD	P_O = 5mW		-90		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 5mW		-88		dB
Output noise floor (A-weighted)		eDRE software enabled		0.7		μV_{RMS}
PSRR (DBVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		102		dB
		100mV (peak-peak) 10kHz		101		
PSRR (MICVDD)	PSRR	100mV (peak-peak) 217Hz		109		dB
		100mV (peak-peak) 10kHz		107		
PSRR (DCVDD)	PSRR	100mV (peak-peak) 217Hz		110		dB
		100mV (peak-peak) 10kHz		109		
PSRR (SPKVDD)	PSRR	100mV (peak-peak) 217Hz		110		dB
		100mV (peak-peak) 10kHz		105		
DAC to Earpiece Output (HPOUTL, HPOUTR, Mono Mode, R_L = 16Ω BTL, Short Circuit Protection disabled)						
Maximum output power	P_O	0.1% THD+N		110		mW
Signal to Noise Ratio (A-weighted)	SNR	Output signal = 1.41Vrms		115		dB
		Output signal = 1.41Vrms, eDRE software enabled		126		
Dynamic Range (A-weighted)	DR	-60dBFS input		115		dB
Total Harmonic Distortion	THD	P_O = 75mW		-85		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 75mW		-83		dB
Total Harmonic Distortion	THD	P_O = 5mW		-86		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 5mW		-85		dB
Output noise floor (A-weighted)		eDRE software enabled		0.7		μV_{RMS}
PSRR (DBVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		102		dB
		100mV (peak-peak) 10kHz		101		
PSRR (MICVDD)	PSRR	100mV (peak-peak) 217Hz		109		dB
		100mV (peak-peak) 10kHz		107		
PSRR (DCVDD)	PSRR	100mV (peak-peak) 217Hz		110		dB
		100mV (peak-peak) 10kHz		109		
PSRR (SPKVDD)	PSRR	100mV (peak-peak) 217Hz		110		dB
		100mV (peak-peak) 10kHz		105		

Test Conditions

DBVDD = CPVDD = AVDD = 1.8V, MICVDD = 2.2V, DCVDD = 1.2V, SPKVDD = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Speaker Output (SPKOUTP+SPKOUTN; Load = 8Ω, 22µH, BTL)						
Maximum output power	P_O	SPKVDD = 5.0V, 1% THD+N		1.4		W
		SPKVDD = 4.2V, 1% THD+N		1.0		
		SPKVDD = 3.6V, 1% THD+N		0.7		
Signal to Noise Ratio (A-weighted)	SNR	Output signal = 2.83Vrms	85	95		dB
Dynamic Range (A-weighted)	DR	-60dBFS input		95		dB
Total Harmonic Distortion	THD	P_O = 1.0W		-40		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 1.0W		-40		dB
Total Harmonic Distortion	THD	P_O = 0.5W		-70	-59	dB
Total Harmonic Distortion + Noise	THD+N	P_O = 0.5W		-69		dB
Output noise floor (A-weighted)				51	158	μV_{RMS}
PSRR (DBVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		76		dB
		100mV (peak-peak) 10kHz		65		
PSRR (MICVDD)	PSRR	100mV (peak-peak) 217Hz		81		dB
		100mV (peak-peak) 10kHz		82		
PSRR (DCVDD)	PSRR	100mV (peak-peak) 217Hz		84		dB
		100mV (peak-peak) 10kHz		88		
PSRR (SPKVDD)	PSRR	100mV (peak-peak) 217Hz		69		dB
		100mV (peak-peak) 10kHz		70		
DAC to Speaker Output (SPKOUTP+SPKOUTN; Load = 4Ω, 15µH, BTL)						
Maximum output power	P_O	SPKVDD = 5.0V, 1% THD+N		2.7		W
		SPKVDD = 4.2V, 1% THD+N		1.9		
		SPKVDD = 3.6V, 1% THD+N		1.4		
Signal to Noise Ratio (A-weighted)	SNR	Output signal = 2.83Vrms		95		dB
Dynamic Range (A-weighted)	DR	-60dBFS input		95		dB
Total Harmonic Distortion	THD	P_O = 1.0W		-70		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 1.0W		-69		dB
Total Harmonic Distortion	THD	P_O = 0.5W		-69		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 0.5W		-68		dB
Output noise floor (A-weighted)				51		μV_{RMS}
PSRR (DBVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		76		dB
		100mV (peak-peak) 10kHz		65		
PSRR (MICVDD)	PSRR	100mV (peak-peak) 217Hz		81		dB
		100mV (peak-peak) 10kHz		82		
PSRR (DCVDD)	PSRR	100mV (peak-peak) 217Hz		84		dB
		100mV (peak-peak) 10kHz		88		
PSRR (SPKVDD)	PSRR	100mV (peak-peak) 217Hz		69		dB
		100mV (peak-peak) 10kHz		70		

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input / Output (except DMICDATn and DMICCLKn)						
Input HIGH Level	V_{IH}	V_{DBVDD} = 1.71V to 1.98V	0.75 × V_{DBVDD}			V
		V_{DBVDD} = 2.25V to 2.75V	0.8 × V_{DBVDD}			
Input LOW Level	V_{IL}	V_{DBVDD} = 1.71V to 1.98V			0.3 × V_{DBVDD}	V
		V_{DBVDD} = 2.25V to 2.75V			0.25 × V_{DBVDD}	
Note that digital input pins should not be left unconnected or floating.						
Output HIGH Level (I_{OH} = 1mA)	V_{OH}	V_{DBVDD} = 1.71V to 1.98V	0.75 × V_{DBVDD}			V
		V_{DBVDD} = 2.25V to 2.75V	0.65 × V_{DBVDD}			
Output LOW Level (I_{OL} = 1mA)	V_{OL}	V_{DBVDD} = 1.71V to 1.98V			0.25 × V_{DBVDD}	V
		V_{DBVDD} = 2.25V to 2.75V			0.3 × V_{DBVDD}	
Input capacitance					5	pF
Input leakage			-10		10	µA
Pull-up / pull-down resistance (where applicable)			42		56	kΩ
Digital Microphone Input / Output (DMICDATn and DMICCLKn) **DMICDATn and DMICCLKn are each referenced to a selectable supply, V_{SUP}, according to the INn_DMIC_SUP registers**						
DMICDATn input HIGH Level	V_{IH}		0.65 × V_{SUP}			V
DMICDATn input LOW Level	V_{IL}				0.35 × V_{SUP}	V
DMICCLKn output HIGH Level	V_{OH}	I_{OH} = 1mA	0.8 × V_{SUP}			V
DMICCLKn output LOW Level	V_{OL}	I_{OL} = -1mA			0.2 × V_{SUP}	V
Input capacitance				25		pF
Input leakage			-1		1	µA
General Purpose Input / Output (GPIOn)						
Clock output frequency		GPIO pin configured as OPCLK or FLL output			50	MHz

Test Conditions

fs ≤ 48kHz

With the exception of the condition(s) noted above, the following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC Interpolation Filters						
Passband		+/- 0.05dB	0		0.454 fs	
		-6dB		0.5 fs		
Passband ripple					+/- 0.05	dB
Stopband			0.546 fs			
Stopband attenuation		f > 0.546 fs	85			dB
Group delay					1.5	ms

Test Conditions

DBVDD = CPVDD = AVDD = 1.8V, MICVDD = 2.2V, DCVDD = 1.2V, SPKVDD = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Bias (MICBIAS1, MICBIAS2) Note - No capacitor on MICBIASn Note - In regulator mode, it is required that V_{MICVDD} - $V_{MICBIAS}$ > 200mV						
Minimum Bias Voltage	$V_{MICBIAS}$	Regulator mode (MICBn_BYPASS=0) Load current ≤ 1.0mA		1.5		V
Maximum Bias Voltage				2.8		V
Bias Voltage output step size				0.1		V
Bias Voltage accuracy			-5%		+5%	V
Bias Current		Regulator mode (MICBn_BYPASS=0), V_{MICVDD} - $V_{MICBIAS}$ >200mV			2.4	mA
		Bypass mode (MICBn_BYPASS=1)			5.0	
Output Noise Density		Regulator mode (MICBn_BYPASS=0), MICBn_LVL = 4h, Load current = 1mA, Measured at 1kHz		40		nV/√Hz
Integrated noise voltage		Regulator mode (MICBn_BYPASS=0), MICBn_LVL = 4h, Load current = 1mA, 100Hz to 7kHz, A-weighted		2.5		µVrms
Power Supply Rejection Ratio (DBVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		100		dB
		100mV (peak-peak) 10kHz		80		
Power Supply Rejection Ratio (MICVDD)	PSRR	100mV (peak-peak) 217Hz		82		dB
		100mV (peak-peak) 10kHz		44		
Power Supply Rejection Ratio (DCVDD)	PSRR	100mV (peak-peak) 217Hz		102		dB
		100mV (peak-peak) 10kHz		94		
Power Supply Rejection Ratio (SPKVDD)	PSRR	100mV (peak-peak) 217Hz		99		dB
		100mV (peak-peak) 10kHz		92		
Load capacitance		Regulator mode (MICBn_BYPASS=0), MICBn_EXT_CAP=0			50	pF
		Regulator mode (MICBn_BYPASS=0), MICBn_EXT_CAP=1	1.8	4.7		µF
Output discharge resistance		MICBn_ENA=0, MICBn_DISCH=1		2		kΩ
Frequency Locked Loop (FLL1, FLL2)						
Output frequency			39		156	MHz
Lock Time		F_{REF} = 32kHz, F_{OUT} = 147.456MHz		10		ms
		F_{REF} = 12MHz, F_{OUT} = 147.456MHz		1		
RESET pin Input						
RESET input pulse width (To trigger a Hardware Reset, the RESET input must be asserted for longer than this duration)			1			µs

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

Device Reset Thresholds						
AVDD Reset Threshold	V_{AVDD}	V_{AVDD} rising			1.56	V
		V_{AVDD} falling	0.92		1.55	
DCVDD Reset Threshold	V_{DCVDD}	V_{DCVDD} rising			1.04	V
		V_{DCVDD} falling	0.49		0.64	
DBVDD Reset Threshold	V_{DBVDD}	V_{DBVDD} rising			1.54	V
		V_{DBVDD} falling	0.58		1.52	
Note that the reset thresholds are derived from simulations only, across all operational and process corners. Device performance is not assured outside the voltage ranges defined in the “Recommended Operating Conditions” section. Refer to this section for the CS47L24 power-up sequencing requirements.						

TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is a measure of the difference in level between the maximum full scale output signal and the output with no input signal applied. (Note that this is measured without any mute function enabled.)
2. Total Harmonic Distortion (dB) – THD is the ratio of the RMS sum of the harmonic distortion products in the specified bandwidth (see note below) relative to the RMS amplitude of the fundamental (i.e., test frequency) output.
3. Total Harmonic Distortion plus Noise (dB) – THD+N is the ratio of the RMS sum of the harmonic distortion products plus noise in the specified bandwidth (see note below) relative to the RMS amplitude of the fundamental (i.e., test frequency) output.
4. Power Supply Rejection Ratio (dB) - PSRR is the ratio of a specified power supply variation relative to the output signal that results from it. PSRR is measured under quiescent signal path conditions.
5. Common Mode Rejection Ratio (dB) – CMRR is the ratio of a specified input signal (applied to both sides of a differential input), relative to the output signal that results from it.
6. Channel Separation (L/R) (dB) – left-to-right and right-to-left channel separation is the difference in level between the active channel (driven to maximum full scale output) and the measured signal level in the idle channel at the test signal frequency. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel.
7. Multi-Path Crosstalk (dB) – is the difference in level between the output of the active path and the measured signal level in the idle path at the test signal frequency. The active path is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the specified idle path.
8. Mute Attenuation – This is a measure of the difference in level between the full scale output signal and the output with mute applied.
9. All performance measurements are specified with a 20kHz low pass ‘brick-wall’ filter and, where noted, an A-weighted filter. Failure to use these filters will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low pass filter removes out-of-band noise.

TYPICAL PERFORMANCE

TYPICAL POWER CONSUMPTION

Test Conditions:

DCVDD = 1.2V, DBVDD = MICVDD = CPVDD = AVDD = 1.8V, SPKVDD = 4.2V,
SYSCLK = 12.288MHz (direct MCLK1 input), T_A = +25ºC.

OPERATING MODE	TEST CONDITIONS	SUPPLY CURRENT (1.2V)	SUPPLY CURRENT (1.8V)	SUPPLY CURRENT (4.2V)	TOTAL POWER
Music Playback to Headphone					
AIF1 to DAC to HPOUT (stereo), fs=48kHz, 24-bit I2S, Slave mode, Load = 32Ω, eDRE enabled.	Quiescent	1.54mA	0.75mA	0.0mA	3.19mW
	1kHz sine wave, P_O=10mW	1.59mA	38.2mA	0.0mA	70.6mW
Music Playback to Speaker					
AIF1 to DAC to SPKOUT, fs=48kHz, 24-bit I2S, Slave mode, Load = 8Ω, 22µH, BTL, eDRE enabled	Quiescent	1.26mA	0.08mA	0.00mA	1.65mW
	1kHz sine wave, P_O=700mW	1.28mA	1.03mA	197mA	833mW
Full Duplex Speakerphone Voice Call					
Digital Mic to AIF1 (out), AIF (in) to DAC to SPKOUT, fs=8kHz, 16-bit I2S, Slave mode. MEMS microphone powered from 1.8V MICBIAS output (regulator bypass mode enabled). DMICCLK = 3.072MHz. Speaker load = 8Ω, BTL.	Quiescent	0.77mA	1.28mA	1.29mA	8.63mW
Stereo Line Record					
Digital Mic to AIF1, fs=48kHz, 24-bit I2S, Slave mode. MEMS microphone powered from 1.8V MICBIAS output (regulator bypass mode enabled). DMICCLK = 3.072MHz.	1kHz sine wave, -1dBFS out	1.2mA	1.5mA	0.0mA	4.1mW
Off					
Leakage current only, all clocks disabled, thermal protection disabled, DSP firmware memory disabled.		0.04mA	0.00mA	0.00mA	0.06mW

TYPICAL SIGNAL LATENCY

OPERATING MODE	TEST CONDITIONS			LATENCY
	INPUT	OUTPUT	DIGITAL CORE	
AIF to DAC Stereo Path				
Digital input (AIFn) to analogue output (HPOUT). Signal is routed via the digital core ASRC function in the asynchronous test cases only.	fs = 48kHz	fs = 48kHz	Synchronous	358µs
	fs = 44.1kHz	fs = 44.1kHz	Synchronous	391µs
	fs = 16kHz	fs = 16kHz	Synchronous	720µs
	fs = 8kHz	fs = 8kHz	Synchronous	1428µs
	fs = 8kHz	fs = 44.1kHz	Asynchronous	1940µs
	fs = 16kHz	fs = 44.1kHz	Asynchronous	1240µs
DMIC to AIF Stereo Path				
Digital input (INn) to digital output (AIFn). Digital core High Pass filter included in signal path.	fs = 48kHz	fs = 48kHz	Synchronous	236µs
	fs = 44.1kHz	fs = 44.1kHz	Synchronous	260µs
	fs = 16kHz	fs = 16kHz	Synchronous	732µs
	fs = 8kHz	fs = 8kHz	Synchronous	1543µs

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK & FREQUENCY LOCKED LOOP (FLL)

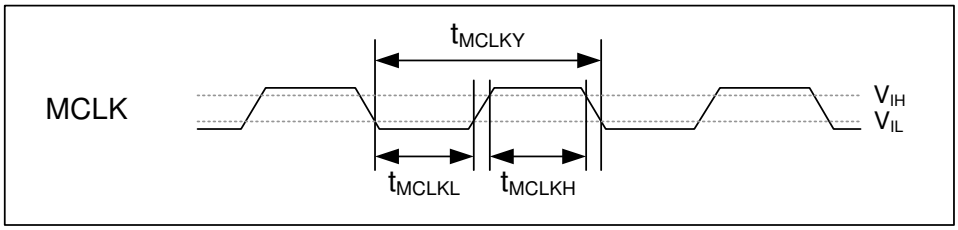


Figure 1 Master Clock Timing

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Master Clock Timing (MCLK1, MCLK2)					
MCLK cycle time	MCLK as input to FLL, FLLn_REFCLK_DIV=00	74			ns
	MCLK as input to FLL, FLLn_REFCLK_DIV=01	37			
	MCLK as input to FLL, FLLn_REFCLK_DIV=10	18			
	MCLK as input to FLL, FLLn_REFCLK_DIV=11	12.5			
	MCLK as direct SYSCLK or ASYNCCLK source	40			
MCLK duty cycle	MCLK as input to FLL	80:20		20:80	%
	MCLK as direct SYSCLK or ASYNCCLK source	60:40		40:60	
Frequency Locked Loops (FLL1, FLL2)					
FLL input frequency	FLLn_REFCLK_DIV=00	0.032		13.5	MHz
	FLLn_REFCLK_DIV=01	0.064		27	
	FLLn_REFCLK_DIV=10	0.128		54	
	FLLn_REFCLK_DIV=11	0.256		80	
FLL synchroniser input frequency	FLLn_SYNCCLK_DIV=00	0.032		13.5	MHz
	FLLn_SYNCCLK_DIV=01	0.064		27	
	FLLn_SYNCCLK_DIV=10	0.128		54	
	FLLn_SYNCCLK_DIV=11	0.256		80	

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal Clocking					
SYSCLK frequency	SYSCLK_FREQ=000, SYSCLK_FRAC=0	-1%	6.144	+1%	MHz
	SYSCLK_FREQ=000, SYSCLK_FRAC=1	-1%	5.6448	+1%	
	SYSCLK_FREQ=001, SYSCLK_FRAC=0	-1%	12.288	+1%	
	SYSCLK_FREQ=001, SYSCLK_FRAC=1	-1%	11.2896	+1%	
	SYSCLK_FREQ=010, SYSCLK_FRAC=0	-1%	24.576	+1%	
	SYSCLK_FREQ=010, SYSCLK_FRAC=1	-1%	22.5792	+1%	
	SYSCLK_FREQ=011, SYSCLK_FRAC=0	-1%	49.152	+1%	
	SYSCLK_FREQ=011, SYSCLK_FRAC=1	-1%	45.1584	+1%	
	SYSCLK_FREQ=100, SYSCLK_FRAC=0	-1%	73.728	+1%	
	SYSCLK_FREQ=100, SYSCLK_FRAC=1	-1%	67.7376	+1%	
	SYSCLK_FREQ=101, SYSCLK_FRAC=0	-1%	98.304	+1%	
	SYSCLK_FREQ=101, SYSCLK_FRAC=1	-1%	90.3168	+1%	
	SYSCLK_FREQ=110, SYSCLK_FRAC=0	-1%	147.456	+1%	
	SYSCLK_FREQ=110, SYSCLK_FRAC=1	-1%	135.4752	+1%	
ASYNCCLK frequency	ASYNC_CLK_FREQ=000	-1%	6.144	+1%	MHz
		-1%	5.6448	+1%	
	ASYNC_CLK_FREQ=001	-1%	12.288	+1%	
		-1%	11.2896	+1%	
	ASYNC_CLK_FREQ=010	-1%	24.576	+1%	
		-1%	22.5792	+1%	
	ASYNC_CLK_FREQ=011	-1%	49.152	+1%	
		-1%	45.1584	+1%	

Note:

When MCLK1 or MCLK2 is selected as a source for SYSCLK or ASYNCCLK (either directly or via one of the FLLs), the frequency must be within 1% of the applicable SYSCLK_FREQ or ASYNCCLK_FREQ register setting.

AUDIO INTERFACE TIMING

DIGITAL MICROPHONE (DMIC) INTERFACE TIMING

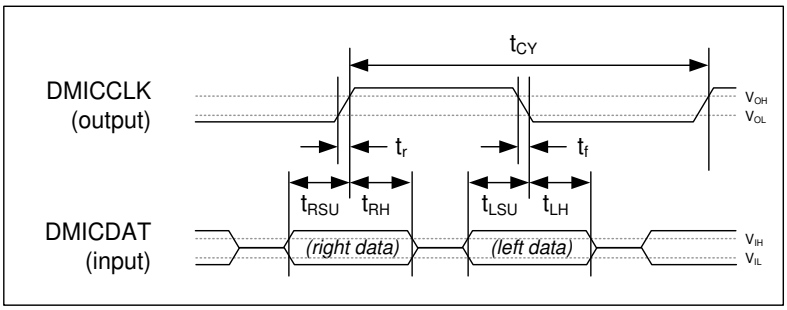


Figure 2 Digital Microphone Interface Timing

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital Microphone Interface Timing					
DMICCLKn cycle time	t_{CY}	160	163	1432	ns
DMICCLKn duty cycle		45		55	%
DMICCLKn rise/fall time (25pF load, 1.8V supply - see note)	t_r, t_f	5		30	ns
DMICDATn (Left) setup time to falling DMICCLK edge	t_{LSU}	15			ns
DMICDATn (Left) hold time from falling DMICCLK edge	t_{LH}	0			ns
DMICDATn (Right) setup time to rising DMICCLK edge	t_{RSU}	15			ns
DMICDATn (Right) hold time from rising DMICCLK edge	t_{RH}	0			ns

Notes:

DMICDATn and DMICCLKn are each referenced to a selectable supply, V_{SUP}.

The applicable supply is selected using the INn_DMIC_SUP registers.

DIGITAL AUDIO INTERFACE - MASTER MODE

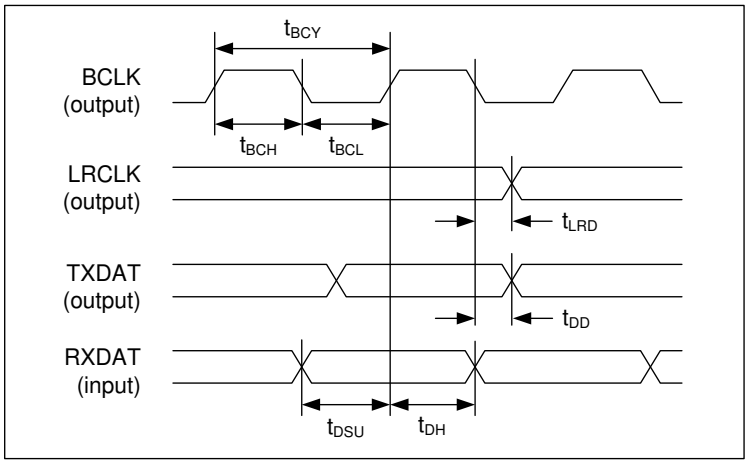


Figure 3 Audio Interface Timing - Master Mode

Note that BCLK and LRCLK outputs can be inverted if required; Figure 3 shows the default, non-inverted polarity.

Test Conditions

The following timing information is valid across the full range of recommended operating conditions, unless otherwise noted.
C_{LOAD} = 15pF to 25pF (output pins). BCLK slew (10% to 90%) = 3.7ns to 5.6ns.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing - Master Mode					
AIFnBCLK cycle time	t_{BCY}	40			ns
AIFnBCLK pulse width high	t_{BCH}	18			ns
AIFnBCLK pulse width low	t_{BCL}	18			ns
AIFn[TX/RX]LRCLK propagation delay from BCLK falling edge	t_{LRD}	0		8.3	ns
AIFnTXDAT propagation delay from BCLK falling edge	t_{DD}	0		5	ns
AIFnRXDAT setup time to BCLK rising edge	t_{DSU}	9.2			ns
AIFnRXDAT hold time from BCLK rising edge	t_{DH}	0			ns
Audio Interface Timing - Master Mode, Slave LRCLK					
AIFnLRCLK setup time to BCLK rising edge	t_{LRSU}	14			ns
AIFnLRCLK hold time from BCLK rising edge	t_{LRH}	0			ns

Note:

The descriptions above assume non-inverted polarity of AIFnBCLK.