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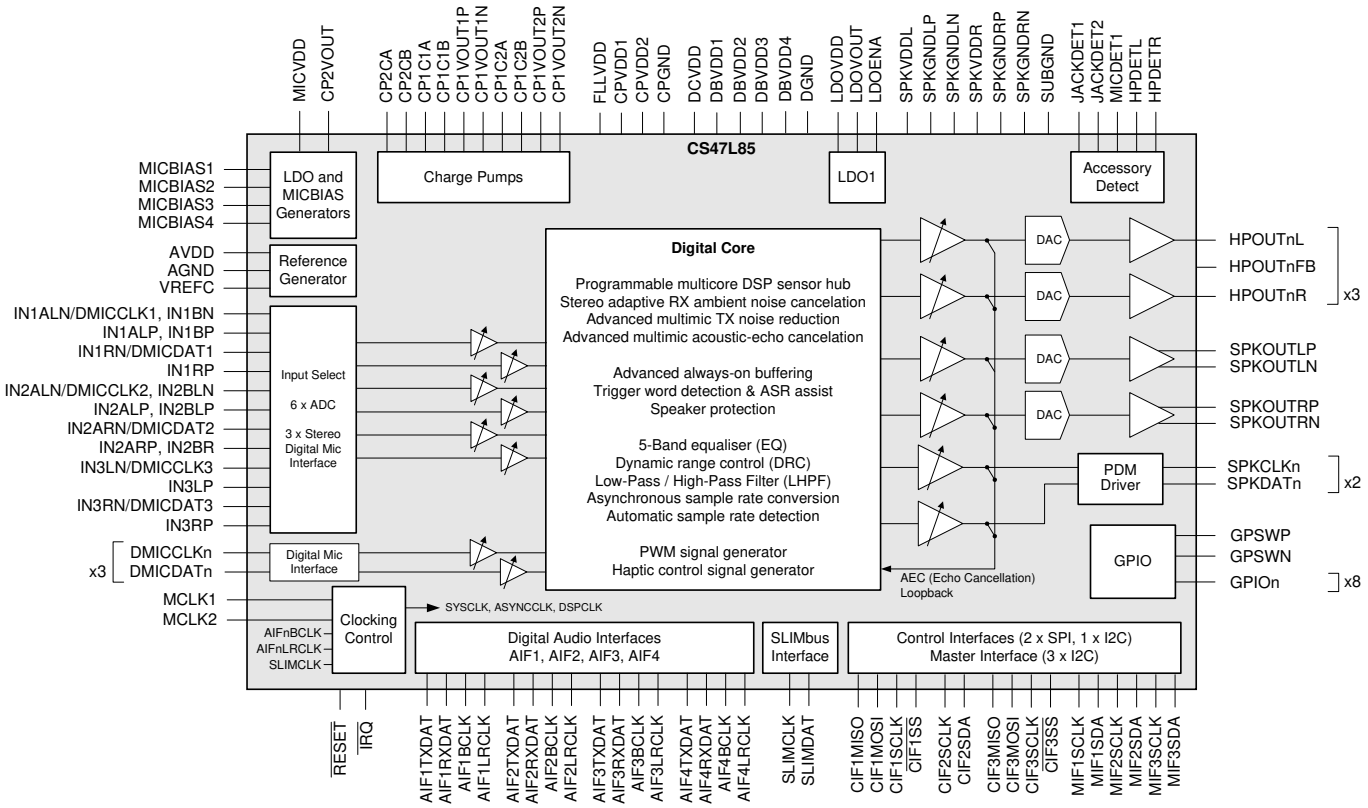
Low-Power Smart Codec with Seven DSP Cores, Voice and Media Enhancement, and Integrated Sensor Hub

Features

- 900 MIPS, 900MMAC multicore audio-signal processor
- Sensor hub capability, with event time-stamp functions
- Programmable wideband, multimic audio processing
  - — Cirrus Logic® adaptive ambient noise cancelation
  - — Transmit-path noise reduction and echo cancelation
  - — Wind noise, sidetone, and other programmable filters
- Multichannel asynchronous sample rate conversion
- Integrated multichannel 24-bit hi-fi audio hub codec
  - — Six ADCs, 100-dB SNR mic input (48 kHz)
  - — Eight DACs, 121-dB SNR headphone playback (48 kHz)
- Up to 9 analog or 12 digital microphone inputs
- Multipurpose headphone/earpiece/line output drivers
  - — 30 mW into 32-Ω load at 0.1% THD+N
- Class D speaker, and digital (PDM) output interfaces
- SLIMbus® audio and control interface
- Four full digital audio interfaces
  - — Standard sample rates from 8 to 192 kHz
  - — Multichannel TDM support on AIF1 and AIF2
- Flexible clocking, derived from MCLKn, AIFn, or SLIMbus
- Low-power frequency-locked loops (FLLs) support reference clocks down to 32 kHz
- Configurable functions on up to 40 GPIO pins
- Integrated regulators and charge pumps
- Small W-CSP package, 0.4-mm staggered ball array

Applications

- Smartphones and multimedia handsets
- Tablets and Mobile Internet Devices (MIDs)



Description

The CS47L85 is a highly integrated, low-power audio and sensor hub system for smartphones, tablets and other portable audio devices. It combines an advanced DSP feature set with a flexible, high-performance audio hub codec. The CS47L85 combines seven programmable DSP cores with a variety of power-efficient fixed-function audio processors. Extensive GPIO and I^2C master interfaces enable powerful sensor fusion functions to be integrated.

The DSP cores support multiple concurrent audio features, including multimic wideband noise reduction, high-performance acoustic-echo cancellation (AEC), stereo ambient noise cancellation (ANC), speech enhancement, advanced media enhancement, and many more. The CS47L85 sensor hub technology enables applications to support increased contextual awareness, including advanced motion sensing and pedestrian navigation functionality. The DSP cores are supported by a fully flexible, all-digital mixing and routing engine with sample rate converters, for wide use-case flexibility. Support for third-party DSP programming provides far-reaching opportunities for product differentiation.

A SLIMbus interface supports multi-channel audio paths and host control register access. Four further digital audio interfaces are provided, each supporting a wide range of standard audio sample rates and serial interface formats. Automatic sample rate detection enables seamless wideband/narrowband voice-call handover.

Three stereo headphone drivers each provide stereo ground-referenced or mono BTL outputs. 121dB SNR, and noise levels as low as 0.8 µVRMS, offer hi-fi quality line or headphone output. The CS47L85 also features a stereo pair of 2.5-W Class D outputs, four channels of stereo PDM output, and an IEC-60958-3–compatible S/PDIF transmitter. A signal generator for controlling haptics devices is included; vibe actuators can connect directly to the Class D speaker output or via an external driver on the PDM output interface. All inputs, outputs, and system interfaces can function concurrently.

The CS47L85 supports up to 9 analog inputs, and up to 12 PDM digital inputs. Microphone activity detection with interrupt is available. A smart accessory interface supports most standard 3.5mm accessories. Impedance sensing and measurement is provided for external accessory and push-button detection.

The CS47L85 is configured using the SLIMbus, SPI™, or I^2C interfaces. Three integrated FLLs provide support for a wide range of system clock frequencies. The device is powered from 1.8- and 1.2-V supplies. (A separate 4.2-V battery supply is typically required for the Class D speaker drivers). The power, clocking and output driver architectures are all designed to maximise battery life in voice, music and standby modes. Low-power (10µA) ‘Sleep’ is supported, with configurable wake-up events.

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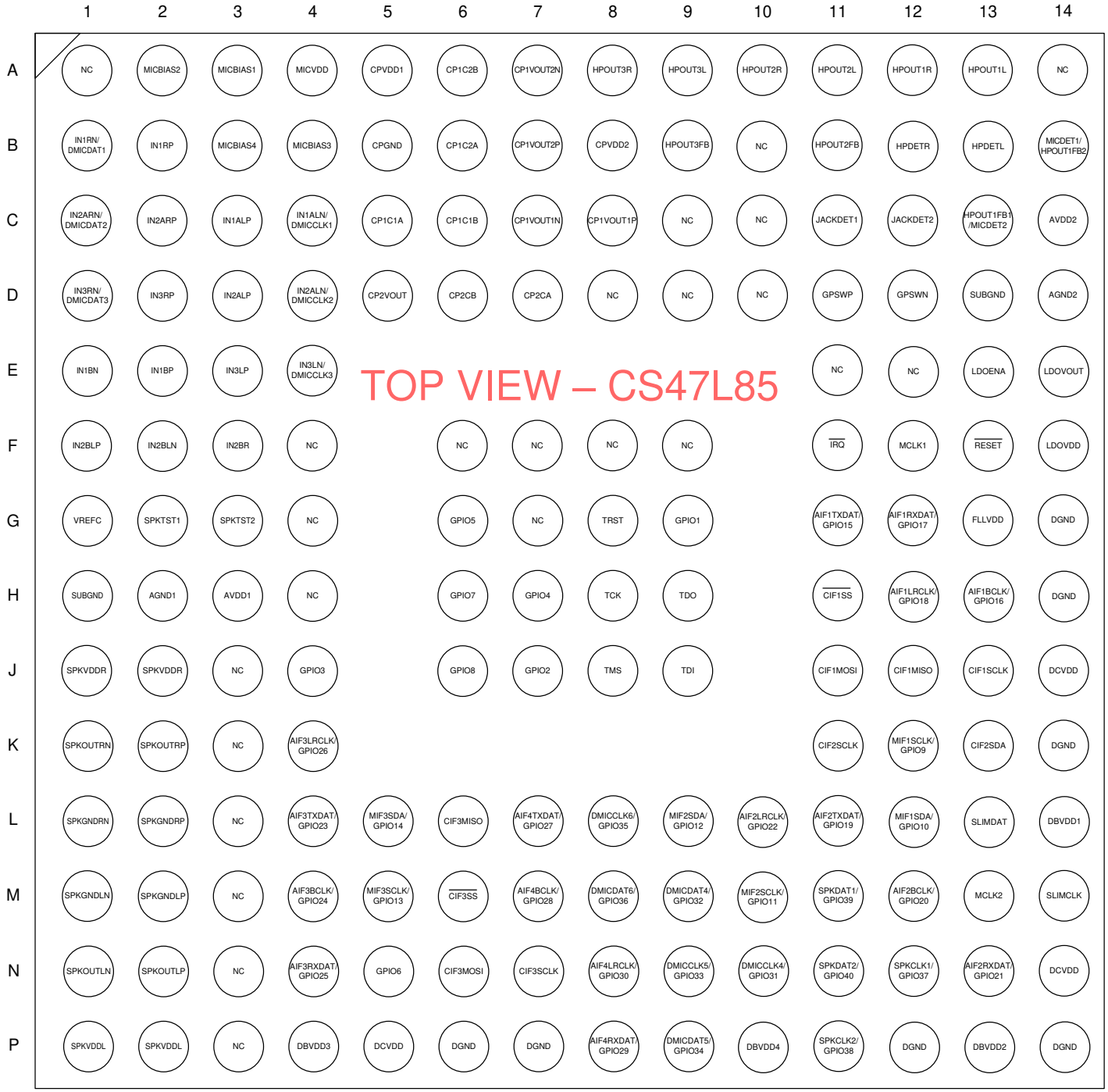
PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
CS47L85-CWZR	-40°C to +85°C	W-CSP (Pb-free, Tape and reel)	MSL1	260°C

Note:
Reel quantity = 4500

PIN DESCRIPTION

A description of each pin on the CS47L85 is provided below.
Note that a table detailing the associated power domain for every input and output pin is provided on the following page.
Note that, where multiple pins share a common name, these pins should be tied together on the PCB.
All Digital Output pins are CMOS outputs, unless otherwise stated.

PIN NO	NAME	TYPE	DESCRIPTION
H2	AGND1	Supply	Analogue ground (Return path for AVDD1)
D14	AGND2	Supply	Analogue ground (Return path for AVDD2)
H13	AIF1BCLK/ GPIO16	Digital Input / Output	Audio interface 1 bit clock / GPIO16. GPIO output is selectable CMOS or Open Drain; BCLK output is CMOS.
H12	AIF1LRCLK/ GPIO18	Digital Input / Output	Audio interface 1 left / right clock / GPIO18. GPIO output is selectable CMOS or Open Drain; LRCLK output is CMOS.
G12	AIF1RXDAT/ GPIO17	Digital Input / Output	Audio interface 1 RX digital audio data / GPIO17. GPIO output is selectable CMOS or Open Drain.
G11	AIF1TXDAT/ GPIO15	Digital Input / Output	Audio interface 1 TX digital audio data / GPIO15. GPIO output is selectable CMOS or Open Drain; TXDAT output is CMOS.
M12	AIF2BCLK/ GPIO20	Digital Input / Output	Audio interface 2 bit clock / GPIO20. GPIO output is selectable CMOS or Open Drain; BCLK output is CMOS.
L10	AIF2LRCLK/ GPIO22	Digital Input / Output	Audio interface 2 left / right clock / GPIO22. GPIO output is selectable CMOS or Open Drain; LRCLK output is CMOS.
N13	AIF2RXDAT/ GPIO21	Digital Input / Output	Audio interface 2 RX digital audio data / GPIO21. GPIO output is selectable CMOS or Open Drain.
L11	AIF2TXDAT/ GPIO19	Digital Input / Output	Audio interface 2 TX digital audio data / GPIO19. GPIO output is selectable CMOS or Open Drain; TXDAT output is CMOS.
M4	AIF3BCLK/ GPIO24	Digital Input / Output	Audio interface 3 bit clock / GPIO24. GPIO output is selectable CMOS or Open Drain; BCLK output is CMOS.
K4	AIF3LRCLK/ GPIO26	Digital Input / Output	Audio interface 3 left / right clock / GPIO26. GPIO output is selectable CMOS or Open Drain; LRCLK output is CMOS.
N4	AIF3RXDAT/GPIO25	Digital Input / Output	Audio interface 3 RX digital audio data / GPIO25. GPIO output is selectable CMOS or Open Drain.
L4	AIF3TXDAT/GPIO23	Digital Input / Output	Audio interface 3 TX digital audio data / GPIO23. GPIO output is selectable CMOS or Open Drain; TXDAT output is CMOS.
M7	AIF4BCLK/ GPIO28	Digital Input / Output	Audio interface 4 bit clock / GPIO28. GPIO output is selectable CMOS or Open Drain; BCLK output is CMOS.
N8	AIF4LRCLK/ GPIO30	Digital Input / Output	Audio interface 4 left / right clock / GPIO30. GPIO output is selectable CMOS or Open Drain; LRCLK output is CMOS.

PIN NO	NAME	TYPE	DESCRIPTION
P8	AIF4RXDAT/ GPIO29	Digital Input / Output	Audio interface 4 RX digital audio data / GPIO29. GPIO output is selectable CMOS or Open Drain.
L7	AIF4TXDAT/ GPIO27	Digital Input / Output	Audio interface 4 TX digital audio data / GPIO27. GPIO output is selectable CMOS or Open Drain; TXDAT output is CMOS.
H3	AVDD1	Supply	Analogue supply
C14	AVDD2	Supply	Analogue supply
J12	CIF1MISO	Digital Output	Control interface 1 (SPI) Master In Slave Out data. The CIFMISO is high impedance when C1F1SS is not asserted.
J11	CIF1MOSI	Digital Input	Control interface 1 (SPI) Master Out Slave In data
J13	CIF1SCLK	Digital Input	Control interface 1 (SPI) clock input
H11	C1F1SS	Digital Input	Control interface 1 (SPI) Slave Select (SS)
K11	CIF2SCLK	Digital Input	Control interface 2 (I2C) clock input
K13	CIF2SDA	Digital Input / Output	Control interface 2 (I2C) data input and output. The SDA output is Open Drain.
L6	CIF3MISO	Digital Output	Control interface 3 (SPI) Master In Slave Out data. The CIFMISO is high impedance when C1F3SS is not asserted.
N6	CIF3MOSI	Digital Input	Control interface 3 (SPI) Master Out Slave In data
N7	CIF3SCLK	Digital Input	Control interface 3 (SPI) clock input
M6	C1F3SS	Digital Input	Control interface 3 (SPI) Slave Select (SS)
C5	CP1C1A	Analogue Output	Charge pump 1 fly-back capacitor 1 pin
C6	CP1C1B	Analogue Output	Charge pump 1 fly-back capacitor 1 pin
B6	CP1C2A	Analogue Output	Charge pump 1 fly-back capacitor 2 pin
A6	CP1C2B	Analogue Output	Charge pump 1 fly-back capacitor 2 pin
C7	CP1VOUT1N	Analogue Output	Charge pump 1 negative output 1 decoupling pin
C8	CP1VOUT1P	Analogue Output	Charge pump 1 positive output 1 decoupling pin
A7	CP1VOUT2N	Analogue Output	Charge pump 1 negative output 2 decoupling pin
B7	CP1VOUT2P	Analogue Output	Charge pump 1 positive output 2 decoupling pin
D7	CP2CA	Analogue Output	Charge pump 2 fly-back capacitor pin
D6	CP2CB	Analogue Output	Charge pump 2 fly-back capacitor pin
D5	CP2VOUT	Analogue Output	Charge pump 2 output decoupling pin / Supply for LDO2
B5	CPGND	Supply	Charge pump ground (Return path for CPVDD1, CPVDD2)
A5	CPVDD1	Supply	Supply for Charge Pumps 1 & 2
B8	CPVDD2	Supply	Secondary supply for Charge Pump 1
L14	DBVDD1	Supply	Digital buffer (I/O) supply (core functions, AIF1, CIF1, CIF2, SLIMbus, MIF1, GPIO1)
P13	DBVDD2	Supply	Digital buffer (I/O) supply (AIF2, PDM, MIF2, MCLK2, GPIO2, JTAG)
P4	DBVDD3	Supply	Digital buffer (I/O) supply (AIF3, AIF4, CIF3, MIF3, GPIO3-8)
P10	DBVDD4	Supply	Digital buffer (I/O) supply (DMIC4, DMIC5, DMIC6)
J14, N14, P5	DCVDD	Supply	Digital core supply
G14, H14, K14, P6, P7, P12, P14	DGND	Supply	Digital ground (Return path for DCVDDn and DBVDDn)
N10	DMICCLK4/ GPIO31	Digital Input / Output	Digital MIC clock output 4 / GPIO31. GPIO output is selectable CMOS or Open Drain; DMICCLK output is CMOS.
M9	DMICDAT4/ GPIO32	Digital Input / Output	Digital MIC data input 4 / GPIO32. GPIO output is selectable CMOS or Open Drain.
N9	DMICCLK5/ GPIO33	Digital Input / Output	Digital MIC clock output 5 / GPIO33. GPIO output is selectable CMOS or Open Drain; DMICCLK output is CMOS.
P9	DMICDAT5/ GPIO34	Digital Input / Output	Digital MIC data input 5 / GPIO34. GPIO output is selectable CMOS or Open Drain.

PIN NO	NAME	TYPE	DESCRIPTION
L8	DMICCLK6/ GPIO35	Digital Input / Output	Digital MIC clock output 6 / GPIO35. GPIO output is selectable CMOS or Open Drain; DMICCLK output is CMOS.
M8	DMICDAT6/ GPIO36	Digital Input / Output	Digital MIC data input 6 / GPIO36. GPIO output is selectable CMOS or Open Drain.
G13	FLLVDD	Supply	Analogue supply (FLL1, FLL2)
G9	GPIO1	Digital Input / Output	General Purpose pin GPIO1. The output configuration is selectable CMOS or Open Drain.
J7	GPIO2	Digital Input / Output	General Purpose pin GPIO2. The output configuration is selectable CMOS or Open Drain.
J4	GPIO3	Digital Input / Output	General Purpose pin GPIO3. The output configuration is selectable CMOS or Open Drain.
H7	GPIO4	Digital Input / Output	General Purpose pin GPIO4. The output configuration is selectable CMOS or Open Drain.
G6	GPIO5	Digital Input / Output	General Purpose pin GPIO5. The output configuration is selectable CMOS or Open Drain.
N5	GPIO6	Digital Input / Output	General Purpose pin GPIO6. The output configuration is selectable CMOS or Open Drain.
H6	GPIO7	Digital Input / Output	General Purpose pin GPIO7. The output configuration is selectable CMOS or Open Drain.
J6	GPIO8	Digital Input / Output	General Purpose pin GPIO8. The output configuration is selectable CMOS or Open Drain.
D11	GPSWP	Analogue Input / Output	General Purpose bi-directional switch contact
D12	GPSWN	Analogue Input / Output	General Purpose bi-directional switch contact
B13	HPDETL	Analogue Input	Headphone left (HPOUT1L) sense input
B12	HPDETR	Analogue Input	Headphone right (HPOUT1R) sense input
C13	HPOUT1FB1/ MICDET2	Analogue Input	HPOUT1L and HPOUT1R ground feedback pin 1/ Microphone & accessory sense input 2
A13	HPOUT1L	Analogue Output	Left headphone 1 output
A12	HPOUT1R	Analogue Output	Right headphone 1 output
B11	HPOUT2FB	Analogue Input	HPOUT2L and HPOUT2R ground loop noise rejection feedback
A11	HPOUT2L	Analogue Output	Left headphone 2 output
A10	HPOUT2R	Analogue Output	Right headphone 2 output
B9	HPOUT3FB	Analogue Input	HPOUT3L and HPOUT3R ground loop noise rejection feedback
A9	HPOUT3L	Analogue Output	Left headphone 3 output
A8	HPOUT3R	Analogue Output	Right headphone 3 output
C4	IN1ALN/ DMICCLK1	Analogue Input / Digital Output	Left channel negative differential Mic/Line input / Digital MIC clock output 1
C3	IN1ALP	Analogue Input	Left channel single-ended Mic/Line input / Left channel positive differential Mic/Line input
E1	IN1BN	Analogue Input	Negative differential Mic/Line input. Also suitable for connection to external accessory interfaces.
E2	IN1BP	Analogue Input	Single-ended Mic/Line input / Positive differential Mic/Line input. Also suitable for connection to external accessory interfaces.
B1	IN1RN/ DMICDAT1	Analogue input / Digital Input	Right channel negative differential Mic/Line input / Digital MIC data input 1
B2	IN1RP	Analogue Input	Right channel single-ended Mic/Line input / Right channel positive differential Mic/Line input
D4	IN2ALN/ DMICCLK2	Analogue Input / Digital Output	Left channel negative differential Mic/Line input / Digital MIC clock output 2
D3	IN2ALP	Analogue Input	Left channel single-ended Mic/Line input / Left channel positive differential Mic/Line input
C1	IN2ARN/ DMICDAT2	Analogue input / Digital Input	Right channel negative differential Mic/Line input / Digital MIC data input 2

PIN NO	NAME	TYPE	DESCRIPTION
C2	IN2ARP	Analogue Input	Right channel single-ended Mic/Line input / Right channel positive differential Mic/Line input
F2	IN2BLN	Analogue Input	Left channel negative differential Mic/Line input. Also suitable for connection to external accessory interfaces.
F1	IN2BLP	Analogue Input	Left channel single-ended Mic/Line input / Left channel positive differential Mic/Line input. Also suitable for connection to external accessory interfaces.
F3	IN2BR	Analogue Input	Right channel single-ended Mic/Line input. Also suitable for connection to external accessory interfaces.
E4	IN3LN/ DMICCLK3	Analogue Input / Digital Output	Left channel negative differential Mic/Line input / Digital MIC clock output 3
E3	IN3LP	Analogue Input	Left channel single-ended Mic/Line input / Left channel positive differential Mic/Line input
D1	IN3RN/ DMICDAT3	Analogue input / Digital Input	Right channel negative differential Mic/Line input / Digital MIC data input 3
D2	IN3RP	Analogue Input	Right channel single-ended Mic/Line input / Right channel positive differential Mic/Line input
F11	IRQ	Digital Output	Interrupt Request (IRQ) output (default is active low). The pin configuration is selectable CMOS or Open Drain.
C11	JACKDET1	Analogue Input	Jack detect input 1
C12	JACKDET2	Analogue Input	Jack detect input 2
E13	LDOENA	Digital Input	Enable pin for LDO1 (generates DCVDD supply). Logic 1 input enables LDO1. If using external DCVDD supply, then LDO1 is not used, and LDOENA must be held at logic 0.
F14	LDOVDD	Supply	Supply for LDO1
E14	LDOVOUT	Analogue Output	LDO1 output. If using external DCVDD, then LDOVOUT must be left floating.
F12	MCLK1	Digital Input	Master clock 1
M13	MCLK2	Digital Input	Master clock 2
A3	MICBIAS1	Analogue Output	Microphone bias 1
A2	MICBIAS2	Analogue Output	Microphone bias 2
B4	MICBIAS3	Analogue Output	Microphone bias 3
B3	MICBIAS4	Analogue Output	Microphone bias 4
B14	MICDET1/ HPOUT1FB2	Analogue Input	Microphone & accessory sense input 1/ HPOUT1L and HPOUT1R ground feedback pin 2
A4	MICVDD	Analogue Output	LDO2 output decoupling pin (generated internally by CS47L85). (Can also be used as reference/supply for external microphones.)
K12	MIF1SCLK/ GPIO9	Digital Input / Output	Master (I2C) Interface 1 clock output / GPIO9. GPIO output is selectable CMOS or Open Drain; SCLK output is Open Drain.
L12	MIF1SDA/ GPIO10	Digital Input / Output	Master (I2C) Interface 1 data input and output / GPIO10. GPIO output is selectable CMOS or Open Drain; SDA output is Open Drain.
M10	MIF2SCLK/ GPIO11	Digital Input / Output	Master (I2C) Interface 2 clock output / GPIO11. GPIO output is selectable CMOS or Open Drain; SCLK output is Open Drain.
L9	MIF2SDA/ GPIO12	Digital Input / Output	Master (I2C) Interface 2 data input and output / GPIO12. GPIO output is selectable CMOS or Open Drain; SDA output is Open Drain.
M5	MIF3SCLK/ GPIO13	Digital Input / Output	Master (I2C) Interface 3 clock output / GPIO13. GPIO output is selectable CMOS or Open Drain; SCLK output is Open Drain.
L5	MIF3SDA/ GPIO14	Digital Input / Output	Master (I2C) Interface 3 data input and output / GPIO14. GPIO output is selectable CMOS or Open Drain; SDA output is Open Drain.
F13	$\overline{\text{RESET}}$	Digital Input	Digital Reset input (active low)
M14	SLIMCLK	Digital Input / Output	SLIM Bus Clock input / output

PIN NO	NAME	TYPE	DESCRIPTION
L13	SLIMDAT	Digital Input / Output	SLIM Bus Data input / output
N12	SPKCLK1/ GPIO37	Digital Input / Output	Digital speaker (PDM) 1 clock output / GPIO37. GPIO output is selectable CMOS or Open Drain; SPKCCLK output is CMOS.
M11	SPKDAT1/ GPIO39	Digital Input / Output	Digital speaker (PDM) 1 data output / GPIO39. GPIO output is selectable CMOS or Open Drain; SPKDAT output is CMOS.
P11	SPKCLK2/ GPIO38	Digital Input / Output	Digital speaker (PDM) 2 clock output / GPIO38. GPIO output is selectable CMOS or Open Drain; SPKCLK output is CMOS.
N11	SPKDAT2/ GPIO40	Digital Input / Output	Digital speaker (PDM) 2 data output / GPIO40. GPIO output is selectable CMOS or Open Drain; SPKDAT output is CMOS.
M1	SPKGNDLN	Supply	Left speaker driver ground (Return path for SPKVDDL). See note.
M2	SPKGNDLP	Supply	Left speaker driver ground (Return path for SPKVDDL). See note.
L1	SPKGNDRN	Supply	Right speaker driver ground (Return path for SPKVDDR). See note.
L2	SPKGNDRP	Supply	Right speaker driver ground (Return path for SPKVDDR). See note.
N1	SPKOUTLN	Analogue Output	Left speaker negative output
N2	SPKOUTLP	Analogue Output	Left speaker positive output
K1	SPKOUTRN	Analogue Output	Right speaker negative output
K2	SPKOUTRP	Analogue Output	Right speaker positive output
G2	SPKTST1	Analogue Output	Test function (recommend no external connection)
G3	SPKTST2	Analogue Output	Test function (recommend no external connection)
P1, P2	SPKVDDL	Supply	Left speaker driver supply
J1, J2	SPKVDDR	Supply	Right speaker driver supply
D13, H1	SUBGND	Supply	Substrate ground
H8	TCK	Digital Input	JTAG clock input. Internal pull-down holds this pin at logic 0 for normal operation.
J9	TDI	Digital Input	JTAG data input. Internal pull-down holds this pin at logic 0 for normal operation.
H9	TDO	Digital Output	JTAG data output
J8	TMS	Digital Input	JTAG mode select input. Internal pull-down holds this pin at logic 0 for normal operation.
G8	TRST	Digital Input	JTAG Test Access Port reset (active low). Internal pull-down holds this pin at logic 0 for normal operation. External connection to DGND is recommended, if the JTAG interface function is not required.
G1	VREFC	Analogue Output	Bandgap reference external capacitor connection

Note:

Separate P/N ground connections are provided for each speaker driver channel; this provides flexible support for current monitoring and output protection circuits. If this option is not used, then the respective ground connections should be tied together on the PCB.

The following table identifies the power domain and ground reference associated with each of the input / output pins.

PIN NO	NAME	POWER DOMAIN	GROUND DOMAIN
H13	AIF1BCLK/GPIO16	DBVDD1	DGND
H12	AIF1LRCLK/GPIO18	DBVDD1	DGND
G12	AIF1RXDAT/GPIO17	DBVDD1	DGND
G11	AIF1TXDAT/GPIO15	DBVDD1	DGND
M12	AIF2BCLK/GPIO20	DBVDD2	DGND
L10	AIF2LRCLK/GPIO22	DBVDD2	DGND
N13	AIF2RXDAT/GPIO21	DBVDD2	DGND
L11	AIF2TXDAT/GPIO19	DBVDD2	DGND
M4	AIF3BCLK/GPIO24	DBVDD3	DGND
K4	AIF3LRCLK/GPIO26	DBVDD3	DGND
N4	AIF3RXDAT/GPIO25	DBVDD3	DGND
L4	AIF3TXDAT/GPIO23	DBVDD3	DGND
M7	AIF4BCLK/GPIO28	DBVDD3	DGND
N8	AIF4LRCLK/GPIO30	DBVDD3	DGND
P8	AIF4RXDAT/GPIO29	DBVDD3	DGND
L7	AIF4TXDAT/GPIO27	DBVDD3	DGND
J12	CIF1MISO	DBVDD1	DGND
J11	CIF1MOSI	DBVDD1	DGND
J13	CIF1SCLK	DBVDD1	DGND
H11	CIF1SS	DBVDD1	DGND
K11	CIF2SCLK	DBVDD1	DGND
K13	CIF2SDA	DBVDD1	DGND
L6	CIF3MISO	DBVDD3	DGND
N6	CIF3MOSI	DBVDD3	DGND
N7	CIF3SCLK	DBVDD3	DGND
M6	CIF3SS	DBVDD3	DGND
N10	DMICCLK4/GPIO31	DBVDD4	DGND
N9	DMICCLK5/GPIO33	DBVDD4	DGND
L8	DMICCLK6/GPIO35	DBVDD4	DGND
M9	DMICDAT4/GPIO32	DBVDD4	DGND
P9	DMICDAT5/GPIO34	DBVDD4	DGND
M8	DMICDAT6/GPIO36	DBVDD4	DGND
G9	GPIO1	DBVDD1	DGND
J7	GPIO2	DBVDD2	DGND
J4	GPIO3	DBVDD3	DGND
H7	GPIO4	DBVDD3	DGND
G6	GPIO5	DBVDD3	DGND
N5	GPIO6	DBVDD3	DGND
H6	GPIO7	DBVDD3	DGND
J6	GPIO8	DBVDD3	DGND
B13	HPDETL	AVDD	AGND
B12	HPDETR	AVDD	AGND
C4	IN1ALN/ DMICCLK1	MICVDD (analogue) / MICVDD, MICBIAS1, MICBIAS2, MICBIAS3 (digital) The DMICCLK1 power domain is selectable using IN1_DMIC_SUP	AGND
C3	IN1ALP	MICVDD	AGND
E1	IN1BN	MICVDD	AGND
E2	IN1BP	MICVDD	AGND
B1	IN1RN/ DMICDAT1	MICVDD (analogue) / MICVDD, MICBIAS1, MICBIAS2, MICBIAS3 (digital) The DMICDAT1 power domain is selectable using IN1_DMIC_SUP	AGND
B2	IN1RP	MICVDD	AGND

PIN NO	NAME	POWER DOMAIN	GROUND DOMAIN
D4	IN2ALN/ DMICCLK2	MICVDD (analogue) / MICVDD, MICBIAS1, MICBIAS2, MICBIAS3 (digital) The DMICCLK2 power domain is selectable using IN2_DMIC_SUP	AGND
D3	IN2ALP	MICVDD	AGND
C1	IN2ARN/ DMICDAT2	MICVDD (analogue) / MICVDD, MICBIAS1, MICBIAS2, MICBIAS3 (digital) The DMICDAT2 power domain is selectable using IN2_DMIC_SUP	AGND
C2	IN2ARP	MICVDD	AGND
F2	IN2BLN	MICVDD	AGND
F1	IN2BLP	MICVDD	AGND
F3	IN2BR	MICVDD	AGND
E4	IN3LN/ DMICCLK3	MICVDD (analogue) / MICVDD, MICBIAS1, MICBIAS2, MICBIAS3 (digital) The DMICCLK3 power domain is selectable using IN3_DMIC_SUP	AGND
E3	IN3LP	MICVDD	AGND
D1	IN3RN/ DMICDAT3	MICVDD (analogue) / MICVDD, MICBIAS1, MICBIAS2, MICBIAS3 (digital) The DMICDAT3 power domain is selectable using IN3_DMIC_SUP	AGND
D2	IN3RP	MICVDD	AGND
F11	IRQ	DBVDD1	DGND
C11	JACKDET1	AVDD	AGND
C12	JACKDET2	AVDD	AGND
E13	LDOENA	DBVDD1	DGND
F12	MCLK1	DBVDD1	DGND
M13	MCLK2	DBVDD2	DGND
K12	MIF1SCLK/GPIO9	DBVDD1	DGND
L12	MIF1SDA/GPIO10	DBVDD1	DGND
M10	MIF2SCLK/GPIO11	DBVDD2	DGND
L9	MIF2SDA/GPIO12	DBVDD2	DGND
M5	MIF3SCLK/GPIO13	DBVDD3	DGND
L5	MIF3SDA/GPIO14	DBVDD3	DGND
F13	RESET	DBVDD1	DGND
M14	SLIMCLK	DBVDD1	DGND
L13	SLIMDAT	DBVDD1	DGND
N12	SPKCLK1/GPIO37	DBVDD2	DGND
P11	SPKCLK2/GPIO38	DBVDD2	DGND
M11	SPKDAT1/GPIO39	DBVDD2	DGND
N11	SPKDAT2/GPIO40	DBVDD2	DGND
H8	TCK	DBVDD2	DGND
J9	TDI	DBVDD2	DGND
H9	TDO	DBVDD2	DGND
J8	TMS	DBVDD2	DGND
G8	TRST	DBVDD2	DGND

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Cirrus Logic tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages (DCVDD, FLLVDD)	-0.3V	1.6V
Supply voltages (CPVDD1, CPVDD2)	-0.3V	2.5V
Supply voltages (DBVDD1, DBVDD2, DBVDD3, DBVDD4, LDOVDD, AVDD, MICVDD)	-0.3V	5.0V
Supply voltages (SPKVDDL, SPKVDDR)	-0.3V	6.0V
Voltage range digital inputs (DBVDD1 domain)	SUBGND - 0.3V	DBVDD1 + 0.3V
Voltage range digital inputs (DBVDD2 domain)	SUBGND - 0.3V	DBVDD2 + 0.3V
Voltage range digital inputs (DBVDD3 domain)	SUBGND - 0.3V	DBVDD3 + 0.3V
Voltage range digital inputs (DMICDAT1, DMICDAT2, DMICDAT3)	SUBGND - 0.3V	MICVDD + 0.3V
Voltage range digital inputs (DMICDAT4, DMICDAT5, DMICDAT6)	SUBGND - 0.3V	DBVDD4 + 0.3V
Voltage range analogue inputs (IN1Axx, IN2Axx, IN3xx)	SUBGND - 0.3V	MICVDD + 0.3V
Voltage range analogue inputs (IN1Bx, IN2Bxx)	SUBGND - 0.9V	MICVDD + 0.3V
Voltage range analogue inputs (HPOUT1FB1, HPOUT1FB2, HPOUTnFB)	SUBGND - 0.3V	SUBGND + 0.3V
Voltage range analogue inputs (MICDETn)	SUBGND - 0.3V	MICVDD + 0.3V
Voltage range analogue inputs (JACKDET1, JACKDET2, HPDETL, HPDETR)	CP1VOUT2N - 0.3V	AVDD + 0.3V
Voltage range analogue inputs (GPSWP, GPSWN)	SUBGND - 0.3V	MICVDD + 0.3V
Ground (AGND, DGND, CPGND, SPKGNDL, SPKGNDR)	SUBGND - 0.3V	SUBGND + 0.3V
Operating temperature range, T_A	-40ºC	+85ºC
Operating junction temperature, T_J	-40ºC	+125ºC
Storage temperature after soldering	-65ºC	+150ºC

Notes:

1. The DCVDD and FLLVDD pins should be tied together. The associated power domain is referred to as DCVDD.
2. The AVDD1 and AVDD2 pins should be tied together. The associated power domain is referred to as AVDD.
3. The AGND1 and AGND2 pins should be tied together. The associated ground domain is referred to as AGND.
4. The HPOUT1FBn and MICDETn functions share common pins. The Absolute Maximum Rating varies according to the applicable function of each pin.
5. CP1VOUT2N is an internal supply, generated by the CS47L85 Charge Pump (CP1). The CP1VOUT2N voltage may vary between CPGND and -CPVDD.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital Core and FLL supply range See notes 3, 4, 5, 6, 7	DCVDD, FLLVDD	1.14	1.2	1.26	V
Digital supply range (I/O) See note 8	DBVDD1, DBVDD2, DBVDD3, DBVDD4	1.71		3.6	V
LDO supply range See note 3	LDOVDD	1.71	1.8	1.89	V
Charge Pump supply range	CPVDD1	1.71	1.8	1.89	V
	CPVDD2	1.14	1.2	1.26	V
Speaker supply range	SPKVDDL, SPKVDDR	2.4		5.5	V
Analogue supply range See notes 9, 10	AVDD	1.71	1.8	1.89	V
Analogue supply range (FLL) See note 4	FLLVDD	1.14	1.2	1.26	V
Microphone Bias supply See note 11	MICVDD	0.9	2.5	3.78	V
Ground See note 1	DGND, AGND, CPGND, SPKGNDL, SPKGNDR, SUBGND		0		V
Power supply rise time See notes 12 to 17	DCVDD	10		2000	µs
	LDOVDD	10		50000	
	All other supplies	10			
Operating temperature range	T_A	-40		85	°C

Notes:

1. The impedance between DGND, AGND, CPGND and SUBGND should be less than 0.1Ω. The impedance between SPKGNDL, SPKGNDR and SUBGND should be less than 0.2Ω.
2. There are no switch-on power sequencing requirements; the supplies may be enabled in any order.
3. When powering down the device, if DCVDD is powered using the internal LDO (LDO1), then the LDO must be disabled, or else $\overline{\text{RESET}}$ must be asserted (low), before the LDOVDD supply is removed. There are no other switch-off power sequencing requirements.
4. The DCVDD and FLLVDD pins should be tied together. The associated power domain is referred to as DCVDD.
5. An internal LDO (powered by LDOVDD) can be used to provide the DCVDD and FLLVDD supplies.
6. 'Sleep' mode is supported when DCVDD is below the limits noted, provided AVDD and DBVDD1 are present.
7. It is recommended to connect a 4.7Ω resistor in series with the FLLVDD pin connection. Note that the minimum voltage limit applies at the supply end of the 4.7Ω resistor in this case.
8. If the SLIMbus interface is enabled, then the maximum DBVDD1 voltage is 1.98V.
9. The AVDD1 and AVDD2 pins should be tied together. The associated power domain is referred to as AVDD.
10. The AGND1 and AGND2 pins should be tied together. The associated ground domain is referred to as AGND.
11. An internal Charge Pump and LDO (powered by CPVDD1) provide the Microphone Bias supply; the MICVDD pin should not be connected to an external supply.
12. DCVDD and MICVDD minimum rise times do not apply when these domains are powered using the internal LDOs.
13. If DCVDD is supplied externally, and the rise time exceeds 2ms, then $\overline{\text{RESET}}$ must be asserted (low) during the rise, and held asserted until after DCVDD is within the recommended operating limits.
14. LDOVDD maximum rise time does not apply when DCVDD is supplied externally.
15. If DCVDD is powered using the internal LDO (LDO1), and the LDOVDD rise time exceeds 50ms, then $\overline{\text{RESET}}$ must be asserted (low), or LDOENA held low, during the rise. One or both these signals must be held low until after LDOVDD is within the recommended operating limits.
16. The specified minimum power supply rise times assume a minimum decoupling capacitance of 100nF per pin. However, Cirrus Logic strongly advises that the recommended decoupling capacitors are present on the PCB and that appropriate layout guidelines are observed.
17. The specified minimum power supply rise times also assume a maximum PCB inductance of 10nH between decoupling capacitor and pin.

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD = 1.8V,

With the exception of the condition(s) noted above, the following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Input Signal Level (IN1AL, IN1BL, IN1R, IN2AL, IN2BL, IN2AR, IN2BR, IN3L, IN3R)						
Full-scale input signal level (0dBFS output)	V_{INFS}	Single-ended PGA input, 0dB PGA gain		0.5 -6		V_{RMS} dBV
		Differential PGA input, 0dB PGA gain		1 0		V_{RMS} dBV

Notes:

1. The full-scale input signal level is also the maximum analogue input level, before clipping occurs.
2. The full-scale input signal level changes in proportion with AVDD. For differential input, it is calculated as AVDD / 1.8.
3. A $1.0V_{RMS}$ differential signal equates to $0.5V_{RMS}$/-6dBV per input.
4. A sinusoidal input signal is assumed.

Test Conditions

T_A = +25°C

With the exception of the condition(s) noted above, the following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Input Pin Characteristics (IN1AL, IN1BL, IN1R, IN2AL, IN2BL, IN2AR, IN2BR, IN3L, IN3R)						
Input resistance	R_{IN}	Single-ended PGA input, All PGA gain settings	9	12		kΩ
		Differential PGA input, All PGA gain settings	18	24		
Input capacitance	C_{IN}				5	pF

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Programmable Gain Amplifiers (PGAs)						
Minimum programmable gain				0		dB
Maximum programmable gain				31		dB
Programmable gain step size		Guaranteed monotonic		1		dB

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Microphone Input Signal Level (DMICDAT1, DMICDAT2, DMICDAT3, DMICDAT4, DMICDAT5, DMICDAT6)						
Full-scale input signal level (0dBFS signal to digital core)		0dB gain		-6		dBFS

Notes:

1. The digital microphone input signal level is measured in dBFS, where 0dBFS is a signal level equal to the full-scale range (FSR) of the PDM input. The FSR is defined as the amplitude of a 1kHz sine wave whose positive and negative peaks are represented by the maximum and minimum digital codes respectively - this is the largest 1kHz sine wave that will fit in the digital output range without clipping.

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Line / Headphone / Earpiece Output Driver (HPOUTnL, HPOUTnR)						
Load resistance		Normal operation, Single-ended mode	6			Ω
		Normal operation, Differential (BTL) mode	15			
		Device survival with load applied indefinitely	0			
Load capacitance		Single-ended mode			500	pF
		Differential (BTL) mode			200	
Speaker Output Driver (SPKOUTLP+SPKOUTLN, SPKOUTRP+SPKOUTRN)						
Load resistance		Normal operation	4			Ω
		Device survival with load applied indefinitely	0			
Load capacitance					200	pF
Digital Speaker Output (SPKDAT1, SPKDAT2)						
Full-scale output level (0dBFS digital core output)		0dB gain		-6		dBFS

Notes:

1. The digital output signal level is measured in dBFS, where 0dBFS is a signal level equal to the full-scale range (FSR) of the PDM output. The FSR is defined as the amplitude of a 1kHz sine wave whose positive and negative peaks are represented by the maximum and minimum digital codes respectively - this is the largest 1kHz sine wave that will fit in the digital output range without clipping.

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = DBVDD4 = CPVDD1 = AVDD = LDOVDD = 1.8V, CPVDD2 = 1.2V,
DCVDD = FLLVDD = 1.2V (powered from LDO1), MICVDD = 2.5V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
TA = +25ºC, 1kHz sinusoid signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Line / Headphone / Earpiece Output Driver (HPOUTnL, HPOUTnR)						
DC offset at Load		Single-ended mode		100	100	µV
		Differential (BTL) mode		200		
Speaker Output Driver (SPKOUTLP+SPKOUTLN, SPKOUTRP+SPKOUTRN)						
DC offset at Load				3		mV
SPKVDD leakage current				1		µA

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = DBVDD4 = CPVDD1 = AVDD = LDOVDD = 1.8V, CPVDD2 = 1.2V,
DCVDD = FLLVDD = 1.2V (powered from LDO1), MICVDD = 2.5V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
TA = +25ºC, 1kHz sinusoid signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Input Paths (INnL, INnR) to ADC (Differential Input Mode)						
Signal to Noise Ratio (A-weighted)	SNR	48kHz sample rate	93	100		dB
		16kHz sample rate, (wideband voice)		106		
Total Harmonic Distortion	THD	-1dBV input		-89	-81	dB
Total Harmonic Distortion + Noise	THD+N	-1dBV input		-88		dB
Channel separation (Left/Right)		100Hz to 10kHz		100		dB
Input-referred noise floor		A-weighted, PGA gain = +20dB		3.2		μV_{RMS}
Common mode rejection ratio	CMRR	PGA gain = +30dB		80		dB
		PGA gain = 0dB		70		
PSRR (DBVDDn, LDOVDD, CPVDD1, AVDD)	PSRR	100mV (peak-peak) 217Hz		90		dB
		100mV (peak-peak) 10kHz		80		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		100		dB
		100mV (peak-peak) 10kHz		80		
Analogue Input Paths (INnLP, INnRP) to ADC (Single-Ended Input Mode)						
Signal to Noise Ratio (A-weighted)	SNR	48kHz sample rate	91	100		dB
		16kHz sample rate, (wideband voice)		102		
Total Harmonic Distortion	THD	-7dBV input		-85	-78	dB
Total Harmonic Distortion + Noise	THD+N	-7dBV input		-84		dB
Channel separation (Left/Right)		100Hz to 10kHz		100		dB
Input-referred noise floor		A-weighted, PGA gain = +20dB		4		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD1, AVDD)	PSRR	100mV (peak-peak) 217Hz		77		dB
		100mV (peak-peak) 10kHz		50		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		90		dB
		100mV (peak-peak) 10kHz		50		

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = DBVDD4 = CPVDD1 = AVDD = LDOVDD = 1.8V, CPVDD2 = 1.2V,
DCVDD = FLLVDD = 1.2V (powered from LDO1), MICVDD = 2.5V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
TA = +25ºC, 1kHz sinusoid signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Line Output (HPOUTnL, HPOUTnR; Load = 10kΩ, 50pF)						
Full-scale output signal level	V_{OUT}	0dBFS input		1 0		Vrms dBV
Signal to Noise Ratio	SNR	A-weighted, Output signal = 1Vrms		121		dB
Dynamic Range	DR	A-weighted, -60dBFS input	105	115		dB
Total Harmonic Distortion	THD	0dBFS input		-92	-84	dB
Total Harmonic Distortion + Noise	THD+N	0dBFS input		-91		dB
Channel separation (Left/Right)		100Hz to 10kHz		100		dB
Output noise floor		A-weighted		0.8		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD1, AVDD)	PSRR	100mV (peak-peak) 217Hz		90		dB
		100mV (peak-peak) 10kHz		72		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		110		dB
		100mV (peak-peak) 10kHz		110		
DAC to Headphone Output (HPOUTnL, HPOUTnR; R_L = 32Ω)						
Maximum output power	P_O	0.1% THD+N		32		mW
Signal to Noise Ratio	SNR	A-weighted, Output signal = 1Vrms		121		dB
Dynamic Range	DR	A-weighted, -60dBFS input	105	115		dB
Total Harmonic Distortion	THD	P_O = 20mW		-90		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 20mW		-89		dB
Total Harmonic Distortion	THD	P_O = 2mW		-91	-84	dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 2mW		-90		dB
Channel separation (Left/Right)		100Hz to 10kHz		94		dB
Output noise floor		A-weighted		0.8		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD1, AVDD)	PSRR	100mV (peak-peak) 217Hz		90		dB
		100mV (peak-peak) 10kHz		73		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		110		dB
		100mV (peak-peak) 10kHz		110		
DAC to Headphone Output (HPOUTnL, HPOUTnR; R_L = 16Ω)						
Maximum output power	P_O	0.1% THD+N		42		mW
Signal to Noise Ratio	SNR	A-weighted, Output signal = 1Vrms		121		dB
Dynamic Range	DR	A-weighted, -60dBFS input	105	115		dB
Total Harmonic Distortion	THD	P_O = 20mW		-90		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 20mW		-89		dB
Total Harmonic Distortion	THD	P_O = 2mW		-91	-84	dB
Total Harmonic Distortion + Noise	THD+N	P_O = 2mW		-90		dB
Channel separation (Left/Right)		100Hz to 10kHz		92		dB
Output noise floor		A-weighted		0.8		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD1, AVDD)	PSRR	100mV (peak-peak) 217Hz		90		dB
		100mV (peak-peak) 10kHz		73		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		110		dB
		100mV (peak-peak) 10kHz		110		

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = DBVDD4 = CPVDD1 = AVDD = LDOVDD = 1.8V, CPVDD2 = 1.2V,
DCVDD = FLLVDD = 1.2V (powered from LDO1), MICVDD = 2.5V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
TA = +25ºC, 1kHz sinusoid signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Earpiece Output (HPOUTnL, HPOUTnR, Mono Mode, R_L = 32Ω BTL)						
Maximum output power	P_O	0.1% THD+N		106		mW
Signal to Noise Ratio	SNR	A-weighted, Output signal = 1.41Vrms		127		dB
Dynamic Range	DR	A-weighted, -60dBFS input		119		dB
Total Harmonic Distortion	THD	P_O = 75mW		-92		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 75mW		-91		dB
Total Harmonic Distortion	THD	P_O = 5mW		-92		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 5mW		-91		dB
Output noise floor		A-weighted		0.7		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD1, AVDD)	PSRR	100mV (peak-peak) 217Hz		85		dB
		100mV (peak-peak) 10kHz		73		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		110		dB
		100mV (peak-peak) 10kHz		110		
DAC to Earpiece Output (HPOUTnL, HPOUTnR, Mono Mode, R_L = 16Ω BTL)						
Maximum output power	P_O	0.1% THD+N		106		mW
Signal to Noise Ratio	SNR	A-weighted, Output signal = 1.41Vrms		127		dB
Dynamic Range	DR	A-weighted, -60dBFS input		119		dB
Total Harmonic Distortion	THD	P_O = 75mW		-89		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 75mW		-88		dB
Total Harmonic Distortion	THD	P_O = 5mW		-90		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 5mW		-89		dB
Output noise floor		A-weighted		0.7		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD1, AVDD)	PSRR	100mV (peak-peak) 217Hz		85		dB
		100mV (peak-peak) 10kHz		73		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		110		dB
		100mV (peak-peak) 10kHz		110		

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = DBVDD4 = CPVDD1 = AVDD = LDOVDD = 1.8V, CPVDD2 = 1.2V,
DCVDD = FLLVDD = 1.2V (powered from LDO1), MICVDD = 2.5V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
TA = +25ºC, 1kHz sinusoid signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Speaker Output (SPKOUTLP+SPKOUTLN, SPKOUTRP+SPKOUTRN, Load = 8Ω, 22µH, BTL)						
Maximum output power	P_O	SPKVDD = 5.0V, 1% THD+N		1.4		W
		SPKVDD = 4.2V, 1% THD+N		1.0		
		SPKVDD = 3.6V, 1% THD+N		0.7		
Signal to Noise Ratio	SNR	A-weighted, Output signal = 2.83Vrms		127		dB
Dynamic Range	DR	A-weighted, -60dBFS input	90	101		dB
Total Harmonic Distortion	THD	P_O = 1.0W		-40		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 1.0W		-40		dB
Total Harmonic Distortion	THD	P_O = 0.5W		-70	-59	dB
Total Harmonic Distortion + Noise	THD+N	P_O = 0.5W		-69		dB
Channel separation (Left/Right)		100Hz to 10kHz		80		dB
Output noise floor		A-weighted		0.7		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD1, AVDD)	PSRR	100mV (peak-peak) 217Hz		100		dB
		100mV (peak-peak) 10kHz		80		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		100		dB
		100mV (peak-peak) 10kHz		95		
DAC to Speaker Output (SPKOUTLP+SPKOUTLN, SPKOUTRP+SPKOUTRN, Load = 4Ω, 15µH, BTL)						
Maximum output power	P_O	SPKVDD = 5.0V, 1% THD+N		2.5		W
		SPKVDD = 4.2V, 1% THD+N		1.8		
		SPKVDD = 3.6V, 1% THD+N		1.3		
Signal to Noise Ratio	SNR	A-weighted, Output signal = 2.83Vrms		127		dB
Dynamic Range	DR	A-weighted, -60dBFS input		95		dB
Total Harmonic Distortion	THD	P_O = 1.0W		-40		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 1.0W		-40		dB
Total Harmonic Distortion	THD	P_O = 0.5W		-70		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 0.5W		-69		dB
Channel separation (Left/Right)		100Hz to 10kHz		80		dB
Output noise floor		A-weighted		0.7		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD1, AVDD)	PSRR	100mV (peak-peak) 217Hz		100		dB
		100mV (peak-peak) 10kHz		80		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		100		dB
		100mV (peak-peak) 10kHz		95		

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input / Output (except DMICDAT1/2/3 and DMICCLK1/2/3) **Digital I/O is referenced to DBVDD1, DBVDD2, DBVDD3 or DBVDD4.**						
Input HIGH Level	V_{IH}	V_{DBVDD} = 1.71V to 1.98V	0.75 × V_{DBVDDn}			V
		V_{DBVDDn} = 2.5V ±10%	0.8 × V_{DBVDDn}			
		V_{DBVDDn} = 3.3V ±10%	0.7 × V_{DBVDDn}			
Input LOW Level	V_{IL}	V_{DBVDD} = 1.71V to 1.98V			0.3 × V_{DBVDDn}	V
		V_{DBVDDn} = 2.5V ±10%			0.25 × V_{DBVDDn}	
		V_{DBVDDn} = 3.3V ±10%			0.2 × V_{DBVDDn}	
Note that digital input pins should not be left unconnected or floating.						
Output HIGH Level (I_{OH} = 1mA)	V_{OH}	V_{DBVDD} = 1.71V to 1.98V	0.75 × V_{DBVDDn}			V
		V_{DBVDDn} = 2.5V ±10%	0.65 × V_{DBVDDn}			
		V_{DBVDDn} = 3.3V ±10%	0.7 × V_{DBVDDn}			
Output LOW Level (I_{OL} = 1mA)	V_{OL}	V_{DBVDD} = 1.71V to 1.98V			0.25 × V_{DBVDDn}	V
		V_{DBVDDn} = 2.5V ±10%			0.3 × V_{DBVDDn}	
		V_{DBVDDn} = 3.3V ±10%			0.15 × V_{DBVDDn}	
Input capacitance					5	pF
Input leakage			-10		10	µA
Pull-up / pull-down resistance (where applicable)			35		55	kΩ
Digital Microphone Input / Output (DMICDAT1/2/3 and DMICCLK1/2/3) **DMICDAT1/2/3 and DMICCLK1/2/3 are referenced to a selectable supply, V_{SUP}, according to the INn_DMIC_SUP registers**						
DMICDATn input HIGH Level	V_{IH}		0.65 × V_{SUP}			V
DMICDATn input LOW Level	V_{IL}				0.35 × V_{SUP}	V
DMICCLKn output HIGH Level	V_{OH}	I_{OH} = 1mA	0.8 × V_{SUP}			V
DMICCLKn output LOW Level	V_{OL}	I_{OL} = -1mA			0.2 × V_{SUP}	V
Input capacitance				25		pF
Input leakage			-1		1	µA
General Purpose Input / Output (GPIOn)						
Clock output frequency		GPIO pin configured as OPCLK or FLL output			50	MHz
General Purpose Switch The GPSWP pin should be positive-biased with respect to GPSWN. The GPSWN pin voltage must not exceed GPSWP + 0.3V.						
Switch resistance	$R_{DS(ON)}$	Switch closed, I=1mA		25	40	Ω
Switch resistance	$R_{DS(OFF)}$	Switch open		100		MΩ

Test Conditions

fs ≤ 48kHz

With the exception of the condition(s) noted above, the following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Decimation Filters						
Passband		+/- 0.05dB	0		0.454 fs	
		-6dB		0.5 fs		
Passband ripple					+/- 0.05	dB
Stopband			0.546 fs			
Stopband attenuation		f > 0.546 fs	85			dB
Group delay					2	ms
DAC Interpolation Filters						
Passband		+/- 0.05dB	0		0.454 fs	
		-6dB		0.5 fs		
Passband ripple					+/- 0.05	dB
Stopband			0.546 fs			
Stopband attenuation		f > 0.546 fs	85			dB
Group delay					1.5	ms

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = DBVDD4 = CPVDD1 = AVDD = LDOVDD = 1.8V, CPVDD2 = 1.2V
DCVDD = FLLVDD = 1.2V (powered from LDO1), MICVDD = 2.5V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Bias (MICBIAS1, MICBIAS2, MICBIAS3, MICBIAS4) Note - No capacitor on MICBIASn Note - In regulator mode, it is required that V_{MICVDD} - $V_{MICBIAS}$ > 200mV						
Minimum Bias Voltage	$V_{MICBIAS}$	Regulator mode (MICBn_BYPASS=0) Load current ≤ 1.0mA		1.5		V
Maximum Bias Voltage				2.8		V
Bias Voltage output step size				0.1		V
Bias Voltage accuracy			-5%		+5%	V
Bias Current		Regulator mode (MICBn_BYPASS=0), V_{MICVDD} - $V_{MICBIAS}$ >200mV			2.4	mA
		Bypass mode (MICBn_BYPASS=1)			5.0	
Output Noise Density		Regulator mode (MICBn_BYPASS=0), MICBn_LVL = 4h, Load current = 1mA, Measured at 1kHz		50		nV/√Hz
Integrated noise voltage		Regulator mode (MICBn_BYPASS=0), MICBn_LVL = 4h, Load current = 1mA, 100Hz to 7kHz, A-weighted		4		µVrms
Power Supply Rejection Ratio (DBVDDn, LDOVDD, CPVDD1, AVDD)	PSRR	100mV (peak-peak) 217Hz		90		dB
		100mV (peak-peak) 10kHz		80		
Load capacitance		Regulator mode (MICBn_BYPASS=0), MICBn_EXT_CAP=0			50	pF
		Regulator mode (MICBn_BYPASS=0), MICBn_EXT_CAP=1	1.8	4.7		µF
Output discharge resistance		MICBn_ENA=0, MICBn_DISCH=1		2		kΩ