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CS49300 Family DSP

Multi-Standard Audio Decoder Family

Features

- CS4930X: DVD Audio Sub-family
  - PES Layer decode for A/V sync
  - DVD Audio Pack Layer Support
  - Meridian Lossless Packing Specification (MLP)™
  - Dolby Digital™, Dolby Pro Logic II™
  - MPEG-2, Advanced Audio Coding Algorithm (AAC)
  - MPEG Multichannel
  - DTS Digital Surround™, DTS-ES Extended Surround™
- CS4931X: Broadcast Sub-family
  - PES Layer decode for A/V sync
  - Dolby Digital
  - MPEG-2, Advanced Audio Coding Algorithm (AAC)
  - MPEG-1 (Layers 1, 2, 3) Stereo
  - MPEG-2 (Layers 2, 3) Stereo
- CS4932X: AVR Sub-family
  - Dolby Digital, Dolby Pro Logic II
  - DTS & DTS-ES decoding with integrated DTS tables
  - Cirrus Original Surround 5.1 PCM Enhancement
  - MPEG-2, Advanced Audio Coding Algorithm (AAC)
  - MPEG Multichannel
  - MP3 (MPEG-1, Layer 3)
- CS49330: General Purpose Audio DSP
  - THX® Surround EX™ and THX® Ultra2 Cinema
  - General Purpose AVR and Broadcast Audio Decoder (MPEG Multichannel, MPEG Stereo, MP3, C.O.S.)
  - Car Audio
- Features are a super-set of the CS4923/4/5/6/7/8/9
  - 8 channel output, including dual zone output capability
  - Dynamic Channel Remapability
  - Supports up to 192 kHz Fs @ 24-bit throughput
  - Increased memory/MIPs
  - SRAM Interface for increased delay and buffer capability
  - Dual-Precision Bass Manager
  - Enhance your system functionality via firmware upgrades through the Crystal Ware™ Software Licensing Program

Description

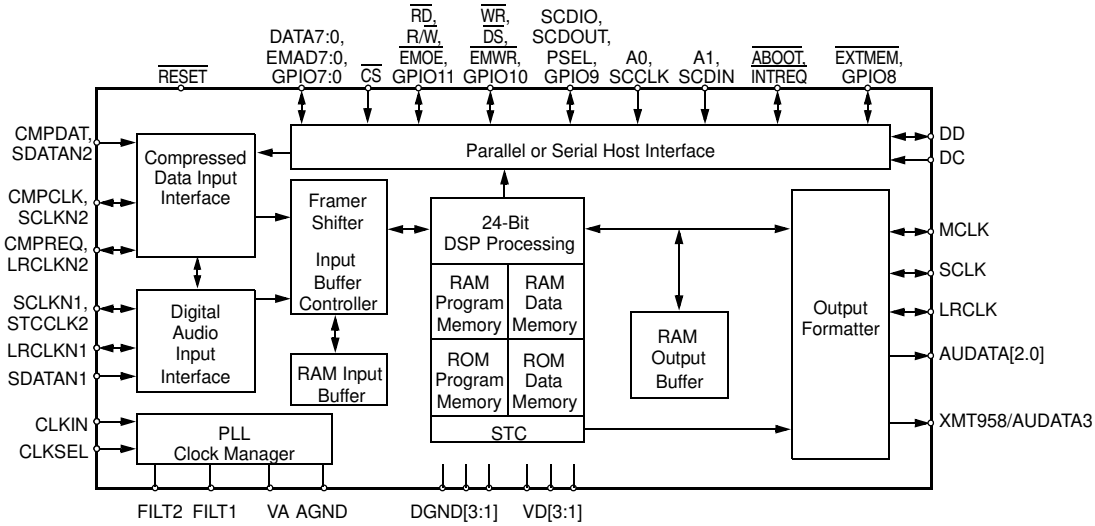
The CS493XX is a family of multichannel audio decoders intended to supersede the CS4923/4/5/6/7/8/9 family as the leader of audio decoding in both the DVD, broadcast and receiver markets. The family will be split into parts tailored for each of these distinct market segments.

For the DVD market, parts will be offered which support Meridian Lossless Packing (MLP), Dolby Digital, Dolby Pro Logic II, MPEG Multichannel, DTS Digital Surround, DTS-ES, AAC, and subsets thereof. For the receiver market, parts will be offered which support Dolby Digital, Dolby Pro Logic II, MPEG Multichannel, DTS Digital Surround, DTS-ES, AAC, and various virtualizers and PCM enhancement algorithms such as HDCD®, DTS Neo:6™, LOGIC7®, and SRS Circle Surround II®. For the broadcast market, parts will be offered which support Dolby Digital, AAC, MPEG-1, Layers 1,2 and 3, MPEG-2, Layers 2 and 3.

Under the Crystal brand, Cirrus Logic is the only single supplier of high-performance 24-bit multi-standard audio DSP decoders, DSP firmware, and high-resolution data converters. This combination of DSPs, system firmware, and data converters simplify rapid creation of world-class high-fidelity digital audio products for the Internet age.

Ordering Information: See page 87

	APPLICATION	CORE DECODER FUNCTIONALITY
CS49300	DVD Audio	MLP, AC-3, AAC, DTS, MPEG 5.1, MP3, etc.
CS49310	Broadcast	AAC, AC-3, MPEG Stereo, MP3, etc.
CS49311	Broadcast	AAC, MPEG Stereo, MP3, etc.
CS49312	Broadcast	AC-3, MPEG Stereo, MP3, etc.
CS49325	AVR	AC-3, COS, MPEG 5.1, MP3, etc.
CS49326	AVR	AC-3, DTS, COS, MPEG 5.1, MP3, etc.
CS49329	AVR	AC-3, AAC, DTS, MPEG 5.1, MP3, etc.
CS49330	Car Audio DSP	Car Audio Code
CS49330	General Purpose	MPEG 5.1, MPEG Stereo, MP3, C.O.S., etc
CS49330	Post-Processor	DPP, THX Surround EX, THX Ultra2 Cinema



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Contacting Cirrus Logic Support

For a complete listing of Direct Sales, Distributor, and Sales Representative contacts, visit the Cirrus Logic web site at:
http://www.cirrus.com

1. CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25°C.)

1.1. Specified Operating Conditions

(AGND, DGND = 0 V; all voltages with respect to 0 V)

Parameter		Symbol	Min	Typ	Max	Unit
DC power supplies:	Positive digital	VD	2.37	2.5	2.63	V
	Positive analog	VA	2.37	2.5	2.63	V
	||VA| – |VD||		-	-	0.3	V
Ambient operating temperature		T_A	0	-	70	°C

1.2. Absolute Maximum Ratings

(AGND, DGND = 0 V; all voltages with respect to 0 V)

Parameter		Symbol	Min	Max	Unit
DC power supplies:	Positive digital	VD	–0.3	2.75	V
	Positive analog	VA	–0.3	2.75	V
	||VA| – |VD||		-	0.3	V
Input current, any pin except supplies		I_{in}	-	±10	mA
Digital input voltage		V_{IND}	–0.3	3.63	V
Storage temperature		T_{stg}	–65	150	°C

CAUTION: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

1.3. Thermal Data

(VA, VD[3:1] = 2.5 V ±5%; measurements performed under operating conditions)

Parameter	Symbol	Min	Typ	Max	Unit
Thermal Resistance (Junction to Ambient)					
Two-layer Board (Note 1)	θ_{ja}	-	-	44.5	°C / Watt
Four-layer Board (Note 2)		-	-	36.3	
Thermal Resistance (Junction to Top of Package)					
Two-layer Board (Note 1)	ψ_{jt}	-	-	2.0	°C / Watt
Four-layer Board (Note 2)		-	-	3.8	

Notes:
1. Two-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-oz copper covering 20 % of the top & bottom layers.
2. Four-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-oz copper covering 20 % of the top & bottom layers and 0.5-oz copper covering 90 % of the internal power plane & ground plane layers.
3. To calculate the die temperature for a given power dissipation

   T_j = Ambient Temperature + [(Power Dissipation in Watts) * θ_{ja}]
4. To calculate the case temperature for a given power dissipation

   $T_c = T_j$ - [(Power Dissipation in Watts) * ψ_{jt}]

1.4. Digital D.C. Characteristics

(VA, VD[3:1] = 2.5 V ±5%; measurements performed under static conditions.)

Parameter	Symbol	Min	Typ	Max	Unit
High-level input voltage	V_{IH}	2.0	-	-	V
Low-level input voltage	V_{IL}	-	-	0.8	V
High-level output voltage at I_O = −2.0 mA	V_{OH}	VD × 0.9	-	-	V
Low-level output voltage at I_O = 2.0 mA	V_{OL}	-	-	VD × 0.11	V
Input leakage current	I_{in}	-	-	1.0	µA

1.5. Power Supply Characteristics

(VA, VD[3:1] = 2.5 V ±5%; measurements performed under operating conditions)

Parameter		Symbol	Min	Typ	Max	Unit
Power supply current:	Digital operating: VD[3:1]		-	200	310	mA
	Analog operating: VA		-	1.7	4	mA

1.6. Switching Characteristics — $\overline{\text{RESET}}$

(VA, VD[3:1] = 2.5 V ±5%; Inputs: Logic 0 = DGND, Logic 1 = VD, C_L = 20 pF)

Parameter		Symbol	Min	Max	Unit
$\overline{\text{RESET}}$ minimum pulse width low (-CL)	(Note 5)	T_{rstl}	100	-	µs
$\overline{\text{RESET}}$ minimum pulse width low (-IL)	(Note 5)	T_{rstl}	530	-	µs
All bidirectional pins high-Z after $\overline{\text{RESET}}$ low	(Note 6)	T_{rst2z}	-	100	ns
Configuration bits setup before $\overline{\text{RESET}}$ high		T_{rstsu}	50	-	ns
Configuration bits hold after $\overline{\text{RESET}}$ high		T_{rsthld}	15	-	ns

Notes: 5. The minimum $\overline{\text{RESET}}$ pulse listed above is valid only when using the recommended pull-up/pull-down resistors on the $\overline{\text{RD}}$, $\overline{\text{WR}}$, PSEL and $\overline{\text{ABOOT}}$ mode pins. For Rev. D and older parts, pull-up/pull-down resistors may be 4.7 k or 3.3 k. For Rev. E and newer parts, pull-up/pull-down resistors must be 3.3 k.

6. This specification is characterized but not production tested.

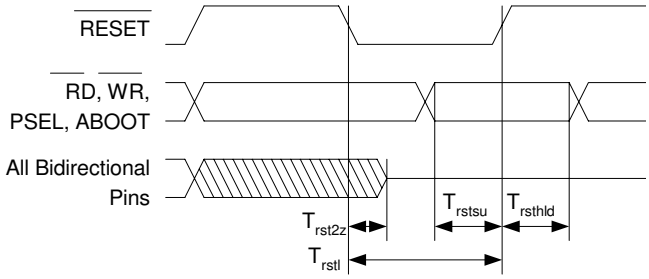


Figure 1. RESET Timing

1.7. Switching Characteristics — CLKIN

(VA, VD[3:1] = 2.5 V ±5%; Inputs: Logic 0 = DGND, Logic 1 = VD, C_L = 20 pF, PLL Enabled)

Parameter	Symbol	Min	Max	Unit
CLKIN period for internal DSP clock mode	T_{clki}	35	3800	ns
CLKIN high time for internal DSP clock mode	T_{clkih}	14	-	ns
CLKIN low time for internal DSP clock mode	T_{clkil}	14	-	ns

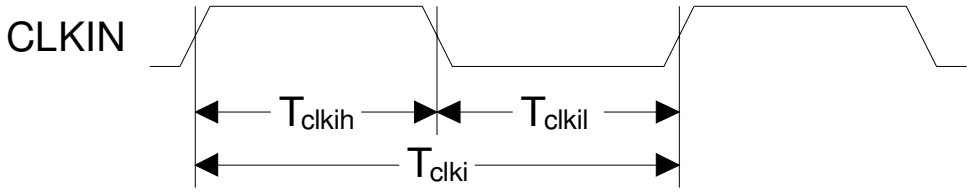


Figure 2. CLKIN with CLKSEL = VSS = PLL Enable

1.8. Switching Characteristics — Intel® Host Mode

(VA, VD[3:1] = 2.5 V ±5%; Inputs: Logic 0 = DGND, Logic 1 = VD, C_L = 20 pF)

Parameter		Symbol	Min	Max	Unit
Address setup before $\overline{CS}$ and $\overline{RD}$ low or $\overline{CS}$ and $\overline{WR}$ low		T_{ias}	5	-	ns
Address hold time after $\overline{CS}$ and $\overline{RD}$ low or $\overline{CS}$ and $\overline{WR}$ low		T_{iah}	5	-	ns
Delay between $\overline{RD}$ then $\overline{CS}$ low or $\overline{CS}$ then $\overline{RD}$ low		T_{icdr}	0	∞	ns
Data valid after $\overline{CS}$ and $\overline{RD}$ low	(Note 3)	T_{idd}	-	21	ns
$\overline{CS}$ and $\overline{RD}$ low for read	(Note 1)	T_{irpw}	DCLKP + 10	-	ns
Data hold time after $\overline{CS}$ or $\overline{RD}$ high		T_{idhr}	5	-	ns
Data high-Z after $\overline{CS}$ or $\overline{RD}$ high	(Note 2)	T_{idis}	-	22	ns
$\overline{CS}$ or $\overline{RD}$ high to $\overline{CS}$ and $\overline{RD}$ low for next read	(Note 1)	T_{ird}	2*DCLKP + 10	-	ns
$\overline{CS}$ or $\overline{RD}$ high to $\overline{CS}$ and $\overline{WR}$ low for next write	(Note 1)	T_{irdtw}	2*DCLKP + 10	-	ns
Delay between $\overline{WR}$ then $\overline{CS}$ low or $\overline{CS}$ then $\overline{WR}$ low		T_{icdw}	0	∞	ns
Data setup before $\overline{CS}$ or $\overline{WR}$ high		T_{idsu}	20	-	ns
$\overline{CS}$ and $\overline{WR}$ low for write	(Note 1)	T_{iwpw}	DCLKP + 10	-	ns
Data hold after $\overline{CS}$ or $\overline{WR}$ high		T_{idhw}	5	-	ns
$\overline{CS}$ or $\overline{WR}$ high to $\overline{CS}$ and $\overline{RD}$ low for next read	(Note 1)	T_{iwtrd}	2*DCLKP + 10	-	ns
$\overline{CS}$ or $\overline{WR}$ high to $\overline{CS}$ and $\overline{WR}$ low for next write	(Note 1)	T_{iwd}	2*DCLKP + 10	-	ns

Notes: 1. Certain timing parameters are normalized to the DSP clock, DCLKP, in nanoseconds. DCLKP = 1/DCLK. The DSP clock can be defined as follows:

External CLKIN Mode:
DCLK == CLKIN/4 before and during boot
DCLK == CLKIN after boot

Internal Clock Mode:
DCLK == 10MHz before and during boot, i.e. DCLKP == 100ns
DCLK == 65 MHz after boot, i.e. DCLKP == 15.4ns

It should be noted that DCLK for the internal clock mode is application specific. The application code users guide should be checked to confirm DCLK for the particular application.

2. This specification is characterized but not production tested. A 470 ohm pull-up resistor was used for characterization to minimize the effects of external bus capacitance.
3. See T_{idd} from Intel Host Mode in Table 6 on page 46

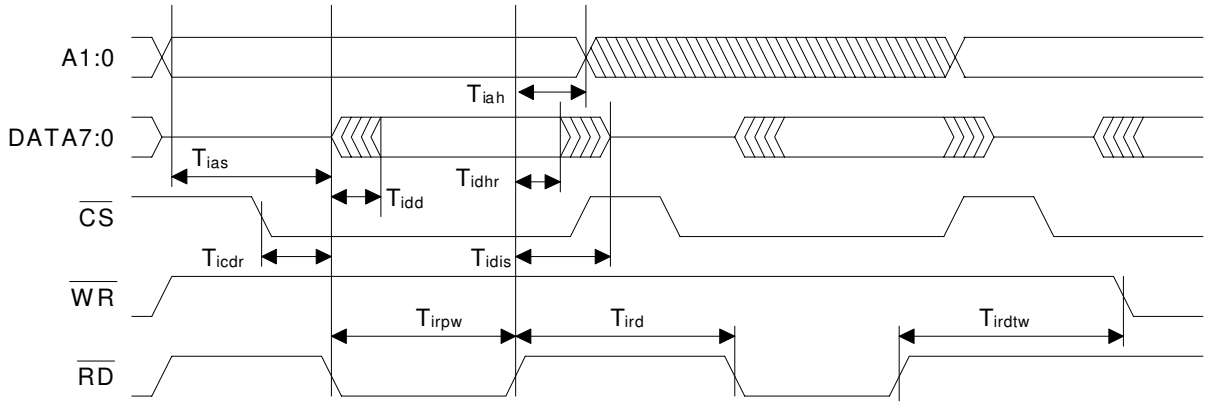


Figure 3. Intel® Parallel Host Mode Read Cycle

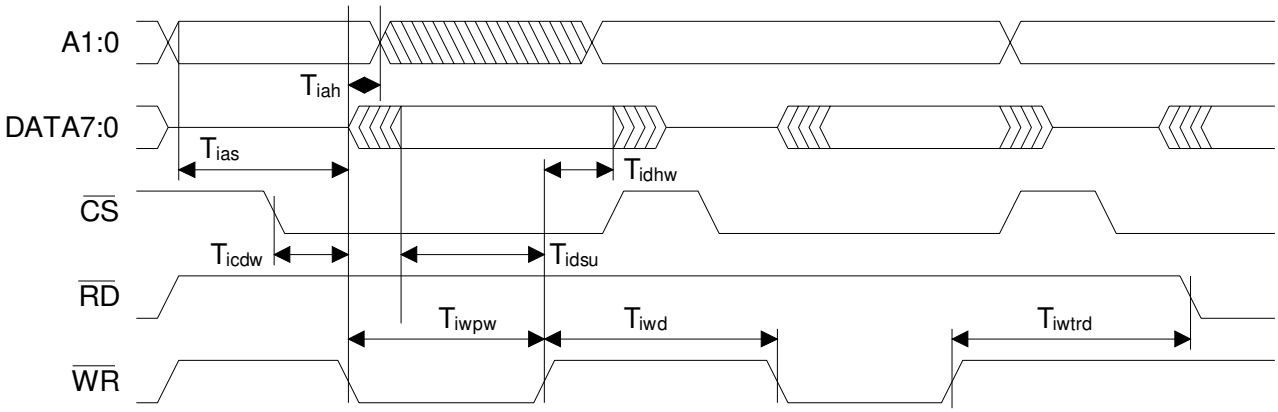


Figure 4. Intel® Parallel Host Mode Write Cycle

1.9. Switching Characteristics — Motorola® Host Mode

(VA, VD[3:1] = 2.5 V ±5%; Inputs: Logic 0 = DGND, Logic 1 = VD, C_L = 20 pF)

Parameter	Symbol	Min	Max	Unit
Address setup before $\overline{CS}$ and $\overline{DS}$ low	T_{mas}	5	-	ns
Address hold time after $\overline{CS}$ and $\overline{DS}$ low	T_{mah}	5	-	ns
Delay between $\overline{DS}$ then $\overline{CS}$ low or $\overline{CS}$ then $\overline{DS}$ low	T_{mcdr}	0	∞	ns
Data valid after $\overline{CS}$ and $\overline{DS}$ low with R/$\overline{W}$ high (Note 3)	T_{mdd}	-	21	ns
$\overline{CS}$ and $\overline{DS}$ low for read (Note 1)	T_{mrpw}	DCLKP + 10	-	ns
Data hold time after $\overline{CS}$ or $\overline{DS}$ high after read	T_{mdhr}	5	-	ns
Data high-Z after $\overline{CS}$ or $\overline{DS}$ high after read (Note 2)	T_{mdis}	-	22	ns
$\overline{CS}$ or $\overline{DS}$ high to $\overline{CS}$ and $\overline{DS}$ low for next read (Note 1)	T_{mrd}	2*DCLKP + 10	-	ns
$\overline{CS}$ or $\overline{DS}$ high to $\overline{CS}$ and $\overline{DS}$ low for next write (Note 1)	T_{mrdtw}	2*DCLKP + 10	-	ns
Delay between $\overline{DS}$ then $\overline{CS}$ low or $\overline{CS}$ then $\overline{DS}$ low	T_{mcdw}	0	∞	ns
Data setup before $\overline{CS}$ or $\overline{DS}$ high	T_{mdsu}	20	-	ns
$\overline{CS}$ and $\overline{DS}$ low for write (Note 1)	T_{mwpw}	DCLKP + 10	-	ns
R/$\overline{W}$ setup before $\overline{CS}$ AND $\overline{DS}$ low	T_{mrwsu}	5	-	ns
R/$\overline{W}$ hold time after $\overline{CS}$ or $\overline{DS}$ high	T_{mrwhld}	5	-	ns
Data hold after $\overline{CS}$ or $\overline{DS}$ high	T_{mdhw}	5	-	ns
$\overline{CS}$ or $\overline{DS}$ high to $\overline{CS}$ and $\overline{DS}$ low with R/$\overline{W}$ high for next read (Note 1)	T_{mwtrd}	2*DCLKP + 10	-	ns
$\overline{CS}$ or $\overline{DS}$ high to $\overline{CS}$ and $\overline{DS}$ low for next write (Note 1)	T_{mwd}	2*DCLKP + 10	-	ns

Notes: 1. Certain timing parameters are normalized to the DSP clock, DCLKP, in nanoseconds. DCLKP = 1/DCLK. The DSP clock can be defined as follows:

External CLKIN Mode:
DCLK == CLKIN/4 before and during boot
DCLK == CLKIN after boot

Internal Clock Mode:
DCLK == 10MHz before and during boot, i.e. DCLKP == 100ns
DCLK == 65 MHz after boot, i.e. DCLKP == 15.4ns

It should be noted that DCLK for the internal clock mode is application specific. The application code users guide should be checked to confirm DCLK for the particular application.

2. This specification is characterized but not production tested. A 470 ohm pull-up resistor was used for characterization to minimize the effects of external bus capacitance.
3. See T_{mdd} from Motorola Host Mode in Table 7 on page 47

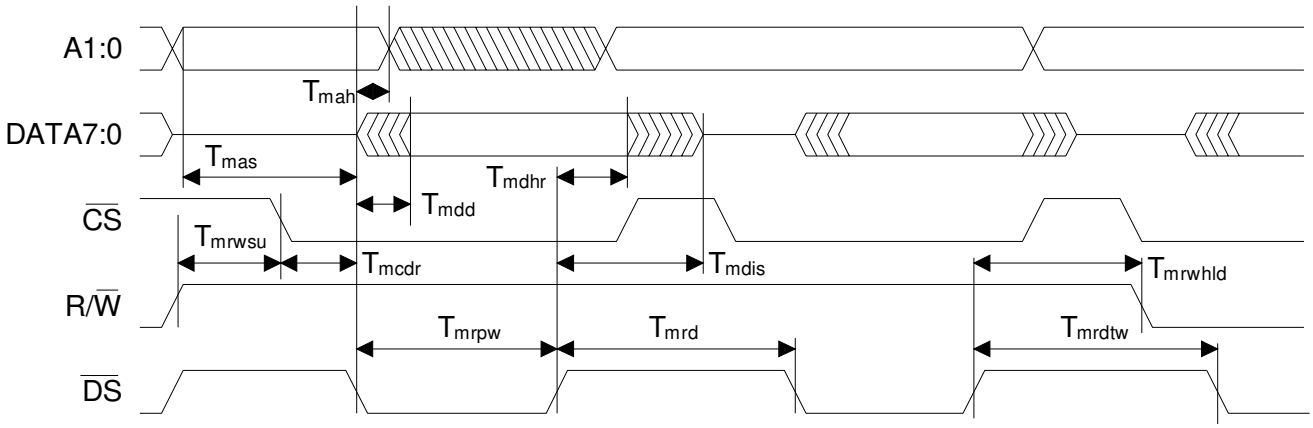


Figure 5. Motorola® Parallel Host Mode Read Cycle

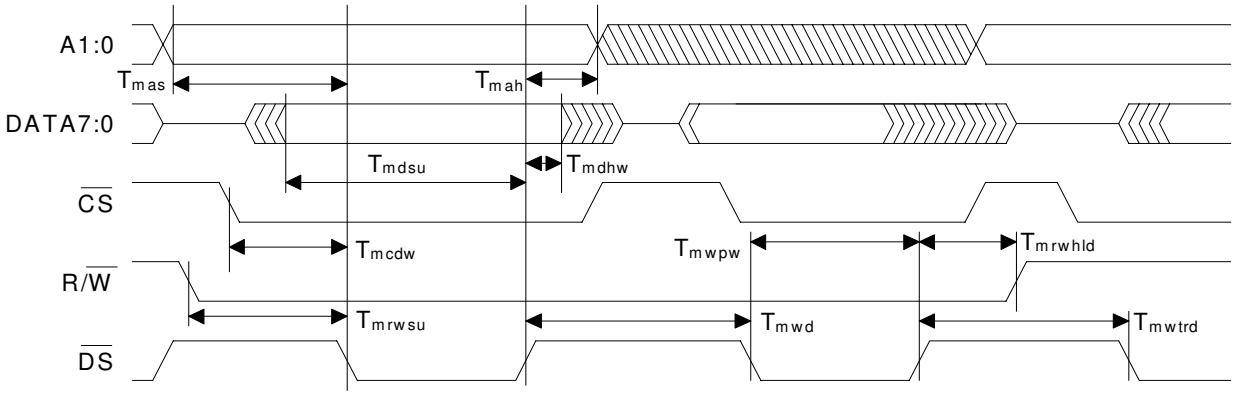


Figure 6. Motorola® Parallel Host Mode Write Cycle

1.10. Switching Characteristics — SPI™ Control Port

(VA, VD[3:1] = 2.5 V ±5%; Inputs: Logic 0 = DGND, Logic 1 = VD, C_L = 20 pF)

Parameter		Symbol	Min	Max	Units
SCCLK clock frequency	(Note 1)	f_{sck}	-	2000	kHz
$\overline{CS}$ falling to SCCLK rising		t_{css}	20	-	ns
Rise time of SCCLK line	(Note 7)	t_r	-	50	ns
Fall time of SCCLK lines	(Note 7)	t_f	-	50	ns
SCCLK low time		t_{scl}	150	-	ns
SCCLK high time		t_{sch}	150	-	ns
Setup time SCDIN to SCCLK rising		t_{cdisu}	50	-	ns
Hold time SCCLK rising to SCDIN	(Note 2)	t_{cdih}	50	-	ns
Transition time from SCCLK to SCDOUT valid	(Note 3)	t_{scdov}	-	40	ns
Time from SCCLK rising to $\overline{INTREQ}$ rising	(Note 4)	t_{scrh}	-	200	ns
Rise time for $\overline{INTREQ}$	(Note 4)	t_{rr}	-	(Note 6)	ns
Hold time for $\overline{INTREQ}$ from SCCLK rising	(Note 5, 7)	t_{scrl}	0	-	ns
Time from SCCLK falling to $\overline{CS}$ rising		t_{sccsh}	20	-	ns
High time between active $\overline{CS}$		t_{csht}	200	-	ns
Time from $\overline{CS}$ rising to SCDOUT high-Z	(Note 7)	t_{cscdo}		20	ns

Notes:
1. The specification f_{sck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the software. The relevant application code user's manual should be consulted for the software speed limitations.
2. Data must be held for sufficient time to bridge the 50 ns transition time of SCCLK.
3. SCDOUT should *not* be sampled during this time period.
4. $\overline{INTREQ}$ goes high only if there is no data to be read from the DSP at the rising edge of SCCLK for the second-to-last bit of the last byte of data during a read operation as shown.
5. If $\overline{INTREQ}$ goes high as indicated in (Note 4), then $\overline{INTREQ}$ is guaranteed to remain high until the next rising edge of SCCLK. If there is more data to be read at this time, $\overline{INTREQ}$ goes active low again. Treat this condition as a new read transaction. Raise chip select to end the current read transaction and then drop it, followed by the 7-bit address and the R/$\overline{W}$ bit (set to 1 for a read) to start a new read transaction.
6. With a 3.3k Ohm pull-up resistor this value is typically 260ns. As this pin is open drain adjusting the pull up value will affect the rise time.
7. This time is by design and not tested.

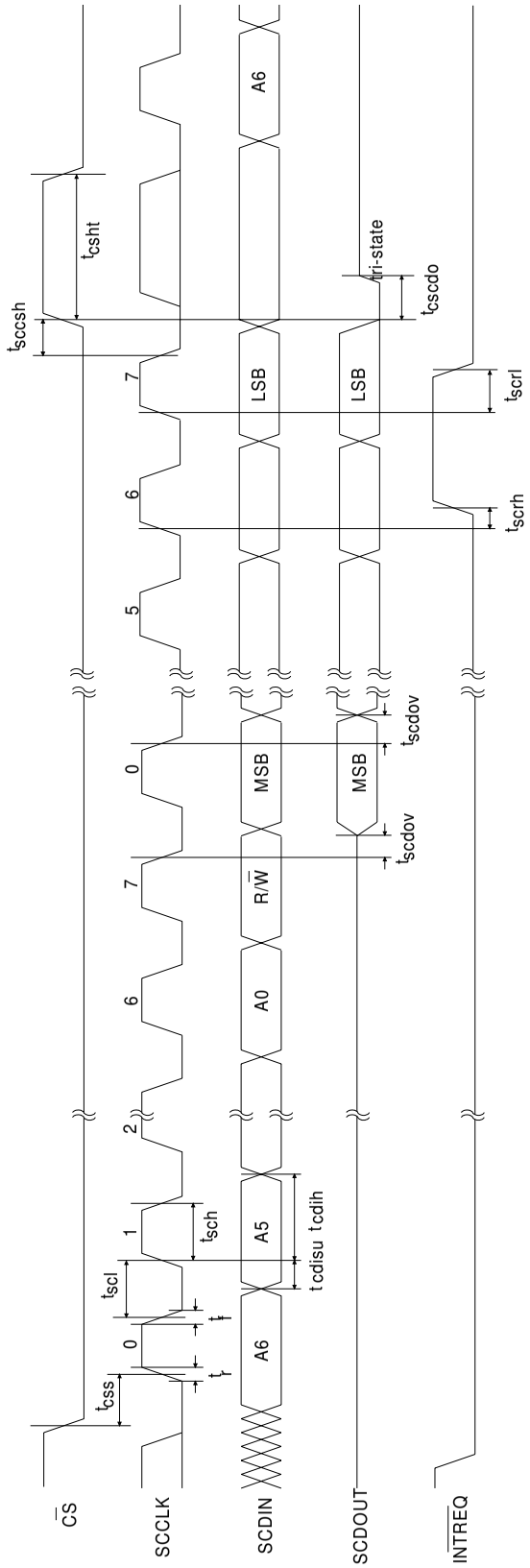


Figure 7. SPI Control Port Timing

1.11. Switching Characteristics — I²C® Control Port

(VA, VD[3:1] = 2.5 V ±5%; Inputs: Logic 0 = DGND, Logic 1 = VD, C_L = 20 pF)

Parameter		Symbol	Min	Max	Units
SCCLK clock frequency	(Note 1)	f_{scl}		400	kHz
Bus free time between transmissions		t_{buf}	4.7		µs
Start-condition hold time (prior to first clock pulse)		t_{hdst}	4.0		µs
Clock low time		t_{low}	1.2		µs
Clock high time		t_{high}	1.0		µs
SCDIO setup time to SCCLK rising		t_{sud}	250		ns
SCDIO hold time from SCCLK falling	(Note 2)	t_{hdd}	0		µs
Rise time of SCCLK	(Note 3), (Note 7)	t_r		50	ns
Fall time of SCCLK	(Note 7)	t_f		300	ns
Time from SCCLK falling to CS493XX ACK		t_{sca}		40	ns
Time from SCCLK falling to SCDIO valid during read operation		t_{scsdv}		40	ns
Time from SCCLK rising to $\overline{\text{INTREQ}}$ rising	(Note 4)	t_{scrh}		200	ns
Hold time for $\overline{\text{INTREQ}}$ from SCCLK rising	(Note 5)	t_{scrl}	0		ns
Rise time for $\overline{\text{INTREQ}}$	(Note 6)	t_{rr}		**	ns
Setup time for stop condition		t_{susp}	4.7		µs

Notes:. 1. The specification f_{scl} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the software. The relevant application code user's manual should be consulted for the software speed limitations.

2. Data must be held for sufficient time to bridge the 300-ns transition time of SCCLK. This hold time is by design and not tested.
3. This rise time is *shorter* than that recommended by the I²C specifications. For more information, see Section 6.1, "Serial Communication" on page 36.
4. $\overline{\text{INTREQ}}$ goes high only if there is no data to be read from the DSP at the rising edge of SCCLK for the last data bit of the last byte of data during a read operation as shown.
5. If $\overline{\text{INTREQ}}$ goes high as indicated in Note 8, then $\overline{\text{INTREQ}}$ is guaranteed to remain high until the next rising edge of SCCLK. If there is more data to be read at this time, $\overline{\text{INTREQ}}$ goes active low again. Treat this condition as a new read transaction. Send a new start condition followed by the 7-bit address and the R/$\overline{\text{W}}$ bit (set to 1 for a read). This time is by design and is not tested.
6. With a 3.3k Ohm pull-up resistor this value is typically 260ns. As this pin is open drain adjusting the pull up value will affect the rise time.
7. This time is by design and not tested.

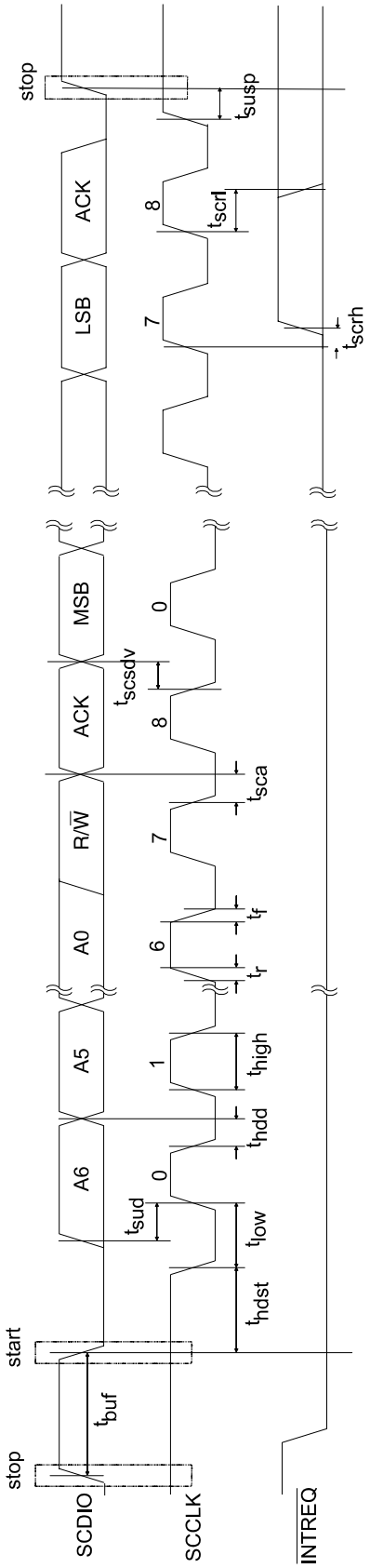


Figure 8. I²C® Control Port Timing

1.12. Switching Characteristics — Digital Audio Input

(VA, VD[3:1] = 2.5 V ±5%; Inputs: Logic 0 = DGND, Logic 1 = VD, C_L = 20 pF)

Parameter		Symbol	Min	Max	Unit
SCLKN1(2) period for both Master and Slave mode	(Note 1)	T_{sclki}	40	-	ns
SCLKN1(2) duty cycle for Master and Slave mode	(Note 1)		45	55	%
Master Mode	(Note 1, 2)				
LRCLKN1(2) delay after SCLKN1(2) transition	(Note 3)	T_{lrds}	-	10	ns
SDATAN1(2) setup to SCLKN1(2) transition	(Note 4)	T_{sdsum}	10	-	ns
SDATAN1(2) hold time after SCLKN1(2) transition	(Note 4)	T_{sdhm}	5	-	ns
Slave Mode	(Note 5)				
Time from active edge of SCLKN1(2) to LRCLKN1(2) transition		T_{stlr}	10	-	ns
Time from LRCLKN1(2) transition to SCLKN1(2) active edge		T_{lrts}	10	-	ns
SDATAN1(2) setup to SCLKN1(2) transition	(Note 4)	T_{sdsus}	5	-	ns
SDATAN1(2) hold time after SCLKN1(2) transition	(Note 4)	T_{sdhs}	5	-	ns

Notes:
1. Master mode timing specifications are characterized, not production tested.
2. Master mode is defined as the CS493XX driving LRCLKN1(2) and SCLKN1(2). Master or Slave mode can be programmed.
3. This timing parameter is defined from the non-active edge of SCLKN1(2). The active edge of SCLKN1(2) is the point at which the data is valid.
4. This timing parameter is defined from the active edge of SCLKN1(2). The active edge of SCLKN1(2) is the point at which the data is valid.
5. Slave mode is defined as SCLKN1(2) and LRCLKN1(2) being driven by an external source.

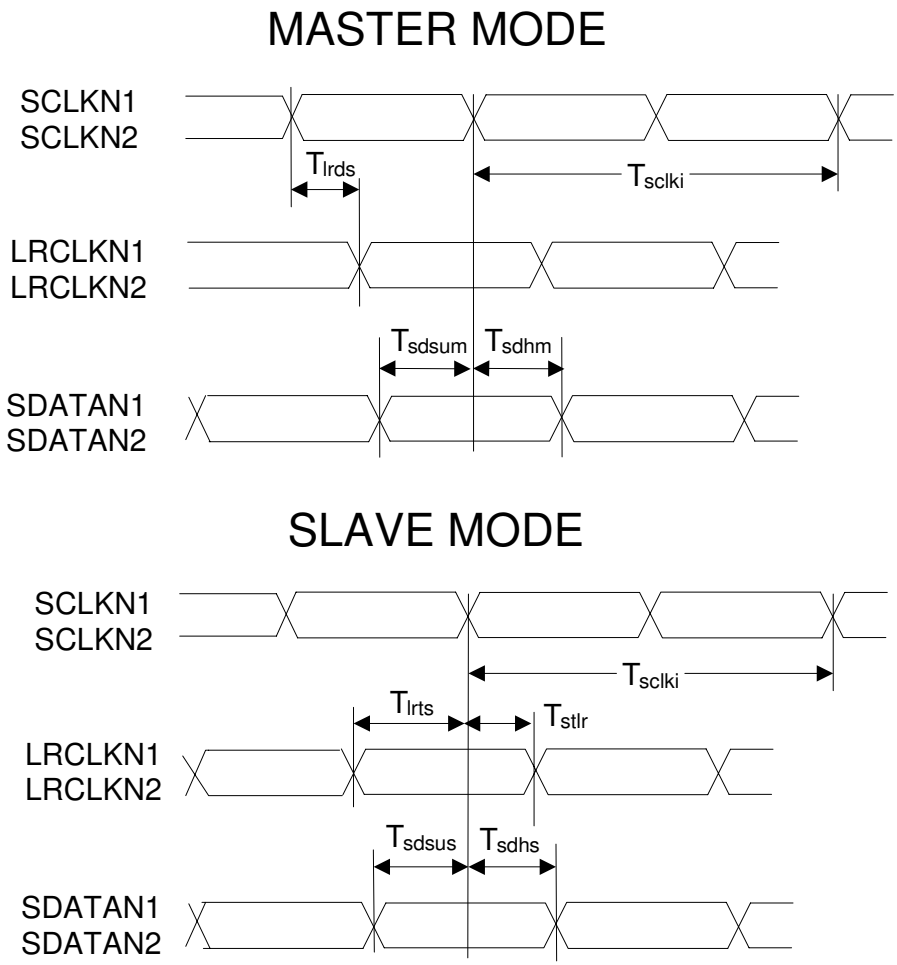


Figure 9. Digital Audio Input Data, Master and Slave Clock Timing

1.13. Switching Characteristics — Serial Bursty Data Input

(VA, VD[3:1] = 2.5 V ±5%; Inputs: Logic 0 = DGND, Logic 1 = VD, C_L = 20 pF)

Parameter	Symbol	Min	Max	Unit
Serial compressed data clock CMPCLK period	T_{cmpclk}	-	27	MHz
CMPDAT setup before CMPCLK high	T_{cmpsu}	5	-	ns
CMPDAT hold after CMPCLK high	T_{cmphld}	3	-	ns
Delay from falling edge of CMPREQ to CMPCLK rising edge	T_{reqclk}	0	-	ns

Notes: 1. CMPREQ signal is asynchronous to CLKIN and can change at any time relative to CLKIN.

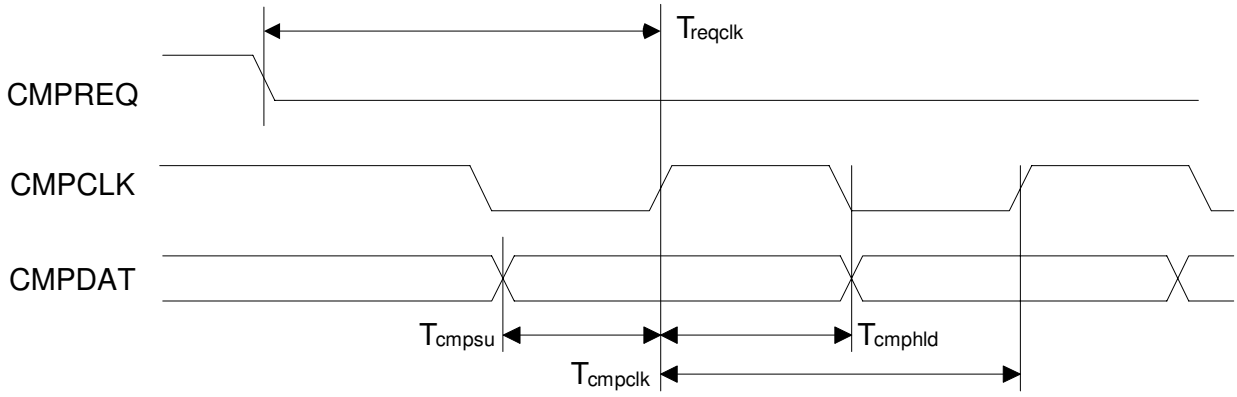


Figure 10. Serial Compressed Data Timing

1.14. Switching Characteristics — Parallel Data Input

(VA, VD[3:1] = 2.5 V ±5%; Inputs: Logic 0 = DGND, Logic 1 = VD, C_L = 20 pF)

Parameter	Symbol	Min	Max	Unit
CMPCLK Period	T_{cmpclk}	4*DCLK + 10	-	ns
DATA[7:0] setup before CMPCLK high	T_{cmpsu}	10	-	ns
DATA[7:0] hold after CMPCLK high	T_{cmphld}	10	-	ns
Delay from falling edge of CMPREQ to CMPCLK rising edge	T_{reqclk}	0	-	ns

Notes: 1. CMPREQ signal is asynchronous to CLKIN and can change at any time relative to CLKIN.

2. Certain timing parameters are normalized to the DSP clock, DCLK, in nanoseconds. The DSP clock can be defined as follows:

   External CLKIN Mode:
   DCLK == CLKIN/4 before and during boot
   DCLK == CLKIN after boot

   Internal Clock Mode:
   DCLK == 10MHz before and during boot, i.e. DCLK == 100ns
   DCLK == 65 MHz after boot, i.e. DCLK == 15.4ns

   It should be noted that DCLK for the internal clock mode is application specific. The application code users guide should be checked to confirm DCLK for the particular application.

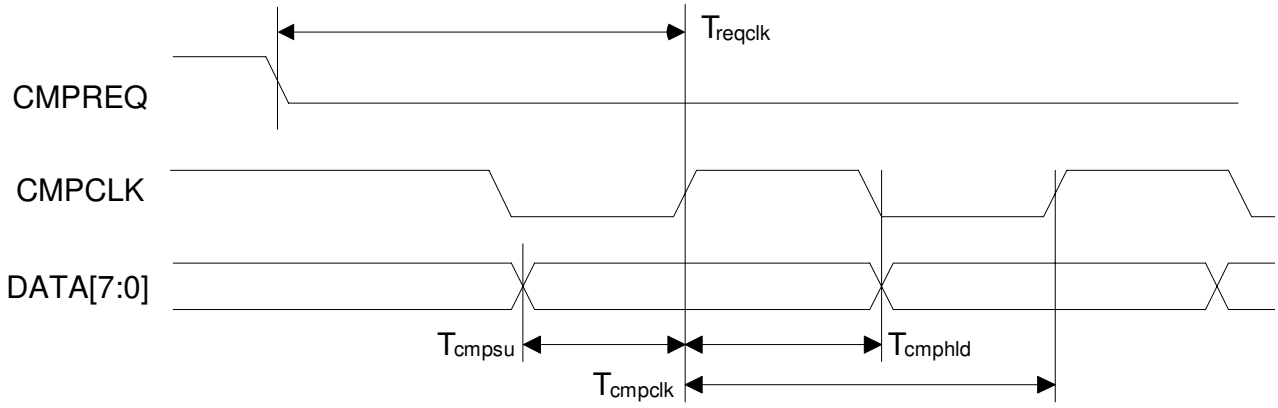


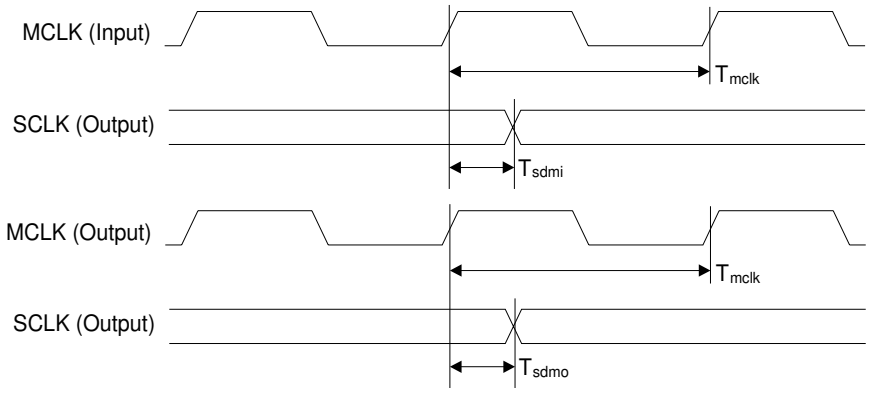
Figure 11. Parallel Data Timing (when not in a parallel control mode)

1.15. Switching Characteristics — Digital Audio Output

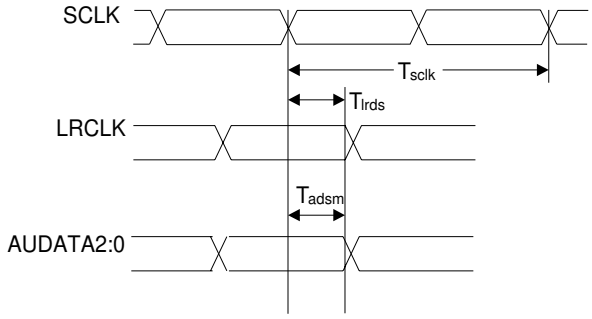
(VA, VD[3:1] = 2.5 V ±5%; Inputs: Logic 0 = DGND, Logic 1 = VD, C_L = 20 pF)

Parameter		Symbol	Min	Max	Unit
MCLK period	(Note 1)	T_{mclk}	40	-	ns
MCLK duty cycle	(Note 1)		40	60	%
SCLK period for Master or Slave mode	(Note 2)	T_{sclk}	40	-	ns
SCLK duty cycle for Master or Slave mode	(Note 2)		45	55	%
Master Mode	(Note 2, 3)				
SCLK delay from MCLK rising edge, MCLK as an input		T_{sdmi}		15	ns
SCLK delay from MCLK rising edge, MCLK as an output		T_{sdmo}	–5	10	ns
LRCLK delay from SCLK transition	(Note 4)	T_{lrds}		10	ns
AUDATA2–0 delay from SCLK transition	(Note 4)	T_{adsm}		10	ns
Slave Mode	(Note 5)				
Time from active edge of SCLKN1(2) to LRCLKN1(2) transition		T_{stlr}	10	-	ns
Time from LRCLKN1(2) transition to SCLKN1(2) active edge		T_{lrts}	10	-	ns
AUDATA2–0 delay from SCLK transition	(Note 4, 6)	T_{adss}		15	ns

Notes:
1. MCLK can be an input or an output. These specifications apply for both cases.
2. Master mode timing specifications are characterized, not production tested.
3. Master mode is defined as the CS493XX driving both SCLK and LRCLK. When MCLK is an input, it is divided to produce SCLK and LRCLK.
4. This timing parameter is defined from the non-active edge of SCLK. The active edge of SCLK is the point at which the data is valid.
5. Slave mode is defined as SCLK and LRCLK being driven by an external source.
6. This specification is characterized, not production tested.



MASTER MODE



SLAVE MODE

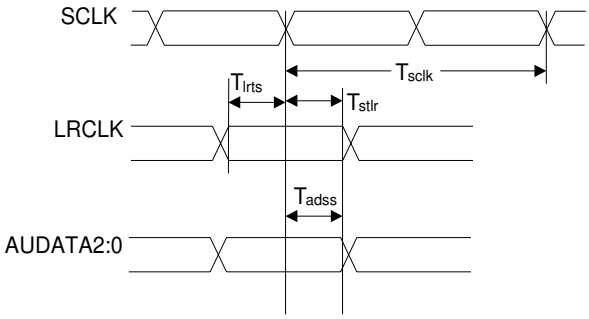


Figure 12. Digital Audio Output Data, Input and Output Clock Timing

2. FAMILY OVERVIEW

The CS49300 family contains system on a chip solutions for multichannel audio decompression and digital signal processing. The CS49300 family is split into 4 sub-families targeted at the DVD, broadcast and audio/video receiver (AVR), and effects and post processing markets.

This document focuses on the electrical features and characteristics of these parts. Different features are described from a hardware design perspective. It should be understood that not all of the features portrayed in this document are supported by all of the versions of application code available. The application code user's guides should be consulted to confirm which hardware features are supported by the software.

The parts use a combination of internal ROM and RAM. Depending on the application being used, a download of application software may be required each time the part is powered up. This document uses "download" and "code load" interchangeably. These terms should be interpreted as meaning the transfer of application code into the internal memory of the part from either an external microcontroller or through the autoboot procedure.

2.1. CS493XX Document Strategy

The documents described below are integral in defining the functionality and usage of the CS39300 family of DSPs.

1) CS49300 Datasheet (*DS339)*

2) CS49300 Errata - (*ER339)* - This document contain updates/corrections/exceptions to the datasheet.

3) Application Note (*AN162)* - This document contains firmware usage information for Broadcast Systems. It serves mainly to assist the microcontroller programmer but may also be highly useful to the system designer.

4) Application Note (*AN163*) - This document contains firmware usage information for Outboard Decoder Systems - e.g. AVR. It serves mainly to assist the microcontroller programmer but may also be highly useful to the system designer.

Note: Please also contact your local Cirrus Logic FAE to obtain other relevant documents of new technology and also latest versions of the above mentioned documents.

2.2. Multichannel Decoder Family of Parts

CS49300 - DVD Audio Decoder. The CS49300 device is targeted at audio decoding in the DVD via ES or PES in a serial or parallel bursty fashion for MLP or for DVD Audio Pack Layer Support. (All the other decoding/processing algorithms listed below require delivery of PCM or IEC61937-packed compressed data via I^2S or LJ formatted digital audio to the CS49300). Specifically the CS49300 will support all of the following decoding/processing standards:

- Meridian Lossless Packing™ (MLP™)* (for ES and PES data delivery only)
- DVD Audio Pack Layer Support* (for ES and PES data delivery only)
- Dolby Digital™ (AC-3™) with Dolby Pro Logic™
- Dolby Digital™ with Dolby Pro Logic™ plus Cirrus Extra Surround™
- Dolby Digital™ with Dolby Pro Logic II™
- Dolby Digital™ with Dolby Pro Logic II™ plus Cirrus Extra Surround™
- Virtual Dolby Digital™
- MPEG-2, Advanced Audio Coding Algorithm (AAC)
- MPEG Multichannel
- MPEG Multichannel with Dolby Pro Logic II™
- MPEG Multichannel plus Cirrus Extra Surround™
- MPEG-1, Layer 3 (MP3)
- DTS Digital Surround™
- DTS Digital Surround™ with Dolby Pro Logic II™
- DTS Digital Surround™ plus Cirrus Extra Surround™
- DTS-ES Extended Surround™ (DTS-ES Discrete 6.1 & Matrix 6.1)
- DTS Neo:6™
- LOGIC5® (5.1 Channel, Max Fs=48kHz and LOGIC7® (7.1 Channel, Max Fs=96kHz)
- VMAx VirtualTheater® (Virtual Dolby Digital)
- SRS TruSurround™ (Virtual Dolby Digital and

DTS Virtual 5.1™ Versions)
- SRS Circle Surround™ I/II
- HDCD®
- Cirrus P.D.F. (Dolby Pro Logic 2Fs Decoder and PCM Upsampler)
- Cirrus PL2_2FS (Dolby Pro Logic II 2Fs Decoder and PCM Upsampler)

Please refer to the CS4932x/CS49330 Part Matrix vs. Code Matrix (PDF) document available from the CS49300 Web Site Page for the latest listing of audio decoding/processing algorithms. The part will also support PES layer decode for audio/video synchronization and DVD Audio Pack layer support. The CS49300 will support all of the above decoding and PCM processing standards.

CS4931X - Broadcast Sub-family. The CS4931X sub-family is targeted at audio decoding in the broadcast markets in systems such as digital TV, HDTV, set-top boxes and digital audio broadcast units (digital radios). Specifically the CS4931X sub-family will support the following decode standards:

- Dolby Digital™ (AC-3™) with Dolby Pro Logic™
- MPEG-2, Advanced Audio Coding Algorithm (AAC)
- MPEG-1, Layers 1, 2 Stereo
- MPEG-1, Layers 3 (MP3) Stereo
- MPEG-2, Layer 2 Stereo
- MPEG-2, Layer 3 (MP3) Stereo

The part will also support PES layer decode for audio/video synchronization. The CS49310 will support all of the above decode standards while other parts in the CS4931X sub-family will decode subsets of the above audio decoding standards.

CS4932X - Audio/Video Receiver (AVR) Sub-family. The CS4932X sub-family is targeted at audio decoding in the audio/video receiver markets. Typical applications will include amplifiers with integrated decoding capability, outboard decoder pre-amplifiers, car radios and any system where the compressed audio is received in an IEC61937 format. Specifically the CS4932X sub-family will support the following decode standards:

- Dolby Digital™ (AC-3™) with Dolby Pro Logic™
- Dolby Digital™ with Dolby Pro Logic™ plus Cirrus Extra Surround™
- Dolby Digital™ with Dolby Pro Logic II™
- Dolby Digital™ with Dolby Pro Logic II™ plus Cirrus Extra Surround™
- Virtual Dolby Digital™
- MPEG-2, Advanced Audio Coding Algorithm (AAC)
- MPEG Multichannel
- MPEG Multichannel with Dolby Pro Logic II™
- MPEG Multichannel plus Cirrus Extra Surround™
- MPEG-1, Layer 3 (MP3)
- DTS Digital Surround™
- DTS Digital Surround™ with Dolby Pro Logic II™
- DTS Digital Surround™ plus Cirrus Extra Surround™
- DTS-ES Extended Surround™ (DTS-ES Discrete 6.1 & Matrix 6.1)
- DTS Neo:6™
- LOGIC5® (5.1 Channel, Max Fs=48kHz and LOGIC7® (7.1 Channel, Max Fs=96kHz)
- VMAx VirtualTheater® (Virtual Dolby Digital)
- SRS TruSurround™ (Virtual Dolby Digital and DTS Virtual 5.1™ Versions)
- SRS Circle Surround™ I/II
- HDCD®
- Cirrus P.D.F. (Dolby Pro Logic 2Fs Decoder and PCM Upsampler)
- Cirrus PL2_2FS (Dolby Pro Logic II 2Fs Decoder and PCM Upsampler)

The CS49326 will support all of the above decode standards while other parts in the CS4932X sub-family will decode subsets of the above audio decoding standards.

Except for the CS49329 which offers AAC support this subfamily will offer integrated ROM support for the AC-3 code, DTS code, Cirrus Original Surround code and DTS tables. The CS49329 will require an external download for all applications but will still support the DTS tables on chip.

CS49330 - General Purpose, Car Audio Processor, PCM Effects & Multichannel Post-Processing Device. The CS49330 sub-family is