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FEATURES

- Multi-standard 32-bit Audio Decoding plus Post processing
- Supports legacy audio formats and a wide array of post-processing
  - Dolby Digital® EX, Dolby Pro Logic® II, IIx, IIz 7.1, Dolby Headphone® 2, Dolby Virtual Speaker® 2, Dolby Volume® (original), Dolby Volume 258™ (lite), Audistry®
  - DTS-ES 96/24™ Discrete 7.1, DTS-ES™ Discrete 7.1, DTS-ES™ Matrix 6.1, DTS Neo:6®, DTS Neural Surround™ DTS Surround Sensation Speaker
  - MPEG-2 AAC™ LC 5.1
  - SRS® Circle Surround® II, SRS Circle Surround Auto, SRS Circle Surround Decoder Optimized, SRS TruVolume™ 7.1 (V 2.1.0.0), SRS TruSurround HD/HD4®, SRS WOW HD™, SRS CS Headphone™, SRS Circle Cinema 3D™, SRS Studio Sound HD™
  - THX® Ultra2™, THX Select2™
- Cirrus Logic's Applications Library
  - Cirrus Original Multi-Channel Surround 2 (COMS2), Cirrus Band XpandeR™, Cirrus Virtualization Technology (CVT), Cirrus Intelligent Room Calibration 2 (IRC2), Cirrus Bass Enhancement (CBE)
  - Crossbar Mixer, Signal Generator
  - Advanced Post-Processors including: 7.1 Bass Manager Quadruple Crossover, Tone Control, 11-Band Parametric EQ, Delay, 2:1/4:1 Decimator, 1:2/1:4 Upsampler
- Up to 12 Channels of 32-bit Serial Audio Input

Audio Decoder DSP Family with Dual 32-bit DSP Engine Technology

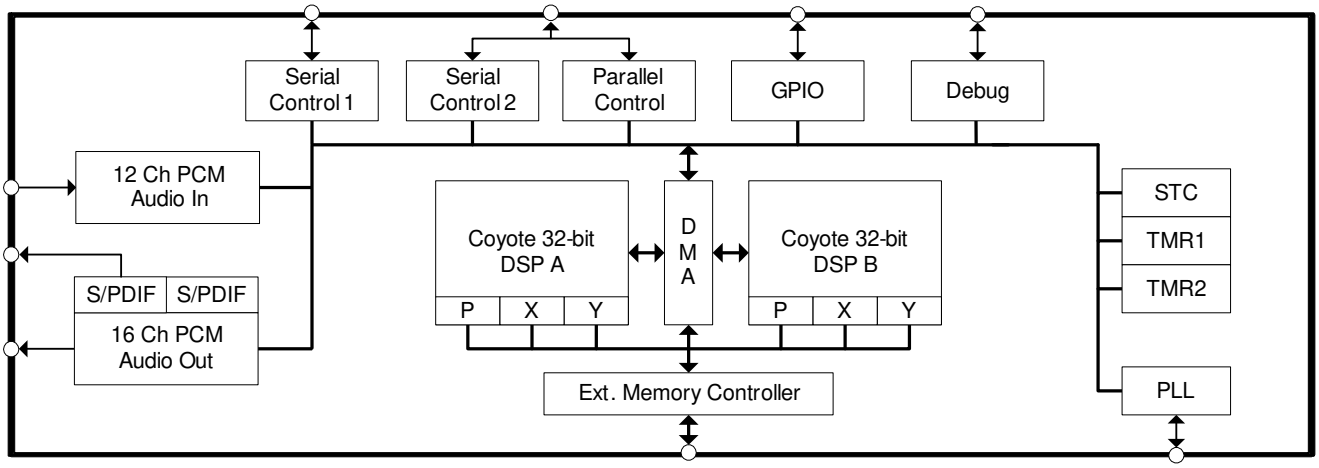
- 16 Ch x 32-bit PCM Out with Dual 192 kHz S/PDIF Tx
- Two SPI™/I²C™ Ports
- Customer Software Security Keys
- Large On-chip X, Y, and Program RAM & ROM
- SDRAM and Serial Flash Memory Support

The CS4953xx DSP family are the enhanced versions of the CS495xx DSP family with higher overall performance and lower system cost. The CS4953xx includes all mainstream audio processing codes in on-chip ROM. This saves external memory for code storage. In addition, the intensive decoding tasks of Dolby Digital Surround EX®, AAC multi-channel, DTS-ES 96/24, THX Ultra2 Cinema and Dolby Headphone can be accomplished without the expense of external SDRAM memory.

With larger internal memories than the CS495xx, the CS49531x is designed to support up to 150 ms per channel of lip-sync delay. With 150 MHz internal clock speed, the CS4953xx supports the most demanding post-processing requirements. It is also designed for easy upgrading. Customers currently using the CS495xx can upgrade to the CS4953xx with minor hardware and software changes.

Ordering Information

See page 28 for ordering information.



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1 Documentation Strategy

The CS4953xx data sheet describes the CS4953xx family of multichannel audio decoders. This document should be used in conjunction with the following documents when evaluating or designing a system around the CS4953xx family of processors.

Table 1. CS4953xx Related Documentation

Document Name	Description
CS4953xx Data Sheet	This document, which contains the hardware specifications for the CS4953xx family
CS4953xx Hardware User's Manual	Includes detailed system design information for CS4953x3 product family, including Typical Connection Diagrams, Boot-Procedures, Pin Descriptions, etc.
CS495314/CS4970x4 System Designer's Guide	A new consolidated documentation set for the CS4953x4 product family that includes: • Detailed system design information including typical connection diagrams, boot procedures, pin descriptions, etc. Also describes use of DSP Condenser™ tool • Detailed firmware design information including signal processing flow diagrams and control API information
AN288 - *CS4953xx/CS4970x4 Firmware User's Manual*	Includes detailed firmware design information including signal processing flow diagrams and control API information

The scope of the CS4953xx data sheet is primarily the hardware specifications of the CS4953xx family of devices. This includes hardware functionality, characteristic data, pinout, and packaging information.

The intended audience for the CS4953xx data sheet is the system PCB designer, MCU programmer, and the quality control engineer.

2 Overview

The CS4953xx DSP Family, together with Cirrus Logic's comprehensive library of audio processing algorithms enables the development of next-generation audio solutions. There are two classes of devices in the CS4953xx DSP family:

- CS4953x3 Class (ROM ID 3), comprising the CS495303 and the CS495313
- CS4953x4 Class (ROM ID 4), comprising the CS495304 and the CS495314

The primary difference between the CS4953x3 and the CS4953x4 classes is the support of the DSP Condenser application on the CS4953x4 class of products only. The DSP Condenser is a tool set that enables the DSP to automatically boot and configure itself from an external serial FLASH, thus reducing the traditional heavy loading on the part of the system microcontroller. Because of the design time savings, enhanced tools support, and better performance associated with the CS4953x4 product set, Cirrus Logic recommends that the CS4953x4 family be used for all new designs. More information on the DSP Condenser can be found in the *CS4953x4/CS497xx System Designer's Guide*.

Within each ROM ID class (3, 4), the breakdown into two devices per class (CS49530x and CS49531x) is based on the differences between the internal memory size and DSP firmware supported. Essentially, the audio processing features of the CS49531x are a superset of audio features available in the CS49530x. Table 2, "Device and Firmware Selection Guide," on page 6 provides details of the differences between the two product classes.

Note: The CS495303/04/14 is available in a 128-pin LQFP package and the CS495313 is available in a 128-pin or 144-pin LQFP package.

2.1 Migrating from CS4953x3 to CS4953x4

- The recommended way to boot the DSP for normal operation is “master boot”. Refer to Chapter 1 of the *CS4953x4/CS4970x4 System Designer’s Guide*. CS4953x4 supports slave boot mode as well (used for programming the serial flash with the DSP code, through the SCP2 port).
- CS4953x4 DSPs are only available in 128 pin package.
- The serial flash chip select pin used is pin 14 (GPIO0) for master boot. Cirrus Logic recommends that at least an 8-Mb serial flash device be used. Refer to *CS4953x4/CS4970x4 System Designer’s Guide* for a list of flash types that are currently supported.
- CS4953x4 DSP family supports DSP Condenser and DSP Manager API for runtime control/host communication. Refer to *CS4953x4/CS4970x4 System Designer’s Guide* for details.

2.2 Licensing

Licenses are required for all third party audio decoding/processing algorithms, including the application notes. contact your local Cirrus Sales representative for more information.

3 Code Overlays

The suite of software available for the CS4953xx family consists of an operating system (OS) and a library of overlays. The overlays have been divided into three main groups called Decoders, Matrix-processors, and Post-processors. All software components are defined below:

- **OS/Kernel** - Encompasses all non-audio processing tasks, including loading data from external memory, processing host messages, calling audio-processing subroutines, error concealment, etc.
- **Decoders** - Any Module that initially writes data into the audio I/O buffers, e.g. AC-3™, DTS, PCM, etc. All the decoding/processing algorithms listed below require delivery of PCM or IEC61937-packed, compressed data via I^2S- or LJ-formatted digital audio to the CS4953xx.
- **Matrix-processors** - Any module that processes audio I/O buffer PCM data in-place before the Post-processors. Generally speaking, these modules alter the number of valid channels in the audio I/O buffer through processes like Virtualization (n⇨2 channels) or Matrix Decoding (2⇨n channels). Examples are Dolby ProLogic II, IIx, IIz and DTS Neo:6.
- **Post-processors** - Any module that processes audio I/O buffer PCM data in-place after the Matrix-Processors. Examples are Bass Management, Audio Manager, Tone Control, EQ, Delay, Customer-specific Effects, Dolby Headphone 2 and Dolby Virtual Speaker 2, etc.

The overlay structure reduces the time required to reconfigure the DSP when a processing change is requested. Each overlay can be reloaded independently without disturbing the other overlays. For example, when a new decoder is selected, the OS, matrix-, and post-processors do not need to be reloaded — only the new decoder (the same is true for the other overlays).

Table 2 below lists the firmware available based on device selection. Refer to AN288, *CS4953xx/CS497xxx Firmware User’s Manual* for the latest listing of application codes and Cirrus Framework™ modules available.

Table 2. Device and Firmware Selection Guide[1]

Device	Pre-Process	Decode Processor (DSP-A)[2]	Matrix-processor (DSP-A)[2]	Virtualizer-processor (DSP-B)[2]	Post-processor (DSP-B)[2]
CS49530x **300 M ACS**	N/A	Stereo PCM Multi-Channel PCM (2:1 Down-sampling Option) Dolby Digital AAC MP3 HDCD	Dolby Pro Logic II/IIx/IIz 7.1 Circle Surround II (Stereo In) Cirrus Original Multi-Channel Surround (Effects / Reverb Processor) Down-mix (Simultaneous Process)	Dolby Headphone Dolby Virtual Speaker SRS TruSurround XT THX Select	APP (Advanced Post-processing) –Tone Control –Select 2 –PEQ (up to 11 Bands) –Delay –7.1 Bass Manager –Audio Manager 1:2 Up-sampling
CS49531x ***(Superset of CS49530x)*** **300 M ACS**	Lip Sync Delay	Same as CS49530x + DTS DTS-ES DTS 96/24	Same as CS49530x + DTS Neo:6, DTS Neural Sound (Stereo In)	Same as CS49530x + THX Ultra2	

1.This feature list is a snapshot of features available as of the publication date of this revision of the data sheet. More features may now be available. Check with your Cirrus Logic Field Application Engineer (FAE) to obtain the latest feature list for the CS49530x and CS49531x products.

2. Additional processing (MPMA, MPMB, VPM, PPM) post any of the HD audio decoders may be limited. Contact your Cirrus Logic FAE for concurrency matrix.

4 Hardware Functional Description

4.1 Coyote 32-bit DSP Core

The CS4953xx is a dual-core DSP with separate X and Y data and P code memory spaces. Each core is a high-performance, 32-bit, user-programmable, fixed-point DSP that is capable of performing two multiply accumulate (MAC) operations per clock cycle. Each core has eight 72-bit accumulators, four X- and four Y-data registers, and 12 index registers.

Both DSP cores are coupled to a flexible DMA engine. The DMA engine can move data between peripherals such as the digital audio input (DAI) and digital audio output (DAO), external memory, or any DSP core memory, all without the intervention of the DSP. The DMA engine offloads data move instructions from the DSP core, leaving more MIPS available for signal processing instructions.

CS4953xx functionality is controlled by application codes that are stored in on-board ROM or downloaded to the CS4953xx from a host MCU or external FLASH/EEPROM. Users can choose to use standard audio decoder and post-processor modules which are available from Cirrus Logic.

The CS4953xx is suitable for audio decoder, audio post-processor, audio encoder, DVD audio/video player, and digital broadcast decoder applications.

4.1.1 DSP Memory

Each DSP core has its own on-chip data and program RAM and ROM and does not require external memory for any of today's popular audio algorithms including Dolby Digital Surround EX, AAC Multichannel, DTS-ES 96/24, and THX Ultra2.

The memory maps for the DSPs are as follows. All memory sizes are composed of 32-bit words.

Table 3. CS49530x DSP Memory Sizes

Memory Type	DSP A	DSP B
X	16K SRAM, 16K ROM	10K SRAM, 8K ROM
Y	16K SRAM, 32K ROM	16K SRAM, 16K ROM
P	8K SRAM, 32K ROM	8K SRAM, 24K ROM

Table 4. CS49531x DSP Memory Sizes

Memory Type	DSP A	DSP B
X	16K SRAM, 16K ROM	10K SRAM, 8K ROM
Y	24K SRAM, 32K ROM	16K SRAM, 16K ROM
P	8K SRAM, 32K ROM	8K SRAM, 24K ROM

4.1.2 DMA Controller

The powerful 12-channel DMA controller can move data between eight on-chip resources. Each resource has its own arbiter: X, Y, and P RAM/ROMs on DSP A; X, Y, and P RAM/ROMs on DSP B; external memory; and the peripheral bus. Modulo and linear addressing modes are supported, with flexible start address and increment controls. The service interval for each DMA channel as well as up to six interrupt events, is programmable.

4.2 On-chip DSP Peripherals

4.2.1 Digital Audio Input Port (DAI)

The 12-channel (6-line) DAI port supports a wide variety of data input formats. The port is capable of accepting PCM or IEC61937. Up to 32-bit word lengths are supported.

The port has two independent slave-only clock domains. Each data input can be independently assigned to a clock domain. The sample rate of the input clock domains can be determined automatically by the DSP, which off-loads the task of monitoring the S/PDIF receiver from the host. A time-stamping feature allows the input data to be sample-rate converted via software.

4.2.2 Digital Audio Output Port (DAO)

Note: There are two DAO ports. Each port can output eight channels of up to 32-bit PCM data. The port supports data rates from 32 kHz to 192 kHz. Each port can be configured as an independent clock domain in slave mode, or the ratio of the two clocks can be set to even multiples of each other in master mode. The two ports can also be ganged together into a single clock domain. Each port has one serial audio pin that can be configured as a 192 kHz S/PDIF transmitter (data with embedded clock on a single line).
Note: Only one S/PDIF transmitter pin is available in the 128-pin package.

4.2.3 Serial Control Port 1 & 2 (I^2C or SPI)

There are two on-chip serial control ports that are capable of operating as master or slave in either I^2C or SPI modes. SCP1 defaults to slave operation. It is dedicated for external host-control and supports an external clock up to 50 MHz in SPI mode. It is present in both the 144- and 128-pin packages. This high clock speed enables very fast code download, control or data delivery. SCP2 defaults to master mode and is dedicated for booting from external serial Flash memory or for audio sub-system control. SCP2 does not include the SCP2_BSY# pin in the 128-pin package.

4.2.4 Parallel Control Port

The CS4953xx parallel port supports both Motorola® and Intel® interfaces. It can be used for both control and data delivery. The parallel port pins are multiplexed with serial control port 2 and are available in the 144-pin package.

4.2.5 External Memory Interface

The external memory interface controller supports up to 128 Mb of SDRAM, using a 16-bit data bus.

4.2.6 General Purpose Input/Output (GPIO)

Many of the CS4953xx peripheral pins are multiplexed with GPIO. Each GPIO can be configured as an output, an input, or an input with interrupt. Each input-pin interrupt can be configured as rising edge, falling edge, active-low, or active-high.

4.2.7 Phase-Locked Loop (PLL)-based Clock Generator

The low-jitter PLL generates integer or fractional multiples of a reference frequency which are used to clock the DSP core and peripherals. Through a second PLL divider chain, a dependent clock domain can be output on the DAO port for driving audio converters. The CS4953xx defaults to running from the external reference frequency and can be switched to use the PLL output after overlays have been loaded and configured, either through master boot from an external serial FLASH or through host control. A built-in crystal oscillator circuit with a buffered output is provided. The buffered output frequency ratio is selectable between 1:1 (default) or 2:1.

4.3 DSP I/O Description

4.3.1 Multiplexed Pins

Many of the CS4953xx pins are multi-functional. For details on pin functionality, refer to the *CS4953xx Hardware User's Manual*.

4.3.2 Termination Requirements

Open-drain pins on the CS4953xx must be pulled high for proper operation. Refer to the *CS4953xx Hardware User's Manual* to identify which pins are open-drain and what value of pull-up resistor is required for proper operation.

Mode select pins on the CS4953xx are used to select the boot mode upon the rising edge of reset. A detailed explanation of termination requirements for each communication mode select pin can be found in the *CS4953xx Hardware User's Manual*.

4.3.3 Pads

The CS4953xx I/O operates from the 3.3 V supply and is 5 V tolerant.

4.4 Application Code Security

The external program code may be encrypted by the programmer to protect any intellectual property it may contain. A secret, customer-specific key is used to encrypt the program code that is to be stored external to the device.

5 Characteristics and Specifications

Note: All data sheet minimum and maximum timing parameters are guaranteed over the rated voltage and temperature. All data sheet typical parameters are measured under the following conditions: T = 25 °C, C_L = 20 pF, VDD = VDDA = 1.8 V, VDDIO = 3.3 V, GNDD = GNDIO = GNDA = 0 V.

5.1 Absolute Maximum Ratings

(GNDD = GNDIO = GNDA = 0 V; all voltages with respect to 0 V)

Parameter	Symbol	Min	Max	Unit
DC power supplies: Core supply	VDD	–0.3	2.0	V
PLL supply	VDDA	–0.3	3.6	V
I/O supply	VDDIO	–0.3	3.6	V
|VDDA – VDDIO|		-	0.3	V
Input pin current, any pin except supplies	I_{in}	—	+/- 10	mA
Input voltage on PLL_REF_RES	V_{filt}	-0.3	3.6	V
Input voltage on I/O pins	V_{inio}	-0.3	5.0	V
Storage temperature	T_{stg}	–65	150	°C

CAUTION: Operation at **or** beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

5.2 Recommended Operating Conditions

(GNDD = GNDIO = GNDA = 0 V; all voltages with respect to 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
DC power supplies: Core supply	VDD	1.71	1.8	1.89	V
PLL supply	VDDA	3.13	3.3	3.46	V
I/O supply	VDDIO	3.13	3.3	3.46	V
|VDDA – VDDIO|			0		V
Ambient operating temperature	T_A				
Commercial Grade (CQZ/CVZ)		0	+25	+ 70	°C
Automotive Grade (DQZ/DVZ)		- 40	+25	+ 85	
Commercial	T_j	0	—	+125	ºC
Automotive		-40		+125	

Note: It is recommended that the 3.3 V IO supply come up ahead of or simultaneously with the 1.8 V core supply.

5.3 Digital DC Characteristics

(Measurements performed under static conditions.)

Parameter	Symbol	Min	Typ	Max	Unit
High-level input voltage	V_{IH}	2.0	—	—	V
Low-level input voltage, except XTI	V_{IL}	—	—	0.8	V
Low-level input voltage, XTI	V_{ILXTI}	—	—	0.6	V
Input Hysteresis	V_{hys}	—	0.4	—	V
High-level output voltage (I_O = -4mA), except XTI, SDRAM pins	V_{OH}	VDDIO * 0.9	—	—	V
Low-level output voltage (I_O = 4mA), except XTI, SDRAM pins	V_{OL}	—	—	VDDIO * 0.1	V
SDRAM High-level output voltage (I_O = -8mA)	V_{OH}	VDDIO * 0.9	—	—	V
SDRAM Low-level output voltage (I_O = 8mA)	V_{OL}	—	—	VDDIO * 0.1	V
Input leakage current (all digital pins with internal pull-up resistors disabled)	I_{IN}	—	—	5	µA
Input leakage current (all digital pins with internal pull-up resistors enabled, and XTI)	I_{IN-PU}	—	—	70	µA

5.4 Power Supply Characteristics

(measurements performed under operating conditions)

Parameter	Min	Typ	Max	Unit
Power supply current:				
Core and I/O operating: VDD[1]	—	350	—	mA
PLL operating: VDDA	—	3.5	—	mA
With external memory and most ports operating: VDDIO	—	120	—	mA

1. Dependent on application firmware and DSP clock speed.

5.5 Thermal Data (144-pin LQFP)

Parameter	Symbol	Min	Typ	Max	Unit
Thermal Resistance (Junction to Ambient)	θ_{ja}				°C / Watt
Two-layer Board[1]		—	48	—	
Four-layer Board[2]		—	40	—	
Thermal Resistance (Junction to Top of Package)	ψ_{jt}				°C / Watt
Two-layer Board[1]		—	.39	—	
Four-layer Board[2]		—	.33	—	

5.6 Thermal Data (128-pin LQFP)

Parameter	Symbol	Min	Typ	Max	Unit
Thermal Resistance (Junction to Ambient)	θ_{ja}				°C / Watt
Two-layer Board[1]		—	53	—	
Four-layer Board[2]		—	44	—	
Thermal Resistance (Junction to Top of Package)	ψ_{jt}				°C / Watt
Two-layer Board[1]		—	.45	—	
Four-layer Board[2]		—	.39	—	

Notes: 1. Two-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-oz copper covering 20 % of the top & bottom layers.

2. Four-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-ounce copper covering 20 % of the top & bottom layers and 0.5-ounce copper covering 90 % of the internal power plane and ground plane layers.

3. To calculate the die temperature for a given power dissipation

$$T_j = \text{Ambient Temperature} + [\ (\text{Power Dissipation in Watts}) * \theta_{ja}\ ]$$

4. To calculate the case temperature for a given power dissipation

$$T_c = T_j - [\ (\text{Power Dissipation in Watts}) * \psi_{jt}\ ]$$

5.7 Switching Characteristics—$\overline{\text{RESET}}$

Parameter	Symbol	Min	Max	Unit
$\overline{\text{RESET}}$ minimum pulse width low	T_{rstl}	1	—	µs
All bidirectional pins high-Z after $\overline{\text{RESET}}$ low	T_{rst2z}	/m	100	ns
Configuration pins setup before $\overline{\text{RESET}}$ high	T_{rstsu}	50	—	ns
Configuration pins hold after $\overline{\text{RESET}}$ high	T_{rsthld}	20	—	ns

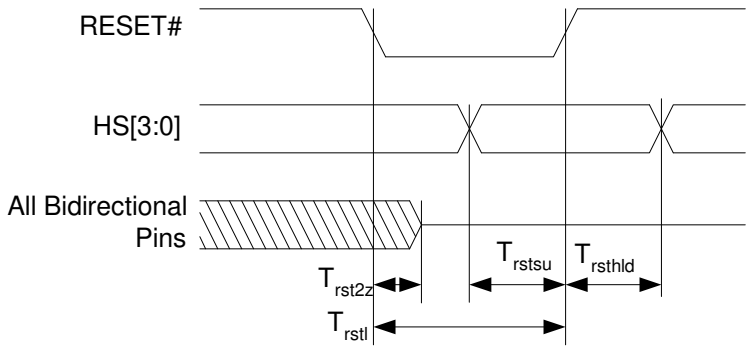


Figure 1. $\overline{\text{RESET}}$ Timing

5.8 Switching Characteristics — XTI

Parameter	Symbol	Min	Max	Unit
External Crystal operating frequency[1]	F_{xtal}	12.288	24.576	MHz
XTI period	T_{clki}	41	81.4	ns
XTI high time	T_{clkih}	16.4	/m	ns
XTI low time	T_{clkil}	16.4	—	ns
External Crystal Load Capacitance (parallel resonant)[2]	C_L	10	18	pF
External Crystal Equivalent Series Resistance	ESR	—	50	Ω

1. Part characterized with the following crystal frequency values: 12.288 and 24.576
2. C_L refers to the total load capacitance as specified by the crystal manufacturer. Crystals which require a C_L outside this range should be avoided. The crystal oscillator circuit design should follow the crystal manufacturer's recommendation for load capacitor selection.

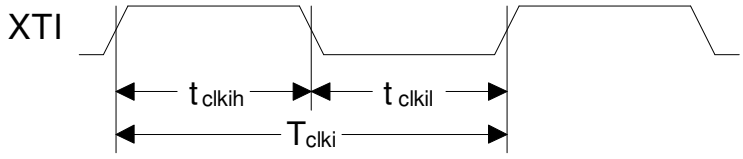


Figure 2. XTI Timing

5.9 Switching Characteristics — Internal Clock

Parameter	Symbol	Min	Max	Unit
Internal DCLK frequency[1]	F_{dclk}	—	130	MHz
CS49530x-CVZ CS49531x-CQZ CS49531x-CVZ CS49530x-DVZ CS49531x-DVZ	—	F_{xtal} F_{xtal} F_{xtal} F_{xtal} F_{xtal}	150 150 150 131 131	—
Internal DCLK period[1]	DCLKP	—	7.7	ns
CS49530x-CVZ CS49531x-CQZ CS49531x-CVZ CS49530x-DVZ CS49531x-DVZ	—	6.7 6.7 6.7 7.63 7.63	$1/F_{xtal}$ $1/F_{xtal}$ $1/F_{xtal}$ $1/F_{xtal}$ $1/F_{xtal}$	—

1. After initial power-on reset, $F_{dclk} = F_{xtal}$. After initial kick-start commands, the PLL is locked to max F_{dclk} and remains locked until the next power-on reset.

5.10 Switching Characteristics — Serial Control Port - SPI Slave Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1,2]	f_{spisck}	—	—	25	MHz
SCP_CS falling to SCP_CLK rising[2]	t_{spicss}	24	—	—	ns
SCP_CLK low time[2]	t_{spickl}	20	—	—	ns
SCP_CLK high time[2]	t_{spickh}	20	—	—	ns
Setup time SCP_MOSI input	t_{spidsu}	5	—	—	ns
Hold time SCP_MOSI input	t_{spidh}	5	—	—	ns
SCP_CLK low to SCP_MISO output valid[2]	t_{spidov}	—	—	11	ns
SCP_CLK falling to $\overline{\text{SCP\_IRQ}}$ rising[2]	$t_{spiirqh}$	—	—	20	ns
$\overline{\text{SCP\_CS}}$ rising to $\overline{\text{SCP\_IRQ}}$ falling[2]	$t_{spiirql}$	0	—	—	ns
SCP_CLK low to $\overline{\text{SCP\_CS}}$ rising[2]	t_{spicsh}	24	—	—	ns
$\overline{\text{SCP\_CS}}$ rising to SCP_MISO output high-Z	$t_{spicsdz}$	—	20	—	ns
SCP_CLK rising to $\overline{\text{SCP\_BSY}}$ falling[2]	$t_{spicbsyl}$	—	3*DCLKP+20	—	ns

1. The specification f_{spisck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Flow control using the $\overline{\text{SCP\_BSY}}$ pin should be implemented to prevent overflow of the input data buffer. At boot the maximum speed is $F_{xtal}/3$.
2. When SCP1 is in SPI slave mode, very slow rise and fall times of the SCP_CLK edges may make the edges of the SCP_CLK more susceptible to noise, resulting in non-smooth edges. Any glitch at the threshold levels of the SCP port input signals could result in abnormal operation of the port.

   In systems that have noise coupling onto SCP_CLK, slow rise and fall times may cause host communication problems. Increasing rise time makes host communication more reliable.

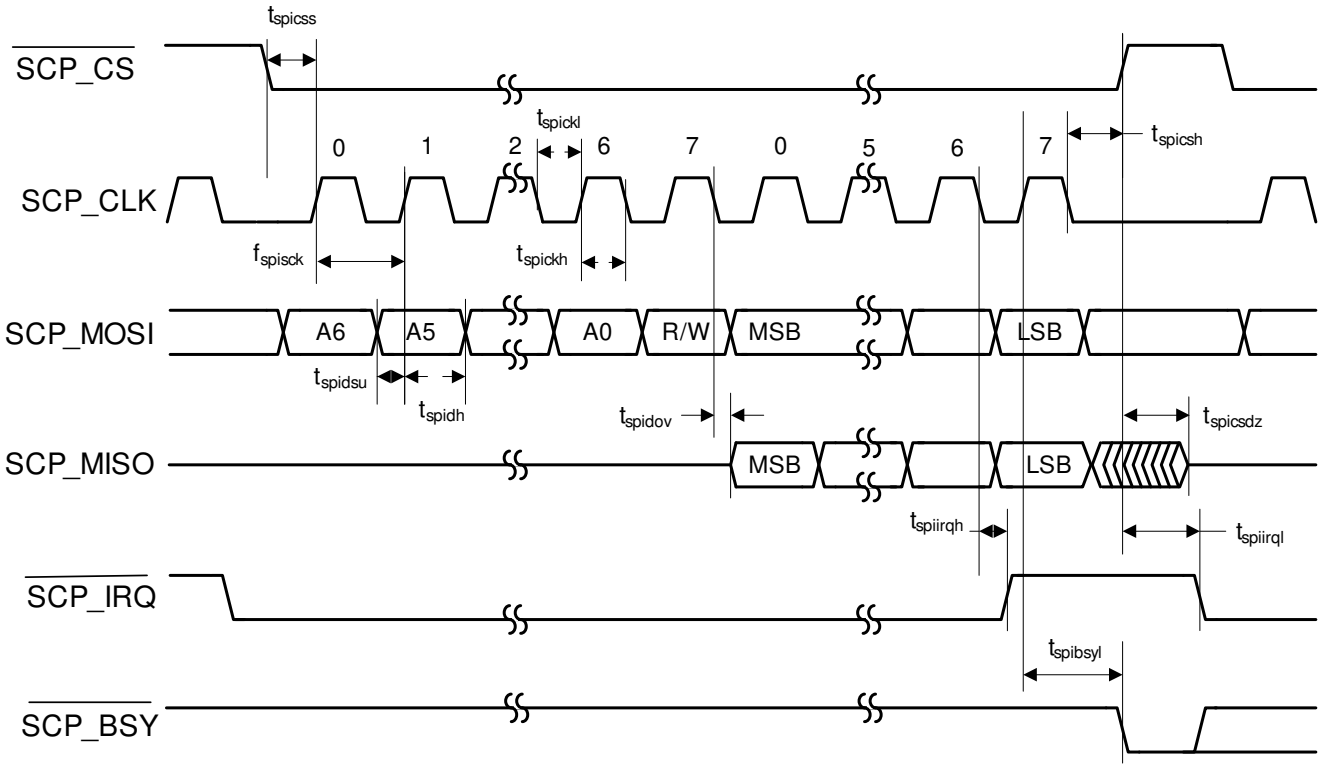


Figure 3. Serial Control Port - SPI Slave Mode Timing

5.11 Switching Characteristics — Serial Control Port - SPI Master Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1,2]	f_{spisck}	—	—	$F_{xtal}/2$	MHz
$\overline{\text{SCP\_CS}}$ falling to SCP_CLK rising [3]	t_{spicss}	—	11*DCLKP + (SCP_CLK PERIOD)/2	—	ns
SCP_CLK low time	t_{spickl}	16.9	—	—	ns
SCP_CLK high time	t_{spickh}	16.9	—	—	ns
Setup time SCP_MISO input	t_{spidsu}	11	—	—	ns
Hold time SCP_MISO input	t_{spidh}	5	—	—	ns
SCP_CLK low to SCP_MOSI output valid	t_{spidov}	—	—	11	ns
SCP_CLK low to $\overline{\text{SCP\_CS}}$ falling	t_{spicsl}	7	—	—	ns
SCP_CLK low to $\overline{\text{SCP\_CS}}$ rising	t_{spicsh}	—	11*DCLKP + (SCP_CLK PERIOD)/2	—	ns
Bus free time between active $\overline{\text{SCP\_CS}}$	t_{spicsx}	—	3*DCLKP	—	ns
SCP_CLK falling to SCP_MOSI output high-Z	t_{spidz}	—	—	20	ns

1. The specification f_{spisck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application.
2. See Section 5.8.
3. SCP_CLK PERIOD refers to the period of SCP_CLK as being used in a given application. It does not refer to a tested parameter

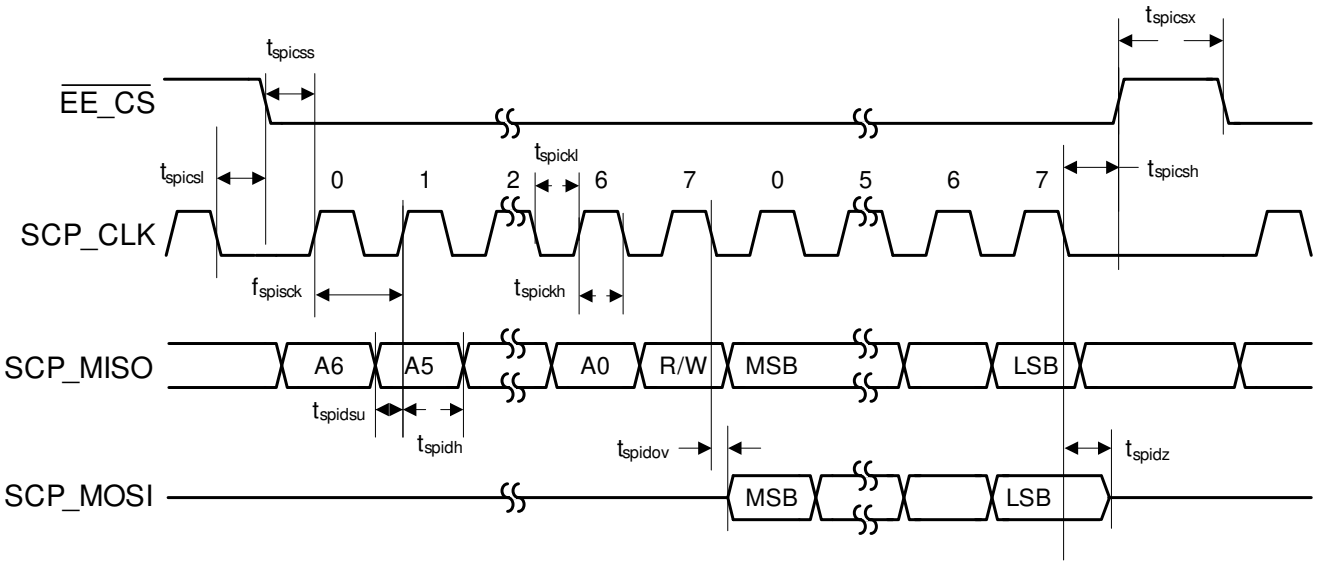


Figure 4. Serial Control Port - SPI Master Mode Timing

5.12 Switching Characteristics — Serial Control Port - I²C Slave Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1]	f_{iicck}	—	—	400	kHz
SCP_CLK low time	t_{iicckl}	1.25	—	—	µs
SCP_CLK high time	t_{iicckh}	1.25	—	—	µs
SCP_SCK rising to SCP_SDA rising or falling for START or STOP condition	$t_{iicckcmd}$	1.25	—	—	µs
START condition to SCP_CLK falling	$t_{iicstscl}$	1.25	—	—	µs
SCP_CLK falling to STOP condition	t_{iicstp}	2.5	—	—	µs
Bus free time between STOP and START conditions	t_{iicbft}	3	—	—	µs
Setup time SCP_SDA input valid to SCP_CLK rising	t_{iicsu}	100	—	—	ns
Hold time SCP_SDA input after SCP_CLK falling[2]	t_{iich}	0	—	—	ns
SCP_CLK low to SCP_SDA out valid	t_{iicdov}	—	—	18	ns
SCP_CLK falling to $\overline{\text{SCP\_IRQ}}$ rising	$t_{iicirqh}$	—	—	3*DCLKP + 40	ns
NAK condition to $\overline{\text{SCP\_IRQ}}$ low	$t_{iicirql}$	—	3*DCLKP + 20	—	ns
SCP_CLK rising to $\overline{\text{SCB\_BSY}}$ low	$t_{iicbsyl}$	—	3*DCLKP + 20	—	ns

1. The specification f_{iicck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Flow control using the $\overline{\text{SCP\_BSY}}$ pin should be implemented to prevent overflow of the input data buffer.
2. This parameter is measured from the ViL level at the falling edge of the clock.

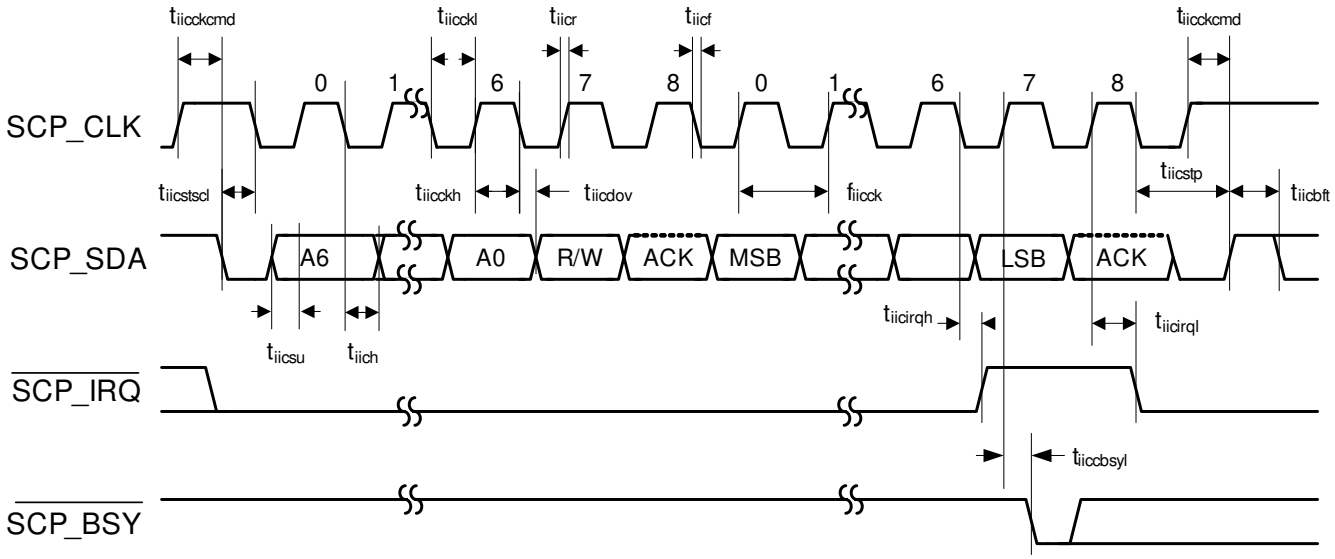


Figure 5. Serial Control Port - I²C Slave Mode Timing

5.13 Switching Characteristics — Serial Control Port - I²C Master Mode

Parameter	Symbol	Min	Max	Units
SCP_CLK frequency[1]	f_{iicck}	—	400	kHz
SCP_CLK low time	t_{iicckl}	1.25	—	µs
SCP_CLK high time	t_{iicckh}	1.25	—	µs
SCP_SCK rising to SCP_SDA rising or falling for START or STOP condition	$t_{iicckcmd}$	1.25	—	µs
START condition to SCP_CLK falling	$t_{iicstscl}$	1.25	—	µs
SCP_CLK falling to STOP condition	t_{iicstp}	2.5	—	µs
Bus free time between STOP and START conditions	t_{iicbft}	3	—	µs
Setup time SCP_SDA input valid to SCP_CLK rising	t_{iicsu}	100	—	ns
Hold time SCP_SDA input after SCP_CLK falling[2]	t_{iich}	0	—	ns
SCP_CLK low to SCP_SDA out valid	t_{iicdov}	—	36	ns

1. The specification f_{iicck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application.
2. This parameter is measured from the ViL level at the falling edge of the clock.

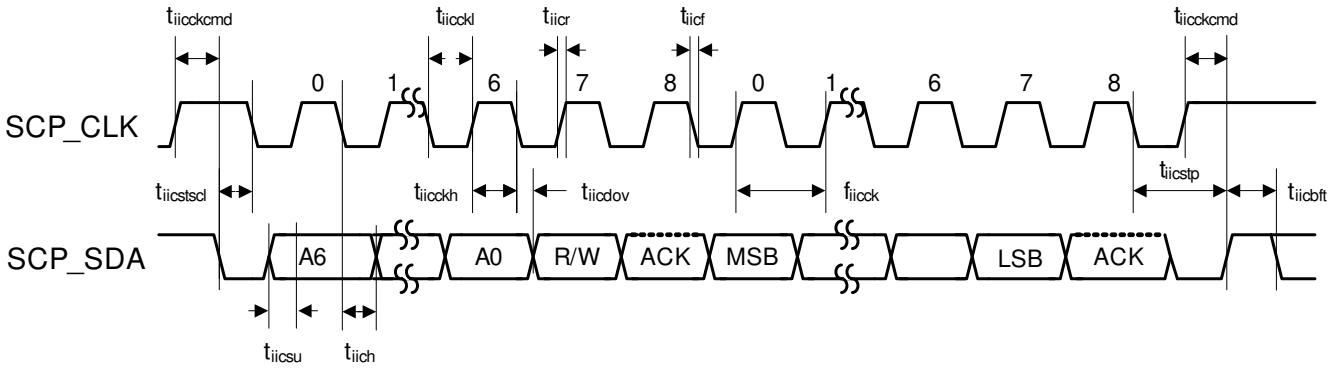


Figure 6. Serial Control Port - I²C Master Mode Timing

5.14 Switching Characteristics — Parallel Control Port - Intel Slave Mode

Parameter	Symbol	Min	Typical	Max	Unit
Address setup before PCP_CS and PCP_RD low or PCP_CS and PCP_WR low	t_{ias}	5	—	—	ns
Address hold time after PCP_CS and PCP_RD low or PCP_CS and PCP_WR high	t_{iah}	5	—	—	ns
Read					
Delay between PCP_RD then PCP_CS low or PCP_CS then PCP_RD low	t_{icdr}	0	—	—	ns
Data valid after PCP_CS and PCP_RD low	t_{idd}	—	—	18	ns
PCP_CS and PCP_RD low for read	t_{irpw}	24	—	—	ns
Data hold time after PCP_CS or PCP_RD high	t_{idhr}	8	—	—	ns
Data high-Z after PCP_CS or PCP_RD high	t_{idis}	—	—	18	ns
PCP_CS or PCP_RD high to PCP_CS and PCP_RD low for next read[1]	t_{ird}	30	—	—	ns
PCP_CS or PCP_RD high to PCP_CS and PCP_WR low for next write[1]	t_{irdtw}	30	—	—	ns
PCP_RD rising to PCP_IRQ rising	$t_{irdirqhl}$	—	—	12	ns
Write					
Delay between PCP_WR then PCP_CS low or PCP_CS then PCP_WR low	t_{icdw}	0	—	—	ns
Data setup before PCP_CS or PCP_WR high	t_{idsu}	8	—	—	ns
PCP_CS and PCP_WR low for write	t_{iwpw}	24	—	—	ns
Data hold after PCP_CS or PCP_WR high	t_{idhw}	8	—	—	ns
PCP_CS or PCP_WR high to PCP_CS and PCP_RD low for next read[1]	t_{iwtrd}	30	—	—	ns
PCP_CS or PCP_WR high to PCP_CS and PCP_WR low for next write[1]	t_{iwd}	30	—	—	ns
PCP_WR rising to PCP_BSY falling	$t_{iwrbsyl}$	—	2*DCLKP + 20	—	ns

1. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Hardware handshaking on the PCP_BSY pin/bit should be observed to prevent overflowing the input data buffer. AN288 *CS4953xx /CS497xxx Firmware User's Manual* should be consulted for the firmware speed limitations.

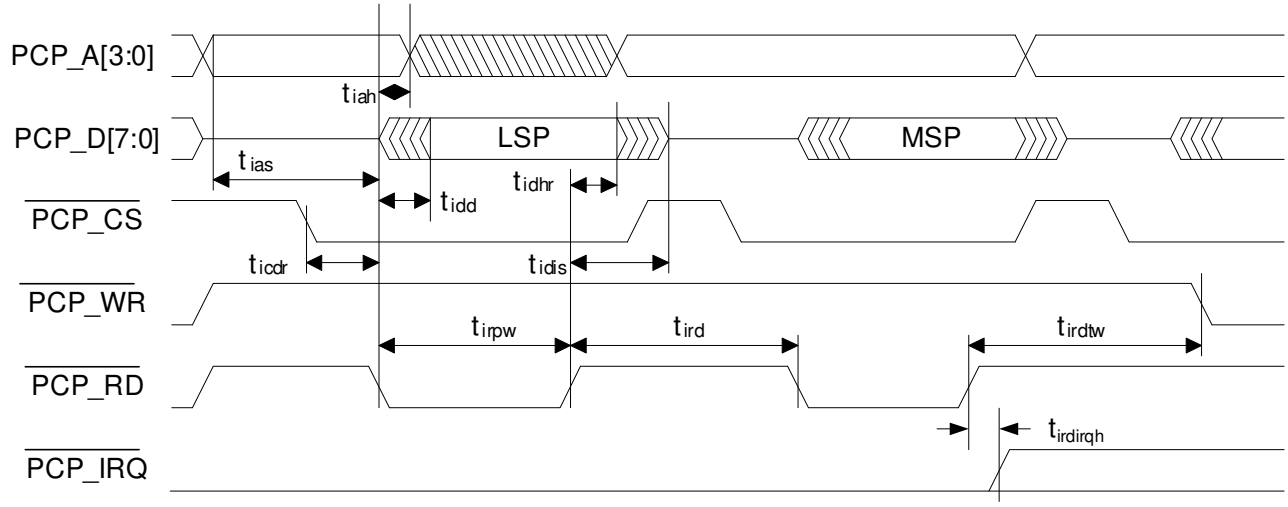


Figure 7. Parallel Control Port - Intel Slave Mode Read Cycle

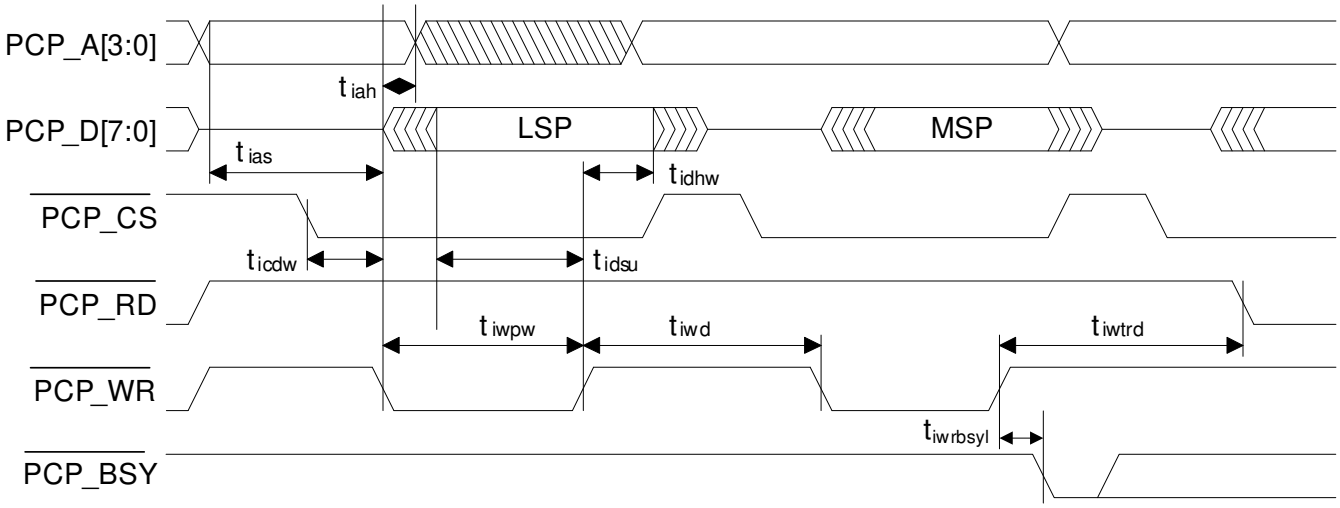


Figure 8. Parallel Control Port - Intel Slave Mode Write Cycle

5.15 Switching Characteristics — Parallel Control Port - Motorola Slave Mode

Parameter	Symbol	Min	Typical	Max	Unit
Address setup before PCP_CS and PCP_DS low	t_{mas}	5	—	—	ns
Address hold time after PCP_CS and PCP_DS low	t_{mah}	5	—	—	ns
Read					
Delay between PCP_DS then PCP_CS low or PCP_CS then PCP_DS# low	t_{mcdr}	0	—	—	ns
Data valid after PCP_CS and PCP_DS low with PCP_R/W high	t_{mdd}	—	—	19	ns
PCP_CS and PCP_DS low for read	t_{mrpw}	24	—	—	ns
Data hold time after PCP_CS or PCP_DS high after read	t_{mdhr}	8	—	—	ns
Data high-Z after PCP_CS or PCP_DS high after read	t_{mdis}	—	—	18	ns
PCP_CS or PCP_DS high to PCP_CS and PCP_DS low for next read[1]	t_{mrd}	30	—	—	ns
PCP_CS or PCP_DS high to PCP_CS and PCP_DS low for next write[1]	t_{mrdtw}	30	—	—	ns
PCP_RW rising to PCP_IRQ falling	$t_{mrwirqh}$	—	—	12	ns
Write					
Delay between PCP_DS then PCP_CS low or PCP_CS then PCP_DS low	t_{mcdw}	0	—	—	ns
Data setup before PCP_CS or PCP_DS high	t_{mdsu}	8	—	—	ns
PCP_CS and PCP_DS low for write	t_{mwpw}	24	—	—	ns
PCP_R/W setup before PCP_CS AND PCP_DS low	t_{mrwsu}	24	—	—	ns
PCP_R/W hold time after PCP_CS or PCP_DS high	t_{mrwhld}	8	—	—	ns
Data hold after PCP_CS or PCP_DS high	t_{mdhw}	8	—	—	ns
PCP_CS or PCP_DS high to PCP_CS and PCP_DS low with PCP_R/W high for next read[1]	t_{mwtrd}	30	—	—	ns
PCP_CS or PCP_DS high to PCP_CS and PCP_DS low for next write[1]	t_{mwd}	30	—	—	ns
PCP_RW rising to PCP_BSY falling	$t_{mrwbsyl}$	—	2*DCLKP + 20	—	ns

1. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Hardware handshaking on the PCP_BSY pin/bit should be observed to prevent overflowing the input data buffer. AN288 *CS4953xx/CS497xxx Firmware User's Manual* should be consulted for the firmware speed limitations.

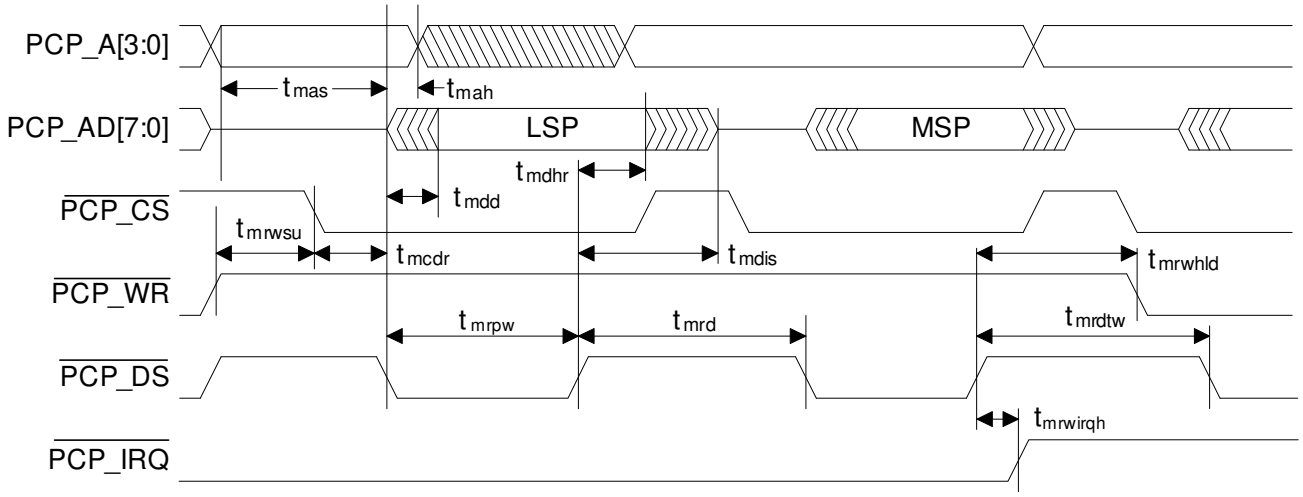


Figure 9. Parallel Control Port - Motorola Slave Mode Read Cycle Timing

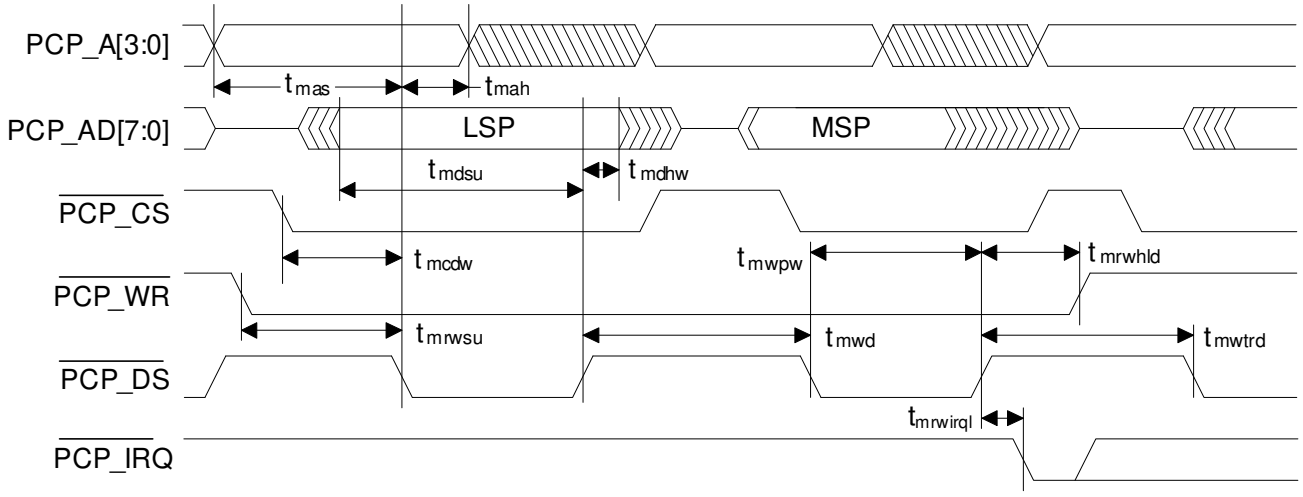


Figure 10. Parallel Control Port - Motorola Slave Mode Write Cycle Timing

5.16 Switching Characteristics — Digital Audio Slave Input Port

Parameter	Symbol	Min	Max	Unit
DAI_SCLK period	$T_{daiclkp}$	40	—	ns
DAI_SCLK duty cycle	—	45	55	%
DAI_LRCLK transition from DAI_SCLK active edge	$t_{daisstlr}$	10	—	ns
DAI_SCLK active edge from DAI_LRCLK transition	$t_{daislrts}$	10	—	ns
Setup time DAI_DATAn	t_{daidsu}	10	—	ns
Hold time DAI_DATAn	t_{daidh}	5	—	ns

Note: In these diagrams, falling edge is the inactive edge of DAI_SCLK.

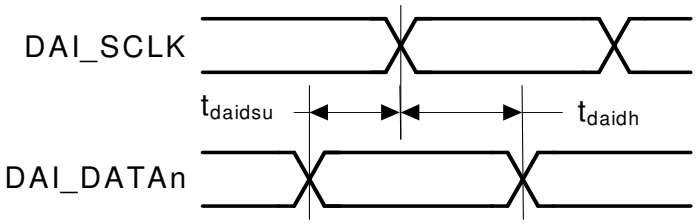


Figure 11. Digital Audio Input (DAI) Port Timing Diagram

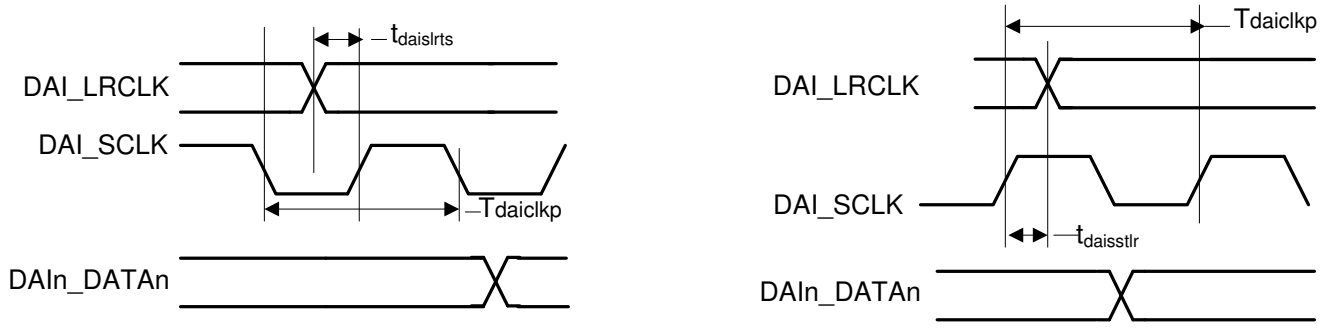
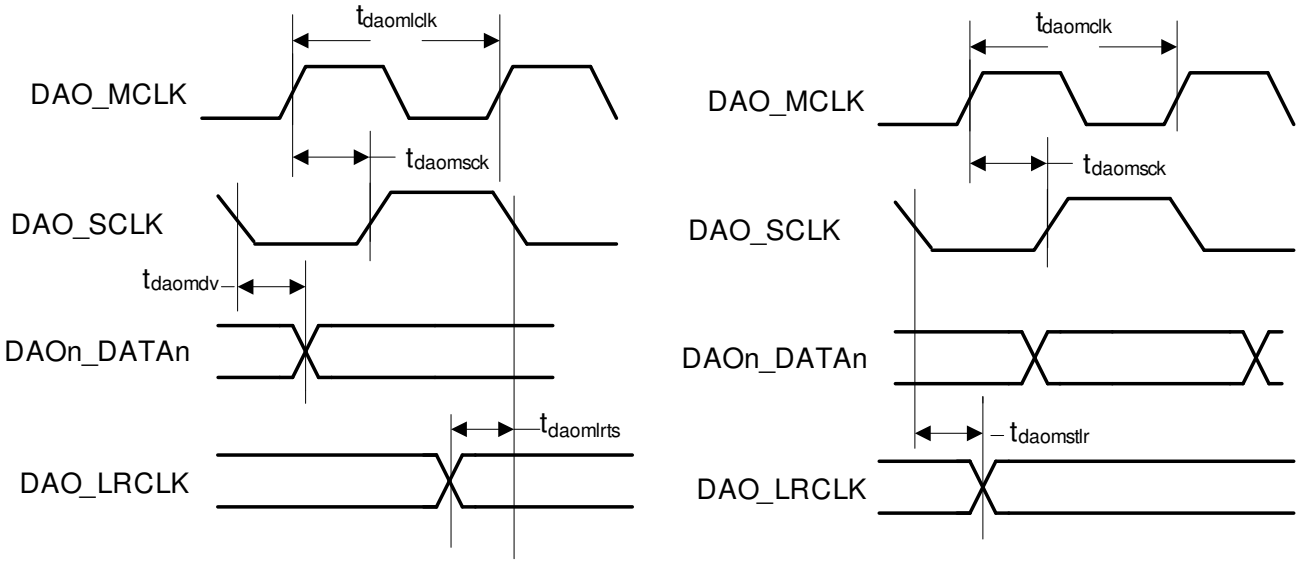


Figure 12. DAI Slave Timing Diagram

5.17 Switching Characteristics — Digital Audio Output Port

Parameter	Symbol	Min	Max	Unit
DAO_MCLK period	$T_{daomclk}$	40	—	ns
DAO_MCLK duty cycle	—	45	55	%
DAO_SCLK period for Master or Slave mode[1]	$T_{daosclk}$	40	—	ns
DAO_SCLK duty cycle for Master or Slave mode[1]	—	40	60	%
Master Mode (Output A1 Mode)[1,2]				
DAO_SCLK delay from DAO_MCLK rising edge, DAO_MCLK as an input	$t_{daomsck}$	—	19	ns
DAO_SCLK delay from DAO_LRCLK transition[3]	$t_{daomlrts}$	—	8	ns
DAO_LRCLK delay from DAO_SCLK transition[3]	$t_{daomstlr}$	—	8	ns
DAO1_DATA[3:0], DAO2_DATA[1:0] delay from DAO_SCLK transition[3]	t_{daomdv}	—	10	ns
Slave Mode (Output A0 Mode)[4]				
DAO_SCLK active edge to DAO_LRCLK transition	$t_{daosstlr}$	10	—	ns
DAO_LRCLK transition to DAO_SCLK active edge	$t_{daoslrts}$	10	—	ns
DAO_Dx delay from DAO_SCLK inactive edge	t_{daosdv}	—	12.5	ns

1. Master mode timing specifications are characterized, not production tested.
2. Master mode is defined as the CS4953xx driving both DAO_SCLK and DAO_LRCLK. When MCLK is an input, it is divided to produce DAO_SCLK, DAO_LRCLK.
3. This timing parameter is defined from the non-active edge of DAO_SCLK. The active edge of DAO_SCLK is the point at which the data is valid.
4. Slave mode is defined as DAO_SCLK, DAO_LRCLK driven by an external source.



Note: In these diagrams, Falling edge is the inactive edge of DAO_SCLK

Figure 13. Digital Audio Port Output Timing Master Mode

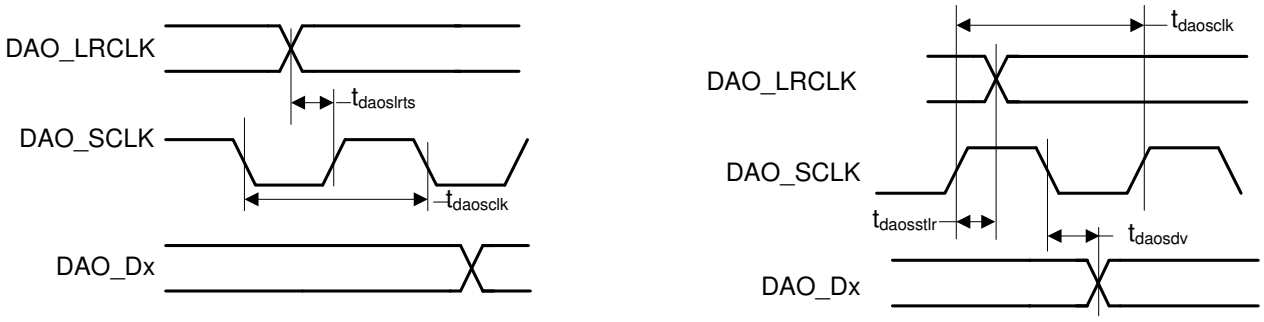


Figure 14. Digital Audio Output Timing, Slave Mode

5.18 Switching Characteristics — SDRAM Interface

Refer to Figure 15 through Figure 18.

(SD_CLKOUT = SD_CLKIN)

Parameter	Symbol	Min	Typical	Max	Unit
SD_CLKIN high time	t_{sdclkh}	2.3	—	—	ns
SD_CLKIN low time	t_{sdclkl}	2.3	—	—	ns
SD_CLKOUT rise/fall time	$t_{sdclkrf}$	—	—	1	ns
SD_CLKOUT Frequency	—	—	150	—	MHz
SD_CLKOUT duty cycle	—	45	—	55	%
SD_CLKOUT rising edge to signal valid	t_{sdcmdv}	—	—	3.8	ns
Signal hold from SD_CLKOUT rising edge	t_{sdcmdh}	—	1.1	—	ns
SD_CLKOUT rising edge to SD_DQMn valid	t_{sddqv}	—	3.8	—	ns
SD_DQMn hold from SD_CLKOUT rising edge	t_{sddqh}	1.38	—	—	ns
SD_DATA valid setup to SD_CLKIN rising edge	t_{sddsu}	1.3	—	—	ns
SD_DATA valid hold to SD_CLKIN rising edge	t_{sddh}	2.1	—	—	ns
SD_CLKOUT rising edge to ADDRn valid	t_{sdav}	—	3.8	—	ns