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CS5345

104 dB, 24-Bit, 192 kHz Stereo Audio ADC

A/D Features

- Multi-Bit Delta Sigma Modulator
- 104 dB Dynamic Range
- -95 dB THD+N
- Stereo 6:1 Input Multiplexer
- Programmable Gain Amplifier (PGA)
  - ± 12 dB Gain, 0.5 dB Step Size
  - Zero Crossing, Click-Free Transitions
- Stereo Microphone Inputs
  - +32 dB Gain Stage
  - Low-Noise Bias Supply
- Up to 192 kHz Sampling Rates
- Selectable Serial Audio Interface Formats
  - Left-Justified up to 24-bit
  - I²S up to 24-bit
- High-Pass Filter or DC Offset Calibration

System Features

- Power-Down Mode
- +3.3 V to +5 V Analog Power Supply, Nominal
- +3.3 V to +5 V Digital Power Supply, Nominal
- Direct Interface with 1.8 V to 5 V Logic Levels
- Pin-Compatible with CS4245

General Description

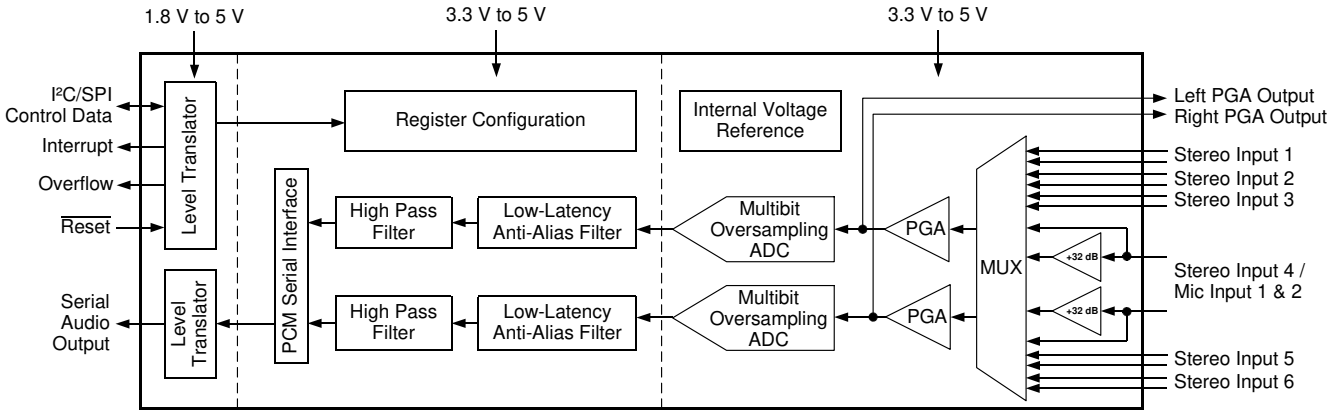
The CS5345 integrates an analog multiplexer, programmable gain amplifier, and stereo audio analog-to-digital converter. The CS5345 performs stereo analog-to-digital (A/D) conversion of up to 24-bit serial values at sample rates up to 192 kHz.

A 6:1 stereo input multiplexer is included for selecting between line-level and microphone-level inputs. The microphone input path includes a +32 dB gain stage and a low-noise bias voltage supply. The PGA is available for line or microphone inputs and provides gain/attenuation of ± 12 dB in 0.5 dB steps.

The output of the PGA is followed by an advanced 5th-order, multi-bit delta sigma modulator and digital filtering/decimation. Sampled data is transmitted by the serial audio interface at rates from 4 kHz to 192 kHz in either Slave or Master Mode.

Integrated level translators allow easy interfacing between the CS5345 and other devices operating over a wide range of logic levels.

The CS5345 is available in a 48-pin LQFP package in Commercial (-10° to +70° C) grade. The CDB5345 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please refer to "Ordering Information" on page 42 for complete details.



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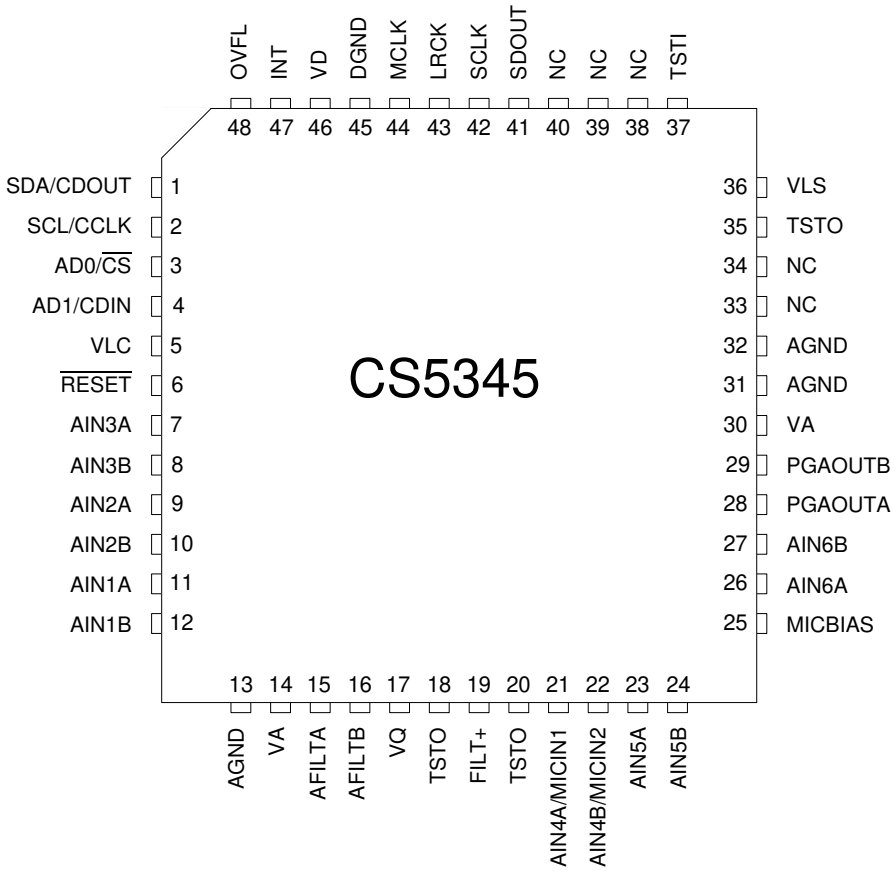
1. PIN DESCRIPTIONS



Pin Name	#	Pin Description
SDA/CDOUT	1	**Serial Control Data** (*Input*/*Output*) - SDA is a data I/O in I²C® Mode. CDOUT is the output data line for the control port interface in SPI™ Mode.
SCL/CCLK	2	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port.
AD0/CS	3	**Address Bit 0 (I²C) / Control Port Chip Select (SPI)** *(Input)* - AD0 is a chip address pin in I²C Mode; CS is the chip-select signal for SPI format.
AD1/CDIN	4	**Address Bit 1 (I²C) / Serial Control Data Input (SPI)** *(Input)* - AD1 is a chip address pin in I²C Mode; CDIN is the input data line for the control port interface in SPI Mode.
VLC	5	**Control Port Power** (*Input*) - Determines the required signal level for the control port interface. Refer to the Recommended Operating Conditions for appropriate voltages.
RESET	6	**Reset** (*Input*) - The device enters a low-power mode when this pin is driven low.
AIN3A AIN3B	7 8	**Stereo Analog Input 3** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table.
AIN2A AIN2B	9 10	**Stereo Analog Input 2** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table.

AIN1A AIN1B	11 12	**Stereo Analog Input 1** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table.
AGND	13	**Analog Ground** (*Input*) - Ground reference for the internal analog section.
VA	14	**Analog Power** *(Input)* - Positive power for the internal analog section.
AFILTA	15	**Antialias Filter Connection** (*Output*) - Antialias filter connection for the channel A ADC input.
AFILTB	16	**Antialias Filter Connection** (*Output*) - Antialias filter connection for the channel B ADC input.
VQ	17	**Quiescent Voltage** (*Output*) - Filter connection for the internal quiescent reference voltage.
TSTO	18	**Test Pin** (*Output*) - This pin must be left unconnected.
FILT+	19	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits.
TSTO	20	**Test Pin -** This pin must be left unconnected.
AIN4A/MICIN1 AIN4B/MICIN2	21 22	**Stereo Analog Input 4** / **Microphone Input 1 & 2** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table.
AIN5A AIN5B	23 24	**Stereo Analog Input 5** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table.
MICBIAS	25	**Microphone Bias Supply** (*Output*) - Low-noise bias supply for external microphone. Electrical characteristics are specified in the DC Electrical Characteristics specification table.
AIN6A AIN6B	26 27	**Stereo Analog Input 6** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table.
PGAOUTA PGAOUTB	28 29	**PGA Analog Audio Output** (*Output*) - Either an analog output from the PGA block or high impedance. See "PGAOut Source Select (Bit 6)" on page 34.
VA	30	**Analog Power** *(Input)* - Positive power for the internal analog section.
AGND	31 32	**Analog Ground** (*Input*) - Ground reference for the internal analog section.
NC	33 34	**No Connect** - These pins are not connected internally and should be tied to ground to minimize any potential coupling effects.
TSTO	35	**Test Pin** (*Output*) - This pin must be left unconnected.
VLS	36	**Serial Audio Interface Power** (*Input*) - Determines the required signal level for the serial audio interface. Refer to the Recommended Operating Conditions for appropriate voltages.
TSTI	37	**Test Pin** (*Input*) - This pin must be connected to ground.
NC	38, 39, 40	**No Connect** - These pins are not connected internally and should be tied to ground to minimize any potential coupling effects.
SDOUT	41	**Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data.
SCLK	42	**Serial Clock** *(Input/Output)* - Serial clock for the serial audio interface.
LRCK	43	**Left Right Clock** *(Input/Output)* - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	44	**Master Clock** (*Input*) - Clock source for the ADC's delta-sigma modulators.
DGND	45	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
VD	46	**Digital Power** (*Input*) - Positive power for the internal digital section.
INT	47	**Interrupt** (*Output*) - Indicates an interrupt condition has occurred.
OVFL	48	**Overflow** (*Output*) - Indicates an ADC overflow condition is present.

2. CHARACTERISTICS AND SPECIFICATIONS

SPECIFIED OPERATING CONDITIONS

AGND = DGND = 0 V; All voltages with respect to ground.

Parameters		Symbol	Min	Nom	Max	Units
DC Power Supplies:	Analog	VA	3.13	5.0	5.25	V
	Digital	VD	3.13	3.3	(Note 1)	V
	Logic - Serial Port	VLS	1.71	3.3	5.25	V
	Logic - Control Port	VLC	1.71	3.3	5.25	V
Ambient Operating Temperature (Power Applied)		T_A	-10	-	+70	°C

Notes: 1. Maximum of VA+0.25 V or 5.25 V, whichever is less.

ABSOLUTE MAXIMUM RATINGS

AGND = DGND = 0 V All voltages with respect to ground. (Note 2)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Analog	VA	-0.3	+6.0	V
	Digital	VD	-0.3	+6.0	V
	Logic - Serial Port	VLS	-0.3	+6.0	V
	Logic - Control Port	VLC	-0.3	+6.0	V
Input Current	(Note 3)	I_{in}	-	±10	mA
Analog Input Voltage		V_{INA}	AGND-0.3	VA+0.3	V
Digital Input Voltage	Logic - Serial Port	V_{IND-S}	-0.3	VLS+0.3	V
	Logic - Control Port	V_{IND-C}	-0.3	VLC+0.3	V
Ambient Operating Temperature (Power Applied)		T_A	-50	+125	°C
Storage Temperature		T_{stg}	-65	+150	°C

2. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.
3. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

ADC ANALOG CHARACTERISTICS

Test conditions (unless otherwise specified): AGND = DGND = 0 V; VA = 3.13 V to 5.25 V; VD = 3.13 V to 5.25 V or VA + 0.25 V, whichever is less; VLS = VLC = 1.71 V to 5.25 V; T_A = -10° to +70° C for Commercial; Input test signal: 1 kHz sine wave; measurement bandwidth is 10 Hz to 20 kHz; Fs = 48/96/192 kHz.; All connections as shown in Figure 7 on page 22.

Line-Level Inputs					
Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Performance for VA = 4.75 V to 5.25 V					
Dynamic Range					
PGA Setting: -12 dB to +6 dB					
A-weighted		98	104	-	dB
unweighted		95	101	-	dB
(Note 6) 40 kHz bandwidth unweighted		-	98	-	dB
PGA Setting: +12 dB Gain					
A-weighted		92	98	-	dB
unweighted		89	95	-	dB
(Note 6) 40 kHz bandwidth unweighted		-	92	-	dB
Total Harmonic Distortion + Noise (Note 5)					
PGA Setting: -12 dB to +6 dB					
-1 dB		-	-95	-89	dB
-20 dB		-	-81	-	dB
-60 dB		-	-41	-	dB
(Note 6) 40 kHz bandwidth -1 dB	THD+N	-	-92	-	dB
PGA Setting: +12 dB Gain					
-1 dB		-	-92	-86	dB
-20 dB		-	-75	-	dB
-60 dB		-	-35	-	dB
(Note 6) 40 kHz bandwidth -1 dB		-	-89	-	dB
Dynamic Performance for VA = 3.13 V to 3.46 V					
Dynamic Range					
PGA Setting: -12 dB to +6 dB					
A-weighted		93	101	-	dB
unweighted		90	98	-	dB
(Note 6) 40 kHz bandwidth unweighted		-	95	-	dB
PGA Setting: +12 dB Gain					
A-weighted		89	95	-	dB
unweighted		86	92	-	dB
(Note 6) 40 kHz bandwidth unweighted		-	89	-	dB
Total Harmonic Distortion + Noise (Note 5)					
PGA Setting: -12 dB to +6 dB					
-1 dB		-	-92	-86	dB
-20 dB		-	-78	-	dB
-60 dB		-	-38	-	dB
(Note 6) 40 kHz bandwidth -1 dB	THD+N	-	-84	-	dB
PGA Setting: +12 dB Gain					
-1 dB		-	-89	-83	dB
-20 dB		-	-72	-	dB
-60 dB		-	-32	-	dB
(Note 6) 40 kHz bandwidth -1 dB		-	-81	-	dB

Line-Level Inputs					
		Commercial Grade			
Parameter	Symbol	Min	Typ	Max	Unit
Interchannel Isolation		-	90	-	dB

DC Accuracy					
Gain Error		-	-	±10	%
Gain Drift		-	±100	-	ppm/°C
Line-Level Input Characteristics					
Full-scale Input Voltage		0.51*VA	0.57*VA	0.63*VA	V_{pp}
Input Impedance (Note 4)		6.12	6.8	7.48	kΩ
Maximum Interchannel Input Impedance Mismatch		-	5	-	%

Line-Level and Microphone-Level Inputs

Parameter	Symbol	Commercial Grade			Unit
		Min	Typ	Max	
DC Accuracy					
Interchannel Gain Mismatch		-	0.1	-	dB
Programmable Gain Characteristics					
Gain Step Size		-	0.5	-	dB
Absolute Gain Step Error		-	-	0.4	dB

4. Valid for the selected input pair.

ADC ANALOG CHARACTERISTICS

(Continued)

Microphone-Level Inputs					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Dynamic Performance for VA = 4.75 V to 5.25 V					
Dynamic Range					
PGA Setting: -12 dB to 0 dB					
A-weighted		77	83	-	dB
unweighted		74	80	-	dB
PGA Setting: +12 dB					
A-weighted		65	71	-	dB
unweighted		62	68	-	dB
Total Harmonic Distortion + Noise (Note 5)					
PGA Setting: -12 dB to 0 dB					
-1 dB	THD+N	-	-80	-74	dB
-20 dB		-	-60	-	dB
-60 dB		-	-20	-	dB
PGA Setting: +12 dB					
-1 dB		-	-68	-	dB
Dynamic Performance for VA = 3.13 V to 3.46 V					
Dynamic Range					
PGA Setting: -12 dB to 0 dB					
A-weighted		77	83	-	dB
unweighted		74	80	-	dB
PGA Setting: +12 dB					
A-weighted		65	71	-	dB
unweighted		62	68	-	dB
Total Harmonic Distortion + Noise (Note 5)					
PGA Setting: -12 dB to 0 dB					
-1 dB	THD+N	-	-80	-74	dB
-20 dB		-	-60	-	dB
-60 dB		-	-20	-	dB
PGA Setting: +12 dB					
-1 dB		-	-68	-	dB
Interchannel Isolation		-	80	-	dB
DC Accuracy					
Gain Error		-	±5	-	%
Gain Drift		-	±300	-	ppm/°C
Microphone-Level Input Characteristics					
Full-scale Input Voltage		0.013*VA	0.017*VA	0.021*VA	V_{pp}
Input Impedance (Note 7)		-	60	-	kΩ

5. Referred to the typical line-level full-scale input voltage
6. Valid for Double- and Quad-Speed Modes only.
7. Valid when the microphone-level inputs are selected.

ADC DIGITAL FILTER CHARACTERISTICS

Parameter (Notes 8, 10)			Symbol	Min	Typ	Max	Unit
Single-Speed Mode							
Passband	(-0.1 dB)			0	-	0.4896	Fs
Passband Ripple				-	-	0.035	dB
Stopband				0.5688	-	-	Fs
Stopband Attenuation				70	-	-	dB
Total Group Delay (Fs = Output Sample Rate)			t_{gd}	-	12/Fs	-	s
Double-Speed Mode							
Passband	(-0.1 dB)			0	-	0.4896	Fs
Passband Ripple				-	-	0.025	dB
Stopband				0.5604	-	-	Fs
Stopband Attenuation				69	-	-	dB
Total Group Delay (Fs = Output Sample Rate)			t_{gd}	-	9/Fs	-	s
Quad-Speed Mode							
Passband	(-0.1 dB)			0	-	0.2604	Fs
Passband Ripple				-	-	0.025	dB
Stopband				0.5000	-	-	Fs
Stopband Attenuation				60	-	-	dB
Total Group Delay (Fs = Output Sample Rate)			t_{gd}	-	5/Fs	-	s
High-Pass Filter Characteristics							
Frequency Response	-3.0 dB			-	1	-	Hz
	-0.13 dB	(Note 9)			20	-	Hz
Phase Deviation	@ 20 Hz	(Note 9)		-	10	-	Deg
Passband Ripple				-	-	0	dB
Filter Settling Time					10^5/Fs		s

8. Filter response is guaranteed by design.
9. Response shown is for Fs = 48 kHz.
10. Response is clock-dependent and will scale with Fs. Note that the response plots (Figures 13 to 24) are normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.

PGAOUT ANALOG CHARACTERISTICS

Test conditions (unless otherwise specified): AGND = DGND = 0 V; VA = 3.13 V to 5.25 V; VD = 3.13 V to 5.25 V or VA + 0.25 V, whichever is less; VLS = VLC = 1.71 V to 5.25 V; T_A = -10° to +70° C; Input test signal: 1 kHz sine wave; Measurement bandwidth: 10 Hz to 20 kHz; Fs = 48/96/192 kHz; Synchronous mode; All connections as shown in Figure 7 on page 22.

VA = 4.75 V to 5.25 V					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Dynamic Performance with PGA Line-Level Input Selected					
Dynamic Range					
PGA Setting: -12 dB to +6 dB					
A-weighted		98	104	-	dB
unweighted		95	101	-	dB
PGA Setting: +12 dB Gain					
A-weighted		92	98	-	dB
unweighted		89	95	-	dB
Total Harmonic Distortion + Noise (Note 11)					
PGA Setting: -12 dB to +6 dB					
-1 dB		-	-80	-74	dB
-20 dB		-	-81	-	dB
-60 dB	THD+N	-	-41	-	dB
PGA Setting: +12 dB Gain					
-1 dB		-	-80	-74	dB
-20 dB		-	-75	-	dB
-60 dB		-	-35	-	dB
Dynamic Performance with PGA Mic-Level Input Selected					
Dynamic Range					
PGA Setting: -12 dB to 0 dB					
A-weighted		77	83	-	dB
unweighted		74	80	-	dB
PGA Setting: +12 dB					
A-weighted		65	71	-	dB
unweighted		62	68	-	dB
Total Harmonic Distortion + Noise (Note 11)					
PGA Setting: -12 dB to 0 dB					
-1 dB		-	-74	-68	dB
-20 dB	THD+N	-	-60	-	dB
-60 dB		-	-20	-	dB
PGA Setting: +12 dB					
-1 dB		-	-68	-	dB

11. Referred to the typical Line-Level Full-Scale Input Voltage.

PGAOUT ANALOG CHARACTERISTICS

(Continued)

VA = 3.13 V to 3.46 V					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Dynamic Performance with PGA Line-Level Input Selected					
Dynamic Range					
PGA Setting: -12 dB to +6 dB					
A-weighted		93	101	-	dB
unweighted		90	98	-	dB
PGA Setting: +12 dB Gain					
A-weighted		89	95	-	dB
unweighted		86	92	-	dB
Total Harmonic Distortion + Noise (Note 11)					
PGA Setting: -12 dB to +6 dB					
-1 dB	THD+N	-	-80	-74	dB
-20 dB		-	-78	-	dB
-60 dB		-	-38	-	dB
PGA Setting: +12 dB Gain					
-1 dB		-	-80	-74	dB
-20 dB		-	-72	-	dB
-60 dB		-	-32	-	dB
Dynamic Performance with PGA Mic Level-Input Selected					
Dynamic Range					
PGA Setting: -12 dB to 0 dB					
A-weighted		77	83	-	dB
unweighted		74	80	-	dB
PGA Setting: +12 dB					
A-weighted		65	71	-	dB
unweighted		62	68	-	dB
Total Harmonic Distortion + Noise (Note 11)					
PGA Setting: -12 dB to 0 dB					
-1 dB	THD+N	-	-74	-68	dB
-20 dB		-	-60	-	dB
-60 dB		-	-20	-	dB
PGA Setting: +12 dB					
-1 dB		-	-68	-	dB

PGAOUT ANALOG CHARACTERISTICS

(Continued)

VA = 3.13 V to 5.25 V					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
DC Accuracy with PGA Line Level Input Selected					
Interchannel Gain Mismatch		-	0.1	-	dB
Gain Error		-	±5	-	%
Gain Drift		-	±100	-	ppm/°C
DC Accuracy with PGA Mic Level Input Selected					
Interchannel Gain Mismatch		-	0.3	-	dB
Gain Error		-	±5	-	%
Gain Drift		-	±300	-	ppm/°C
Analog Output					
Frequency Response 10 Hz to 20 kHz (Note 12)		-0.1dB	-	+0.1dB	dB
Analog In to Analog Out Phase Shift		-	180	-	deg
DC Current draw from a PGAOUT pin	I_{OUT}	-	-	1	µA
AC-Load Resistance	R_L	100	-	-	kΩ
Load Capacitance	C_L	-	-	20	pF

12. Guaranteed by design.

DC ELECTRICAL CHARACTERISTICS

AGND = DGND = 0 V, all voltages with respect to ground. MCLK=12.288 MHz; Fs=48 kHz; Master Mode.

Parameter		Symbol	Min	Typ	Max	Unit
Power Supply Current	VA = 5 V	I_A	-	41	50	mA
(Normal Operation)	VA = 3.3 V	I_A	-	37	45	mA
	VD, VLS, VLC = 5 V	I_D	-	39	47	mA
	VD, VLS, VLC = 3.3 V	I_D	-	23	28	mA
Power Supply Current	VA = 5 V	I_A	-	0.50	-	mA
(Power-Down Mode) (Note 13)	VLS, VLC, VD=5 V	I_D	-	0.54	-	mA
Power Consumption						
(Normal Operation)	VA, VD, VLS, VLC = 5 V	-	-	400	485	mW
	VA, VD, VLS, VLC = 3.3 V	-	-	198	241	mW
(Power-Down Mode)	VA, VD, VLS, VLC = 5 V	-	-	4.2	-	mW
Power Supply Rejection Ratio (1 kHz)	(Note 14)	PSRR	-	55	-	dB
VQ Characteristics						
Quiescent Voltage		VQ	-	0.5 x VA	-	VDC
DC Current from VQ	(Note 15)	I_Q	-	-	1	µA
VQ Output Impedance		Z_Q	-	23	-	kΩ
FILT+ Nominal Voltage		FILT+	-	VA	-	VDC
Microphone Bias Voltage		MICBIAS	-	0.8 x VA	-	VDC
Current from MICBIAS		I_{MB}	-	-	2	mA

13. Power-Down Mode is defines as $\overline{\text{RESET}}$ = Low with all clock and data lines held static and no analog input.
14. Valid with the recommended capacitor values on FILT+ and VQ as shown in the Typical Connection Diagram.
15. Guaranteed by design. The DC current draw represents the allowed current draw due to typical leakage through the electrolytic de-coupling capacitors.

DIGITAL INTERFACE CHARACTERISTICS

Test conditions (unless otherwise specified): AGND = DGND = 0 V; VLS = VLC = 1.71 V to 5.25 V.

Parameters (Note 16)		Symbol	Min	Typ	Max	Units
High-Level Input Voltage						
VL = 1.71 V	Serial Port	V_{IH}	0.8xVLS	-	-	V
	Control Port	V_{IH}	0.8xVLC	-	-	V
VL > 2.0 V	Serial Port	V_{IH}	0.7xVLS	-	-	V
	Control Port	V_{IH}	0.7xVLC	-	-	V
Low-Level Input Voltage	Serial Port	V_{IL}	-	-	0.2xVLS	V
	Control Port	V_{IL}	-	-	0.2xVLC	V
High-Level Output Voltage at I_o = 2 mA	Serial Port	V_{OH}	VLS-1.0	-	-	V
	Control Port	V_{OH}	VLC-1.0	-	-	V
Low-Level Output Voltage at I_o = 2 mA	Serial Port	V_{OL}	-	-	0.4	V
	Control Port	V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	-	±10	µA
Input Capacitance	(Note 17)		-	-	1	pF
Minimum OVFL Active Time			$\frac{10^6}{LRCK}$	-	-	µs

16. Serial Port signals include: MCLK, SCLK, LRCK, SDOUT.
    Control Port signals include: SCL/CCLK, SDA/CDOUT, AD0/$\overline{CS}$, AD1/CDIN, $\overline{RESET}$, INT, OVFL.
17. Guaranteed by design.

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT

Logic '0' = DGND = AGND = 0 V; Logic '1' = VL, C_L = 20 pF. (Note 18)

Parameter		Symbol	Min	Typ	Max	Unit
Sample Rate	Single-Speed Mode	Fs	4	-	50	kHz
	Double-Speed Mode	Fs	50	-	100	kHz
	Quad-Speed Mode	Fs	100	-	200	kHz
MCLK Specifications						
MCLK Frequency		fmclk	1.024	-	51.200	MHz
MCLK Input Pulse Width High/Low		tclkhl	8	-	-	ns
Master Mode						
LRCK Duty Cycle			-	50	-	%
SCLK Duty Cycle			-	50	-	%
SCLK falling to LRCK edge		t_{slr}	-10	-	10	ns
SCLK falling to SDOUT valid		t_{sdo}	0	-	36	ns
Slave Mode						
LRCK Duty Cycle			40	50	60	%
SCLK Period						
	Single-Speed Mode	t_{sclkw}	$\frac{10^9}{(128)Fs}$	-	-	ns
	Double-Speed Mode	t_{sclkw}	$\frac{10^9}{(64)Fs}$	-	-	ns
	Quad-Speed Mode	t_{sclkw}	$\frac{10^9}{(64)Fs}$	-	-	ns
SCLK Pulse Width High		t_{sclkh}	30	-	-	ns
SCLK Pulse Width Low		t_{sclkl}	48	-	-	ns
SCLK falling to LRCK edge		t_{slr}	-10	-	10	ns
SCLK falling to SDOUT valid		t_{sdo}	0	-	36	ns

18. See Figure 1 and Figure 2 on page 18.

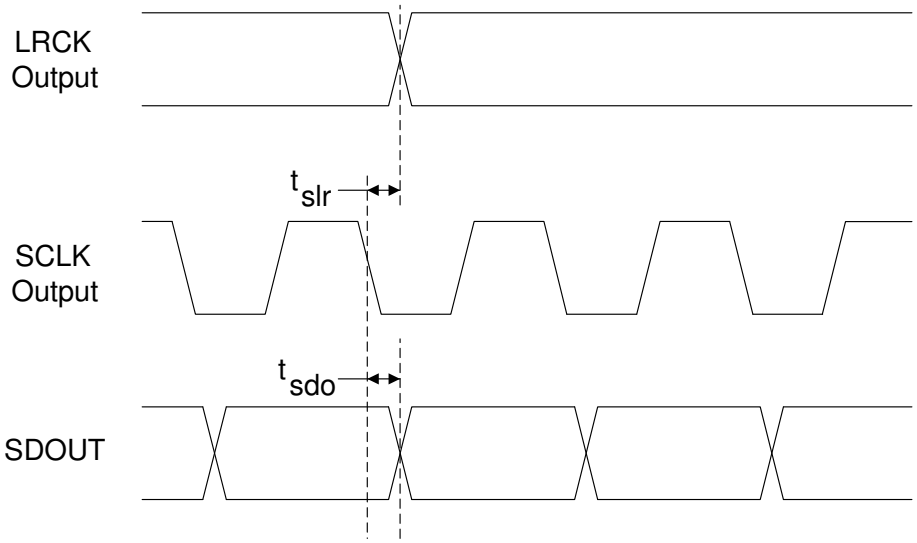


Figure 1. Master Mode Serial Audio Port Timing

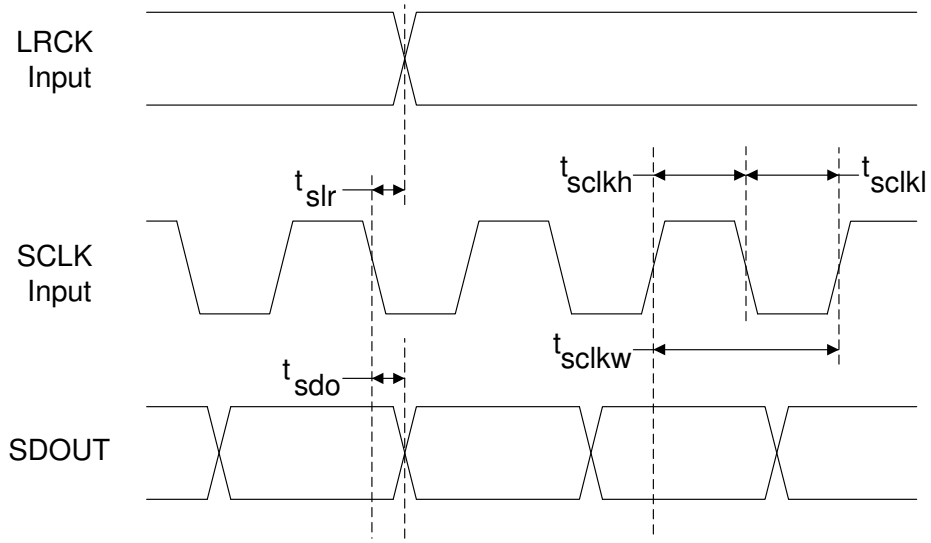


Figure 2. Slave Mode Serial Audio Port Timing

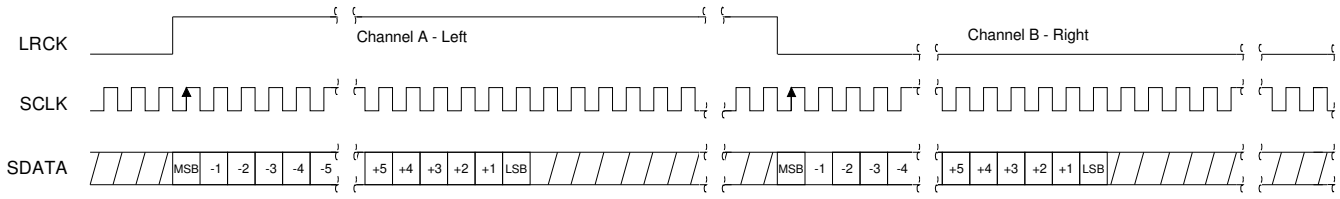


Figure 3. Format 0, Left-Justified up to 24-Bit Data

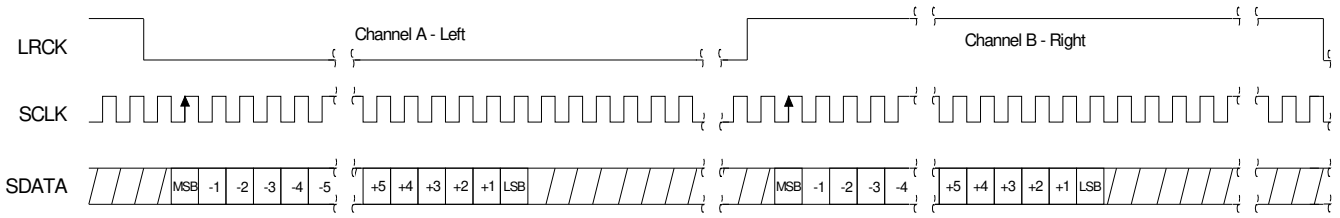


Figure 4. Format 1, I²S up to 24-Bit Data

SWITCHING CHARACTERISTICS - CONTROL PORT - I²C FORMAT

Inputs: Logic 0 = DGND = AGND = 0 V, Logic 1 = VLC, C_L = 30 pF.

Parameter		Symbol	Min	Max	Unit
SCL Clock Frequency		f_{scl}	-	100	kHz
$\overline{\text{RESET}}$ Rising Edge to Start		t_{irs}	500	-	ns
Bus Free Time Between Transmissions		t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)		t_{hdst}	4.0	-	µs
Clock Low time		t_{low}	4.7	-	µs
Clock High Time		t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition		t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling	(Note 19)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising		t_{sud}	250	-	ns
Rise Time of SCL and SDA	(Note 20)	t_{rc}, t_{rd}	-	1	µs
Fall Time SCL and SDA	(Note 20)	t_{fc}, t_{fd}	-	300	ns
Setup Time for Stop Condition		t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling		t_{ack}	300	1000	ns

19. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.
20. Guaranteed by design.

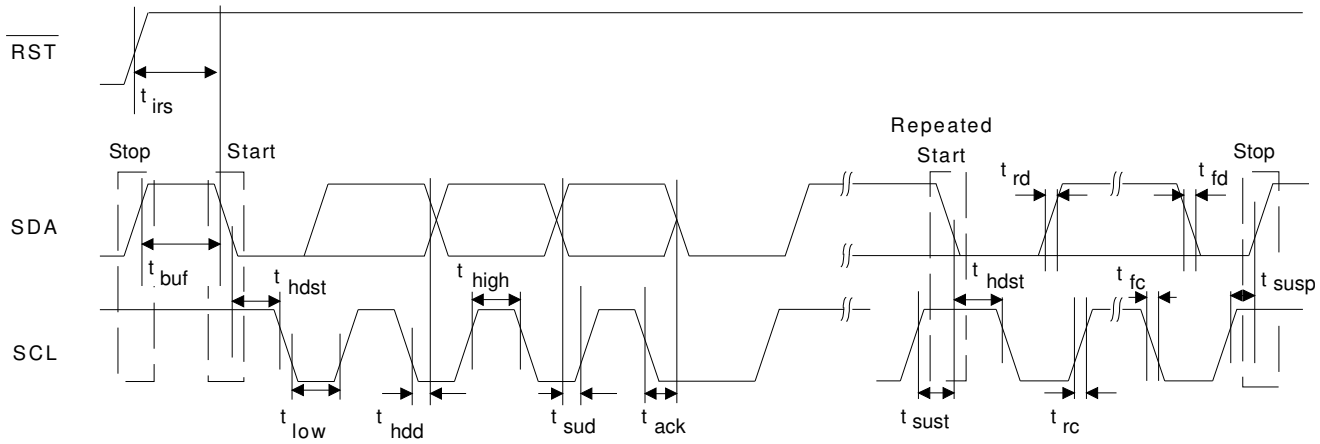


Figure 5. Control Port Timing - I²C Format

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI FORMAT

Inputs: Logic 0 = DGND = AGND = 0 V, Logic 1 = VLC, C_L = 30 pF.

Parameter		Symbol	Min	Max	Units
CCLK Clock Frequency		f_{sck}	-	6.0	MHz
$\overline{\text{RESET}}$ Rising Edge to $\overline{\text{CS}}$ Falling		t_{srs}	500	-	ns
$\overline{\text{CS}}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
$\overline{\text{CS}}$ Falling to CCLK Edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 21)	t_{dh}	15	-	ns
CCLK Falling to CDOUT Stable		t_{pd}	-	50	ns
Rise Time of CDOUT		t_{r1}	-	25	ns
Fall Time of CDOUT		t_{f1}	-	25	ns
Rise Time of CCLK and CDIN	(Note 22)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 22)	t_{f2}	-	100	ns

21. Data must be held for sufficient time to bridge the transition time of CCLK.
22. For f_{sck} <1 MHz.

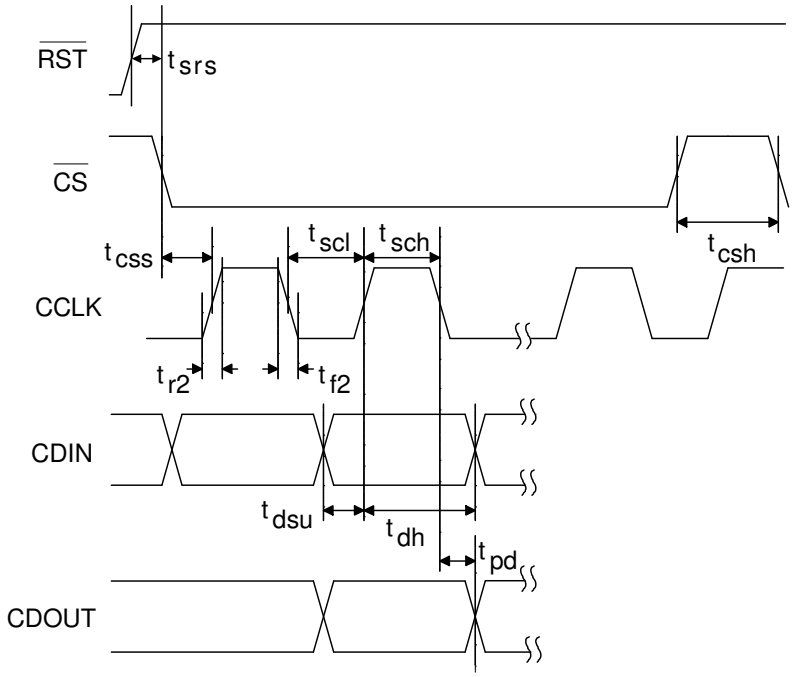


Figure 6. Control Port Timing - SPI Format

3. TYPICAL CONNECTION DIAGRAM

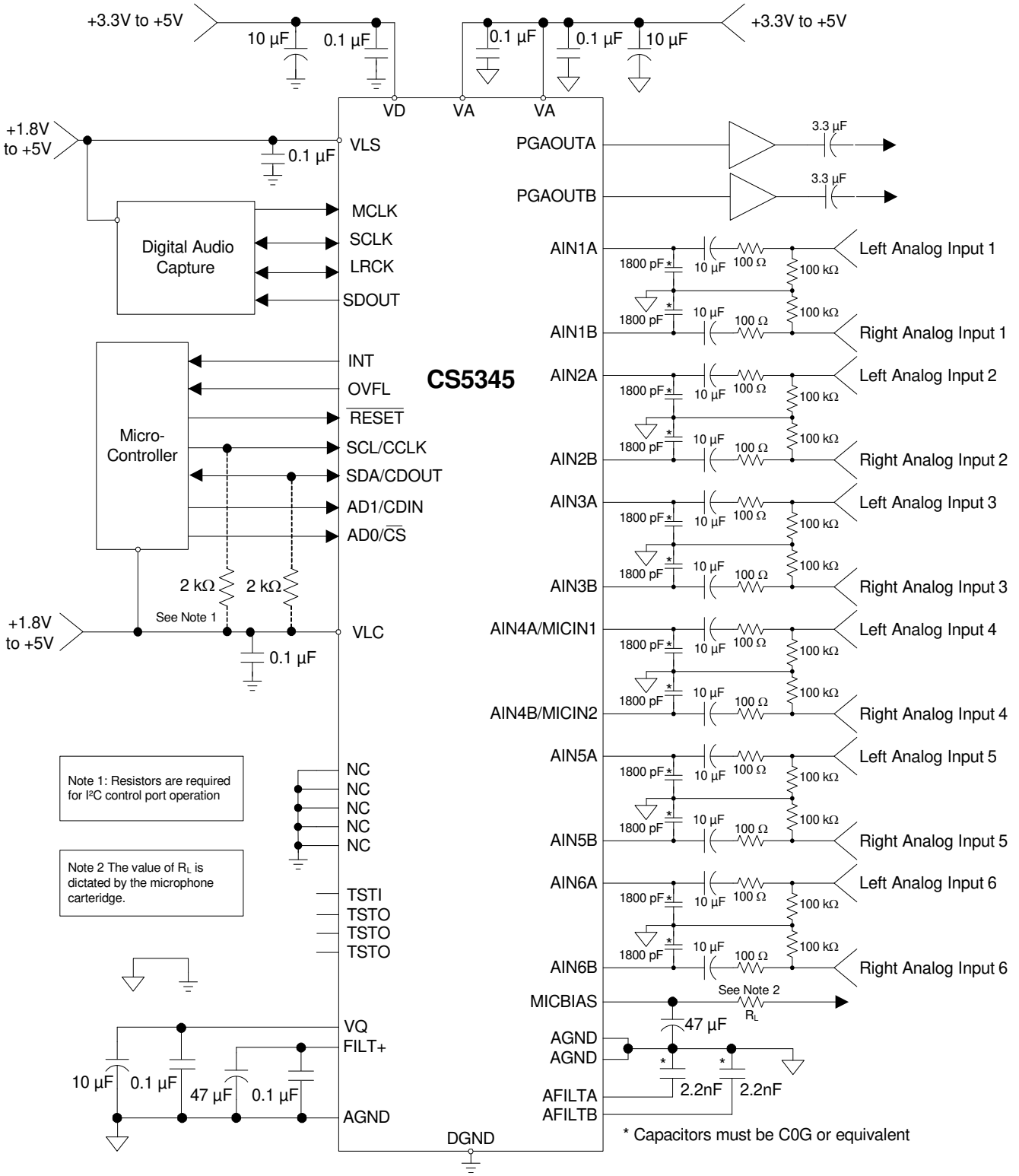


Figure 7. Typical Connection Diagram

4. APPLICATIONS

4.1 Recommended Power-Up Sequence

1. Hold $\overline{\text{RESET}}$ low until the power supply, MCLK, and LRCK are stable. In this state, the Control Port is reset to its default settings.
2. Bring $\overline{\text{RESET}}$ high. The device will remain in a low power state with the PDN bit set by default. The control port will be accessible.
3. The desired register settings can be loaded while the PDN bit remains set.
4. Clear the PDN bit to initiate the power-up sequence.

4.2 System Clocking

The CS5345 will operate at sampling frequencies from 4 kHz to 200 kHz. This range is divided into three speed modes as shown in Table 1.

Mode	Sampling Frequency
Single-Speed	4-50 kHz
Double-Speed	50-100 kHz
Quad-Speed	100-200 kHz

Table 1. Speed Modes

4.2.1 Master Clock

MCLK/LRCK must maintain an integer ratio as shown in Table 2. The LRCK frequency is equal to Fs, the frequency at which audio samples for each channel are clocked out of the device. The FM bits (See "Functional Mode (Bits 7:6)" on page 33.) and the MCLK Freq bits (See "MCLK Frequency - Address 05h" on page 34.) configure the device to generate the proper clocks in Master Mode, and receive the proper clocks in Slave Mode. Table 2 illustrates several standard audio sample rates and the required MCLK and LRCK frequencies.

LRCK (kHz)	MCLK (MHz)								
	64x	96x	128x	192x	256x	384x	512x	768x	1024x
32	-	-	-	-	8.1920	12.2880	16.3840	24.5760	32.7680
44.1	-	-	-	-	11.2896	16.9344	22.5792	33.8680	45.1584
48	-	-	-	-	12.2880	18.4320	24.5760	36.8640	49.1520
64	-	-	8.1920	12.2880	16.3840	24.5760	32.7680	-	-
88.2	-	-	11.2896	16.9344	22.5792	33.8680	45.1584	-	-
96	-	-	12.2880	18.4320	24.5760	36.8640	49.1520	-	-
128	8.1920	12.2880	16.3840	24.5760	32.7680	-	-	-	-
176.4	11.2896	16.9344	22.5792	33.8680	45.1584	-	-	-	-
192	12.2880	18.4320	24.5760	36.8640	49.1520	-	-	-	-
Mode	**QSM**					**DSM**		**SSM**	

Table 2. Common Clock Frequencies

In both Master and Slave Modes, the external MCLK must be divided down based on the MCLK/LRCK ratio to achieve a post-divider MCLK/LRCK ratio of 256x for SSM, 128x for DSM, or 64x for QSM. Table 3 lists the appropriate dividers.

MCLK/LRCK Ratio	MCLK Dividers		
64x	-	-	÷1
96x	-	-	÷1.5
128x	-	÷1	÷2
192x	-	÷1.5	÷3
256x	÷1	÷2	÷4
384x	÷1.5	÷3	-
512x	÷2	÷4	-
768x	÷3	-	-
1024x	÷4	-	-
Mode	**SSM**	**DSM**	**QSM**

Table 3. MCLK Dividers

4.2.2 *Master Mode*

As a clock master, LRCK and SCLK will operate as outputs. LRCK and SCLK are internally derived from MCLK with LRCK equal to Fs and SCLK equal to 64 x Fs as shown in Figure 8.

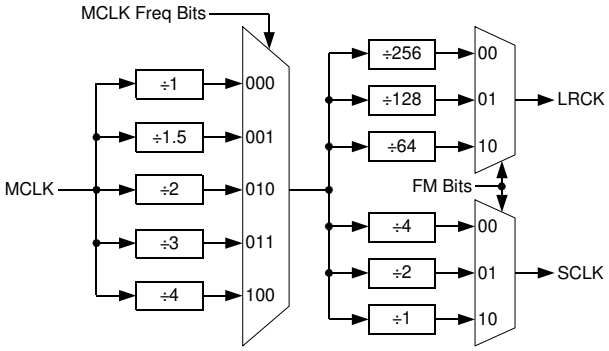


Figure 8. Master Mode Clocking

4.2.3 *Slave Mode*

In Slave Mode, SCLK and LRCK operate as inputs. The Left/Right clock signal must be equal to the sample rate, Fs, and must be synchronously derived from the supplied master clock, MCLK.

The serial bit clock, SCLK, must be synchronously derived from the master clock, MCLK, and be equal to 128x, 64x, 48x or 32x Fs, depending on the desired speed mode. Refer to Table 4 for required clock ratios.

	Single-Speed	Double-Speed	Quad-Speed
SCLK/LRCK Ratio	32x, 48x, 64x, 128x	32x, 48x, 64x	32x, 48x, 64x

Table 4. Slave Mode Serial Bit Clock Ratios

4.3 High-Pass Filter and DC Offset Calibration

When using operational amplifiers in the input circuitry driving the CS5345, a small DC offset may be driven into the A/D converter. The CS5345 includes a high-pass filter after the decimator to remove any DC offset

which could result in recording a DC level, possibly yielding clicks when switching between devices in a multichannel system.

The high-pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. If the HPFFreeze bit (See "High-Pass Filter Freeze (Bit 1)" on page 33.) is set during normal operation, the current value of the DC offset for the each channel is frozen and this DC offset will continue to be subtracted from the conversion result. This feature makes it possible to perform a system DC offset calibration by:

1. Running the CS5345 with the high-pass filter enabled until the filter settles. See the Digital Filter Characteristics section for filter settling time.
2. Disabling the high-pass filter and freezing the stored DC offset.

A system calibration performed in this way will eliminate offsets anywhere in the signal path between the calibration point and the CS5345.