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103-dB, 192-kHz, Stereo Audio ADC with 6:1 Input Mux

ADC Features

- ◆ Multi-bit Delta–Sigma Modulator
- ◆ 103 dB Dynamic Range
- ◆ -95 dB THD+N
- ◆ Stereo 6:1 Input Multiplexer
- ◆ Programmable Gain Amplifier (PGA)
 - ± 12 dB Gain, 0.5-dB Step Size
 - Zero-crossing, Click-free Transitions
- ◆ Stereo Microphone Inputs
 - +32 dB Gain Stage
 - Low-noise Bias Supply
- ◆ Up to 192 kHz Sampling Rates
- ◆ Selectable 24-bit, Left-justified or I²S Serial Audio Interface Formats

System Features

- ◆ Power-down Mode
- ◆ +5 V Analog Power Supply, Nominal
- ◆ +3.3 V Digital Power Supply, Nominal
- ◆ Direct Interface with 3.3 V to 5 V Logic Levels
- ◆ Pin Compatible with CS5345 (*See [Section 2](#) for details.)

General Description

The CS5346 integrates an analog multiplexer, programmable gain amplifier, and stereo audio analog-to-digital converter. The CS5346 performs stereo analog-to-digital (A/D) conversion of 24-bit serial values at sample rates up to 192 kHz.

A 6:1 stereo input multiplexer is included for selecting between line-level and microphone-level inputs. The microphone input path includes a +32 dB gain stage and a low-noise bias voltage supply. The PGA is available for line or microphone inputs and provides gain/attenuation of ± 12 dB in 0.5 dB steps.

The output of the PGA is followed by an advanced 5th-order, multi-bit delta-sigma modulator and digital filtering/decimation. Sampled data is transmitted by the serial audio interface at rates from 8 kHz to 192 kHz in either Slave or Master Mode.

Integrated level translators allow easy interfacing between the CS5346 and other devices operating over a wide range of logic levels.

The CS5346 is available in a 48-pin LQFP package in Commercial (-40° to $+85^{\circ}$ C) grade. The CDB5346 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please refer to [“Ordering Information” on page 38](#) for complete details.

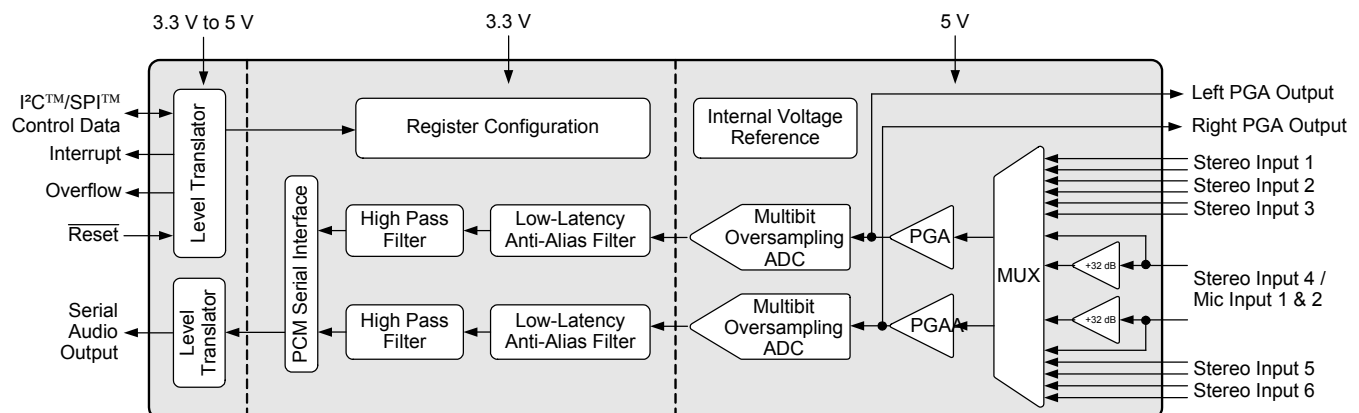


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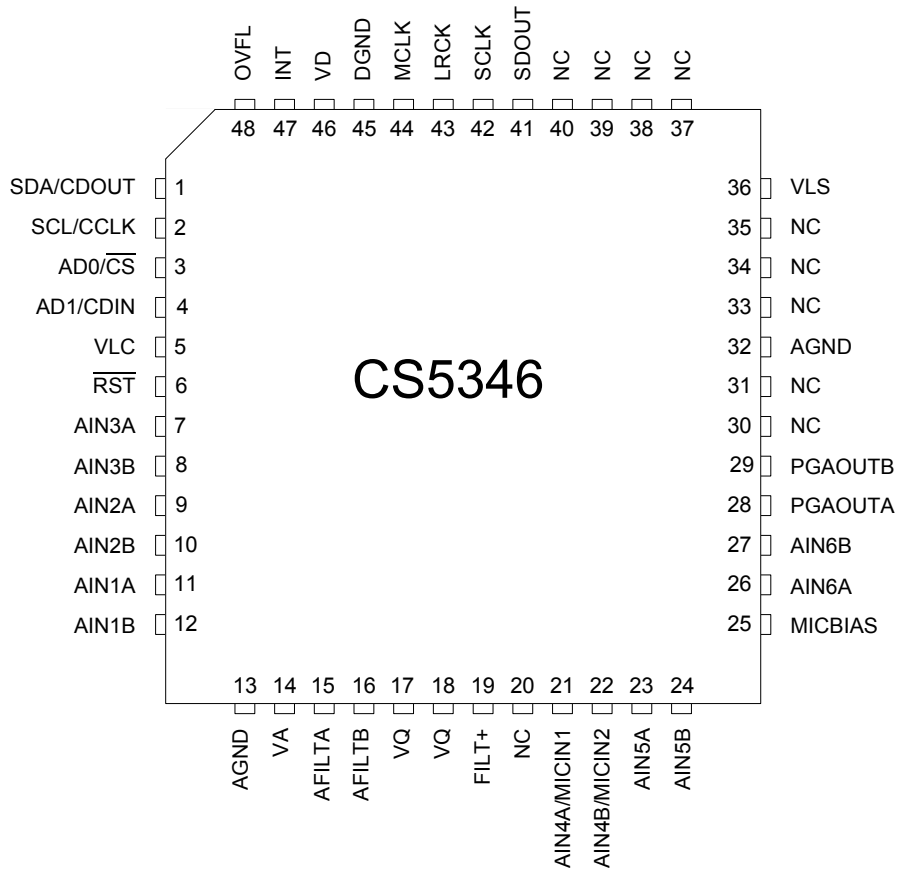
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1. PIN DESCRIPTIONS - CS5346

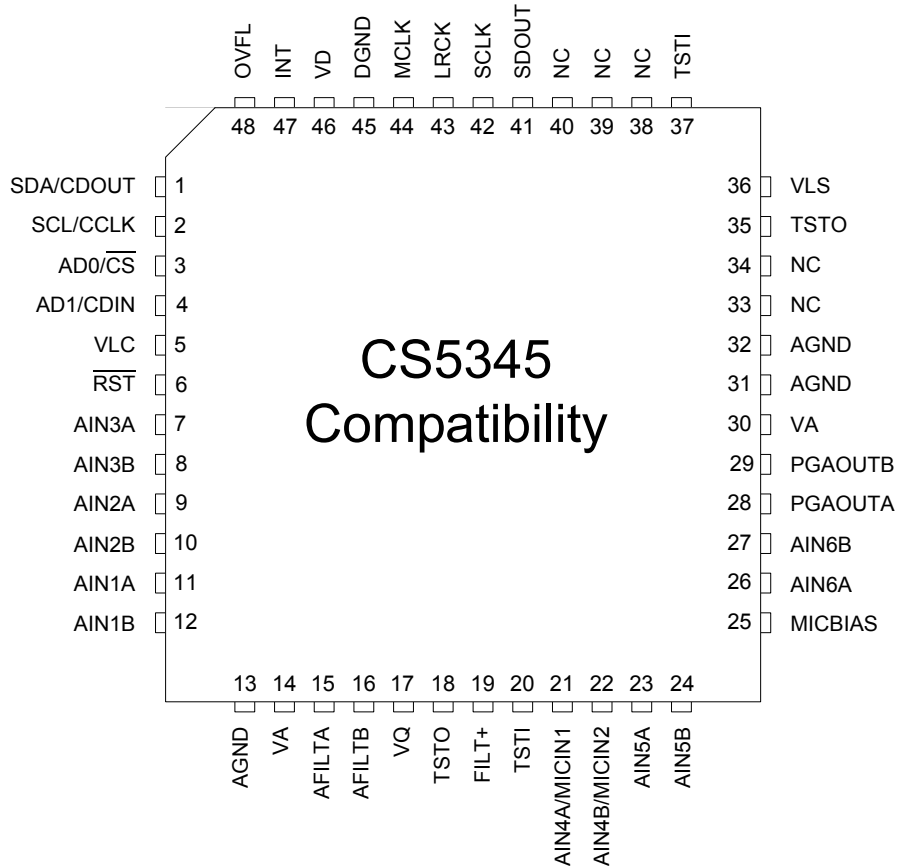


Pin Name	#	Pin Description
SDA/CDOUT	1	Serial Control Data (Input/Output) - SDA is a data I/O in I ² C [®] Mode. CDOUT is the output data line for the control port interface in SPI [™] Mode.
SCL/CCLK	2	Serial Control Port Clock (Input) - Serial clock for the serial control port.
AD0/ \overline{CS}	3	Address Bit 0 (I²C) / Control Port Chip Select (SPI) (Input) - AD0 is a chip address pin in I ² C Mode; \overline{CS} is the chip-select signal for SPI format.
AD1/CDIN	4	Address Bit 1 (I²C) / Serial Control Data Input (SPI) (Input) - AD1 is a chip address pin in I ² C Mode; CDIN is the input data line for the control port interface in SPI Mode.
VLC	5	Control Port Power (Input) - Determines the required signal level for the control port interface. Refer to the Recommended Operating Conditions for appropriate voltages.
\overline{RST}	6	Reset (Input) - The device enters a low-power mode when this pin is driven low.
AIN3A AIN3B	7 8	Stereo Analog Input 3 (Input) - The full-scale level is specified in the Analog Characteristics specification table.
AIN2A AIN2B	9 10	Stereo Analog Input 2 (Input) - The full-scale level is specified in the Analog Characteristics specification table.

AIN1A	11	Stereo Analog Input 1 (Input) - The full-scale level is specified in the Analog Characteristics specification table.
AIN1B	12	
AGND	13	Analog Ground (Input) - Ground reference for the internal analog section.
VA	14	Analog Power (Input) - Positive power for the internal analog section.
AFILTA	15	Anti-alias Filter Connection (Output) - Antialias filter connection for the channel A ADC input.
AFILTB	16	Anti-alias Filter Connection (Output) - Antialias filter connection for the channel B ADC input.
VQ	17 18	Quiescent Voltage (Output) - Filter connection for the internal quiescent reference voltage.
FILT+	19	Positive Voltage Reference (Output) - Positive reference voltage for the internal sampling circuits.
NC	20	No Connect - This pin is not connected internally and should be tied to ground to minimize any potential coupling effects.
AIN4A/MICIN1	21	Stereo Analog Input 4 / Microphone Input 1 & 2 (Input) - The full-scale level is specified in the Analog Characteristics specification table.
AIN4B/MICIN2	22	
AIN5A	23	Stereo Analog Input 5 (Input) - The full-scale level is specified in the Analog Characteristics specification table.
AIN5B	24	
MICBIAS	25	Microphone Bias Supply (Output) - Low-noise bias supply for external microphone. Electrical characteristics are specified in the DC Electrical Characteristics specification table.
AIN6A	26	Stereo Analog Input 6 (Input) - The full-scale level is specified in the Analog Characteristics specification table.
AIN6B	27	
PGAOUTA	28	PGA Analog Audio Output (Output) - Either an analog output from the PGA block or high impedance. See “PGAOut Source Select (Bit 6)” on page 30 .
PGAOUTB	29	
NC	30 31	No Connect - These pins are not connected internally and should be tied to ground to minimize any potential coupling effects.
AGND	32	Analog Ground (Input) - Ground reference for the internal analog section.
NC	33 34 35	No Connect - These pins are not connected internally and should be tied to ground to minimize any potential coupling effects.
VLS	36	Serial Audio Interface Power (Input) - Determines the required signal level for the serial audio interface. Refer to the Recommended Operating Conditions for appropriate voltages.
NC	37 38 39 40	No Connect - These pins are not connected internally and should be tied to ground to minimize any potential coupling effects.
SDOUT	41	Serial Audio Data Output (Output) - Output for two's complement serial audio data.
SCLK	42	Serial Clock (Input/Output) - Serial clock for the serial audio interface.
LRCK	43	Left Right Clock (Input/Output) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	44	Master Clock (Input) - Clock source for the ADC's delta-sigma modulators.
DGND	45	Digital Ground (Input) - Ground reference for the internal digital section.
VD	46	Digital Power (Input) - Positive power for the internal digital section.
INT	47	Interrupt (Output) - Indicates an interrupt condition has occurred.
OVFL	48	Overflow (Output) - Indicates an ADC overflow condition is present.

2. PIN COMPATIBILITY - CS5345/CS5346 DIFFERENCES

The CS5346 is pin compatible with the CS5345 and is a drop in replacement for CS5345 applications where $V_A = 5\text{ V}$, $V_D = 3.3\text{ V}$, $V_{LS} \geq 3.3\text{ V}$, and $V_{LC} \geq 3.3\text{ V}$. The pinout diagram and table below show the requirements for the remaining pins when replacing the CS5345 in these designs with a CS5346.



#	CS5345 Pin Name	CS5346 Pin Name	CS5346 Connection for Compatibility
5	VLC	VLC	Control Port Power (Input) - Limited to nominal 5 or 3.3 V.
14	VA	VA	Analog Power (Input) - Limited to nominal 5 V.
18	TSTO	VQ	This pin must be left unconnected.
20	TSTI	NC	This pin should be tied to ground.
30	VA	NC	This pin may be connected to the analog supply voltage. The decoupling capacitor for the CS5345 is not required.
31	AGND	NC	This pin should be connected to ground.
35	TSTO	NC	This pin may be left unconnected.
36	VLS	VLS	Serial Audio Interface Power (Input) - Limited to nominal 5 or 3.3 V.
37	TSTI	NC	This pin should be tied to ground.
46	VD	VD	Digital Power (Input) - Limited to nominal 3.3 V

3. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

AGND = DGND = 0 V; All voltages with respect to ground.

Parameters	Symbol	Min	Nom	Max	Units	
DC Power Supplies:	Analog	VA	4.75	5.0	5.25	V
	Digital	VD	3.13	3.3	3.47	V
	Logic - Serial Port	VLS	3.13	3.3	5.25	V
	Logic - Control Port	VLC	3.13	3.3	5.25	V
Ambient Operating Temperature (Power Applied)	Commercial	T _A	-40	-	+85	°C

ABSOLUTE MAXIMUM RATINGS

AGND = DGND = 0 V All voltages with respect to ground. (Note 1)

Parameter	Symbol	Min	Max	Units	
DC Power Supplies:	Analog	VA	-0.3	+6.0	V
	Digital	VD	-0.3	+3.63	V
	Logic - Serial Port	VLS	-0.3	+6.0	V
	Logic - Control Port	VLC	-0.3	+6.0	V
Input Current	(Note 2)	I _{in}	-	±10	mA
Analog Input Voltage	V _{INA}	AGND-0.3	VA+0.3	V	
Digital Input Voltage	Logic - Serial Port	V _{IND-S}	-0.3	VLS+0.3	V
	Logic - Control Port	V _{IND-C}	-0.3	VLC+0.3	V
Ambient Operating Temperature (Power Applied)	T _A	-50	+125	°C	
Storage Temperature	T _{stg}	-65	+150	°C	

- Notes:**
1. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.
 2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

ANALOG CHARACTERISTICS

Test conditions (unless otherwise specified): $V_A = 5\text{ V}$; $V_D = V_L = V_{LC} = 3.3\text{ V}$; $AGND = DGND = 0\text{ V}$;
 $T_A = +25^\circ\text{ C}$; Input test signal: 1 kHz sine wave; measurement bandwidth is 10 Hz to 20 kHz; $F_s = 48/96/192\text{ kHz}$;
 PGA gain = 0 dB; All connections as shown in [Figure 7 on page 18](#).

Parameter	Symbol	Min	Typ	Max	Unit
Analog-to-Digital Converter Characteristics					
Dynamic Range (Line Level Inputs)	A-weighted	97	103	-	dB
	unweighted	94	100	-	dB
	(Note 3) 40 kHz bandwidth unweighted	-	98	-	dB
Total Harmonic Distortion + Noise (Line Level Inputs)	(Note 4)				
	-1 dB	-	-95	-89	dB
	-20 dB	-	-80	-	dB
	(Note 3) 40 kHz bandwidth -1 dB	-	-92	-	dB
Dynamic Range (Mic Level Inputs)	A-weighted	77	83	-	dB
	(Note 3) unweighted	74	80	-	dB
Total Harmonic Distortion + Noise (Mic Level Inputs)	(Note 4)				
	-1 dB	-	-80	-74	dB
	-20 dB	-	-60	-	dB
	(Note 3) -60 dB	-	-20	-	dB
Interchannel Isolation	(Line Level Inputs)	-	90	-	dB
	(Mic Level Inputs)	-	80	-	dB
A/D Full-scale Input Voltage		0.51* V_A	0.57* V_A	0.63* V_A	V_{pp}
Gain Error		-	-	± 10	%
Interchannel Gain Mismatch		-	0.1	-	dB
Microphone - Level Input Characteristics					
Pre-amplifier Gain		31	32	33	dB
		35.5	40	44.7	V/V
Interchannel Gain Mismatch		-	0.1	-	dB
Input Impedance	(Note 5)	-	60	-	k Ω

3. Valid for Double- and Quad-Speed Modes only.
4. Referred to the typical A/D full-scale input voltage
5. Valid when the microphone-level inputs are selected.

ANALOG CHARACTERISTICS CONT.

Parameter	Symbol	Min	Typ	Max	Unit
Line-Level Input and Programmable Gain Amplifier					
Gain Range		- 12 -4	- -	+ 12 +4	dB V/V
Gain Step Size		-	0.5	-	dB
Absolute Gain Step Error		-	-	0.4	dB
Maximum Input Level		-	-	0.85*VA	V _{pp}
Input Impedance					
	Selected inputs	28.8	36	43.2	kΩ
	Un-selected inputs	-	-	38	kΩ
Selected Interchannel Input Impedance Mismatch		-	5	-	%
Analog Outputs					
Dynamic Range (Line Level Inputs)					
	A-weighted	98	104	-	dB
	unweighted	95	101	-	dB
Total Harmonic Distortion + Noise (Line Level Inputs)	(Note 6)				
	-1 dB	-	-80	-74	dB
	-20 dB	-	-81	-	dB
	-60 dB	-	-41	-	dB
Dynamic Range (Mic Level Inputs)					
	A-weighted	77	83	-	dB
	unweighted	74	80	-	dB
Total Harmonic Distortion + Noise (Mic Level Inputs)	(Note 6)				
	-1 dB	-	-74	-68	dB
	-20 dB	-	-60	-	dB
	-60 dB	-	-20	-	dB
Frequency Response 10 Hz to 20 kHz		-0.1dB	-	+0.1dB	dB
Analog In to Analog Out Phase Shift		-	180	-	deg
DC Current draw from a PGOOUT pin	I _{OUT}	-	-	1	μA
AC-Load Resistance	R _L	100	-	-	kΩ
Load Capacitance	C _L	-	-	20	pF

6. Referred to the typical A/D Full-Scale Input Voltage.

DIGITAL FILTER CHARACTERISTICS

Parameter (Note 7)	Symbol	Min	Typ	Max	Unit
Single-Speed Mode					
Passband (-0.1 dB)		0	-	0.4896	Fs
Passband Ripple		-	-	0.035	dB
Stopband		0.5688	-	-	Fs
Stopband Attenuation		70	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	12/Fs	-	s
Double-Speed Mode					
Passband (-0.1 dB)		0	-	0.4896	Fs
Passband Ripple		-	-	0.025	dB
Stopband		0.5604	-	-	Fs
Stopband Attenuation		69	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	9/Fs	-	s
Quad-Speed Mode					
Passband (-0.1 dB)		0	-	0.2604	Fs
Passband Ripple		-	-	0.025	dB
Stopband		0.5000	-	-	Fs
Stopband Attenuation		60	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	5/Fs	-	s
High-Pass Filter Characteristics					
Frequency Response	-3.0 dB		-	1	Hz
	-0.13 dB	(Note 8)		20	Hz
Phase Deviation	@ 20 Hz	(Note 8)		10	Deg
Passband Ripple				0	dB
Filter Settling Time				$10^5/Fs$	s

7. Response is clock-dependent and will scale with Fs. Note that the response plots (Figures 17 to 28) are normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
8. Response shown is for Fs = 48 kHz.

DC ELECTRICAL CHARACTERISTICS

AGND = DGND = 0 V, all voltages with respect to ground. MCLK=12.288 MHz; Fs=48 kHz; Master Mode.

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Current (Normal Operation)	VA = 5 V IA	-	41	50	mA
	VD, VLS, VLC = 3.3 V ID	-	23	28	mA
Power Supply Current (Power-Down Mode) (Note 9)	VA = 5 V IA	-	0.50	-	mA
	VLS, VLC, VD = 3.3 V ID	-	0.54	-	mA
Power Consumption (Normal Operation)	VA = 5 V	-	205	250	mW
	VD, VLS, VLC = 3.3 V	-	76	93	mW
	VA = 5V; VD, VLS, VLC = 3.3 V	-	4.2	-	mW
Power Supply Rejection Ratio (1 kHz)	(Note 10) PSRR	-	55	-	dB
VQ Characteristics					
Quiescent Voltage	VQ	-	0.5 x VA	-	VDC
Maximum DC Current from VQ	IQ	-	1	-	μA
VQ Output Impedance	ZQ	-	23	-	kΩ
FILT+ Nominal Voltage	FILT+	-	VA	-	VDC
Microphone Bias Voltage	MICBIAS	-	0.8 x VA	-	VDC
Current from MICBIAS	IMB	-	-	2	mA

9. Power-Down Mode is defines as \overline{RST} = Low with all clock and data lines held static and no analog input.
10. Valid with the recommended capacitor values on FILT+ and VQ as shown in the Typical Connection Diagram.

DIGITAL INTERFACE CHARACTERISTICS

Test conditions (unless otherwise specified): AGND = DGND = 0 V; VLS = VLC = 3.3 V.

Parameters (Note 11)	Symbol	Min	Typ	Max	Units	
High-Level Input Voltage	Serial Port	V_{IH}	0.7xVLS	-	-	V
	Control Port	V_{IH}	0.7xVLC	-	-	V
Low-Level Input Voltage	Serial Port	V_{IL}	-	-	0.3xVLS	V
	Control Port	V_{IL}	-	-	0.3xVLC	V
High-Level Output Voltage at $I_o = 2$ mA	Serial Port	V_{OH}	VLS-1.0	-	-	V
	Control Port	V_{OH}	VLC-1.0	-	-	V
Low-Level Output Voltage at $I_o = 2$ mA	Serial Port	V_{OL}	-	-	0.4	V
	Control Port	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	±10	μA	
Input Capacitance		-	1	-	pF	
Minimum OVFL Active Time		$\frac{10^6}{LRCK}$	-	-	μs	

11. Serial Port signals include: MCLK, SCLK, LRCK, SDOUT.

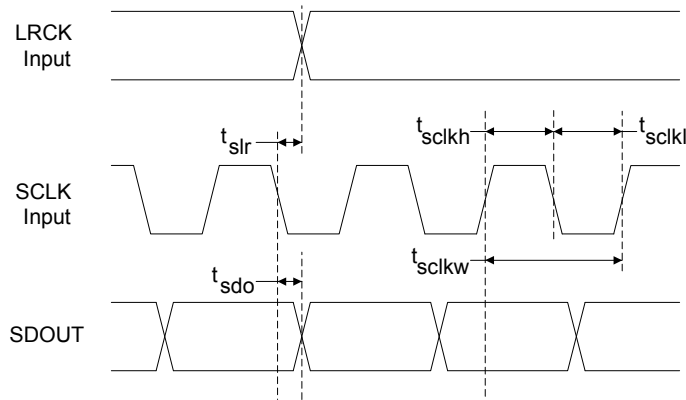
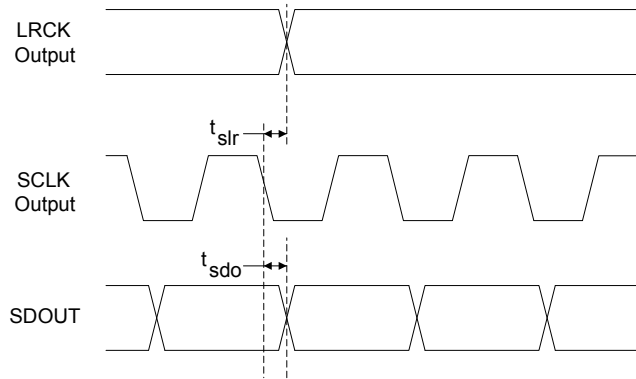
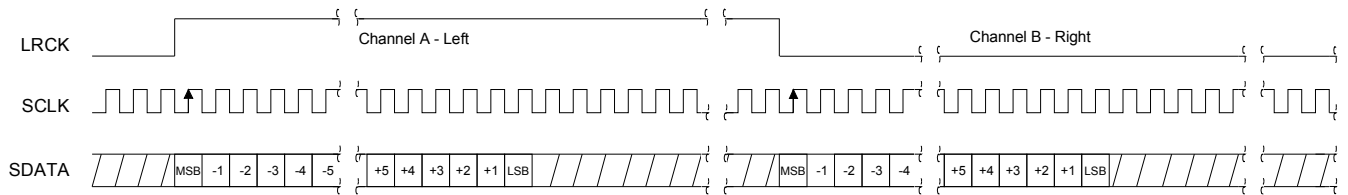
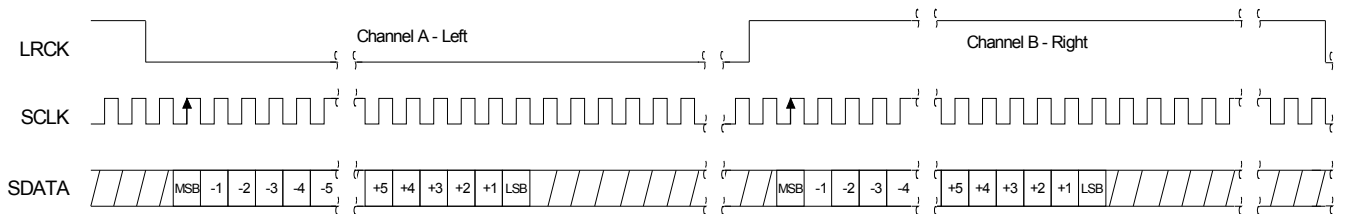
Control Port signals include: SCL/CCLK, SDA/CDOUT, $\overline{AD0/CS}$, $\overline{AD1/CDIN}$, \overline{RST} , INT, OVFL.

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT

Logic '0' = DGND = AGND = 0 V; Logic '1' = VLS, $C_L = 20$ pF. (Note 12)

Parameter	Symbol	Min	Typ	Max	Unit	
Sample Rate	Single-Speed Mode	F_s	8	-	50	kHz
	Double-Speed Mode	F_s	50	-	100	kHz
	Quad-Speed Mode	F_s	100	-	200	kHz
MCLK Specifications						
MCLK Frequency	f _{mclk}	2.048	-	51.200	MHz	
MCLK Input Pulse Width High/Low	t _{clkh}	8	-	-	ns	
Master Mode						
LRCK Duty Cycle		-	50	-	%	
SCLK Duty Cycle		-	50	-	%	
SCLK falling to LRCK edge	t _{slr}	-10	-	10	ns	
SCLK falling to SDOUT valid	t _{sdo}	0	-	36	ns	
Slave Mode						
LRCK Duty Cycle		40	50	60	%	
SCLK Period	Single-Speed Mode	t _{sclkw}	$\frac{10^9}{(128)F_s}$	-	-	ns
	Double-Speed Mode	t _{sclkw}	$\frac{10^9}{(64)F_s}$	-	-	ns
	Quad-Speed Mode	t _{sclkw}	$\frac{10^9}{(64)F_s}$	-	-	ns
SCLK Pulse Width High	t _{sclkh}	30	-	-	ns	
SCLK Pulse Width Low	t _{sclkl}	48	-	-	ns	
SCLK falling to LRCK edge	t _{slr}	-10	-	10	ns	
SCLK falling to SDOUT valid	t _{sdo}	0	-	36	ns	

12. See Figure 1 and Figure 2 on page 15.


Figure 1. Master Mode Serial Audio Port Timing

Figure 2. Slave Mode Serial Audio Port Timing

Figure 3. Format 0, 24-Bit Data Left-Justified

Figure 4. Format 1, 24-Bit Data I²S

SWITCHING CHARACTERISTICS - CONTROL PORT - I²C FORMAT

Inputs: Logic 0 = DGND = AGND = 0 V, Logic 1 = VLC, $C_L = 30$ pF.

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{\text{RST}}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	μs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	μs
Clock Low time	t_{low}	4.7	-	μs
Clock High Time	t_{high}	4.0	-	μs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	μs
SDA Hold Time from SCL Falling	t_{hdd}	0	-	μs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}, t_{rd}	-	1	μs
Fall Time SCL and SDA	t_{fc}, t_{fd}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	μs
Acknowledge Delay from SCL Falling	t_{ack}	300	1000	ns

13. Data must be held for sufficient time to bridge the transition time, t_{fc} , of SCL.

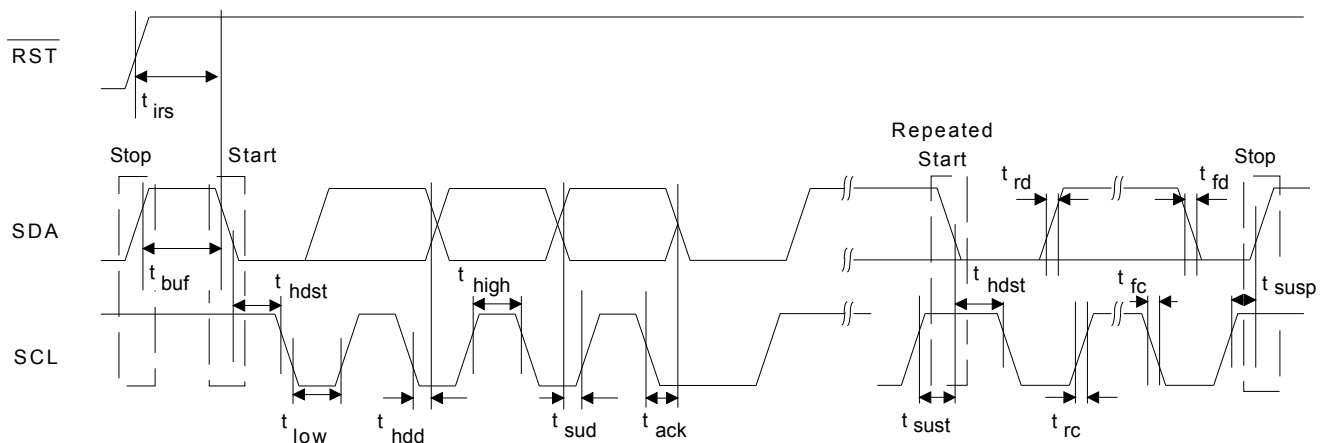


Figure 5. Control Port Timing - I²C Format

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI FORMAT

Inputs: Logic 0 = DGND = AGND = 0 V, Logic 1 = VLC, $C_L = 30$ pF.

Parameter	Symbol	Min	Max	Units
CCLK Clock Frequency	f_{sck}	-	6.0	MHz
\overline{RST} Rising Edge to \overline{CS} Falling	t_{srs}	500	-	ns
\overline{CS} High Time Between Transmissions	t_{csh}	1.0	-	μ s
\overline{CS} Falling to CCLK Edge	t_{css}	20	-	ns
CCLK Low Time	t_{scl}	66	-	ns
CCLK High Time	t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time	t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	t_{dh}	15	-	ns
CCLK Falling to CDOUT Stable	t_{pd}	-	50	ns
Rise Time of CDOUT	t_{r1}	-	25	ns
Fall Time of CDOUT	t_{f1}	-	25	ns
Rise Time of CCLK and CDIN	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	t_{f2}	-	100	ns

14. Data must be held for sufficient time to bridge the transition time of CCLK.

15. For $f_{sck} < 1$ MHz.

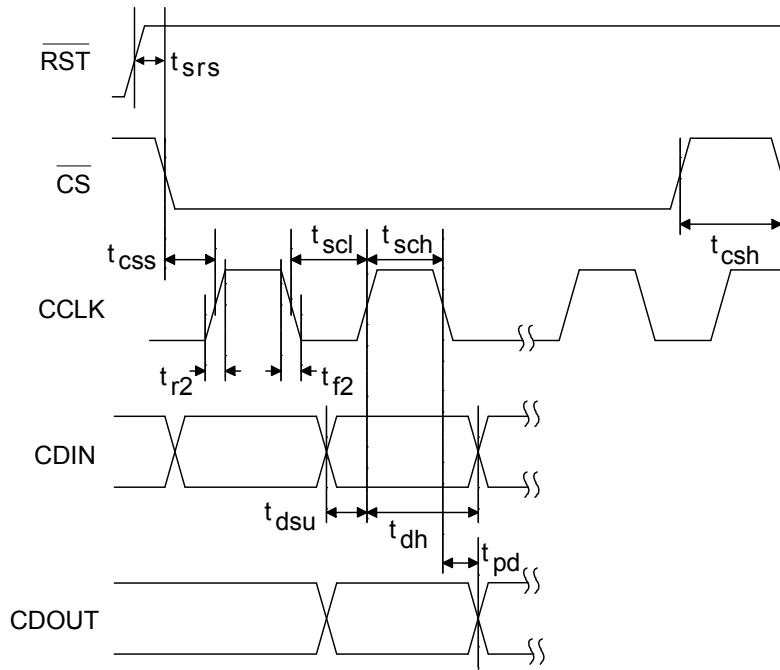


Figure 6. Control Port Timing - SPI Format

4. TYPICAL CONNECTION DIAGRAM

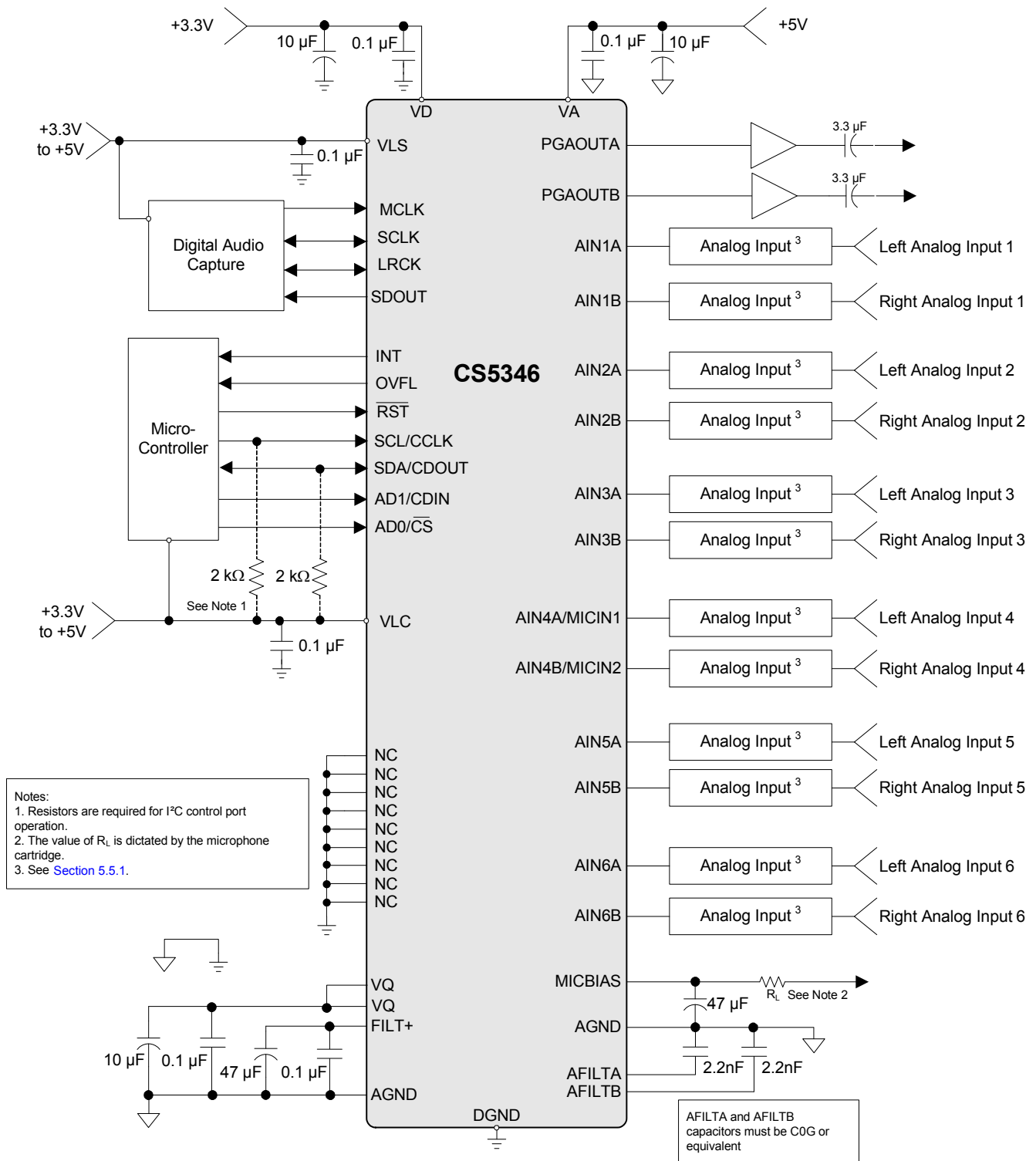


Figure 7. Typical Connection Diagram

5. APPLICATIONS

5.1 Recommended Power-Up Sequence

1. Hold $\overline{\text{RST}}$ low until the power supply, MCLK, and LRCK are stable. In this state, the Control Port is reset to its default settings.
2. Bring $\overline{\text{RST}}$ high. The device will remain in a low power state with the PDN bit set by default. The control port will be accessible.
3. The desired register settings can be loaded while the PDN bit remains set.
4. Clear the PDN bit to initiate the power-up sequence.

5.2 System Clocking

The CS5346 will operate at sampling frequencies from 8 kHz to 200 kHz. This range is divided into three speed modes as shown in [Table 1](#).

Mode	Sampling Frequency
<i>Single-Speed</i>	8-50 kHz
<i>Double-Speed</i>	50-100 kHz
<i>Quad-Speed</i>	100-200 kHz

Table 1. Speed Modes

5.2.1 Master Clock

MCLK/LRCK must maintain an integer ratio as shown in [Table 2](#). The LRCK frequency is equal to F_s , the frequency at which audio samples for each channel are clocked out of the device. The FM bits (See “[Functional Mode \(Bits 7:6\)](#)” on page 29.) and the MCLK Freq bits (See “[MCLK Frequency - Address 05h](#)” on page 30.) configure the device to generate the proper clocks in Master Mode and receive the proper clocks in Slave Mode. [Table 2](#) illustrates several standard audio sample rates and the required MCLK and LRCK frequencies.

LRCK (kHz)	MCLK (MHz)								
	* 64x	* 96x	128x	192x	256x	384x	512x	768x	1024x
32	-	-	-	-	8.1920	12.2880	16.3840	24.5760	32.7680
44.1	-	-	-	-	11.2896	16.9344	22.5792	33.8680	45.1584
48	-	-	-	-	12.2880	18.4320	24.5760	36.8640	49.1520
64	-	-	8.1920	12.2880	16.3840	24.5760	32.7680	-	-
88.2	-	-	11.2896	16.9344	22.5792	33.8680	45.1584	-	-
96	-	-	12.2880	18.4320	24.5760	36.8640	49.1520	-	-
128	8.1920	12.2880	16.3840	24.5760	32.7680	-	-	-	-
176.4	11.2896	16.9344	22.5792	33.8680	45.1584	-	-	-	-
192	12.2880	18.4320	24.5760	36.8640	49.1520	-	-	-	-
Mode	QSM				DSM			SSM	

* Only available in master mode.

Table 2. Common Clock Frequencies

5.2.2 Master Mode

As a clock master, LRCK and SCLK will operate as outputs. LRCK and SCLK are internally derived from MCLK with LRCK equal to F_s and SCLK equal to $64 \times F_s$ as shown in Figure 8.

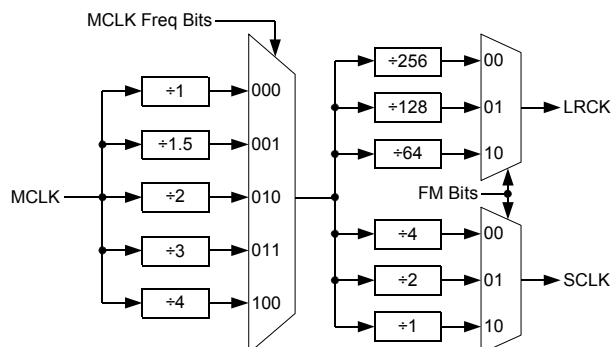


Figure 8. Master Mode Clocking

5.2.3 Slave Mode

In Slave Mode, SCLK and LRCK operate as inputs. The Left/Right clock signal must be equal to the sample rate, F_s , and must be synchronously derived from the supplied master clock, MCLK.

The serial bit clock, SCLK, must be synchronously derived from the master clock, MCLK, and be equal to $128x$, $64x$ or $48x F_s$, depending on the desired speed mode. Refer to Table 3 for required clock ratios.

	Single-Speed	Double-Speed	Quad-Speed
SCLK/LRCK Ratio	48x, 64x, 128x	48x, 64x	48x, 64x

Table 3. Slave Mode Serial Bit Clock Ratios

5.3 High-Pass Filter and DC Offset Calibration

When using operational amplifiers in the input circuitry driving the CS5346, a small DC offset may be driven into the A/D converter. The CS5346 includes a high-pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding clicks when switching between devices in a multichannel system.

The high-pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. If the HPFFreeze bit (See “High-Pass Filter Freeze (Bit 1)” on page 29.) is set during normal operation, the current value of the DC offset for the each channel is frozen and this DC offset will continue to be subtracted from the conversion result. This feature makes it possible to perform a system DC offset calibration by:

1. Running the CS5346 with the high-pass filter enabled until the filter settles. See the Digital Filter Characteristics section for filter settling time.
2. Disabling the high-pass filter and freezing the stored DC offset.

A system calibration performed in this way will eliminate offsets anywhere in the signal path between the calibration point and the CS5346.

5.4 Analog Input Multiplexer, PGA, and Mic Gain

The CS5346 contains a stereo 6-to-1 analog input multiplexer followed by a programmable gain amplifier (PGA). The input multiplexer can select one of six possible stereo analog input sources and route it to the PGA. Analog inputs 4A and 4B are able to insert a +32 dB (+40x) gain stage before the input multiplexer, allowing them to be used for microphone-level signals without the need for any external gain. The PGA stage provides ± 12 dB ($\pm 4x$) adjustment in 0.5 dB steps. Figure 9 shows the architecture of the input multiplexer, PGA, and microphone gain stages.

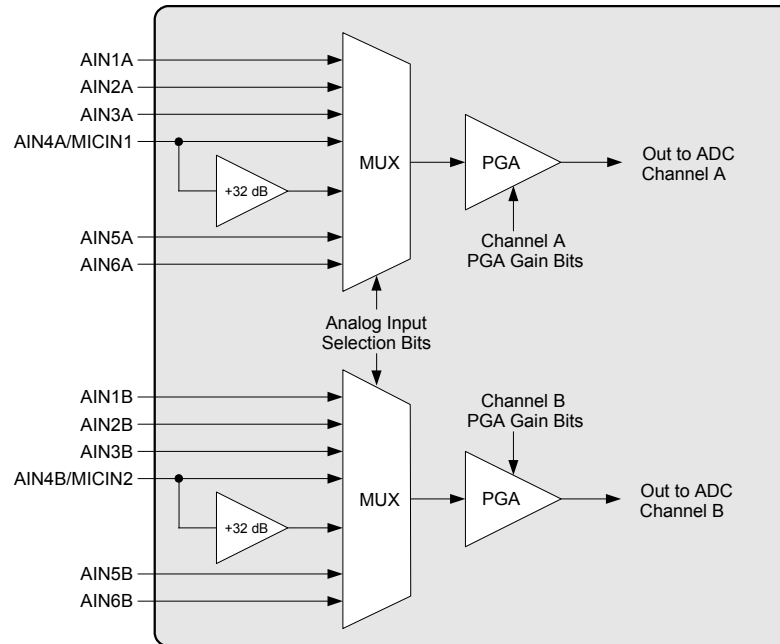


Figure 9. Analog Input Architecture

The “[Analog Input Selection \(Bits 2:0\)](#)” on page 32 outlines the bit settings necessary to control the input multiplexer and mic gain. “[Channel B PGA Control - Address 07h](#)” on page 30 and “[Channel A PGA Control - Address 08h](#)” on page 31 outline the register settings necessary to control the PGA. By default, line-level input 1 is selected, and the PGA is set to 0 dB.

5.5 Input Connections

The analog modulator samples the input at 6.144 MHz (MCLK=12.288 MHz). The digital filter will reject signals within the stopband of the filter. However, there is no rejection for input signals which are $(n \times 6.144 \text{ MHz})$ the digital passband frequency, where $n=0,1,2,\dots$ Refer to the Typical Connection Diagram for the recommended analog input circuit that will attenuate noise energy at 6.144 MHz. The use of capacitors which have a large voltage coefficient (such as general-purpose ceramics) must be avoided since these can degrade signal linearity. Any unused analog input pairs should be left unconnected.

5.5.1 Analog Input Configuration for 1 V_{RMS} Input Levels

The CS5346 PGA, excluding the input multiplexer, is shown in Figure 10 with nominal component values. Interfacing to this circuit is a relatively simple matter and several options are available. The simplest option is shown in Figure 11. However, it may be advantageous in some applications to provide a low-pass filter prior to the PGA to prevent radio frequency interference within the amplifier. The circuit shown in Figure 12

demonstrates a simple solution. The 1800 pF capacitors in the low-pass filter should be C0G or equivalent to avoid distortion issues

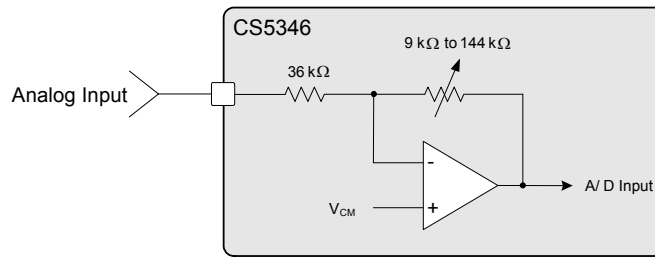


Figure 10. CS5346 PGA

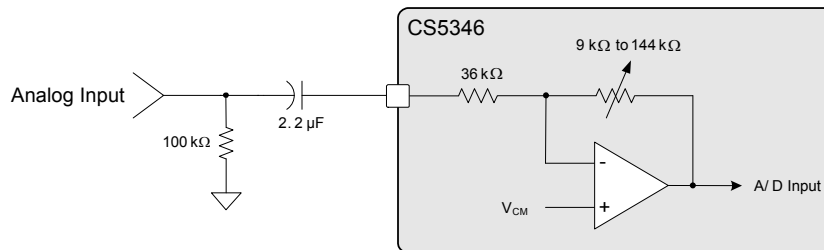


Figure 11. 1 V_{RMS} Input Circuit

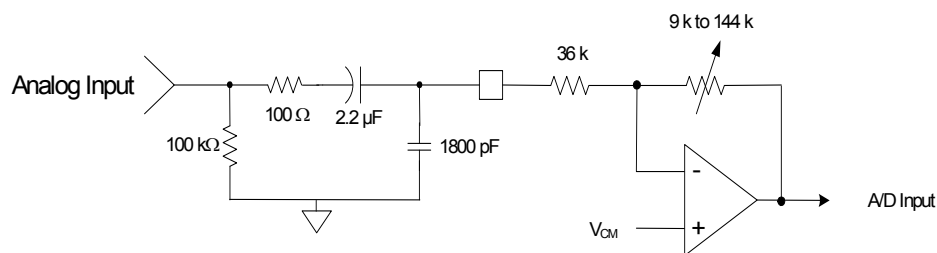


Figure 12. 1 V_{RMS} Input Circuit with RF Filtering

5.5.2 Analog Input Configuration for 2 V_{RMS} Input Levels

The CS5346 can also be easily configured to support an external 2 V_{RMS} input signal, as shown in Figure 13. In this configuration, the 2 V_{RMS} input signal is attenuated to 1.5 V_{RMS} at the analog input with the external 12 kΩ resistor and the input impedance to the network is increased to 48 kΩ. The PGA gain must also be configured to attenuate the 1.5 V_{RMS} at the input pin to the 1.0 V_{RMS} maximum A/D input level to prevent clipping in the ADC.

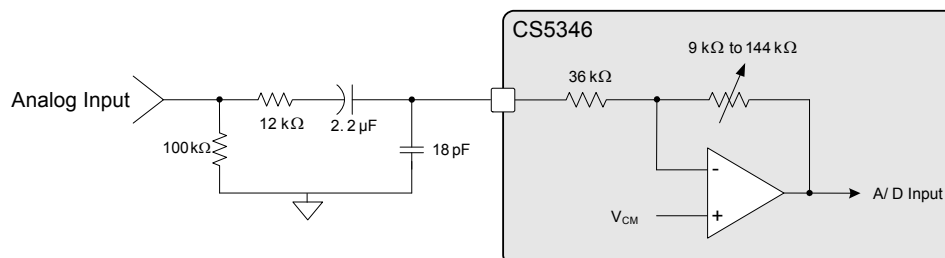


Figure 13. 2 V_{RMS} Input Circuit

5.6 PGA Auxiliary Analog Output

The CS5346 includes an auxiliary analog output through the PGAOUT pins. These pins can be configured to output the analog input to the ADC as selected by the input MUX and gained or attenuated with the PGA, or alternatively, they may be set to high impedance. See the “[PGAOut Source Select \(Bit 6\)](#)” on page 30 for information on configuring the PGA auxiliary analog output.

The PGA auxiliary analog output can source very little current. As current from the PGAOUT pins increases, distortion will increase. For this reason, a high-input impedance buffer must be used on the PGAOUT pins to achieve full performance. An example buffer for PGAOUT is provided on the CDB5346 for reference. Refer to the table in “[DC Electrical Characteristics](#)” on page 12 for acceptable loading conditions.

5.7 Control Port Description and Timing

The control port is used to access the registers, allowing the CS5346 to be configured for the desired operational modes and formats. The operation of the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port has two modes: SPI and I²C, with the CS5346 acting as a slave device. SPI Mode is selected if there is a high-to-low transition on the AD0/CS pin, after the RST pin has been brought high. I²C Mode is selected by connecting the AD0/CS pin through a resistor to VLC or DGND, thereby permanently selecting the desired AD0 bit address state.

5.7.1 SPI Mode

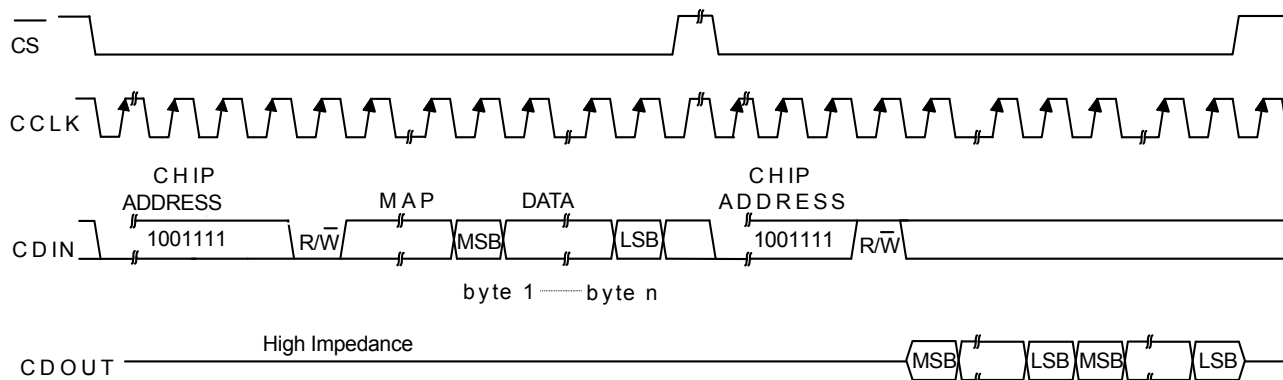
In SPI Mode, \overline{CS} is the chip-select signal; CCLK is the control port bit clock (input into the CS5346 from the microcontroller); CDIN is the input data line from the microcontroller; CDOUT is the output data line to the microcontroller. Data is clocked in on the rising edge of CCLK and out on the falling edge.

Figure 14 shows the operation of the control port in SPI Mode. To write to a register, bring \overline{CS} low. The first seven bits on CDIN form the chip address and must be 1001111. The eighth bit is a read/write indicator (R/W), which should be low to write. The next eight bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next eight bits are the data that will be placed into the register designated by the MAP. During writes, the CDOUT output stays in the Hi-Z state. It may be externally pulled high or low with a 47 k Ω resistor, if desired.

To read a register, the MAP has to be set to the correct address by executing a partial write cycle which finishes (\overline{CS} high) immediately after the MAP byte. To begin a read, bring \overline{CS} low, send out the chip ad-

dress and set the read/write bit ($\overline{R/W}$) high. The next falling edge of CCLK will clock out the MSB of the addressed register (CDOUT will leave the high-impedance state).

For both read and write cycles, the memory address pointer will automatically increment following each data byte in order to facilitate block reads and writes of successive registers.



MAP = Memory Address Pointer, 8 bits, MSB first

Figure 14. Control Port Timing in SPI Mode

5.7.2 I²C Mode

In I²C Mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL. There is no CS pin. Pins AD0 and AD1 form the two least-significant bits of the chip address and should be connected through a resistor to VLC or DGND as desired. The state of the pins is sensed while the CS5346 is being reset.

The signal timings for a read and write cycle are shown in Figure 15 and Figure 16. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS5346 after a Start condition consists of a 7-bit chip address field and a R/W bit (high for a read, low for a write). The upper 5 bits of the 7-bit address field are fixed at 10011. To communicate with a CS5346, the chip address field, which is the first byte sent to the CS5346, should match 10011 followed by the settings of the AD1 and AD0. The 8th bit of the address is the R/W bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Following each data byte, the memory address pointer will automatically increment to facilitate block reads and writes of successive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS5346 after each input byte is read, and is input to the CS5346 from the microcontroller after each transmitted byte.

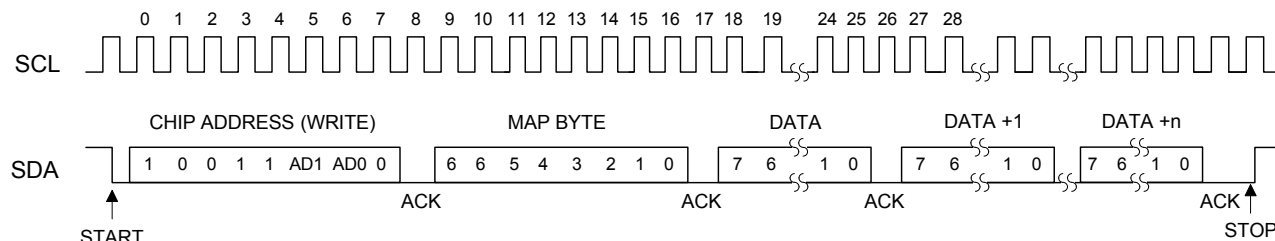


Figure 15. Control Port Timing, I²C Write

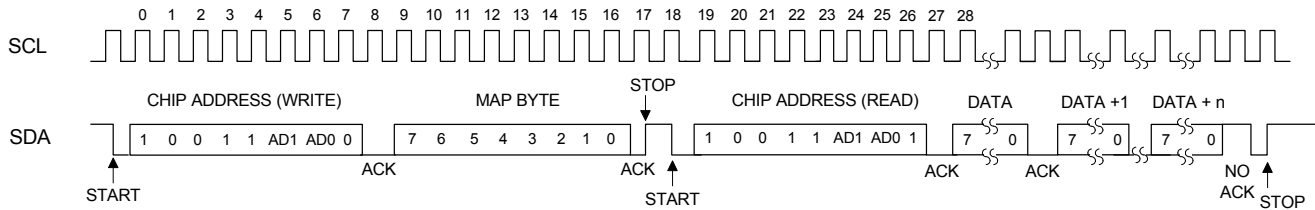


Figure 16. Control Port Timing, I²C Read

Since the read operation cannot set the MAP, an aborted write operation is used as a preamble. As shown in Figure 16, the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

- Send start condition.
- Send 10011xx0 (chip address & write operation).
- Receive acknowledge bit.
- Send MAP byte.
- Receive acknowledge bit.
- Send stop condition, aborting write.
- Send start condition.
- Send 10011xx1(chip address & read operation).
- Receive acknowledge bit.
- Receive byte, contents of selected register.
- Send acknowledge bit.
- Send stop condition.

5.8 Interrupts and Overflow

The CS5346 has a comprehensive interrupt capability. The INT output pin is intended to drive the interrupt input pin on the host microcontroller. The INT pin may function as either an active high CMOS driver or an active-low, open-drain driver (see “Active High/Low (Bit 0)” on page 35). When configured as active low open-drain, the INT pin has no active pull-up transistor, allowing it to be used for wired-OR hook-ups with multiple peripherals connected to the microcontroller interrupt input pin. In this configuration, an external pull-up resistor must be placed on the INT pin for proper operation.

Many conditions can cause an interrupt, as listed in the interrupt status register descriptions (see “Interrupt Status - Address 0Dh” on page 35). Each source may be masked off through mask register bits. In addition, Each source may be set torising edge, falling edge, or level-sensitive. Combined with the option of level-sensitive or edge-sensitive modes within the microcontroller, many different configurations are possible, depending on the needs of the equipment designer.

The CS5346 also has a dedicated overflow output. The OVFL pin functions as active low open drain and has no active pull-up transistor, thereby requiring an external pull-up resistor. The OVFL pin outputs an OR of the ADCOverflow and ADCUnderflow conditions available in the Interrupt Status register; however, these conditions do not need to be unmasked for proper operation of the OVFL pin.