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CS5364

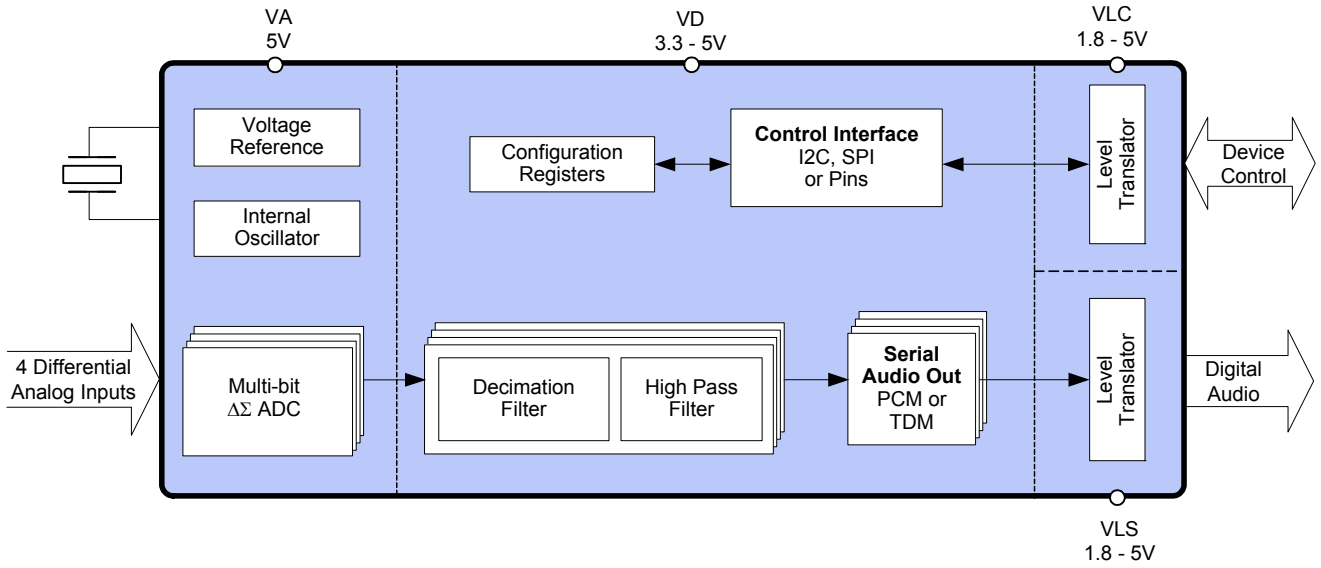
114 dB, 192 kHz, 4-Channel A/D Converter

Features

- Advanced Multi-bit Delta-Sigma Architecture
- 24-Bit Conversion
- 114 dB Dynamic Range
- -105 dB THD+N
- Supports Audio Sample Rates up to 216 kHz
- Selectable Audio Interface Formats
  - Left-Justified, I²S, TDM
  - 4-Channel TDM Interface Formats
- Low Latency Digital Filter
- Less than 365 mW Power Consumption
- On-Chip Oscillator Driver
- Operation as System Clock Master or Slave
- Auto-Detect Speed in Slave Mode
- Differential Analog Architecture
- Separate 1.8 V to 5 V Logic Supplies for Control and Serial Ports
- High-Pass Filter for DC Offset Calibration
- Overflow Detection
- Footprint Compatible with the 8-Channel CS5368

Additional Control Port Features

- Supports I²C or SPI™ Control Interface per specifications on page 17 and page 18
- Individual Channel HPF Disable
- Overflow Detection for Individual Channels
- Mute Control for Individual Channels
- Independent Power-Down Control per Channel Pair



Description

The CS5364 is a complete 4-channel analog-to-digital converter for digital audio systems. It performs sampling, analog-to-digital conversion, and anti-alias filtering, generating 24-bit values for all 4-channel inputs in serial form at sample rates up to 216 kHz per channel.

The CS5364 uses a 5th-order, multi-bit delta sigma modulator followed by low latency digital filtering and decimation, which removes the need for an external anti-aliasing filter. The ADC uses a differential input architecture which provides excellent noise rejection.

Dedicated level translators for the Serial Port and Control Port allow seamless interfacing between the CS5364 and other devices operating over a wide range of logic levels. In addition, an on-chip oscillator driver provides clocking flexibility and simplifies design.

The CS5364 is the industry's first audio A/D to support a high-speed TDM interface which provides a serial output of 4 channels of audio data with sample rates up to 216 kHz within a single data stream. It further reduces layout complexity and relieves input/output constraints in digital signal processors.

The CS5364 is available in a 48-pin LQFP package in both Commercial (-40°C to 85°C) and Automotive grades (-40°C to +105°C). The CDB5364 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please see "Ordering Information" on page 41 for complete ordering information.

The CS5364 is ideal for high-end and pro-audio systems requiring unrivaled sound quality, transparent conversion, wide dynamic range and negligible distortion, such as A/V receivers, digital mixing consoles, multi-channel recorders, outboard converters, digital effect processors, and automotive audio systems.

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1. PIN DESCRIPTION

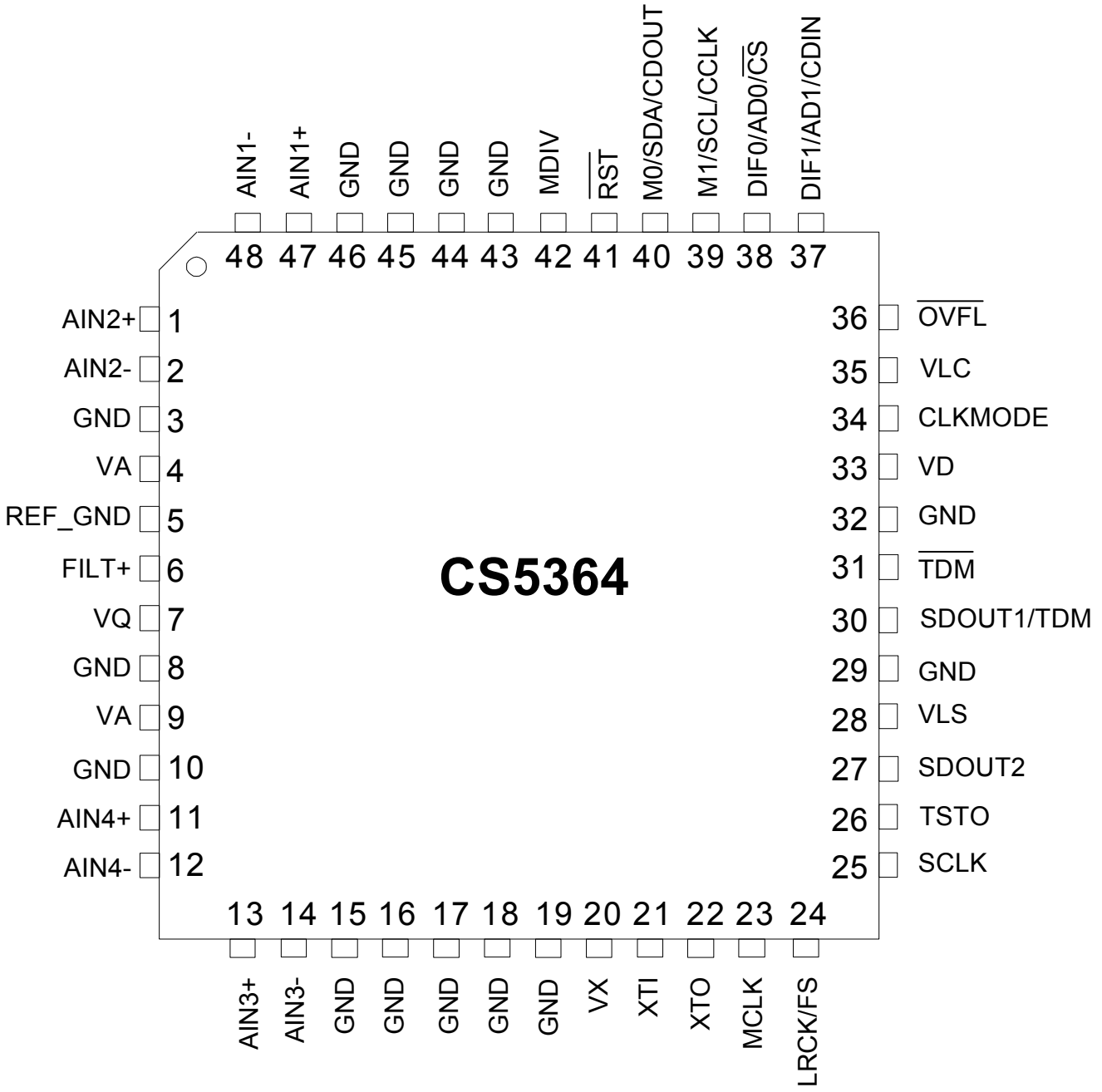

Figure 1. CS5364 Pinout

Pin Name	Pin #	Pin Description
AIN2+, AIN2- AIN4+, AIN4- AIN3+, AIN3- AIN1+, AIN1-	1,2 11,12 13,14 47,48	**Differential Analog** (*Inputs*) - Audio signals are presented differently to the delta sigma modulators via the AIN+/- pins.
GND	3,8 10,15 16,17 18,19 29,32 43,44 45,46	**Ground** (*Input*) - Ground reference. Must be connected to analog ground.
VA	4,9	**Analog Power** (*Input*) - Positive power supply for the analog section.
REF_GND	5	**Reference Ground** (*Input*) - For the internal sampling circuits. Must be connected to analog ground.
FILT+	6	**Positive Voltage Reference** (*Output*) - Reference voltage for internal sampling circuits.
VQ	7	**Quiescent Voltage** (*Output*) - Filter connection for the internal quiescent reference voltage.
VX	20	**Crystal Oscillator Power** (*Input*) - Also powers control logic to enable or disable oscillator circuits.
XTI XTO	21 22	**Crystal Oscillator Connections** (*Input/Output*) - I/O pins for an external crystal which may be used to generate MCLK.
MCLK	23	**System Master Clock** (*Input/Output*) - When a crystal is used, this pin acts as a buffered MCLK Source (Output). When the oscillator function is not used, this pin acts as an input for the system master clock. In this case, the XTI and XTO pins must be tied low.
LRCK/FS	24	**Serial Audio Channel Clock** (*Input/Output*) In I²S mode, Serial Audio Channel Select. When low, the odd channels are selected. In LJ mode, Serial Audio Channel Select. When high, the odd channels are selected. In TDM Mode a frame sync signal. When high, it marks the beginning of a new frame of serial audio samples. In Slave Mode, this pin acts as an input pin.
SCLK	25	**Main timing clock for the Serial Audio Interface** (*Input/Output*) - During Master Mode, this pin acts as an output, and during Slave Mode it acts as an input pin.
TSTO	26	**Test Out** (*Output*) - Must be left unconnected.
SDOUT2	27	**Serial Audio Data** (*Output*) - Channels 3,4.
VLS	28	**Serial Audio Interface Power** - Positive power for the serial audio interface.
SDOUT1/TDM	30	**Serial Audio Data** (*Output*) - Channels 1,2.
$\overline{\text{TDM}}$	31	**$\overline{\text{TDM}}$** - TDM is complementary TDM data.
VD	33	**Digital Power** (*Input*) - Positive power supply for the digital section.
VLC	35	**Control Port Interface Power** - Positive power for the control port interface.
$\overline{\text{OVFL}}$	36	**Overflow** (*Output, open drain*) - Detects an overflow condition on both left and right channels.
$\overline{\text{RST}}$	41	**Reset** (*Input*) - The device enters a low power mode when low.

Stand-Alone Mode		
CLKMODE	34	**CLKMODE** *(Input)* - Setting this pin HIGH places a divide-by-1.5 circuit in the MCLK path to the core device circuitry.
DIF1 DIF0	37 38	**DIF1, DIF0** (*Input*) - Sets the serial audio interface format.
M1 M0	39 40	**Mode Selection** (*Input*) - Determines the operational mode of the device.
MDIV	42	**MCLK Divider** (*Input*) - Setting this pin HIGH places a divide-by-2 circuit in the MCLK path to the core device circuitry.
Control Port Mode		
CLKMODE	34	**CLKMODE** *(Input)* - This pin is ignored in Control Port Mode and the same functionality is obtained from the corresponding bit in the Global Control Register. **Note:** Should be connected to GND when using the part in Control Port Mode.
AD1/CDIN	37	**I²C Format, AD1** (*Input*) - Forms the device address input AD[1]. **SPI Format, CDIN** (*Input*) **-** Becomes the input data pin.
AD0/$\overline{CS}$	38	**I²C Format, AD0** (*Input*) - Forms the device address input AD[0]. **SPI Format, $\overline{CS}$** (Input) - Acts as the active low chip select input.
SCL/CCLK	39	**I²C Format, SCL** (*Input*) – Serial clock for the serial control port. An external pull-up resistor is required for I²C control port operation. **SPI Format, CCLK** (*Input*) – Serial clock for the serial control port.
SDA/CDOUT	40	**I²C Format SDA** (*Input/Output*) - Acts as an input/output data pin. An external pull-up resistor is required for I²C control port operation. **SPI Format CDOUT** (*Output*) - Acts as an output only data pin.
MDIV	42	**MCLK Divider** (*Input*) - This pin is ignored in Control Port Mode, and the same functionality is obtained from the corresponding bit in the Global Control Register. **Note:** Should be connected to GND when using the part in Control Port Mode.

2. TYPICAL CONNECTION DIAGRAM

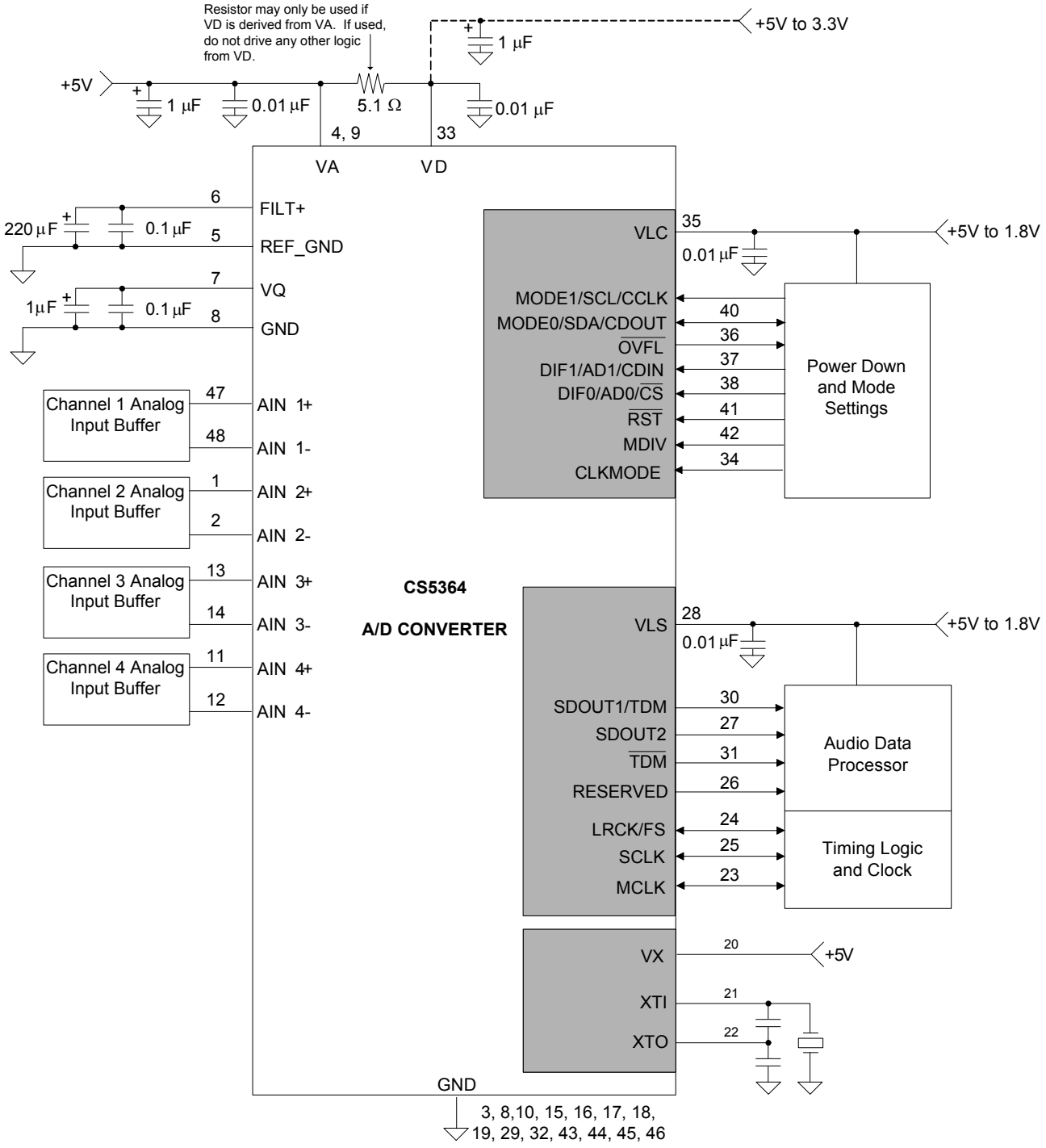

Figure 2. Typical Connection Diagram

For analog buffer configurations, refer to Cirrus Application Note AN241. Also, a low-cost single-ended-to-differential solution is provided on the Customer Evaluation Board.

3. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

GND = 0 V, all voltages with respect to 0 V.

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies:	Positive Analog	VA	4.75	5.0		
	Positive Crystal	VX	4.75	5.0		
	Positive Digital	VD	3.14	3.3	5.25	V
	Positive Serial Logic	VLS	1.71[1]	3.3		
	Positive Control Logic	VLC	1.71	3.3		
Ambient Operating Temperature	(-CQZ)	T_{AC}	-40	-	85	°C
	(-DQZ)	T_{AA}	-40	-	105	

1. TDM Quad-Speed Mode specified to operate correctly at VLS ≥ 3.14 V.

ABSOLUTE RATINGS

Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes. Transient currents up to ±100 mA on the analog input pins will not cause SCR latch-up.

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Analog	VA				
	Positive Crystal	VX				
	Positive Digital	VD	-0.3	-	+6.0	V
	Positive Serial Logic	VLS				
	Positive Control Logic	VLC				
Input Current		I_{in}	-10		+10	mA
Analog Input Voltage		V_{IN}	-0.3		VA+0.3	V
Digital Input Voltage		V_{IND}		-	VL+0.3	
Ambient Operating Temperature (Power Applied)		T_A	-50		+125	°C
Storage Temperature		T_{stg}	-65		+150	

SYSTEM CLOCKING

Parameter	Symbol	Min	Typ	Max	Unit
Input Master Clock Frequency	MCLK	0.512		55.05	MHz
Input Master Clock Duty Cycle	t_{clkhl}	40		60	%

DC POWER

MCLK = 12.288 MHz; Master Mode. GND = 0 V.

Parameter		Symbol	Min	Typ	Max	Unit
Power Supply Current	VA = 5 V	I_A	-	51	56	mA
(Normal Operation)	VX = 5 V	I_X	-	4	8	mA
	VD = 5 V	I_D	-	44	48	mA
	VD = 3.3 V	I_D	-	25	28	mA
	VLS, VLC = 5 V	I_L	-	3	4	mA
	VLS, VLC = 3.3 V	I_L	-	1	2	mA
Power Supply Current	VA = 5 V	I_A	-	50	-	µA
(Power-Down) (Note 1)	VLS, VLC,VD = 5 V	I_D	-	500	-	µA
Power Consumption						mW
(Normal Operation)	All Supplies = 5 V	-	-	510	580	mW
	VA = 5 V, VD = VLS = VLC = 3.3 V	-	-	360	419	mW
(Power-Down) (Note 1)		-	-	2.75	-	mW

1. Power-Down is defined as $\overline{RST}$ = LOW with all clocks and data lines held static at a valid logic level.

LOGIC LEVELS

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	%VLS/VLC	V_{IH}	70	-	-	%
Low-Level Input Voltage	%VLS/VLC	V_{IL}	-	-	30	%
High-Level Output Voltage at 100 µA load	%VLS/VLC	V_{OH}	85	-	-	%
Low-Level Output Voltage at -100 µA load	%VLS/VLC	V_{OL}	-	-	15	%
SDA Low-Level Output Voltage at -2 mA load	%VLC	V_{OL}	-	-	TBD	%
$\overline{OVFL}$ Current Sink				-4		mA
Input Leakage Current	logic pins only	I_{in}	-10	-	10	µA

PSRR, VQ AND FILT+ CHARACTERISTICS

MCLK = 12.288 MHz; Master Mode. Valid with the recommended capacitor values on FILT+ and VQ as shown in the “Typical Connection Diagram”.

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Rejection Ratio at (1 kHz)	PSRR	-	65	-	dB
V_Q Nominal Voltage			VA/2		V
Output Impedance		-	25	-	kΩ
Maximum allowable DC current source/sink			10		µA
Filt+ Nominal Voltage			VA		V
Output Impedance		-	4.4	-	kΩ
Maximum allowable DC current source/sink			10		µA

ANALOG CHARACTERISTICS (COMMERCIAL)

Test Conditions (unless otherwise specified). VA = 5 V, VD = VLS = VLC 3.3 V, and T_A = 25° C. Full-scale input sine wave. Measurement Bandwidth is 10 Hz to 20 kHz.

Parameter		Symbol	Min	Typ	Max	Unit
Single-Speed Mode Fs = 48 kHz						
Dynamic Range	A-weighted		108	114	-	dB
	unweighted		105	111	-	
Total Harmonic Distortion + Noise	-1 dB			-105	-99	
referred to typical full scale	-20 dB	THD+N	-	-91	-	dB
	-60 dB			-51	-45	
Double-Speed Mode Fs = 96 kHz						
Dynamic Range	A-weighted		108	114		
	unweighted		105	111	-	dB
	40 kHz bandwidth unweighted		-	108		
Total Harmonic Distortion + Noise	-1 dB			-105	-99	
referred to typical full scale	-20 dB	THD+N	-	-91	-	dB
	-60 dB			-51	-45	
	40 kHz bandwidth -1dB			-102	-	
Quad-Speed Mode Fs = 192 kHz						
Dynamic Range	A-weighted		108	114		
	unweighted		105	111	-	dB
	40 kHz bandwidth unweighted		-	108		
Total Harmonic Distortion + Noise	-1 dB			-105	-99	
referred to typical full scale	-20 dB	THD+N	-	-91	-	dB
	-60 dB			-51	-45	
	40 kHz bandwidth -1dB			-102	-	
Dynamic Performance for All Modes						
Interchannel Isolation			-	110	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	-	dB
Gain Error			-5	-	5	%
Gain Drift			-	± 100	-	ppm/°C
Offset Error	HPF enabled		0	-	-	LSB
	HPF disabled		-	-	100	
Analog Input Characteristics						
Full-scale Differential Input Voltage			1.07*VA	1.13*VA	1.19*VA	Vpp
Input Impedance (Differential)			-	250	-	kΩ
Common Mode Rejection Ratio		CMRR	-	82	-	dB

ANALOG PERFORMANCE (AUTOMOTIVE)

Test Conditions (unless otherwise specified). VA = 5.25 to 4.75 V, VD = 5.25 to 3.14 V, VLS = VLC = 5.25 to 1.71 V and T_A = -40° to +85° C. Full-scale input sine wave. Measurement Bandwidth is 10 Hz to 20 kHz.

Parameter		Symbol	Min	Typ	Max	Unit
Single-Speed Mode Fs = 48 kHz						
Dynamic Range	A-weighted		106	114	-	dB
	unweighted		103	111		
Total Harmonic Distortion + Noise	-1 dB			-105	-97	
referred to typical full scale	-20 dB	THD+N	-	-91	-	dB
	-60 dB			-51	-45	
Double-Speed Mode Fs = 96 kHz						
Dynamic Range	A-weighted		106	114		
	unweighted		103	111	-	dB
	40 kHz bandwidth unweighted		-	108		
Total Harmonic Distortion + Noise	-1 dB			-105	-97	
referred to typical full scale	-20 dB	THD+N	-	-91	-	dB
	-60 dB			-51	-45	
	40 kHz bandwidth -1 dB			-102	-	
Quad-Speed Mode Fs = 192 kHz						
Dynamic Range	A-weighted		106	114		
	unweighted		103	111	-	dB
	40 kHz bandwidth unweighted		-	108		
Total Harmonic Distortion + Noise	-1 dB			-105	-97	
referred to typical full scale	-20 dB	THD+N	-	-91	-	dB
	-60 dB			-51	-45	
	40 kHz bandwidth -1 dB			-102	-	
Dynamic Performance for All Modes						
Interchannel Isolation			-	110	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	-	dB
Gain Error			-7	-	7	%
Gain Drift			-	± 100	-	ppm/°C
Offset Error	HPF enabled		0	-	-	LSB
	HPF disabled		-	-	100	
Analog Input Characteristics						
Full-scale Input Voltage			1.02*VA	1.13*VA	1.24*VA	Vpp
Input Impedance (Differential)				250	-	kΩ
Common Mode Rejection Ratio		CMRR	-	82	-	dB

DIGITAL FILTER CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Single-Speed Mode (2 kHz to 54 kHz sample rates)					
Passband (Note 1) (-0.1 dB)		0	-	0.47	Fs
Passband Ripple		-0.035		0.035	dB
Stopband (Note 1)		0.58		-	Fs
Stopband Attenuation		-95			dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	12/Fs		s
Double-Speed Mode (54 kHz to 108 kHz sample rates)					
Passband (Note 1) (-0.1 dB)		0	-	0.45	Fs
Passband Ripple		-0.035		0.035	dB
Stopband (Note 1)		0.68		-	Fs
Stopband Attenuation		-92			dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	9/Fs		s
Quad-Speed Mode (108 kHz to 216 kHz sample rates)					
Passband (Note 1) (-0.1 dB)		0	-	0.24	Fs
Passband Ripple		-0.035		0.035	dB
Stopband (Note 1)		0.78		-	Fs
Stopband Attenuation		-92			dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	5/Fs		s
High-Pass Filter Characteristics					
Frequency Response (Note 2) -3.0 dB -0.13 dB		-	1 20	-	Hz
Phase Deviation (Note 2) @ 20 Hz		-	10	-	Deg
Passband Ripple			-	0	dB
Filter Settling Time			10^5/Fs	-	s

Notes:

1. The filter frequency response scales precisely with Fs.
2. Response shown is for Fs equal to 48 kHz. Filter characteristics scale with Fs.

OVERFLOW TIMEOUT

Logic "0" = GND = 0 V; Logic "1" = VLS; C_L = 30 pF, timing threshold is 50% of VLS.

Parameter	Symbol	Min	Typ	Max	Unit
OVFL time-out on overrange condition Fs = 44.1 kHz Fs = 192 kHz		-	$(2^{17}-1)$/Fs 2972 683	-	ms

SERIAL AUDIO INTERFACE - I²S/LJ TIMING

The serial audio port is a three-pin interface consisting of SCLK, LRCK and SDOUT.
Logic "0" = GND = 0 V; Logic "1" = VLS; C_L = 20 pF, timing threshold is 50% of VLS.

Parameter		Symbol	Min	Typ	Max	Unit
Sample Rates	Single-Speed Mode Double-Speed Mode Quad-Speed Mode	-	2 54 108	-	54 108 216	kHz
Master Mode						
SCLK Frequency		-	64*Fs	-	64*Fs	Hz
SCLK Period	1/(64*216 kHz)	t_{PERIOD}	72.3	-	-	ns
SCLK Duty Cycle (Note 1)	(CLKMODE = 0)(Note 2)	t_{HIGH}	40	50	60	%
	(CLKMODE = 1)(Note 2)	t_{HIGH}	28	33	38	%
LRCK setup	before SCLK rising	t_{SETUP1}	20	-	-	ns
LRCK hold	after SCLK rising	t_{HOLD1}	20			
SDOUT setup	before SCLK rising	t_{SETUP2}	10	-	-	ns
SDOUT hold	after SCLK rising (VLS = 1.8 V)	t_{HOLD2}	20			
	after SCLK rising (VLS = 3.3 V)	t_{HOLD2}	10			
	after SCLK rising (VLS = 5 V)	t_{HOLD2}	5			
Slave Mode						
SCLK Frequency (Note 3)		-	-	64*Fs	-	Hz
SCLK Period	1/(64*216 kHz)	t_{PERIOD}	72.3	-	-	ns
SCLK Duty Cycle		t_{HIGH}	28	-	65	%
LRCK setup	before SCLK rising	t_{SETUP1}	20	-	-	ns
LRCK hold	after SCLK rising	t_{HOLD1}	20			
SDOUT setup	before SCLK rising (VLS = 1.8 V)	t_{SETUP2}	4	-	-	ns
	before SCLK rising (VLS = 3.3 V)	t_{SETUP2}	10			
	before SCLK rising (VLS = 5 V)	t_{SETUP2}	10			
SDOUT hold	after SCLK rising (VLS = 1.8 V)	t_{HOLD2}	20			
	after SCLK rising (VLS = 3.3 V)	t_{HOLD2}	10			
	after SCLK rising (VLS = 5 V)	t_{HOLD2}	5			

Notes:

1. Duty cycle of generated SCLK depends on duty cycle of received MCLK as specified under "System Clocking" on page 10.
2. CLKMODE functionality described in Section 4.6.3 "Master Mode Clock Dividers" on page 24.
3. In Slave Mode, the SCLK/LRCK ratio can be set according to preference. However, chip performance is guaranteed only when using the ratios in Section 4.7 Master and Slave Clock Frequencies on page 25.

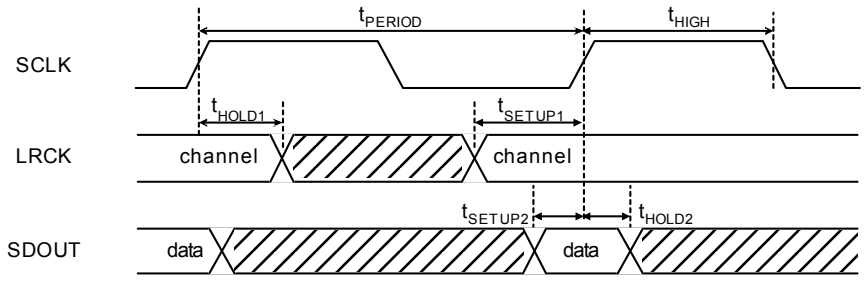

Figure 3. I²S/LJ Timing

SERIAL AUDIO INTERFACE - TDM TIMING

The serial audio port is a three-pin interface consisting of SCLK, LRCK and SDOUT.
Logic "0" = GND = 0 V; Logic "1" = VLS; C_L = 20 pF, timing threshold is 50% of VLS.

Parameter		Symbol	Min	Typ	Max	Unit
Sample Rates	Single-Speed Mode	-	2	-	54	kHz
	Double-Speed Mode	-	54	-	108	kHz
	Quad-Speed Mode[1]	-	108	-	216	kHz
Master Mode						
SCLK Frequency			256*Fs	-	256*Fs	Hz
SCLK Period	1/(256*216 kHz)	t_{PERIOD}	18	-	-	ns
SCLK Duty Cycle (Note 2)	(CLKMODE = 0)(Note 3)	t_{HIGH1}	40	50	60	%
	(CLKMODE = 1)(Note 3)	t_{HIGH1}	28	33	38	%
FS setup	before SCLK rising (Single-Speed Mode)	t_{SETUP1}	20	-	-	ns
FS setup	before SCLK rising (Double-Speed Mode)	t_{SETUP1}	18	-	-	ns
FS setup	before SCLK rising (Quad-Speed Mode)	t_{SETUP1}	5	-	-	ns
FS width	in SCLK cycles	t_{HIGH2}	128	-	128	-
SDOUT setup	before SCLK rising	t_{SETUP2}	5	-	-	ns
SDOUT hold	after SCLK rising	t_{HOLD2}	5	-	-	ns
Slave Mode						
SCLK Frequency (Note 4)			-	256*Fs	-	Hz
SCLK Period	1/(256*216 kHz)	t_{PERIOD}	18	-	-	ns
SCLK Duty Cycle		t_{HIGH1}	28	-	65	%
FS setup	before SCLK rising (Single-Speed Mode)	t_{SETUP1}	20	-	-	ns
FS setup	before SCLK rising (Double-Speed Mode)	t_{SETUP1}	20	-	-	ns
FS setup	before SCLK rising (Quad-Speed Mode)	t_{SETUP1}	10	-	-	ns
FS width	in SCLK cycles	t_{HIGH2}	1	-	244	-
SDOUT setup	before SCLK rising	t_{SETUP2}	5	-	-	ns
SDOUT hold	after SCLK rising	t_{HOLD2}	5	-	-	ns

Notes:

1. TDM Quad-Speed Mode only specified to operate correctly at VLS ≥ 3.14 V.
2. Duty cycle of generated SCLK depends on duty cycle of received MCLK as specified under "System Clocking" on page 10.
3. CLKMODE functionality described in Section 4.6.3 "Master Mode Clock Dividers" on page 24.
4. In Slave Mode, the SCLK/LRCK ratio can be set according to preference; chip performance is guaranteed only when using the ratios in Section 4.7 Master and Slave Clock Frequencies on page 25.

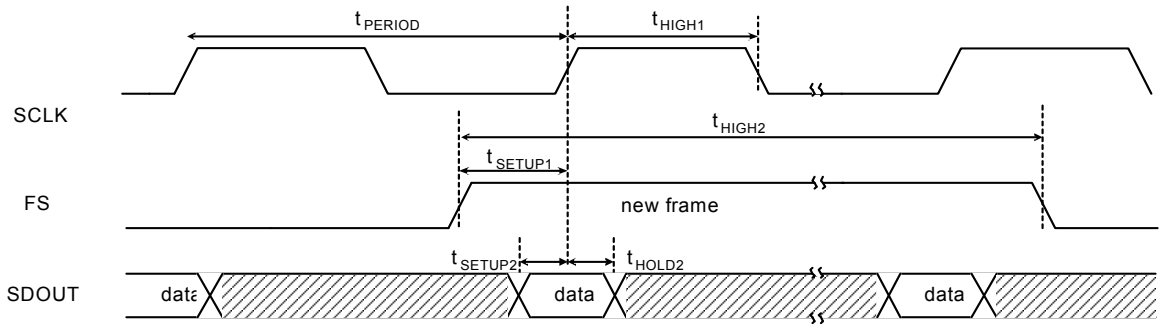

Figure 4. TDM Timing

SWITCHING SPECIFICATIONS - CONTROL PORT - I²C TIMING

Inputs: Logic 0 = DGND, Logic 1 = VLC, SDA C_L = 30 pF

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{RST}$ Rising Edge to Start	t_{irs}	600	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 1)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising (Note 2)	t_{sud}	600	-	ns
Rise Time of SCL and SDA	t_{rc}	-	1	µs
Fall Time SCL and SDA	t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	1000	ns

Notes:

1. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

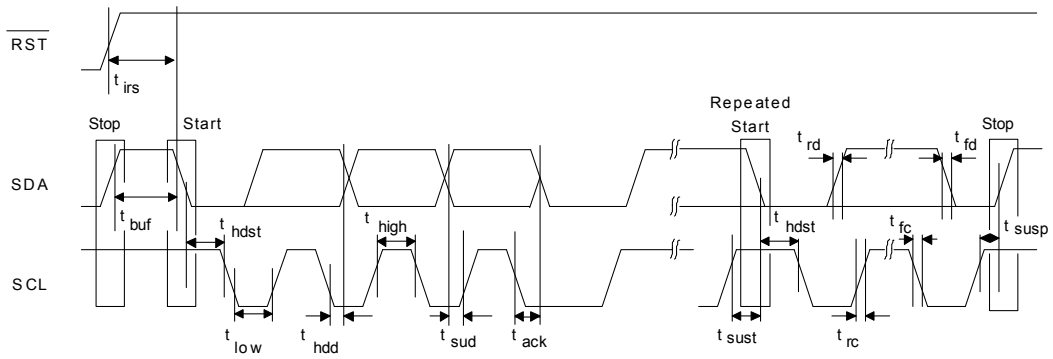

Figure 5. I²C Timing

2. The operational timing specification deviates from the *I2C-Bus Specification and User Manual* of 250 ns.

SWITCHING SPECIFICATIONS - CONTROL PORT - SPI TIMING

Inputs: Logic 0 = DGND, Logic 1 = VLC, CDOUT C_L = 30 pF

Parameter		Symbol	Min	Max	Units
CCLK Clock Frequency		f_{sck}	0	6.0	MHz
$\overline{RST}$ Rising Edge to $\overline{CS}$ Falling		t_{srs}	20		ns
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20		
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0		µs
CCLK Low Time		t_{scl}	66	-	
CCLK High Time		t_{sch}	66		
CDIN to CCLK Rising Setup Time		t_{dsu}	40		
CCLK Rising to DATA Hold Time	(Note 1)	t_{dh}	15		
CCLK Falling to CDOUT Stable		t_{pd}		50	ns
Rise Time of CDOUT		t_{r1}		25	
Fall Time of CDOUT		t_{f1}	-		
Rise Time of CCLK and CDIN	(Note 2)	t_{r2}		100	
Fall Time of CCLK and CDIN	(Note 2)	t_{f2}			

Notes:

1. Data must be held for sufficient time to bridge the transition time of CCLK.
2. For f_{sck} <1 MHz

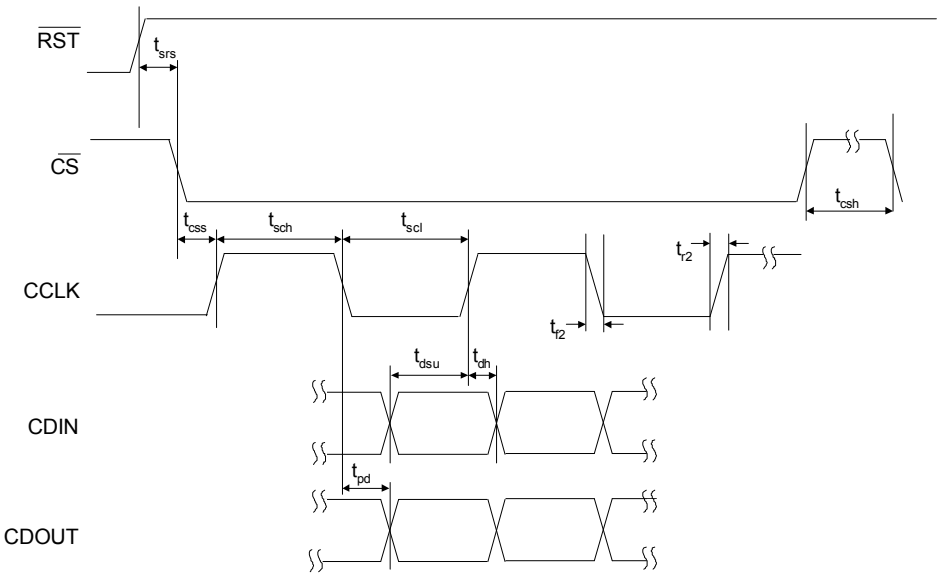

Figure 6. SPI Timing

4. APPLICATIONS

4.1 Power

CS5364 features five independent power pins that power various functional blocks within the device and allow for convenient interfacing to other devices. Table 1 shows what portion of the device is powered from each supply pin. Please refer to "Recommended Operating Conditions" on page 10 for the valid range of each power supply pin. The power supplied to each power pin can be independent of the power supplied to any other pin.

Power Supply Pin		
Pin Name	**Pin Number**	**Functional Block**
VA	4, 9	Analog Core
VX	20	Crystal Oscillator
VD	33	Digital Core
VLS	28	Serial Audio Interface
VLC	35	Control Logic

Table 1. Power Supply Pin Definitions

To meet full performance specifications, the CS5364 requires normal low-noise board layout. The "Typical Connection Diagram" on page 9 shows the recommended power arrangements, with the VA pins connected to a clean supply. VD, which powers the digital filter, may be run from the system logic supply, or it may be powered from the analog supply via a single-pole decoupling filter.

Decoupling capacitors should be placed as near to the ADC as possible, with the lower value high-frequency capacitors placed nearest to the device leads. Clocks should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling of these signals into the device. The FILT+ and VQ decoupling capacitors must be positioned to minimize the electrical path to ground.

The CDB5364 evaluation board demonstrates optimum layout for the device.

4.2 Control Port Mode and Stand-Alone Operation

4.2.1 Stand-Alone Mode

In Stand-Alone Mode, the CS5364 is programmed exclusively with multi-use configuration pins. This mode provides a set of commonly used features, which comprise a subset of the complete set of device features offered in Control Port Mode.

To use the CS5364 in Stand-Alone Mode, the configuration pins must be held in a stable state, at valid logic levels, and $\overline{\text{RST}}$ must be asserted until the power supplies and clocks are stable and valid. More information on the reset function is available in Section 4.5 on page 22.

4.2.2 Control Port Mode

In Control Port Mode, all features of the CS5364 are available. Four multi-use configuration pins become software pins that support the I²C or SPI bus protocol. To initiate Control Port Mode, a controller that supports I²C or SPI must be used to enable the internal register functionality. This is done by setting the CP-EN bit (Bit 7 of the Global Control Port Register). Once CP-EN is set, all of the device configuration pins are ignored, and the internal register settings determine the operating modes of the part. Figure 4.13 on page 30 provides detailed information about the I²C and SPI bus protocols.

4.3 Master Clock Source

The CS5364 requires a Master Clock that can come from one of two sources: an on-chip crystal oscillator driver or an externally generated clock.

4.3.1 On-Chip Crystal Oscillator Driver

When using the on-board crystal oscillator driver, the XTI pin (pin 21) is the input for the Master Clock (MCLK) to the device. The XTO pin (pin 22) must not be used to drive anything other than the oscillator tank circuitry. When using the on-board crystal driver, the topology shown in Figure 7 must be used. The crystal oscillator manufacturer supplies recommended capacitor values. A buffered copy of the XTI input is available as an output on the MCLK pin (pin 23), which is level-controlled by VLS and may be used to synchronize other parts to the device.

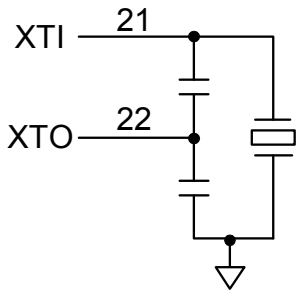

Figure 7. Crystal Oscillator Topology

4.3.2 Externally Generated Master Clock

If an external clock is used, the XTI and XTO pins must be grounded, and the MCLK pin becomes an input for the system master clock. The incoming MCLK should be at the logic level set by the user on the VLS supply pin.

4.4 Master and Slave Operation

CS5364 operation depends on two clocks that are synchronously derived from MCLK: SCLK and LRCK/FS. See Section 4.5 on page 22 for a detailed description of SCLK and LRCK/FS.

The CS5364 can operate as either clock master or clock slave with respect to SCLK and LRCK/FS. In Master Mode, the CS5364 derives SCLK and LRCK/FS synchronously from MCLK and outputs the derived clocks on the SCLK pin (pin 25) and the LRCK/FS pin (pin 24), respectively. In Slave Mode, the SCLK and LRCK/FS are inputs, and the input signals must be synchronously derived from MCLK by a separate device such as another CS5364 or a microcontroller. Figure 8 illustrates the clock flow of SCLK and LRCK/FS in both Master and Slave Modes.

The Master/Slave operation is controlled through the settings of M1 and M0 pins in Stand-Alone Mode or by the M[1] and M[0] bits in the Global Mode Control Register in Control Port Mode. See Section 4.6 on page 23 for more information regarding the configuration of M1 and M0 pins or M[1] and M[0] bits.

Figure 8. Master/Slave Clock Flow

4.4.1 Synchronization of Multiple Devices

To ensure synchronous sampling in applications where multiple ADCs are used, the MCLK and LRCK must be the same for all CS5364 devices in the system. If only one master clock source is needed, one solution is to place one CS5364 in Master Mode, and slave all of the other devices to the one master, as illustrated in Figure 9. If multiple master clock sources are needed, one solution is to supply all clocks from the same external source and time the CS5364 reset de-assertion with the falling edge of MCLK. This will ensure that all converters begin sampling on the same clock edge.

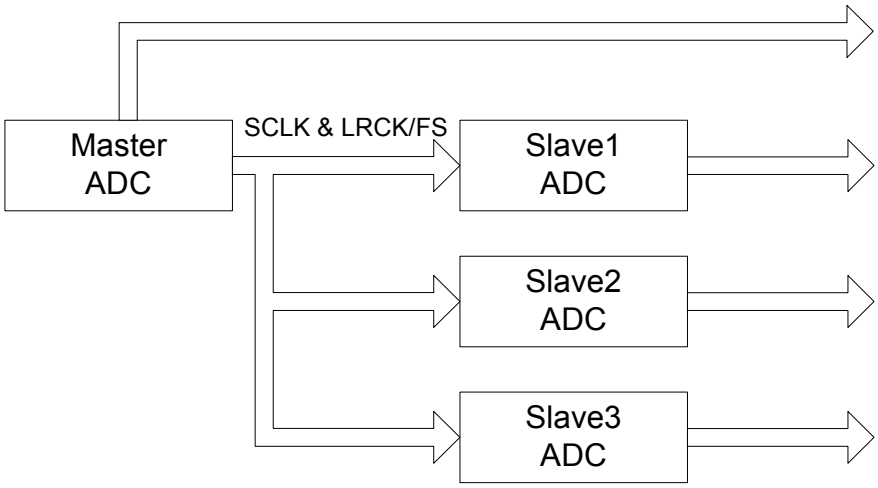

Figure 9. Master and Slave Clocking for a Multi-Channel Application

4.5 Serial Audio Interface (SAI) Format

The SAI port consists of two timing pins (SCLK, LRCK/FS) and four audio data output pins (SDOUT1/TDM, SDOUT2, SDOUT3/TDM and SDOUT4). The CS5364 output is serial data in I²S, Left-Justified (LJ), or Time Division Multiplexed (TDM) digital audio interface formats. These formats are available to the user in both Stand-Alone Mode and Control Port Mode.

4.5.1 I²S and LJ Format

The I²S and LJ formats are both two-channel protocols. During one LRCK period, two channels of data are transmitted, odd channels first, then even. The MSB is always clocked out first.

In Slave Mode, the number of SCLK cycles per channel is fixed as described under "Serial Audio Interface - I²S/LJ Timing" on page 15. In Slave Mode, if more than 32 SCLK cycles per channel are received from a master controller, the CS5364 will fill the longer frame with trailing zeros. If fewer than 24 SCLK cycles per channel are received from a master, the CS5364 will truncate the serial data output to the number of SCLK cycles received. For a complete overview of serial audio interface formats, please refer to Cirrus Logic Application Note AN282.

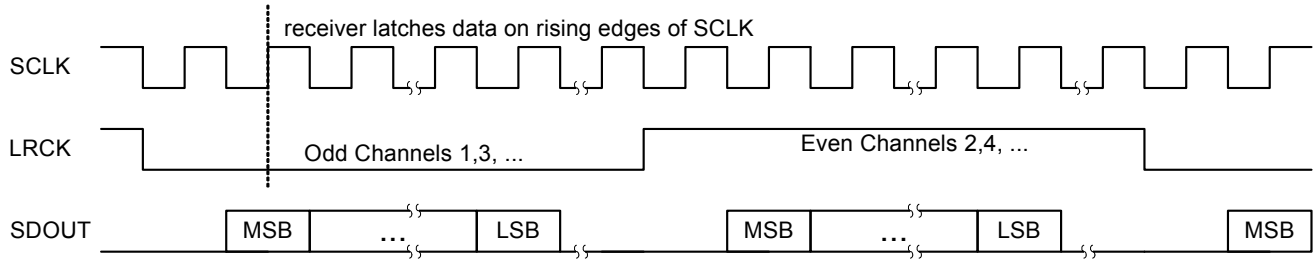

Figure 10. I²S Format

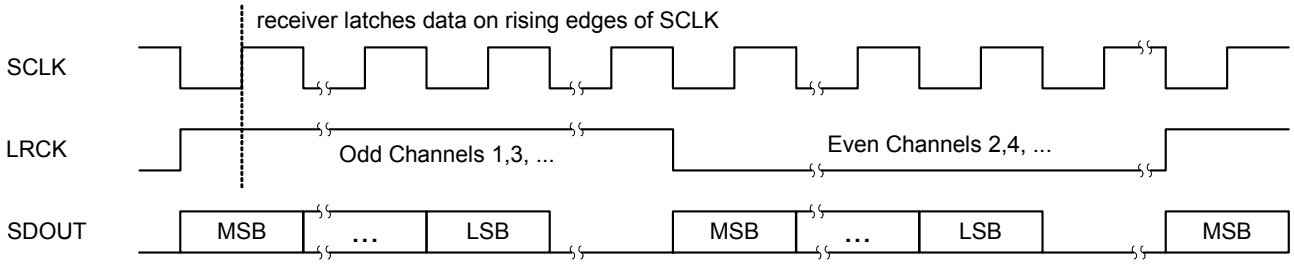

Figure 11. LJ Format

4.5.2 TDM Format

In TDM Mode, all four channels of audio data are serially clocked out during a single Frame Sync (FS) cycle, as shown in Figure 12. The rising edge of FS signifies the start of a new TDM frame cycle. Each channel slot occupies 32 SCLK cycles, with the data left justified and with MSB first. TDM output data should be latched on the rising edge of SCLK within time specified under "Serial Audio Interface - TDM Timing" section on page 16. The TDM data output port resides on the SDOUT1 pin. The $\overline{\text{TDM}}$ output pin is complimentary TDM data. All SDOUT pins will remain active during TDM Mode. Refer to Section 4.11 "Optimizing Performance in TDM Mode" on page 29 for critical system design information.

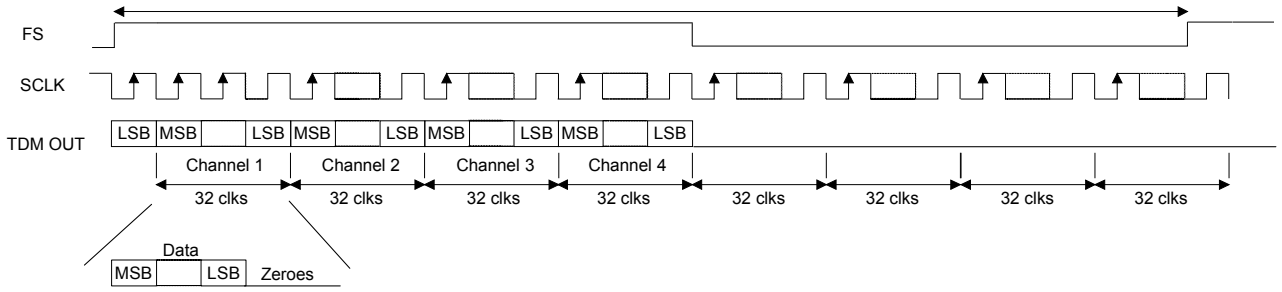

Figure 12. TDM Format

4.5.3 Configuring Serial Audio Interface Format

The serial audio interface format of the data is controlled by the configuration of the DIF1 and DIF0 pins in Stand-Alone Mode or by the DIF[1] and DIF[0] bits in the Global Mode Control Register in Control Port Mode, as shown in Table 2.

DIF1	DIF0	Mode
0	0	Left-Justified
0	1	I²S
1	0	TDM
1	1	Reserved

Table 2. DIF1 and DIF0 Pin Settings

4.6 Speed Modes

4.6.1 Sample Rate Ranges

CS5364 supports sampling rates from 2 kHz to 21 kHz, divided into three ranges: 2 kHz - 54 kHz, 54 kHz - 108 kHz, and 108 kHz - 216 kHz. These sampling speed modes are called Single-Speed Mode (SSM), Double-Speed Mode (DSM), and Quad-Speed Mode (QSM), respectively.

4.6.2 Using M1 and M0 to Set Sampling Parameters

The Master/Slave operation and the sample rate range are controlled through the settings of the M1 and M0 pins in Stand-Alone Mode, or by the M[1] and M[0] bits in the Global Mode Control Register in Control Port Mode, as shown in Table 3.

M1	M0	Mode	Frequency Range
0	0	Single-Speed Master Mode (SSM)	2 kHz - 54 kHz
0	1	Double-Speed Master Mode (DSM)	54 kHz - 108 kHz
1	0	Quadruple-Speed Master Mode (QSM)	108 kHz - 216 kHz
1	1	Auto-Detected Speed Slave Mode	2 kHz - 216 kHz

Table 3. M1 and M0 Settings

4.6.3 Master Mode Clock Dividers

Figure 13 shows the configuration of the MCLK dividers and the sample rate dividers for Master Mode, including the significance of each MCLK divider pin (in Stand-Alone Mode) or bit (in Control Port Mode).

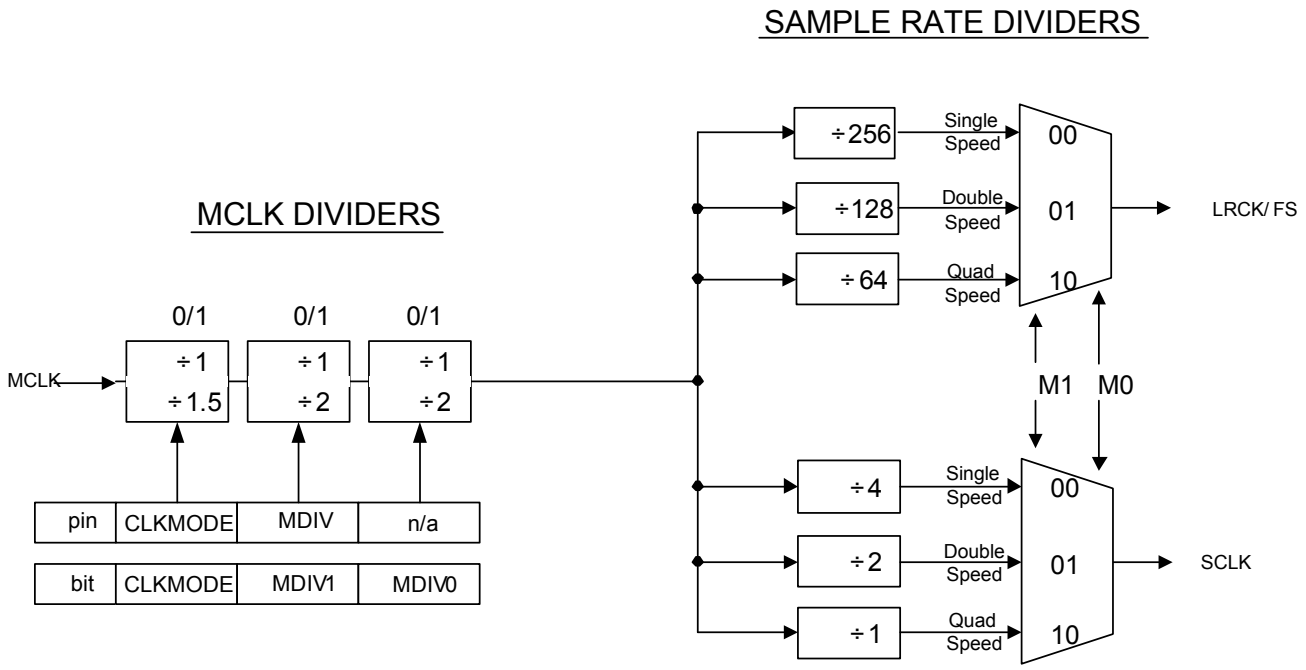

Figure 13. Master Mode Clock Dividers

4.6.4 Slave Mode Audio Clocking With Auto-Detect

In Slave Mode, CS5364 auto-detects speed mode, which eliminates the need to configure M1 and M0 when changing among speed modes. The external MCLK is subject to clock dividers as set by the clock divider pins in Stand-Alone Mode or the clock divider bits in Control Port Mode. The CS5364 compares the divided-down, internal MCLK to the incoming LRCK/FS and sets the speed mode based on the MCLK/LRCK ratio as shown in Figure 14.

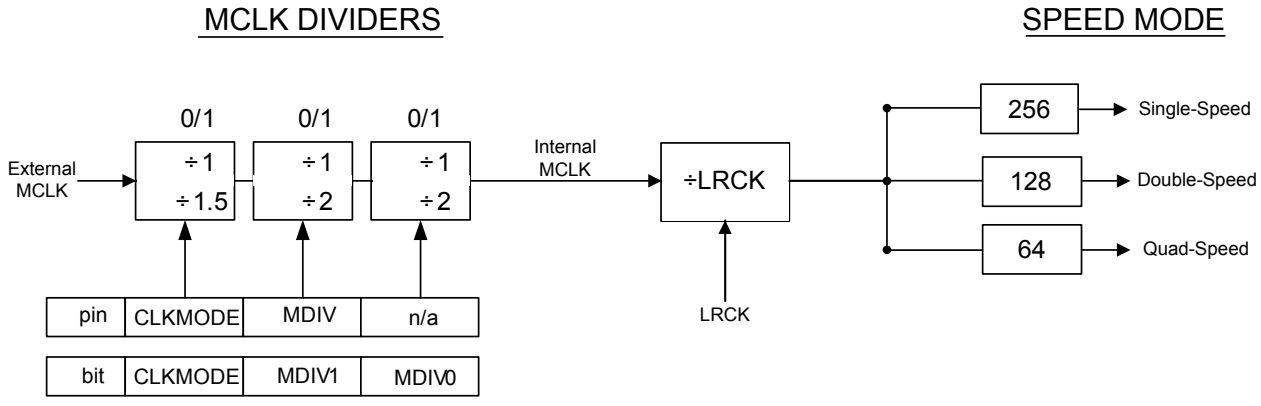

Figure 14. Slave Mode Auto-Detect Speed

4.7 Master and Slave Clock Frequencies

Tables 4 through 12 show the clock speeds for sample rates of 48 kHz, 96 kHz and 192 kHz. The MCLK/LRCK ratio should be kept at a constant value during each mode. In Master Mode, the device outputs the frequencies shown. In Slave Mode, the SCLK/LRCK ratio can be set according to design preference. However, device performance is guaranteed only when using the ratios shown in the tables.

Control Port Mode only

LJ/I²S MASTER OR SLAVE	SSM Fs = 48 kHz				
MCLK Divider	÷**4**	÷3	÷2	÷1.5	÷1
MCLK (MHz)	49.152	36.864	24.576	18.384	12.288
SCLK (MHz)	3.072	3.072	3.072	3.072	3.072
MCLK/LRCK Ratio	1024	768	512	384	256
SCLK/LRCK Ratio	64	64	64	64	64

Table 4. Frequencies for 48 kHz Sample Rate using LJ/I²S

LJ/I²S MASTER OR SLAVE	DSM Fs = 96 kHz				
MCLK Divider	÷**4**	÷3	÷2	÷1.5	÷1
MCLK (MHz)	49.152	36.864	24.567	18.384	12.288
SCLK (MHz)	6.144	6.144	6.144	6.144	6.144
MCLK/LRCK Ratio	512	384	256	192	128
SCLK/LRCK Ratio	64	64	64	64	64

Table 5. Frequencies for 96 kHz Sample Rate using LJ/I²S

LJ/I²S MASTER OR SLAVE	QSM Fs = 192 kHz				
MCLK Divider	÷**4**	÷3	÷2	÷1.5	÷1
MCLK (MHz)	49.152	36.864	24	18.384	12.288
SCLK (MHz)	12.288	12.288	12.288	12.288	12.288
MCLK/LRCK Ratio	256	192	128	96	64
SCLK/LRCK Ratio	64	64	64	64	64

Table 6. Frequencies for 192 kHz Sample Rate using LJ/I²S

TDM MASTER	SSM Fs = 48 kHz				
MCLK Divider	÷**4**	÷3	÷2	÷1.5	÷1
MCLK (MHz)	49.152	36.864	24.567	18.384	12.288
SCLK (MHz)	12.288	12.288	12.288	12.288	12.288
MCLK/FS Ratio	1024	768	512	384	256
SCLK/FS Ratio	256	256	256	256	256

Table 7. Frequencies for 48 kHz Sample Rate using TDM

TDM SLAVE	SSM Fs = 48 kHz				
MCLK Divider	÷**4**	÷3	÷2	÷1.5	÷1
MCLK (MHz)	49.152	36.864	24.567	18.384	12.288
SCLK (MHz)	12.288	12.288	12.288	12.288	12.288
MCLK/FS Ratio	1024	768	512	384	256
SCLK/FS Ratio	256	256	256	256	256

Table 8. Frequencies for 48 kHz Sample Rate using TDM