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CS5373A

Low-power, High-performance ΔΣ Modulator and Test DAC

Modulator Features

- Fourth-order ΔΣ Architecture
  - Clock-jitter-tolerant architecture
  - Input signal bandwidth: DC to 2 kHz
  - Max AC amplitude: 5 V_{pp} differential
  - Max DC amplitude: ± 2.5 V_{dc} differential
- High Dynamic Range
  - 127 dB SNR @ 215 Hz BW (2 ms sampling)
  - 124 dB SNR @ 430 Hz BW (1 ms sampling)
- Low Total Harmonic Distortion
  - -118 dB THD typical (0.000126%)
  - -112 dB THD maximum (0.000251%)
- Low Power Consumption: 25 mW, 10 µW

Test DAC Features

- Digital ΔΣ Input from CS5378 Digital Filter
- Selectable Differential Analog Outputs
  - Precision output (OUT±) for electronics tests
  - Buffered output (BUF±) for sensor tests
- Multiple AC and DC Operational Modes
  - Output signal bandwidth: DC to 100 Hz
  - Max AC amplitude: 5 V_{pp} differential
  - Max DC amplitude: + 2.5 V_{dc} differential
- Selectable Attenuation to Match CS3301A/02A
  - 1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64
- Outstanding Performance
  - OUT AC: -115 dB THD typical, -112 dB maximum
  - BUF AC: -105 dB THD typical, -95 dB maximum
  - OUT DC: Differential VREF ± 10 mV typical
  - BUF DC: Differential VREF ± 25 mV typical
- Low Power Consumption
  - AC modes / DC modes: 40 mW / 25 mW
  - Sleep mode / Power down: 2.5 mW / 600 µW

Common Features

- Extremely Small Footprint
  - 28-pin SSOP package, 8 mm x 10 mm
- Bipolar Power Supply Configuration
  - VA+ = +2.5 V; VA- = -2.5 V; VD = +3.3 V

Description

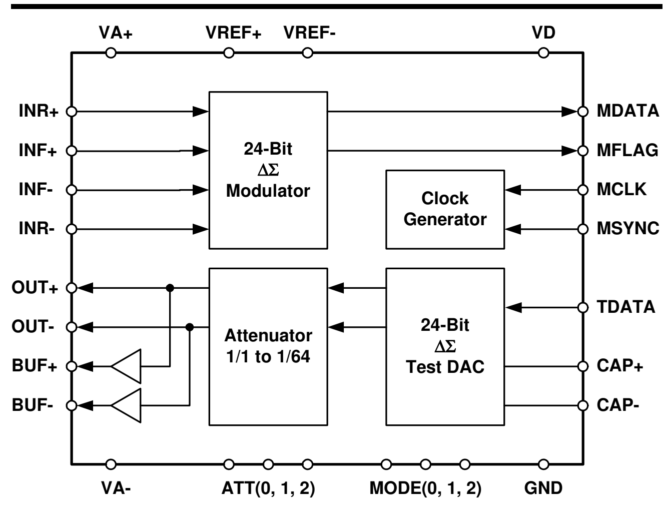
The CS5373A is a high-performance, fourth-order ΔΣ modulator integrated with a ΔΣ digital-to-analog converter (DAC). When combined with a CS3301A/02A differential amplifier and the CS5378 digital filter, a small, low-power, self-testing, high-accuracy, single-channel measurement system results.

The modulator has high dynamic range and low total harmonic distortion with very low power consumption. It converts differential analog input signals from the CS3301A/02A amplifier to an oversampled serial bit stream at 512 kbits per second. This oversampled bit stream is then decimated by the CS5378 digital filter to a 24-bit output at the selected output word rate.

The test DAC operates in either AC or DC test modes. AC test modes measure system dynamic performance through THD and CMRR tests while DC test modes are for gain calibration and pulse tests. It has two sets of differential analog outputs, *OUT* and *BUF*, as dedicated outputs for testing the electronics channel and for in-circuit sensor tests. Output attenuation settings are binary weighted and match the gain settings of the CS3301A/02A differential amplifiers for full-scale testing at all gain ranges.

ORDERING INFORMATION

See page 39.



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1. CHARACTERISTICS AND SPECIFICATIONS

- Min / Max characteristics and specifications are guaranteed over the *Specified Operating Conditions*.
- Typical performance characteristics and specifications are measured at nominal supply voltages and T_A = 25°C.
- GND = 0 V. Single-ended voltages with respect to GND, differential voltages with respect to opposite half.
- Device is connected as shown in Figure 8 on page 20 unless otherwise noted.

SPECIFIED OPERATING CONDITIONS

Parameter		Symbol	Min	Nom	Max	Unit
Bipolar Power Supplies						
Positive Analog	± 2%	VA+	2.45	2.50	2.55	V
Negative Analog	(Note 1) ± 2%	VA-	-2.45	-2.50	-2.55	V
Positive Digital	± 3%	VD	3.20	3.30	3.40	V
Voltage Reference						
{VREF+} - {VREF-}	(Note 2, 3)	VREF	-	2.500	-	V
VREF-	(Note 4)	VREF-	-	VA -	-	V
Thermal						
Ambient Operating Temperature	Industrial (-IS, -ISZ)	T_A	-40	25	85	°C

Notes: 1. VA- must always be the most-negative input voltage to avoid potential SCR latch-up conditions.

2. By design, a 2.500 V voltage reference input results in the best signal-to-noise performance.
3. Full-scale accuracy is directly proportional to the voltage reference absolute accuracy.
4. VREF inputs must satisfy: VA- ≤ VREF- < VREF+ ≤ VA+.

Modes of Operation		
Selection	**MODE [2:0]**	**Mode Description**
0	0 0 0	***Modulator:*** enabled. ***DAC:*** sleep.
1	0 0 1	***Modulator:*** enabled. ***DAC:*** AC OUT and BUF outputs.
2	0 1 0	***Modulator:*** enabled. ***DAC:*** AC OUT only, BUF high-z.
3	0 1 1	***Modulator:*** enabled. ***DAC:*** AC BUF only, OUT high-z.
4	1 0 0	***Modulator:*** enabled. ***DAC:*** DC common mode output.
5	1 0 1	***Modulator:*** enabled. ***DAC:*** DC differential output.
6	1 1 0	***Modulator:*** enabled. ***DAC:*** AC common mode output.
7	1 1 1	***Modulator:*** sleep. ***DAC:*** sleep.

DAC Attenuation			
Selection	**ATT[2:0]**	**Attenuation**	**dB**
0	0 0 0	1/1	0 dB
1	0 0 1	1/2	-6.02 dB
2	0 1 0	1/4	-12.04 dB
3	0 1 1	1/8	-18.06 dB
4	1 0 0	1/16	-24.08 dB
5	1 0 1	1/32	-30.10 dB
6	1 1 0	1/64	-36.12 dB
7	1 1 1	reserved	reserved

Table 1. Selections for Operational Mode and DAC Attenuation

TEMPERATURE CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Operating Temperature	T_A	-40	-	85	ºC
Storage Temperature Range	T_{STR}	-65	-	150	ºC
Allowable Junction Temperature	T_{JCT}	-	-	125	ºC
Junction to Ambient Thermal Impedance (4-layer PCB)	Θ_{JA}	-	65	-	ºC / W

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Parameter
DC Power Supplies	Positive Analog Negative Analog Digital	VA+ VA- VD	-0.5 -6.8 -0.5	6.8 0.5 6.8	V V V
Analog Supply Differential	(VA+) - (VA-)	VA_{DIFF}	-	6.8	V
Digital Supply Differential	(VD) - (VA-)	VD_{DIFF}	-	7.6	V
Input Current, Power Supplies	(Note 5)	I_{PWR}	-	±50	mA
Input Current, Any Pin Except Supplies	(Note 5, 6)	I_{IN}	-	±10	mA
Output Current	(Note 5)	I_{OUT}	-	±25	mA
Power Dissipation		PDN	-	500	mW
Analog Input Voltages		V_{INA}	(VA-) - 0.5	(VA+) + 0.5	V
Digital Input Voltages		V_{IND}	-0.5	(VD) + 0.5	V

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 5. Transient currents up to ±100 mA will not cause SCR latch-up.

6. Includes continuous over-voltage conditions at the modulator analog input pins.

ANALOG INPUT CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
VREF Input					
{VREF+} - {VREF-} (Note 2, 3)	VREF	-	2.500	-	V
VREF- (Note 4)	VREF-	-	VA -	-	V
VREF Input Current, Modulator Only	$VREF_{IMOD}$	-	120	-	µA
VREF Input Current, Modulator + DAC AC Mode	$VREF_{IMAC}$	-	200	-	µA
VREF Input Current, Modulator + DAC DC Mode	$VREF_{IMDC}$	-	160	-	µA
VREF Input Noise (Note 7)	$VREF_{IN}$	-	-	1	μV_{rms}
Modulator INR±, INF± Inputs					
External Anti-alias Filter (Note 8, 9) Series Resistance Differential Capacitance	R_{AA} C_{AA}	- -	680 20	- -	Ω nF
Differential Input Impedance INR± INF±	$ZDIF_{INR}$ $ZDIF_{INF}$	- -	20 1	- -	kΩ MΩ
Single-ended Input Impedance INR± INF±	ZSE_{INR} ZSE_{INF}	- -	40 2	- -	kΩ MΩ
DAC CAP± Input					
External Anti-alias Filter (Note 9) Differential Capacitance	C_{AA}	-	10	-	nF

Notes: 7. Maximum integrated noise over the measurement bandwidth for the voltage reference device attached to the VREF± inputs.

8. The modulator analog inputs are normally driven by a CS3301A/02A amplifier.

9. Differential anti-alias capacitors are discrete external components and must be of good quality (C0G, NPO, poly). Poor quality capacitors will degrade total harmonic distortion (THD) performance.

ANALOG OUTPUT CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
DAC Analog OUT± Output						
Analog External Load at OUT± (Note 10, 11)	Load Resistance	R_{LOUT}	50	-	-	MΩ
	Load Capacitance	C_{LOUT}	-	-	50	pF
Differential Output Impedance	1/1	$ZDIF_{OUT}$	-	1.4	-	kΩ
	1/2		-	10.1	-	kΩ
	1/4		-	7.9	-	kΩ
	1/8		-	5.1	-	kΩ
	1/16		-	3.3	-	kΩ
	1/32		-	2.3	-	kΩ
	1/64		-	1.7	-	kΩ
Single-ended Output Impedance	1/1	ZSE_{OUT}	-	0.8	-	kΩ
	1/2		-	7.4	-	kΩ
	1/4		-	9.0	-	kΩ
	1/8		-	9.4	-	kΩ
	1/16		-	9.5	-	kΩ
	1/32		-	9.5	-	kΩ
	1/64		-	9.2	-	kΩ
High-Z Impedance		HZ_{OUT}	-	3	-	MΩ
Crosstalk to BUF± High-Z Output		XT_{OUT}	-	-120	-	dB
DAC Analog BUF± Output						
Analog External Load at BUF± (Note 10)	Load Resistance	R_{LBUF}	1	-	-	kΩ
	Load Capacitance	C_{LBUF}	-	-	2	nF
Differential Output Impedance	1/1 - 1/64	$ZDIF_{BUF}$	-	6	-	Ω
Single-ended Output Impedance	1/1 - 1/32	ZSE_{BUF}	-	4	-	Ω
	(Note 12) (BUF-) 1/64		-	4	-	
	(Note 12) (BUF+) 1/64		-	100	-	
High-Z Impedance		HZ_{BUF}	-	4.5	-	MΩ
Crosstalk to OUT± High-Z Output		XT_{BUF}	-	-120	-	dB

Notes: 10. Guaranteed by design and/or characterization.

11. Load on the precision OUT± outputs is normally from a CS3301A/02A amplifier, which has 2 GΩ/1 TΩ typical input impedance and 18 pF typical input capacitance.

12. Single-ended output impedance at 1/64 is different for BUF+ and BUF- due to the output attenuator architecture.

MODULATOR CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Input Characteristics						
Input Signal Frequencies	(Note 10, 13)	V_{BW}	DC	-	1720	Hz
Full Scale Differential AC Input	(Note 10)	V_{AC}	-	-	5	V_{pp}
Full Scale Differential DC Input	(Note 10)	V_{DC}	-2.5	-	2.5	V_{dc}
Input Voltage Range (Signal + V_{cm})	(Note 10, 14)	V_{RNG}	(VA-)+0.7	-	(VA+)-1.25	V
Input Common Mode Voltage	(Note 15)	V_{CM}	-	(VA-)+2.5	-	V
Dynamic Performance						
Dynamic Range (Note 16)	DC to 1720 Hz	SNR	-	109	-	dB
	DC to 860 Hz		-	121	-	dB
	DC to 430 Hz		121	124	-	dB
	DC to 215 Hz		-	127	-	dB
	DC to 108 Hz		-	130	-	dB
	DC to 54 Hz		-	133	-	dB
	DC to 27 Hz		-	136	-	dB
Signal Dependent Noise (Note 17, 18)	DC to 430 Hz	SDN	100	110	-	dB
Total Harmonic Distortion	(Note 18)	THD	-	-118	-112	dB
Linearity	(Note 18)	LIN	-	0.000126	0.000251	%
Common Mode Rejection Ratio		CMRR	-	90	-	dB
Gain Accuracy						
Channel to Channel Gain Accuracy	(Note 3)	CGA	-	±1	±2	%
Channel Gain Drift	(Note 19)	CGA_{TC}	-	5	-	ppm/°C
Offset						
Offset Voltage, Differential		OFST	-	100	-	mV
Offset Voltage Drift	(Note 19)	$OFST_{TC}$	-	0.1	-	µV/°C
Offset after Calibration	(Note 20)	$OFST_{CAL}$	-	±1	-	µV
Offset Calibration Range	(Note 21)	$OFST_{RNG}$	-	100	-	%FS

Notes: 13. The upper bandwidth limit is determined by the CS5378 digital filter cut-off frequency.

14. No signals operating from external power supplies should be applied to pins of the device prior to its own supplies being established. Connecting any terminal to voltages greater than VA+ or less than VA- may cause destructive latch-up.
15. Common mode voltage is defined as the mid-point of the differential signal.
16. Dynamic Range defined as 20 log [(RMS full scale) / (RMS idle noise)] where idle noise is measured from a CS3301A/02A amplifier terminated input at 1x gain.
17. Signal Dependent Noise defined as 20 log [(RMS full scale) / (RMS signal noise)] where signal noise is measured by subtracting the signal power at the fundamental and harmonic frequencies.
18. Tested with a 31.25 Hz sine wave at -1 dB amplitude.
19. Specification is for the parameter over the specified temperature range and is for the device only. It does not include the effects of external components.
20. This specification applies to the effective offset voltage calculated from the output codes of the CS5378 digital filter following offset calibration and correction.
21. Offset calibration is performed in the CS5378 digital filter and includes the full-scale signal range.

PERFORMANCE PLOTS

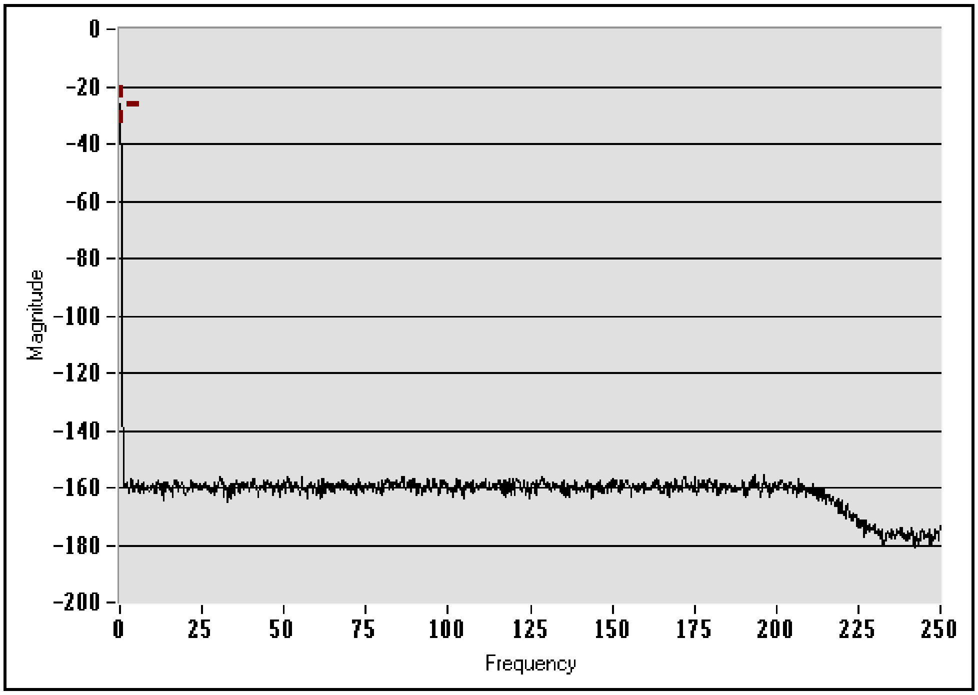

Figure 1. Modulator Noise Performance

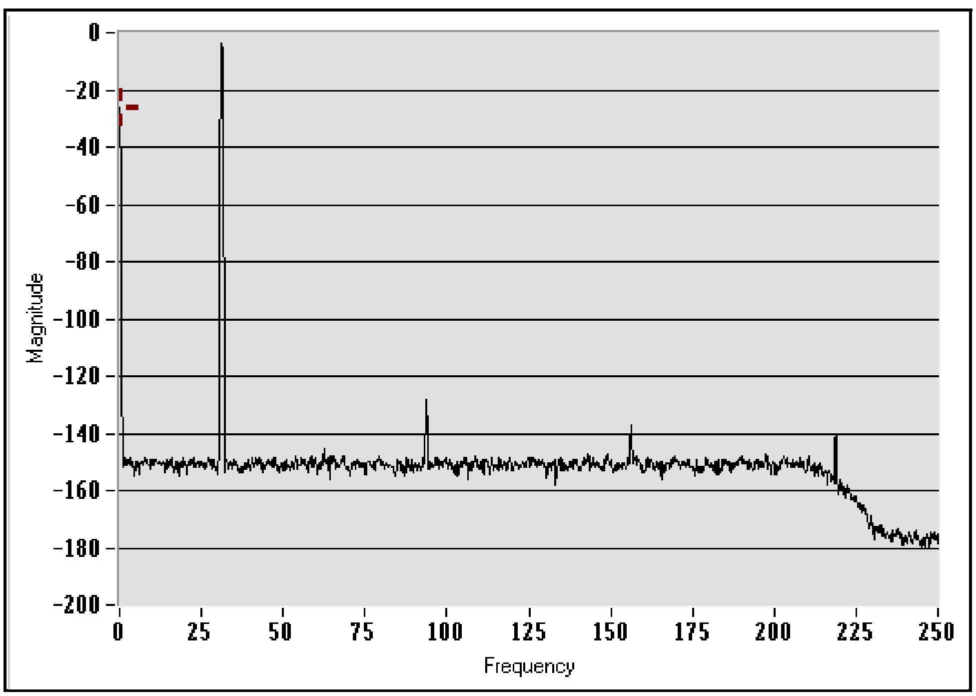

Figure 2. Modulator + Test DAC Dynamic Performance

DAC AC DIFFERENTIAL MODES 1, 2, 3

Parameter		Symbol	Min	Typ	Max	Unit
AC Differential Characteristics						
Full-scale Differential AC Output	1/1	VAC_{FS}	-	5	-	V_{pp}
	1/2		-	2.5	-	V_{pp}
	1/4		-	1.25	-	V_{pp}
	1/8		-	625	-	mV_{pp}
	1/16		-	312.5	-	mV_{pp}
	1/32		-	156.25	-	mV_{pp}
	1/64		-	78.125	-	mV_{pp}
Full-scale Bandwidth	(Note 10)	VAC_{BW}	-	-	100	Hz
Impulse Amplitude	(Note 10, 22)	VAC_{IMP}	-	-	-20	dBfs
AC Differential Accuracy						
Full-scale Accuracy	(Note 3, 23)	VAC_{ABS}	-	±1	±2	%FS
Relative Accuracy	(Note 24)	VAC_{REL}	-	±1	±2	%FS
Full-scale Drift	(Note 19)	VAC_{TC}	-	8	-	µV/°C
DC Common Mode Characteristics						
Common Mode	(Note 15)	VAC_{CM}	-	(VA-)+2.35	-	V
Common Mode Drift	(Note 15, 19)	VAC_{CMTC}	-	2	-	µV/°C

Notes: 22. Maximum amplitude for DAC operation above 100 Hz. A reduced amplitude for higher frequencies is required to guarantee stability of the low-power ΔΣ DAC architecture.

23. Full-scale accuracy tests the matching of 1/1 attenuation across multiple devices.

24. Relative accuracy tests the tracking of 1/1,1/2,1/4,1/16,1/32,1/64 attenuation relative to 1/8 attenuation on a single device.

DAC AC DIFFERENTIAL MODES 1, 2, 3 (CONT.)

Parameter		Symbol	Min	Typ	Max	Unit
Signal to Noise						
Signal to Noise (OUT± Unloaded) (Note 25)	1/1 1/2 1/4 1/8 1/16 1/32 1/64	SNR_{OUT}	110 - - - - - -	114 114 114 113 111 107 102	- - - - - - -	dB dB dB dB dB dB dB
Signal to Noise (BUF± Unloaded) (Note 25, 26)	1/1 1/2 1/4 1/8 1/16 1/32 1/64	SNR_{BUF}	100 - - - - - -	111 107 102 96 90 84 78	- - - - - - -	dB dB dB dB dB dB dB
Signal to Noise (BUF± 1 kΩ load) (Note 25, 26)	1/1	SNR_{BUFL}	100	110	-	dB
Total Harmonic Distortion						
Total Harmonic Distortion (OUT± Unloaded) (Note 18, 27)	1/1 1/2 1/4 1/8 1/16 1/32 1/64	THD_{OUT}	- - - - - - -	-115 -118 -116 -111 -109 -107 -101	-112 - - - - - -	dB dB dB dB dB dB dB
Total Harmonic Distortion (BUF± Unloaded) (Note 18, 26, 27)	1/1 1/2 1/4 1/8 1/16 1/32 1/64	THD_{BUF}	- - - - - - -	-111 -107 -102 -97 -92 -86 -80	-95 - - - - - -	dB dB dB dB dB dB dB
Total Harmonic Distortion (BUF± 1 kΩ load) (Note 18, 26, 27)	1/1	THD_{BUFL}	-	-95	-85	dB

Notes: 25. Specification measured using CS3301A amplifier at corresponding gain with the modulator measuring a 400 Hz bandwidth. Amplified noise dominates for x16, x32, x64 amplifier gains.

26. Buffered outputs (BUF±) include 1/f noise not present on the precision outputs (OUT±).

27. Specification measured using CS3301A amplifier at corresponding gain using the modulator measuring a 400 Hz bandwidth. Amplified noise in the harmonic bins dominates THD measurements for x16, x32, x64 amplifier gains.

DAC DC COMMON MODE 4

Parameter		Symbol	Min	Typ	Max	Unit
DC Common Mode Characteristics						
Common Mode Output		VDC_{CM}	-	(VA-)+2.35	-	V
Common Mode Drift (Note 19)		VDC_{CMTC}	-	2	-	µV/°C
DC Common Mode Accuracy						
Common Mode Match (OUT±)		VDC_{CMM}	-	±10	-	mV
Common Mode Match (BUF±)		VDC_{CMM}	-	±25	-	mV
Noise						
Noise (OUT± Unloaded) (Note 25)	1/1	N_{OUT}	-	4.4	-	μV_{rms}
	1/2		-	5.6	-	μV_{rms}
	1/4		-	5.6	-	μV_{rms}
	1/8		-	5.6	-	μV_{rms}
	1/16		-	5.6	-	μV_{rms}
	1/32		-	9.9	-	μV_{rms}
	1/64		-	17.7	-	μV_{rms}
Noise (BUF± Unloaded) (Note 25, 26)	1/1	N_{BUF}	-	5.6	-	μV_{rms}
	1/2		-	8.9	-	μV_{rms}
	1/4		-	12.5	-	μV_{rms}
	1/8		-	28.0	-	μV_{rms}
	1/16		-	55.9	-	μV_{rms}
	1/32		-	99.4	-	μV_{rms}
	1/64		-	198.3	-	μV_{rms}
Noise (BUF± 1 kΩ load) (Note 25, 26)	1/1	N_{BUFL}	-	5.6	-	μV_{rms}

DAC DC DIFFERENTIAL MODE 5

Parameter		Symbol	Min	Typ	Max	Unit
DC Differential Mode Characteristics						
Full-scale Differential DC Output (Note 28)	1/1 1/2 1/4 1/8 1/16 1/32 1/64	VDC_{FS}	- - - - - - -	2.5 1.25 625 312.5 156.25 78.125 39.0625	- - - - - - -	V V mV mV mV mV mV
DC Differential Accuracy						
Full-scale Accuracy (OUT±)	(Note 3, 23)	VDC_{OUT}	-	VREF ±10	-	mV
Full-scale Accuracy (BUF±)	(Note 3, 23)	VDC_{BUF}	-	VREF ±25	-	mV
Relative Accuracy	(Note 24)	VDC_{REL}	-	±1	-	%FS
Full-scale Drift	(Note 19)	VDC_{TC}	-	8	-	µV/°C
DC Common Mode Characteristics						
Common Mode	(Note 15)	VDC_{CM}	-	(VA-)+2.35	-	V
Common Mode Drift	(Note 15, 19)	VDC_{CMTC}	-	2	-	µV/°C
Noise						
Noise (OUT± Unloaded) (Note 25, 28)	1/1 1/2 1/4 1/8 1/16 1/32 1/64	N_{OUT}	- - - - - - -	6.3 6.3 7.0 7.0 7.0 8.9 12.5	- - - - - - -	μV_{rms} μV_{rms} μV_{rms} μV_{rms} μV_{rms} μV_{rms} μV_{rms}
Noise (BUF± Unloaded) (Note 25, 26, 28)	1/1 1/2 1/4 1/8 1/16 1/32 1/64	N_{BUF}	- - - - - - -	9.9 11.2 15.8 28.0 55.9 99.4 198.3	- - - - - - -	μV_{rms} μV_{rms} μV_{rms} μV_{rms} μV_{rms} μV_{rms} μV_{rms}
Noise (BUF± 1 kΩ load) (Note 25, 26, 28)	1/1	N_{BUFL}	-	9.9	-	μV_{rms}

Notes: 28. DC differential output is chopper stabilized and includes low-level 32 kHz out-of-band noise which is rejected by the digital filter.

DAC AC COMMON MODE 6

Parameter		Symbol	Min	Typ	Max	Unit
AC Common Mode Characteristics						
Full-scale Common Mode AC Output (Note 29)	1/1 1/2 1/4 1/8 1/16 1/32	VCM_{FS}	- - - - - -	2.5 1.25 625 312.5 156.25 78.125	- - - - - -	V_{pp} V_{pp} mV_{pp} mV_{pp} mV_{pp} mV_{pp}
Full-scale Bandwidth	(Note 10)	VCM_{BW}	-	-	100	Hz
Impulse Amplitude	(Note 10, 22)	VCM_{IMP}	-	-	-20	dBfs
AC Common Mode Accuracy						
Common Mode Match (OUT± Unloaded) (Note 18, 27, 29)	1/1 - 1/32	VCM_{CMM}	-	-110	-	dB
Common Mode Match (BUF± Unloaded) (Note 18, 26, 27, 29)	1/1 - 1/32	VCM_{CMM}	-	-90	-	dB
Common Mode Match (BUF± 1 kΩ load) (Note 18, 26, 29)	1/1	VCM_{CMM}	-	-90	-	dB
Full-scale Accuracy	(Note 3, 23)	VCM_{ABS}	-	±1	-	%FS
Relative Accuracy	(Note 24)	VCM_{REL}	-	±1	-	%FS
Full-scale Drift	(Note 19)	VCM_{TC}	-	8	-	µV/°C
DC Common Mode Characteristics						
Common Mode Mean	(Note 30)	VCM_{CM}	-	(VA-)+2.35	-	V
Common Mode Mean Drift	(Note 19, 30)	VCM_{CMTC}	-	2	-	µV/°C

Notes: 29. No AC common mode signal is output at 1/64 attenuation due to the attenuator architecture.

30. Common mode mean is defined as the midpoint between AC common mode peaks.

DIGITAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Digital Inputs						
High-level Input Voltage	(Note 10, 31)	V_{IH}	0.6*VD	-	VD	V
Low-level Input Voltage	(Note 10, 31)	V_{IL}	0.0	-	0.8	V
Input Leakage Current		I_{IN}	-	±1	±10	µA
Digital Input Capacitance		C_{IN}	-	9	-	pF
Input Rise Times Except MCLK	(Note 10)	t_{RISE}	-	-	100	ns
Input Fall Times Except MCLK	(Note 10)	t_{FALL}	-	-	100	ns
Digital Outputs						
High-level Output Voltage, I_{out} = -40 µA	(Note 10)	V_{OH}	VD-0.3	-	-	V
Low-level Output Voltage, I_{out} = 40 µA	(Note 10)	V_{OL}	-	-	0.3	V
High-Z Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Capacitance		C_{OUT}	-	9	-	pF
Output Rise Times	(Note 10)	t_{RISE}	-	-	100	ns
Output Fall Times	(Note 10)	t_{FALL}	-	-	100	ns

Notes: 31. Device is intended to be driven with CMOS logic levels.

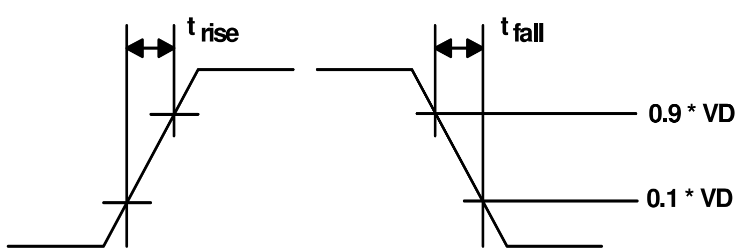

Figure 3. Digital Input Rise and Fall Times

DIGITAL CHARACTERISTICS (CONT.)

Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Input						
MCLK Frequency	(Note 32)	f_{CLK}	-	2.048	-	MHz
MCLK Period	(Note 32)	t_{mclk}	-	488	-	ns
MCLK Duty Cycle	(Note 10)	$MCLK_{DC}$	40	-	60	%
MCLK Rise Time	(Note 10)	t_{RISE}	-	-	50	ns
MCLK Fall Time	(Note 10)	t_{FALL}	-	-	50	ns
MCLK Jitter (In-band or aliased in-band)	(Note 10)	$MCLK_{IBJ}$	-	-	300	ps
MCLK Jitter (Out-of-band)	(Note 10)	$MCLK_{OBJ}$	-	-	1	ns
Master Sync Input						
MSYNC Setup Time to MCLK Rising	(Note 10, 33)	t_{mss}	20	122	-	ns
MSYNC Period	(Note 10, 33)	t_{msync}	40	976	-	ns
MSYNC Hold Time after MCLK Falling	(Note 10, 33)	t_{msh}	20	122	-	ns
MSYNC Instant to TDATA Start	(Note 34)	t_{tdata}	-	1220	-	ns
MDATA Output						
MDATA Output Bit Rate		f_{mdata}	-	512	-	kbits/s
MDATA Output One's Density Range	(Note 10)	$MDAT_{OD}$	14	-	86	%
Full-scale Output Code	(Note 35)	$MDAT_{FS}$	0xA2EAAE	-	0x5D1C41	
TDATA Input						
TDATA Input Bit Rate	(Note 36)	f_{tdata}	-	256	-	kbits/s
TDATA Input One's Density Range	(Note 10)	TBS_{OD}	25	-	75	%
TBSGAIN Full-scale Code	(Note 37)	TBS_{FS}	-	0x04B8F2	-	
TBSGAIN -20 dB Code	(Note 37)	TBS_{-20dB}	-	0x0078E5	-	

Notes: 32. MCLK is generated by the CS5378 digital filter. If MCLK is disabled, the device automatically enters a power-down state.

33. MSYNC is generated by the CS5378 digital filter and is latched on MCLK rising edge, synchronization instant (**t_0**) on next MCLK rising edge.

34. TDATA can be delayed from 0 to 63 full bit periods by the test bit stream generator in the CS5378 digital filter. The timing diagrams show no TBSDATA delay.

35. Decimated, filtered, and offset corrected 24-bit output word from the CS5378 digital filter.

36. TDATA is generated by the test bit stream generator in the CS5378 digital filter.

37. TBSGAIN register value in the CS5378 digital filter.

DIGITAL CHARACTERISTICS (CONT.)

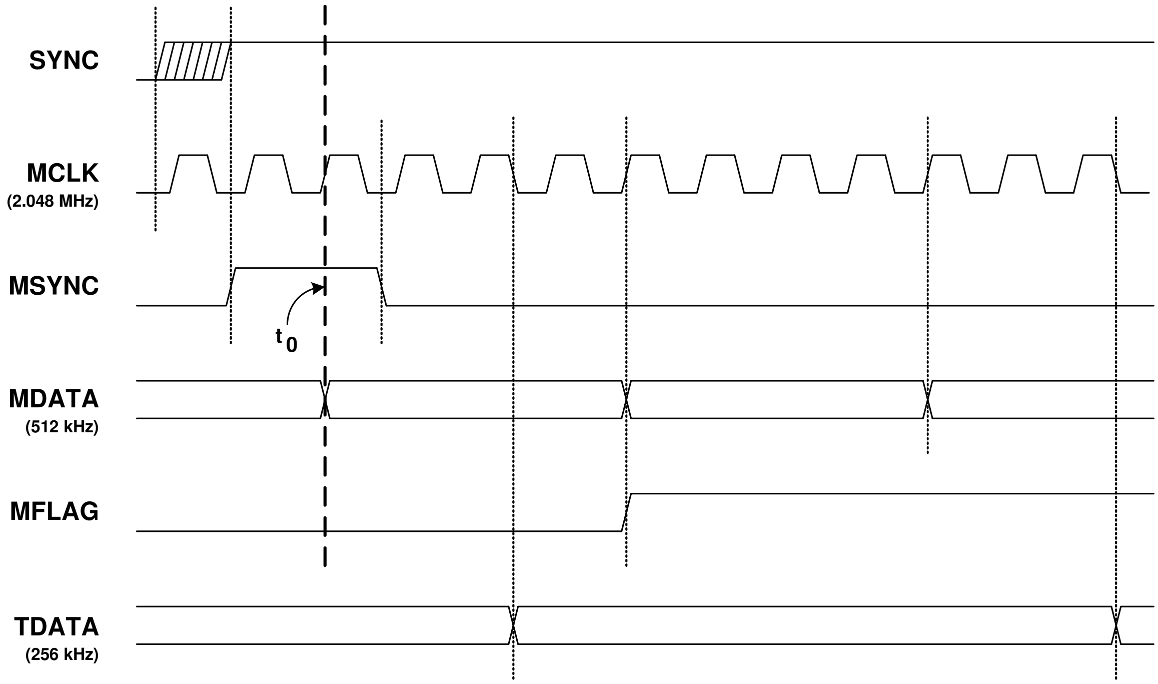

Figure 4. System Timing Diagram

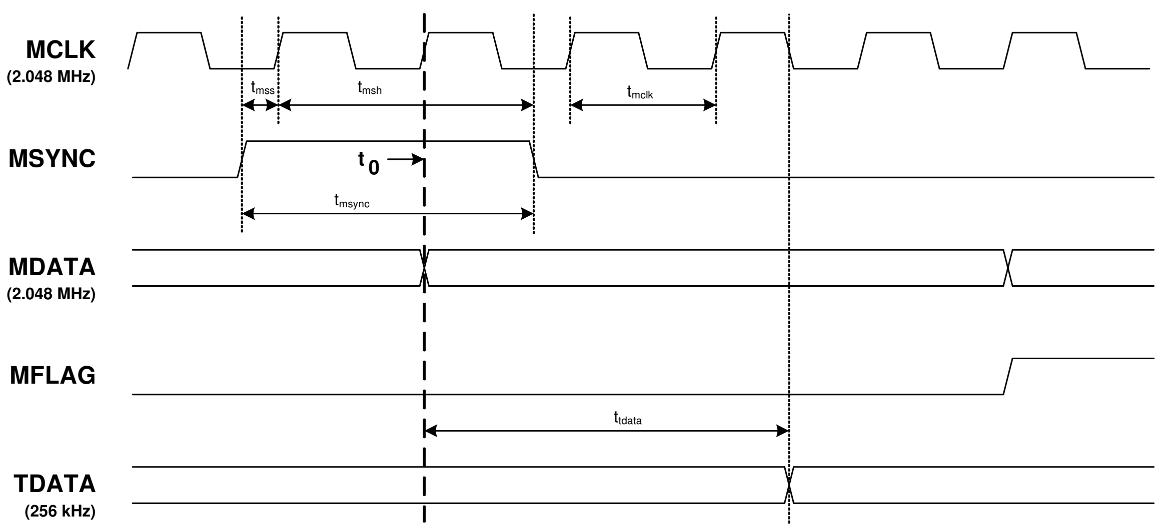

Figure 5. MCLK / MSYNC Timing Detail

POWER SUPPLY CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Modulator Power Supply Current						
Analog Power Supply Current	(Note 38)	I_A	-	5	7	mA
Digital Power Supply Current	(Note 38)	I_D	-	200	300	µA
DAC AC Mode Supply Current						
Analog Power Supply Current	(Note 38)	I_A	-	7.8	10	mA
Digital Power Supply Current	(Note 38)	I_D	-	200	-	µA
DAC DC Mode Supply Current						
Analog Power Supply Current	(Note 38)	I_A	-	4.8	-	mA
Digital Power Supply Current	(Note 38)	I_D	-	200	-	µA
Modulator Sleep Current						
Analog Power Supply Current	(Note 38)	I_A	-	200	-	µA
Digital Power Supply Current	(Note 38)	I_D	-	20	-	µA
DAC Sleep Current						
Analog Power Supply Current	(Note 38)	I_A	-	400	-	µA
Digital Power Supply Current	(Note 38)	I_D	-	100	-	µA
Power Down Current (MCLK = 0)						
Analog Power Supply Current	(Note 38)	I_A	-	100	-	µA
Digital Power Supply Current	(Note 38)	I_D	-	20	-	µA
Time to Enter Power Down (MCLK disabled)	(Note 10)	PD_{TC}	-	40	-	µS
Power Supply Rejection						
Power Supply Rejection Ratio	(Note 39)	PSRR	-	90	-	dB

Notes: 38. All outputs unloaded. Digital inputs forced to VD or GND respectively.

39. Power supply rejection is characterized by applying a 100 mVp-p 50-Hz sine wave to each supply.

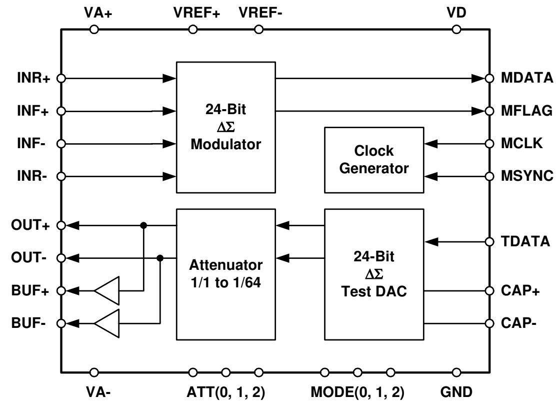

Figure 6. CS5373A Block Diagram

2. GENERAL DESCRIPTION

The CS5373A is a high-performance, fourth-order ΔΣ modulator integrated with a digital-to-analog converter (DAC). When combined with a CS3301A/02A differential amplifier and the CS5378 digital filter, a small low-power self-testing high-accuracy single-channel measurement system results.

2.1 Delta-Sigma Modulator

The CS5373A modulator has high dynamic range and low total harmonic distortion with very low power consumption, and is optimized for extremely high-resolution measurement of 5 V_{pp} or smaller differential signals. It converts analog input signals between DC and 1720 Hz to an oversampled serial bit stream at 512 kbits per second.

The CS5378 digital filter generates the clock and synchronization inputs for the modulator while receiving the modulator one-bit data and over-range flag outputs. The digital filter then decimates the modulator's oversampled output bit stream to a 24-bit output at the selected output word rate.

2.2 Digital-to-Analog Converter

The CS5373A test DAC is driven by a digital ΔΣ bit stream from the CS5378 digital filter's test bit stream (TBS) generator and operates in either AC or DC test modes. AC test modes (MODE 1, 2, 3, 6) are used to measure system THD and CMRR performance. DC test modes (MODE 4, 5) are for gain calibration and pulse tests. The digital filter also provides clock and syncronization signals as well as GPIO control signals to set the operational mode and analog output attenuation.

Two sets of differential analog outputs, *OUT* and *BUF*, simplify system design as dedicated outputs for testing the electronics channel and for in-circuit sensor tests. Output attenuator settings are binary weighted (1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64) and match the CS3301A/02A amplifier input levels for full-scale testing at all gain ranges.

For maximum performance, the precision outputs (OUT±) must drive only high-impedance loads such as the CS3301A/02A amplifier inputs. The buffered outputs (BUF±) can drive lower-impedance loads, down to 1 kΩ, but with reduced performance compared to the precision outputs.

The test DAC is optimized for low-power operation and has a restricted operational bandwidth in the AC modes. For stable operation, full-scale AC test signals must not contain frequencies above 100 Hz. AC test signals above 100 Hz (TBS impulse mode, for example) must have a -20 dB reduced amplitude to ensure stability of the low-power ΔΣ architecture.

3. SYSTEM DIAGRAM

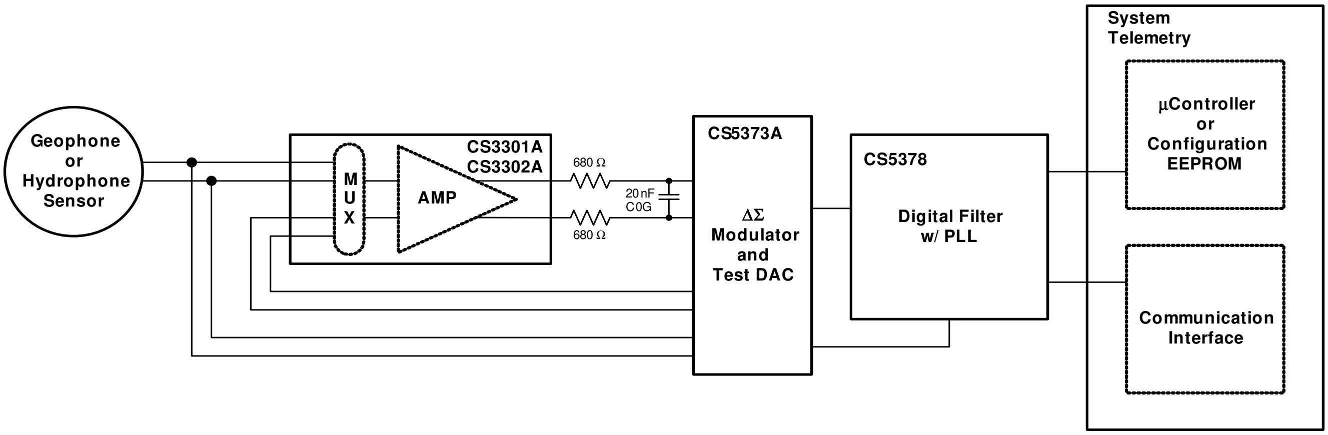

Figure 7. System Diagram

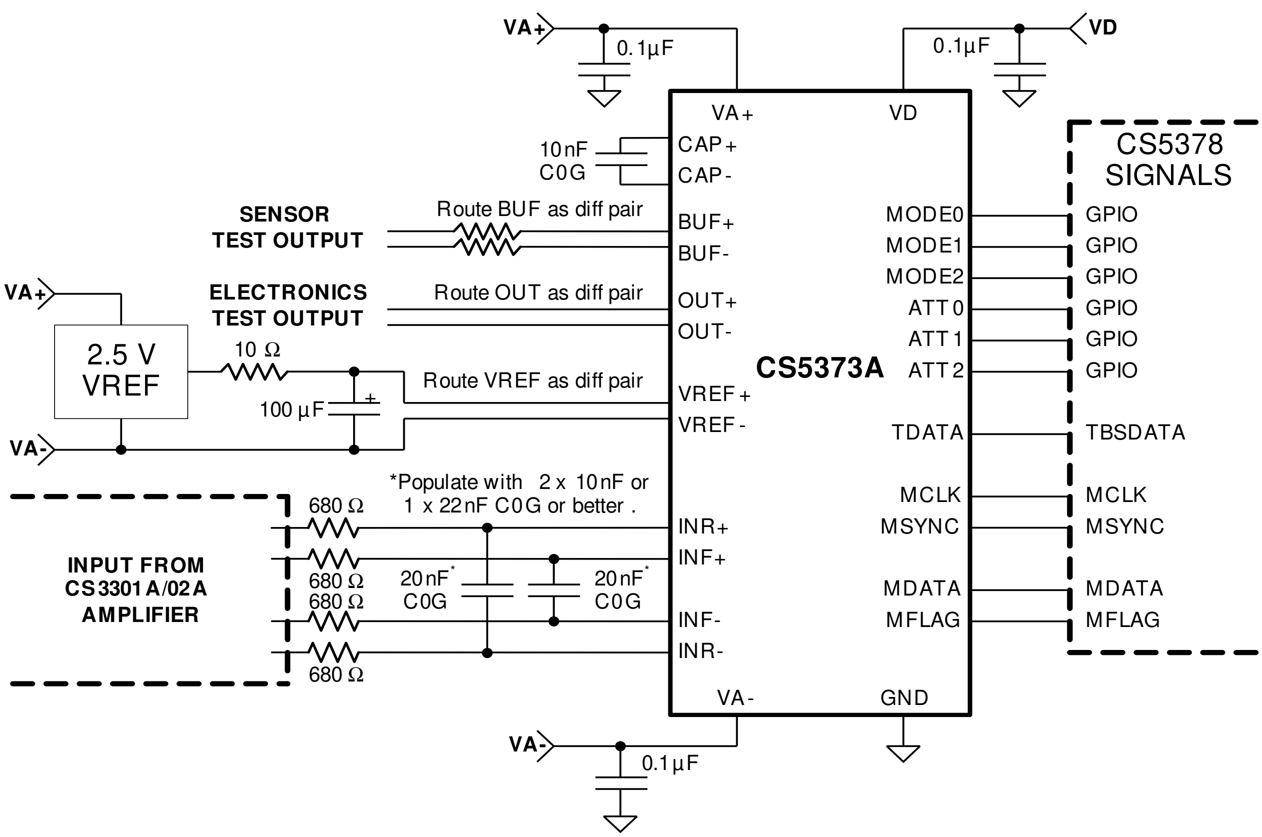

Figure 8. Connection Diagram

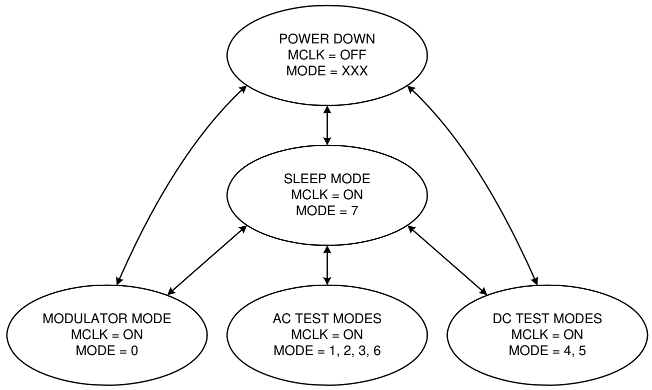

Figure 9. Power Mode Diagram

4. POWER MODES

The CS5373A has five power modes. Modulator mode, AC test modes, and DC test modes are operational modes, while power down and sleep mode are non-operational standby modes.

4.1 Power Down

If MCLK is stopped, an internal loss-of-clock detection circuit automatically places the CS5373A into power down. Power down is independent of the MODE and ATT pin settings, and is automatically invoked after approximately 40 µs without an incoming MCLK edge.

In power down the modulator, AC test circuitry and DC test circuitry are inactive and all outputs are high impedance. When used with the CS5378 digital filter, the CS5373A is in power down immediately after reset since MCLK is disabled by default.

4.2 Sleep Mode

With MCLK active, selecting sleep mode (MODE 7) places the CS5373A into a micro-power sleep state. In sleep mode the modulator, AC test circuitry and DC test circuitry are inactive and all outputs are high impedance.

4.3 Modulator Mode

With MCLK active, selecting modulator mode (MODE 0) enables the CS5373A modulator and places the AC and DC test circuitry into a micro-power sleep state with the analog test outputs high impedance. Following completion of AC and DC system self-tests, the CS5373A is typically set into modulator mode for normal data acquisition.

4.4 AC Test Modes

With MCLK and TDATA active, selecting an AC test mode (MODE 1, 2, 3, 6) enables the modulator and causes the DAC to output AC waveforms on the analog test outputs. AC test modes use the low-power ΔΣ DAC circuitry in the CS5373A to create precision differential or common mode analog AC output signals from the encoded digital test bit stream (TBS) input.

4.5 DC Test Modes

With MCLK active, selecting a DC test mode (MODE 4, 5) enables the modulator and causes the DAC to generate precision DC voltages on the analog test outputs. DC test modes use switch-capacitor level-shifting buffer circuitry in the CS5373A to create differential or common mode DC analog output voltages from the voltage reference input.

5. OPERATIONAL MODES

The CS5373A has seven operational modes and one sleep mode selected by the MODE2, MODE1, and MODE0 pins.

Modes of Operation		
Selection	**MODE [2:0]**	**Mode Description**
0	0 0 0	***Modulator:*** enabled. ***DAC:*** sleep.
1	0 0 1	***Modulator:*** enabled. ***DAC:*** AC OUT and BUF outputs.
2	0 1 0	***Modulator:*** enabled. ***DAC:*** AC OUT only, BUF high-z.
3	0 1 1	***Modulator:*** enabled. ***DAC:*** AC BUF only, OUT high-z.
4	1 0 0	***Modulator:*** enabled. ***DAC:*** DC common mode output.
5	1 0 1	***Modulator:*** enabled. ***DAC:*** DC differential output.
6	1 1 0	***Modulator:*** enabled. ***DAC:*** AC common mode output.
7	1 1 1	***Modulator:*** sleep. ***DAC:*** sleep.

Table 2. Operational Modes

5.1 Modulator Mode

Modulator mode (MODE 0) enables the ΔΣ modulator and disables the DAC AC and DC test circuitry to save power. This mode is used for normal sensor measurements after self-tests are completed.

5.1.1 Modulator One's Density

In modulator mode (and whenever the modulator is enabled) the differential analog input signal is converted to an oversampled ΔΣ serial bit stream on the MDATA output, with a one's density proportional to the differential amplitude of the analog input signal.

One's density of the MDATA output is defined as the ratio of '1' bits to total bits in the serial bit stream output, i.e. an 86% one's density has, on average, a '1' value in 86 of every 100 output data bits. The MDATA output has a nominal 50% one's density for a mid-scale differential input, approximately 86% one's density for a positive full-scale input, and approximately 14% one's density for a negative full-scale input.

5.1.2 Modulator Decimated Output

When the CS5373A modulator operates with the CS5378 digital filter, the final decimated, 24-bit, full-scale output code range depends if digital offset correction is enabled. With digital offset correction enabled, amplifier offset and the modulator internal offset are removed from the final conversion result.

Modulator Differential Analog Input Signal	CS5378 Digital Filter Output Code	
	Offset Corrected	**+100 mV Offset**
> + (VREF + 5%)	Error Flag Possible	
+ VREF	5D1C41	60D5B4
0 V	000000	03B973
- VREF	A2EAAE	A6A421
> - (VREF + 5%)	Error Flag Possible	

Table 3. Output Coding for the CS5373A Modulator and CS5378 Digital Filter Combination

5.1.3 Modulator Synchronization

The modulator is designed to operate synchronously with other modulators in a measurement network, so a rising edge on the MSYNC input resets the internal conversion state machine to synchronize analog sample timing. MSYNC is automatically generated by the CS5378 digital filter after receiving a synchronization signal from the external system, and is chip-to-chip accurate within ± 1 MCLK period.

5.1.4 Modulator Idle Tones

The CS5373A modulator is ΔΣ type and so can produce ‘idle tones’ in the measurement bandwidth when the differential input signal is a steady-state DC signal within ± 50 mV of mid-scale. Idle tones result from low-frequency patterns in the output bit stream and appear in the measurement spectrum as small tones about -135 dB down from full scale.

Idle tones are eliminated within the CS5373A modulator by automatically adding +100 mV of internal differential offset during conversion to push idle tones out of the measurement bandwidth. Care should be taken to ensure external offset voltages do not negate the internally added differential offset.

5.1.5 Modulator Stability

The CS5373A’s ΔΣ modulator has a 4^{th} order architecture which is conditionally stable and may go into an oscillatory condition if the analog inputs are over-ranged more than 5% past either positive or negative full scale.

If an unstable condition is detected, the modulator collapses to a 1^{st} order system and transitions the MFLAG output low-to-high to signal an error condition to the CS5378 digital filter. The analog input signal must be reduced to within the full-scale range for at least 32 MCLK cycles for the modulator to recover from an oscillatory condition. If the analog input remains over-ranged for an extended period, the modulator will cycle between 4^{th} order and 1^{st} order operation and the MFLAG output will be seen to pulse.

5.2 AC Test Modes

AC test modes (MODE 1, 2, 3, 6) enable the modulator and use the digital test bit stream (TBS) input from the CS5378 digital filter to construct analog AC waveforms. The digital bit stream input to the TDATA pin encodes the analog waveform as over-sampled one-bit ΔΣ data, which is then converted into precision differential or common mode analog AC signals by the CS5373A’s test DAC.

5.2.1 AC Differential

The first three AC test modes (MODE 1, 2, 3) enable the modulator and AC test circuitry to create precision differential analog signals for THD and impulse testing of the measurement channel. In mode 1, both sets of differential analog outputs (*OUT* and *BUF*) are enabled. In mode 2 only the *OUT* analog output is enabled, and the *BUF* output is high impedance. In mode 3 only the *BUF* analog output is enabled, and the *OUT* output is high impedance.

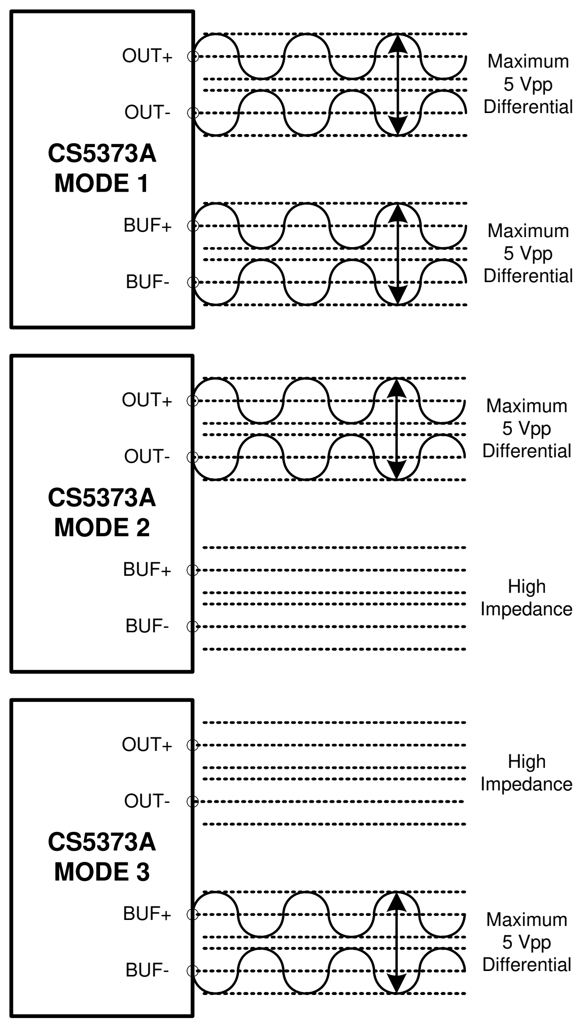

Figure 10. AC Differential Modes

Differential AC test signals out of the CS5373A consist of two halves with equal but opposite magnitude, varying about a common mode voltage. A full-scale 5 V_{PP} differential AC signal centered on a -0.15 V common mode voltage will have:

SIG+ = -0.15 V + 1.25 V = +1.1 V

SIG- = -0.15 V - 1.25 V = -1.4 V

SIG+ is +2.5 V relative to SIG-

For the opposite case:

SIG+ = -0.15 V - 1.25 V = -1.4 V

SIG- = -0.15 V + 1.25 V = +1.1 V

SIG+ is -2.5 V relative to SIG-

So the total swing for SIG+ relative to SIG- is (+2.5 V) - (-2.5 V) = 5 V_{pp} differential. A similar calculation can be done for SIG- relative to SIG+. It's important to note that a 5 V_{pp} differential signal centered on a -0.15 V common mode voltage never exceeds +1.1 V with respect to ground and never drops below -1.4 V with respect to ground on either half. By definition, differential voltages are measured with respect to the opposite half, not relative to ground. A voltmeter differentially measuring between SIG+ and SIG- in the above example would correctly read 1.767 V_{rms}, or 5 V_{pp}.

5.2.2 AC Common Mode

The final AC test mode (MODE 6) enables the modulator and AC test circuitry to create a matched AC common mode analog signal for CMRR testing of the measurement channel. In mode 6, both sets of analog outputs (*OUT* and *BUF*) are enabled. There is no AC common mode output for an attenuator setting of 1/64. Gross leakage in the sensor channel can be detected by applying a full-scale AC common mode signal. If there is a significant differential mismatch in the channel due to sensor leakage, the AC common mode signal will be converted to a measurable differential signal at the fundamental frequency.

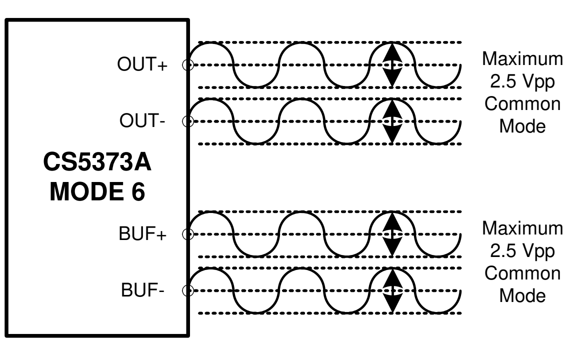

Figure 11. AC Common Mode

5.2.3 DAC Stability

For the CS5373A's low-power ΔΣ DAC architecture to remain stable, the TDATA input bit stream should only encode 100 Hz or lower bandwidth analog signals. For TDATA bit stream frequencies above 100 Hz (for example, TBS impulse mode), the encoded amplitude must be reduced -20 dB below full scale to guarantee stability.

If the CS5373A's low-power ΔΣ DAC architecture becomes unstable, persistent elevated noise will be present on the analog outputs and AC linearity will be poor. To recover stability, place the CS5373A into power down or sleep mode and restart the CS5378 test bit stream generator before placing the CS5373A back into an AC test mode.

5.3 DC Test Modes

DC test modes enable the modulator and DC test circuitry to create precision level-shifted and buffered versions of the voltage reference input as precision DC common mode and DC differential analog outputs. The absolute accuracy of the DC test modes is highly dependent on the absolute accuracy of the voltage reference input voltage.

5.3.1 DC Common Mode

The first DC test mode (MODE 4) enables the modulator and DC test circuitry to create a matched DC common mode analog output voltage as a baseline measurement for gain calibration and differential pulse tests. In mode 4, both sets of analog outputs (*OUT* and *BUF*) are enabled.

5.3.2 DC Differential

The second DC test mode (MODE 5) enables the modulator and DC test circuitry to create a precision differential DC analog output voltage as the final measurement for gain calibration and as the step/pulse output for differential pulse tests. In mode 5, both sets of analog outputs (*OUT* and *BUF*) are enabled.

In DC differential mode (MODE 5) the level-shifting buffer circuitry adds low-level 32 kHz switched-capacitor noise to the DC output. This noise is out of the measurement bandwidth for systems designed with a CS3301A/02A amplifier and CS5373A modulator and is rejected by the CS5378 digital filter. This 32 kHz switched-capacitor noise does not affect DC system tests, though it may be visible on an oscilloscope at high gain levels.

By measuring both DC test modes

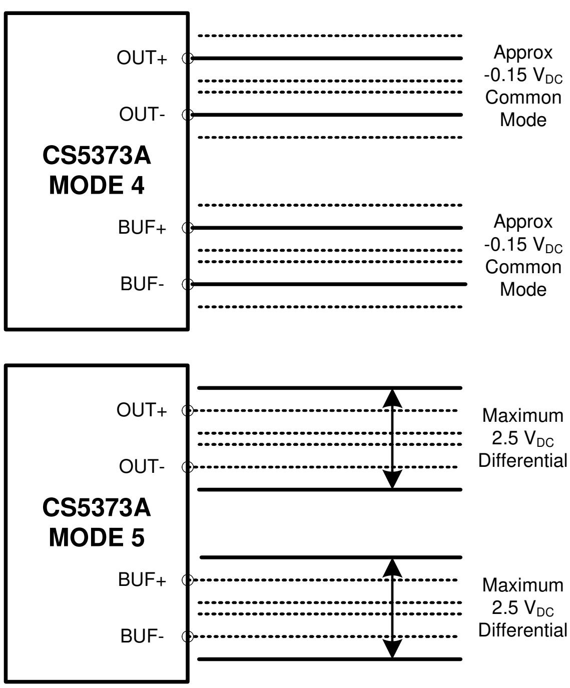

Figure 12. DC Test Modes

(MODE 4, 5), precision gain-calibration coefficients can be calculated for the measurement channel. By first measuring the differential offset of the DC common mode output (MODE 4) and then measuring the DC differential mode amplitude (MODE 5), a precise offset-corrected, volts-to-codes conversion ratio can be calculated. This known ratio is then used along with the CS5378 digital filter GAIN register to normalize the full-scale amplitude to match other channels in the measurement network.

By switching between DC common mode (MODE 4) and DC differential mode (MODE 5), pulse waveforms can be created to characterize the step response of the measurement channel. If a pulse test requires precise timing control, an external controller should directly toggle the MODE pins of the CS5373A to avoid delays associated with writing to the CS5378 digital filter GPIO register.

Sensor impedance can be measured using DC differential mode (MODE 5), provided matched series resistors are installed between the BUF analog outputs and the sensor. Applying the known DC differential voltage to the resistor-sensor-resistor string permits a ratiometric sensor impedance calculation from the measured voltage drop across the sensor.

Switching between DC differential mode (MODE 5) and modulator mode (MODE 0) can, in the case of a moving-coil geophone, test basic parameters of the electro-mechanical transfer function. The voltage relaxation characteristic of the sensor when switching the analog outputs from a differential DC voltage to high impedance depends primarily on the geophone resonant frequency and damping factor.

5.4 Sleep Mode

Sleep mode (MODE 7) saves system power when measurements are not required by turning off the modulator, AC test circuitry, and DC test circuitry. In sleep mode the modulator digital outputs and the *BUF* and *OUT* analog outputs are high impedance.