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CS5376A

Low-power, Multi-channel Decimation Filter

Features

- 1- to 4-channel Digital Decimation Filter
  - Multiple On-chip FIR and IIR Coefficient Sets
  - Programmable Coefficients for Custom Filters
  - Synchronous Operation
- Selectable Output Word Rate
  - 4000, 2000, 1000, 500, 333, 250 SPS
  - 200, 125, 100, 50, 40, 25, 20, 10, 5, 1 SPS
- Digital Gain and Offset Corrections
- Test DAC Bit-stream Generator
  - Digital Sine Wave Output
- Time Break Controller, General Purpose I/O
- Secondary SPI™ Port, Boundary Scan JTAG
- Microcontroller or EEPROM Configuration
- Small-footprint, 64-pin TQFP Package
- Low Power Consumption
  - 9 mW per Channel at 500 SPS
- Flexible Power Supplies
  - I/O Interface: 3.3 V or 5.0 V
  - Digital Logic Core: 3.0 V, 3.3 V or 5.0 V

Description

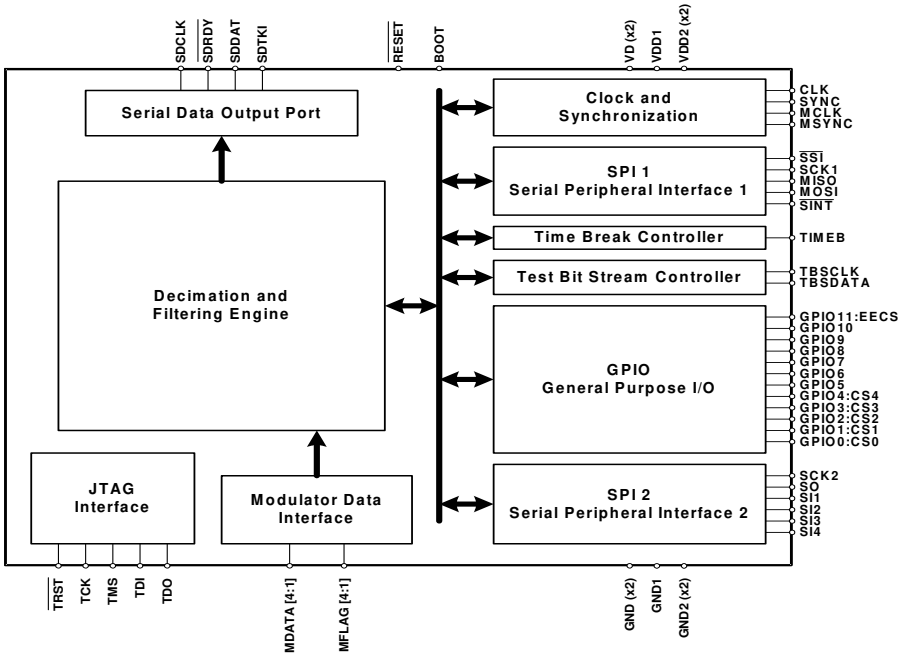
The CS5376A is a multi-function digital filter utilizing a low-power signal processing architecture to achieve efficient filtering for up to four ΔΣ modulators. By combining the CS5376A with CS3301A/02A differential amplifiers, CS5371A/72A ΔΣ modulators, and the CS4373A ΔΣ test DAC a synchronous, high-resolution, self-testing, multi-channel measurement system can be designed quickly and easily.

Digital filter coefficients for the CS5376A FIR and IIR filters are included on-chip for a simple setup, or they can be programmed for custom applications. Selectable digital filter decimation ratios produce output word rates from 4000 SPS to 1 SPS, resulting in measurement bandwidths ranging from 1600 Hz down to 400 mHz when using the on-chip coefficient sets.

The CS5376A includes integrated peripherals to simplify system design: offset and gain corrections, a test DAC bit stream generator, a time-break controller, 12 general-purpose I/O pins, a secondary SPI port, and a boundary scan JTAG port.

ORDERING INFORMATION

See page 106.



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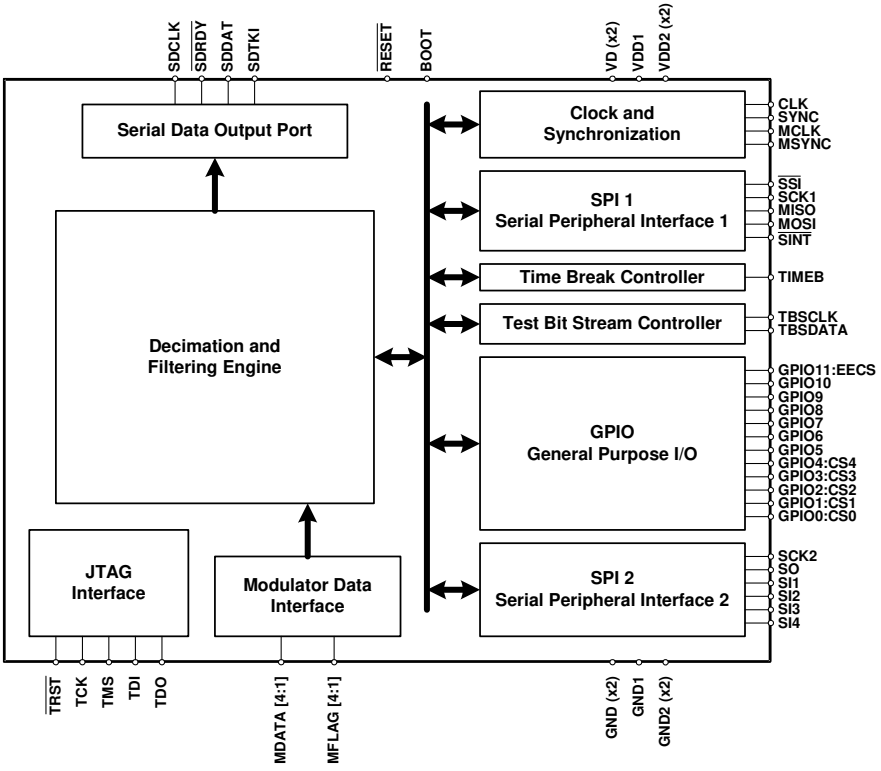


Figure 1. CS5376A Block Diagram

1. GENERAL DESCRIPTION

The CS5376A is a multi-channel digital filter with integrated system peripherals. Figure 1 illustrates a simplified block diagram of the CS5376A.

1.1 Digital Filter Features

- Multi-channel decimation filter for CS5371A/72A ΔΣ modulators.
  - 1, 2, 3, or 4 channel concurrent operation.
- Synchronous operation for simultaneous sampling in multi-sensor systems.
  - Internal synchronization of digital filter phase to an external SYNC signal.
- Multiple output word rates, including low bandwidth rates.
  - Standard output rates: 4000, 2000, 1000, 500, 333, 250 SPS.
  - Low bandwidth rates: 200, 125, 100, 50, 40, 25, 20, 10, 5, 1 SPS.
- Flexible digital filter configuration. (See Figure 2)
  - Cascaded SINC, FIR, and IIR filters with selectable output stage.
  - Linear and minimum phase FIR low-pass filter coefficients included.
  - 3 Hz Butterworth IIR high-pass filter coefficients included.
  - FIR and IIR coefficients are programmable to create a custom filter response.
- Digital gain correction.
  - Individual channel gain correction to normalize signal amplitudes.

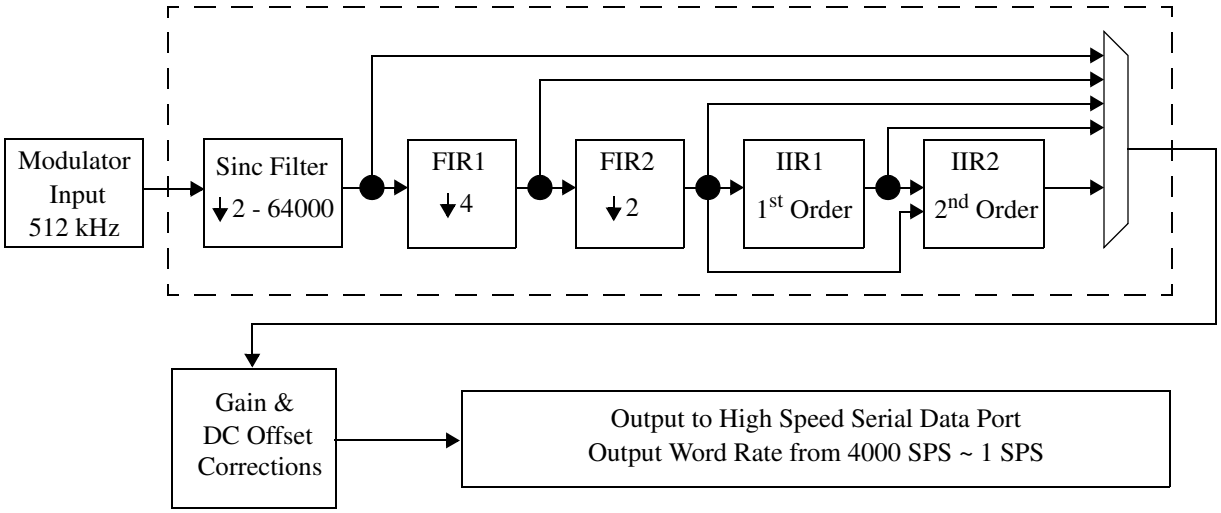


Figure 2. Digital Filtering Stages

- Digital offset correction and calibration.
  - Individual channel offset correction to remove measurement offsets.
  - Calibration engine for automatic calculation of offset correction factors.

1.2 Integrated Peripheral Features

- Synchronous operation for simultaneous sampling in multi-sensor systems.
  - MCLK / MSYNC output signals to synchronize external components.
- High speed serial data output port (SD port).
  - Asynchronous operation to 4 MHz for direct connection to system telemetry.
  - Internal 8-deep data FIFO for flexible output timing.
- Digital test bit stream signal generator suitable for CS4373A ΔΣ test DAC.
  - Sine wave output mode for testing total harmonic distortion.
  - Programmable waveform data for custom test signal generation.
- Time break controller to record system timing information.
  - Dedicated TB status bit in the output data stream.
  - Programmable output delay to match system group delay.
- Additional hardware peripherals simplify system design.
  - 12 General Purpose I/O (GPIO) pins for local hardware control.
  - Secondary SPI 2 serial port to control local serial peripherals.
  - JTAG port for boundary scan (IEEE 1149.1 compliant).

1.3 System Level Features

- Flexible configuration options.
  - Configuration 'on-the-fly' via microcontroller or system telemetry.
  - Fixed configuration via stand-alone boot EEPROM.
- Low power consumption.

  - 37 mW for 4-channel operation at 500 SPS (9.25 mW/channel).
  - 40 µW standby mode.
- Flexible power supply configurations.
  - Separate digital logic core, telemetry I/O, and modulator I/O power supplies.
  - Telemetry I/O and modulator I/O interfaces operate from 3.3 V or 5 V.
  - Digital logic core operates from 3.0 V, 3.3 V or 5 V.
- Small 64-pin TQFP package.
  - Total footprint 12 mm x 12 mm plus five bypass capacitors.

1.4 Configuration Interface

- Configuration from microcontroller or stand-alone boot EEPROM.
  - Microcontroller boot permits reconfiguration during operation.
  - EEPROM boot sets a fixed operational configuration.
- Configuration commands written through Serial Peripheral Interface 1. (See Table 1)
  - Standardized microcontroller interface using SPI 1 registers. (See Table 3)
  - Commands write digital filter registers, filter coefficients, and test bit stream data.
  - Digital filter registers set hardware configuration options.

Microcontroller Boot Configuration Commands

Name	CMD 24-bit	DAT1 24-bit	DAT2 24-bit	Description
NOP	000000	-	-	No Operation
WRITE DF REGISTER	000001	REG	DATA	Write Digital Filter Register
READ DF REGISTER	000002	REG [DATA]	- -	Read Digital Filter Register
WRITE FIR COEFFICIENTS	000003	NUM FIR1 (FIR COEF)	NUM FIR2 (FIR COEF)	Write Custom FIR Coefficients
WRITE IIR COEFFICIENTS	000004	a11 b11 a22 b21	b10 a21 b20 b22	Write Custom IIR Coefficients
WRITE ROM COEFFICIENTS	000005	COEF SEL	-	Use On-Chip Coefficients
WRITE TBS DATA	000006	NUM TBS (TBS DATA)	- (TBS DATA)	Write Custom Test Bit Stream Data
WRITE ROM TBS	000007	-	-	Use On-Chip TBS Data
FILTER START	000008	-	-	Start Digital Filter Operation
FILTER STOP	000009	-	-	Stop Digital Filter Operation

EEPROM Boot Configuration Commands

Name	CMD 8-bit	DATA 24-bit	Description
NOP	00	-	No Operation
WRITE DF REGISTER	01	REG DATA	Write Digital Filter Register
WRITE FIR COEFFICIENTS	02	NUM FIR1 NUM FIR2 (FIR COEF)	Write Custom FIR Coefficients
WRITE IIR COEFFICIENTS	03	a11 b10 b11 a21 a22 b20 b21 b22	Write Custom IIR Coefficients
WRITE ROM COEFFICIENTS	04	COEF SEL	Use On-Chip Coefficients
WRITE TBS DATA	05	NUM TBS (TBS DATA)	Write Custom Test Bit Stream Data
WRITE ROM TBS	06	-	Use On-Chip TBS Data
FILTER START	07	-	Start Digital Filter Operation

[DATA] indicates data word returned from digital filter.

(DATA) indicates multiple words of this type are to be written.

Table 1. Microcontroller and EEPROM Configuration Commands

Bits	23:20	19:16	15:12	11:8	7:4	3:0
Selection	0000	0000	IIR2	IIR1	FIR2	FIR1

Bits 15:12	IIR2 Coefficients
0000	3 Hz @ 2000 SPS
0001	3 Hz @ 1000 SPS
0010	3 Hz @ 500 SPS
0011	3 Hz @ 333 SPS
0100	3 Hz @ 250 SPS

Bits 11:8	IIR1 Coefficients
0000	3 Hz @ 2000 SPS
0001	3 Hz @ 1000 SPS
0010	3 Hz @ 500 SPS
0011	3 Hz @ 333 SPS
0100	3 Hz @ 250 SPS

Bits 3:0	FIR1 Coefficients
0000	Linear Phase
0001	Minimum Phase

Bits 7:4	FIR2 Coefficients
0000	Linear Phase
0001	Minimum Phase

Figure 3. FIR and IIR Coefficient Set Selection Word

Test Bit Stream Characteristic Equation:

*(Signal Freq) * (# TBS Data) * (Interpolation + 1) = Output Rate*

Example: *(31.25 Hz) * (1024) * (0x07 + 1) = 256 kHz*

Signal Frequency (TBSDATA)	Output Rate (TBSCLK)	Output Rate Selection (RATE)	Interpolation Selection (INTP)
10.00 Hz	256 kHz	0x4	0x18
10.00 Hz	512 kHz	0x5	0x31
25.00 Hz	256 kHz	0x4	0x09
25.00 Hz	512 kHz	0x5	0x13
31.25 Hz	256 kHz	0x4	0x07
31.25 Hz	512 kHz	0x5	0x0F
50.00 Hz	256 kHz	0x4	0x04
50.00 Hz	512 kHz	0x5	0x09
125.00 Hz	256 kHz	0x4	0x01
125.00 Hz	512 kHz	0x5	0x03

Table 2. TBS Configurations Using On-Chip Data

SPI 1 Registers

Name	Addr.	Type	# Bits	Description
SPI1CTRL	00 - 02	R/W	8, 8, 8	SPI 1 Control
SPI1CMD	03 - 05	R/W	8, 8, 8	SPI 1 Command
SPI1DAT1	06 - 08	R/W	8, 8, 8	SPI 1 Data 1
SPI1DAT2	09 - 0B	R/W	8, 8, 8	SPI 1 Data 2

Digital Filter Registers

Name	Addr.	Type	# Bits	Description
CONFIG	00	R/W	24	Hardware Configuration
RESERVED	01-0D	R/W	24	Reserved
GPCFG0	0E	R/W	24	GPIO[7:0] Direction, Pull-up Enable, and Data
GPCFG1	0F	R/W	24	GPIO[11:8] Direction, Pull-up Enable, and Data
SPI2CTRL	10	R/W	24	SPI 2 Control
SPI2CMD	11	R/W	16	SPI 2 Command
SPI2DAT	12	R/W	24	SPI 2 Data
RESERVED	13-1F	R/W	24	Reserved
FILTCFG	20	R/W	24	Digital Filter Configuration
GAIN1	21	R/W	24	Gain Correction Channel 1
GAIN2	22	R/W	24	Gain Correction Channel 2
GAIN3	23	R/W	24	Gain Correction Channel 3
GAIN4	24	R/W	24	Gain Correction Channel 4
OFFSET1	25	R/W	24	Offset Correction Channel 1
OFFSET2	26	R/W	24	Offset Correction Channel 2
OFFSET3	27	R/W	24	Offset Correction Channel 3
OFFSET4	28	R/W	24	Offset Correction Channel 4
TIMEBRK	29	R/W	24	Time Break Delay
TBSCFG	2A	R/W	24	Test Bit Stream Configuration
TBSGAIN	2B	R/W	24	Test Bit Stream Gain
SYSTEM1	2C	R/W	24	User Defined System Register 1
SYSTEM2	2D	R/W	24	User Defined System Register 2
VERSION	2E	R/W	24	Hardware Version ID
SELFTEST	2F	R/W	24	Self-Test Result Code

Table 3. SPI 1 and Digital Filter Registers

2. CHARACTERISTICS AND SPECIFICATIONS

- Min / Max characteristics and specifications are guaranteed over the Specified Operating Conditions.
- Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25°C.
- GND, GND1, GND2 = 0 V, all voltages with respect to 0 V.

SPECIFIED OPERATING CONDITIONS

Parameter		Symbol	Min	Nom	Max	Unit
Logic Core Power Supply		VD	2.85	3.0	5.25	V
Microcontroller Interface Power Supply		VDD1	3.135	3.3	5.25	V
Modulator Interface Power Supply		VDD2	3.135	3.3	5.25	V
Ambient Operating Temperature	Industrial (-IQ)	T_A	-40	-	85	°C

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Power Supplies	Logic Core	VD	-0.3	6.0	V
	Microcontroller Interface	VDD1	-0.3	6.0	V
	Modulator Interface	VDD2	-0.3	6.0	V
Input Current, Any Pin Except Supplies	(Note 1)	I_{IN}	-	±10	mA
Input Current, Power Supplies	(Note 1)	I_{IN}	-	±50	mA
Output Current	(Note 1)	I_{OUT}	-	±25	mA
Power Dissipation		P_{DN}	-	500	mW
Digital Input Voltages		V_{IND}	-0.5	VDD+0.5	V
Ambient Operating Temperature (Power Applied)		T_A	-40	85	°C
Storage Temperature Range		T_{STG}	-65	150	°C

1. Transient currents up to 100 mA will not cause SCR latch-up.

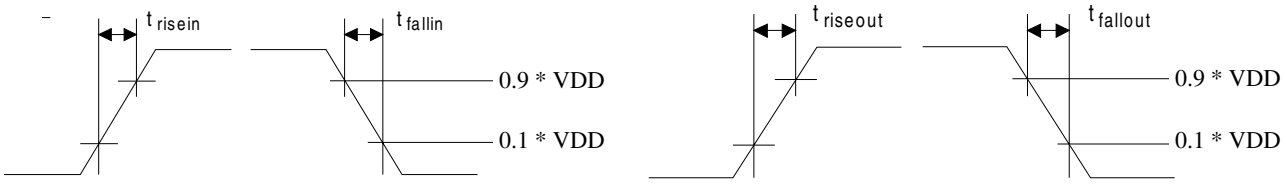
THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Allowable Junction Temperature	T_J	-	-	135	°C
Junction to Ambient Thermal Impedance	Θ_{JA}	-	65		°C / W
Ambient Operating Temperature (Power Applied)	T_A	-40	-	+85	°C

DIGITAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
High-Level Input Drive Voltage		V_{IH}	0.6 * VDD	-	VDD	V
Low-Level Input Drive Voltage		V_{IL}	0.0	-	0.8	V
High-Level Output Drive Voltage	I_{out} = -40 µA	V_{OH}	VDD - 0.3	-	VDD	V
Low-Level Output Drive Voltage	I_{out} = +40 µA	V_{OL}	0.0	-	0.3	V
Rise Times, Digital Inputs		t_{RISE}	-	-	100	ns
Fall Times, Digital Inputs		t_{FALL}	-	-	100	ns
Rise Times, Digital Outputs		t_{RISE}	-	-	100	ns
Fall Times, Digital Outputs		t_{FALL}	-	-	100	ns
Input Leakage Current	(Note 2)	I_{IN}	-	± 1	± 10	µA
3-State Leakage Current		I_{OZ}	-	-	± 10	µA
Digital Input Capacitance		C_{IN}	-	9	-	pF
Digital Output Pin Capacitance		C_{OUT}	-	9	-	pF

Notes: 2. Max leakage for pins with pull-up resistors ($\overline{TRST}$, TMS, TDI, $\overline{SSI}$, GPIO, MOSI, SCK1) is ±250 µA.



POWER CONSUMPTION

Parameter	Symbol	Min	Typ	Max	Unit
Operational Power Consumption					
1.024 MHz Digital Filter Clock	PWR_1	-	21	-	mW
2.048 MHz Digital Filter Clock	PWR_2	-	26	-	mW
4.096 MHz Digital Filter Clock	PWR_4	-	37	-	mW
8.192 MHz Digital Filter Clock	PWR_8	-	57	-	mW
16.384 MHz Digital Filter Clock	PWR_{16}	-	85	-	mW
Standby Power Consumption					
32 kHz Digital Filter Clock, Filter Stopped	PWR_S	-	40	-	µW

SWITCHING CHARACTERISTICS

SPI 1 Interface Timing (External Master)

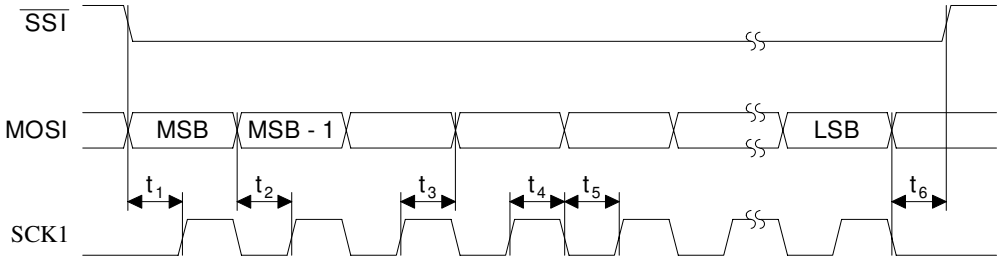


Figure 4. MOSI Write Timing in SPI Slave Mode

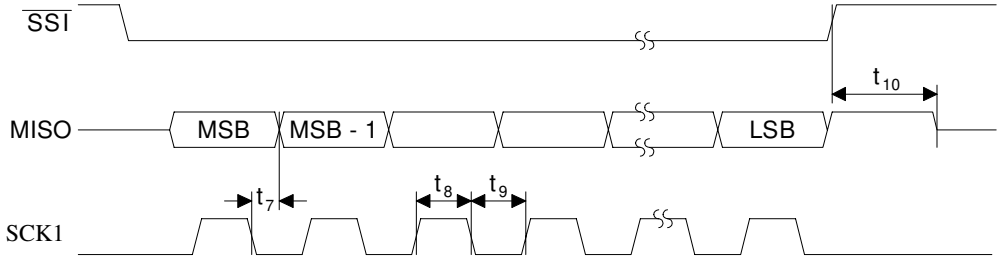


Figure 5. MISO Read Timing in SPI Slave Mode

Parameter	Symbol	Min	Typ	Max	Unit
MOSI Write Timing					
$\overline{SSI}$ Enable to Valid Latch Clock	t_1	60	-	-	ns
Data Set-up Time Prior to SCK1 Rising	t_2	60	-	-	ns
Data Hold Time After SCK1 Rising	t_3	120	-	-	ns
SCK1 High Time	t_4	120	-	-	ns
SCK1 Low Time	t_5	120	-	-	ns
SCK1 Falling Prior to $\overline{SSI}$ Disable	t_6	60	-	-	ns
MISO Read Timing					
SCK1 Falling to New Data Bit	t_7	-	-	60	ns
SCK1 High Time	t_8	120	-	-	ns
SCK1 Low Time	t_9	120	-	-	ns
$\overline{SSI}$ Rising to MISO Hi-Z	t_{10}	-	-	150	ns

SWITCHING CHARACTERISTICS

Serial Data Port (SD Port)

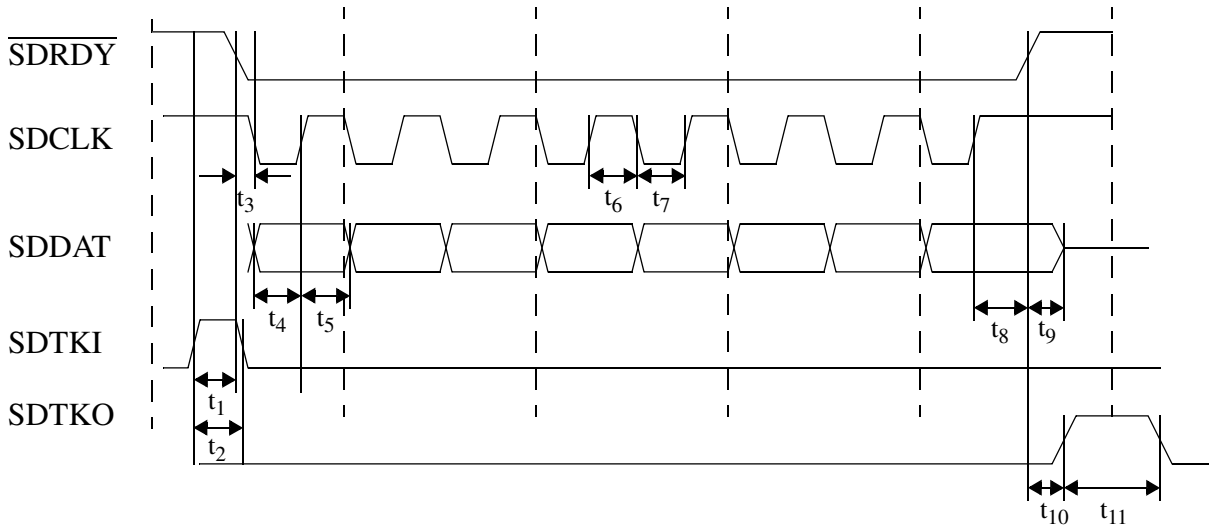
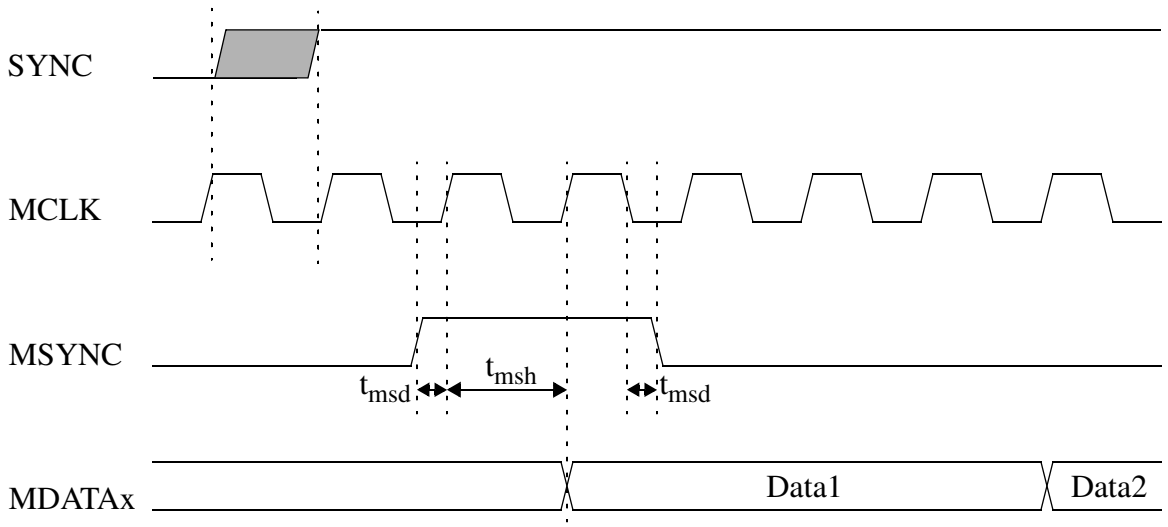


Figure 6. SD Port Read Timing

Parameter	Symbol	Min	Typ	Max	Unit
SDTKI to $\overline{\text{SDRDY}}$ Falling Edge	t_1	60	-	-	ns
SDTKI High Time Width	t_2	60	-	1000	ns
$\overline{\text{SDRDY}}$ Falling Edge to SDCLK Falling Edge	t_3	50	-	-	ns
Data Setup Time Prior to SDCLK Rising	t_4	60	-	-	ns
Data Hold Time After SDCLK Rising	t_5	60	-	-	ns
SDCLK High Time	t_6	120	-	-	ns
SDCLK Low Time	t_7	120	-	-	ns
SDCLK Rising to $\overline{\text{SDRDY}}$ Rising	t_8	60	-	-	ns
Data Hold Time After $\overline{\text{SDRDY}}$ Rising	t_9	-	-	150	ns
$\overline{\text{SDRDY}}$ High to SDTKO Rising Edge	t_{10}	-	-	60	ns
SDTKO High Time	t_{11}	90	-	-	ns

SWITCHING CHARACTERISTICS

CLK, SYNC, MCLK, MSYNC, and MDATAx



Note: SYNC input latched on MCLK rising edge. MSYNC output triggered by MCLK falling edge.

f_{MCLK}	2.048 MHz	1.024 MHz
$t_{msd} = T_{MCLK} / 4$	t_{msd} = 122 ns	t_{msd} = 244 ns
$t_{msh} = T_{MCLK}$	t_{msh} = 488 ns	t_{msh} = 976 ns

Figure 7. SYNC, MCLK, MSYNC, MDATA Interface Timing

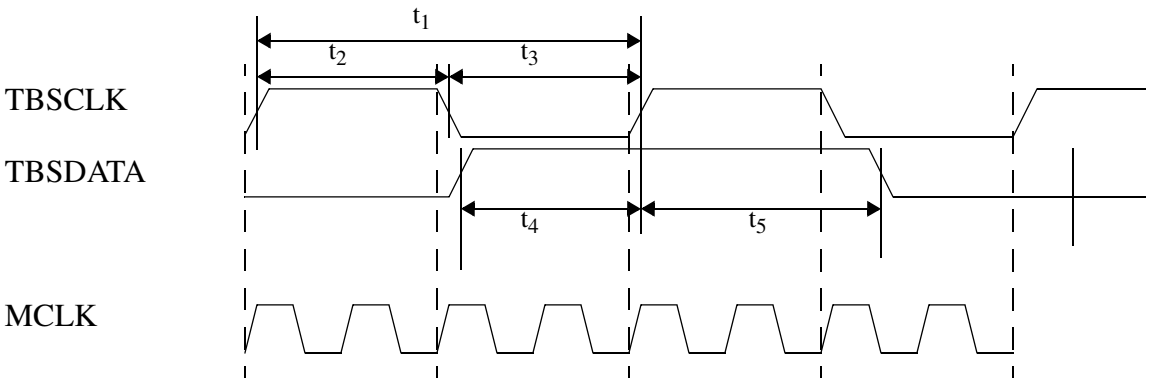
Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Frequency	(Note 3)	CLK	32	32.768	33	MHz
Master Clock Duty Cycle		DTY	40	-	60	%
Master Clock Rise Time		t_{RISE}	-	-	20	ns
Master Clock Fall Time		t_{FALL}	-	-	20	ns
Master Clock Jitter		JTR	-	-	300	ps
Synchronization after SYNC rising	(Note 4)	SYNC	-2	-	2	µs
MSYNC Setup Time to MCLK rising		t_{msr}	20	-	-	ns
MCLK rising to Valid MDATA		t_{mdv}	-	-	75	ns
MSYNC falling to MCLK rising		t_{msf}	20	-	-	ns

Notes: 3. Master clock frequencies above or below 32.768 MHz will affect generated clock frequencies.

4. Sampling synchronization between multiple CS5376A devices receiving identical SYNC signals.

SWITCHING CHARACTERISTICS

Test Bit Stream (TBS)



Note: Example timing shown for a 256 kHz output rate and no programmable delays.

Figure 8. TBS Output Clock and Data Timing

Parameter		Symbol	Min	Typ	Max	Unit
TBS Clock Timing						
TBS Clock Period		t_1	-	3.906	-	µs
TBS Clock High Time	(Note 5)	t_2	40	-	60	%
TBS Clock Low Time		t_3	40	-	60	%
TBS Data Output Timing						
TBS Data Bit Rate			-	256	-	kbps
TBS Data Rising to TBS Clock Rising Setup Time		t_4	60	-	-	ns
TBS Clock Rising to TBS Data Falling Hold Time	(Note 6)	t_5	60	-	-	ns

5. TBSCLK phase can be delayed in 1/8 increments. The timing diagram shows no TBSCLK delay.
6. TBSDATA can be delayed from 0 to 63 full bit periods. The timing diagram shows no TBSDATA delay.

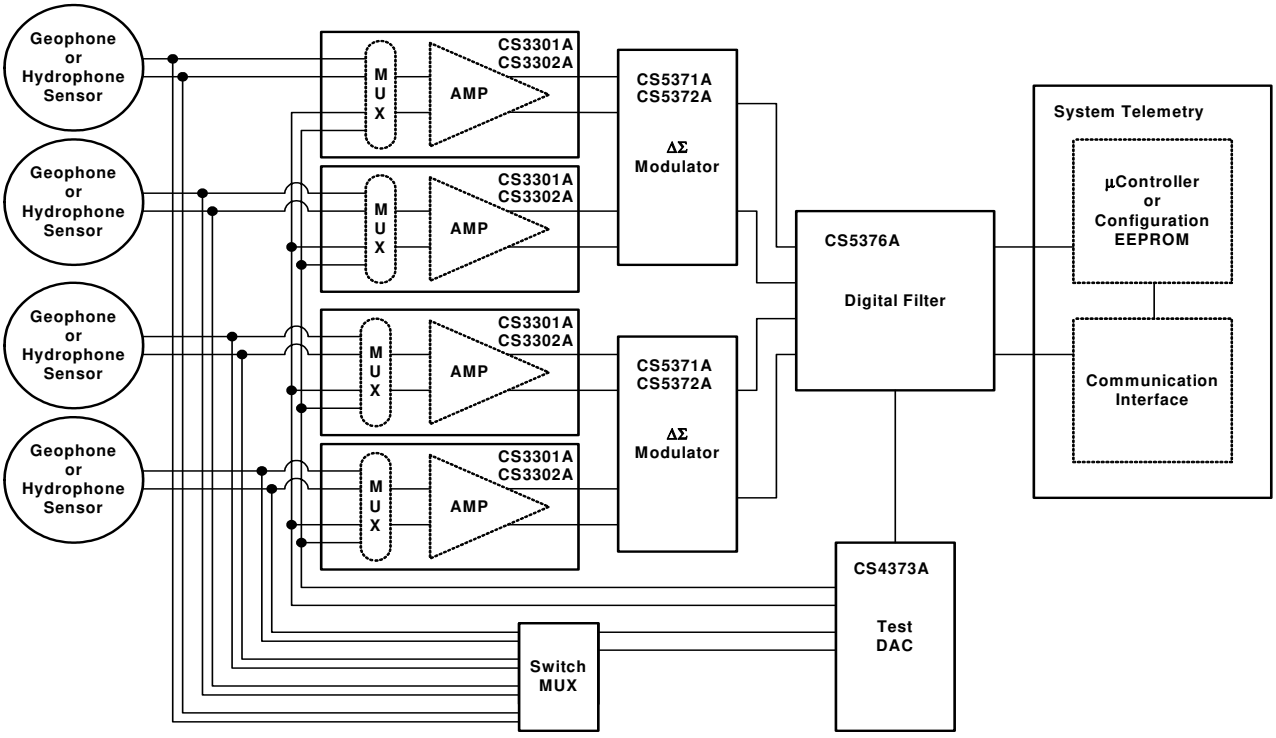


Figure 9. Multi-Channel System Block Diagram

3. SYSTEM DESIGN WITH CS5376A

Figure 9 illustrates a simplified block diagram of the CS5376A in a multi-channel measurement system.

Up to four differential sensors are connected through CS3301A/02A differential amplifiers to the CS5371A/72A ΔΣ modulators, where analog to digital conversion occurs. Each modulators 1-bit output connects to a CS5376A MDATA input, where the oversampled ΔΣ data is decimated and filtered to 24-bit output samples at a programmed output rate. These output samples are buffered in an 8-deep data FIFO and passed to the system telemetry on command.

System self tests are performed by connecting the CS5376A test bit stream (TBS) generator to the CS4373A test DAC. Analog tests drive differential signals from the CS4373A test DAC into the multiplexed inputs of the CS3301A/02A amplifiers or directly to the sensors through external analog switches. Digital loopback tests internally connect the TBS digital output directly to the CS5376A modulator inputs.

3.1 Power Supplies

The multi-channel system shown in Figure 9 typically operates from a ±2.5 V analog power supply and a 3.3 V digital power supply. The CS5376A logic core can be powered from 3 V to minimize power consumption, if required.

3.2 Reset Control

System reset is required only for the CS5376A device, and is a standard active low signal that can be generated by a power supply monitor or microcontroller. Other system devices default to a power-down state when the CS5376A is reset.

3.3 Clock Generation

A single 32.768 MHz low-jitter clock input, which can be generated from a VCXO based PLL, is required to drive the CS5376A device. Clock inputs for other system devices are driven by clock outputs from the CS5376A.

3.4 Synchronization

Digital filter phase and analog sample timing of the four ΔΣ modulators connected to the CS5376A are synchronized by a rising edge on the SYNC pin. If a synchronization signal is received identically by all CS5376A devices in a measurement network, synchronous sampling across the network is guaranteed.

3.5 System Configuration

Through the SPI 1 serial port, filter coefficients and digital filter register settings can either be programmed by a microcontroller or automatically loaded from an external EEPROM after reset. System configuration is only required for the CS5376A device, as other devices are configured via the CS5376A General Purpose I/O pins.

Two registers in the digital filter, SYSTEM1 and SYSTEM2 (0x2C, 0x2D), are provided for user defined system information. These are general purpose registers that will hold any 24-bit data values written to them.

3.6 Digital Filter Operation

After analog to digital conversion occurs in the modulators, the oversampled 1-bit ΔΣ data is read into the CS5376A through the MDATA pins. The digital filter then processes data through the enabled filter stages, decimating it to 24-bit words at a programmed output word rate. The final 24-bit samples are concatenated with 8-bit status words and placed into an output FIFO.

3.7 Data Collection

Data is collected from the CS5376A through the Serial Data port (SD port). Automatically or upon request, depending how the SDTKI pin is connected, the SD port initiates serial transactions to transfer 32-bit data from the output FIFO to the system telemetry. The output FIFO has eight data locations to permit latency in data collection.

3.8 Integrated peripherals

Test Bit Stream (TBS)

A digital signal generator built into the CS5376A produces a 1-bit ΔΣ sine wave. This digital test bit stream can be connected to the CS4373A test DAC to create high quality analog test signals or it can be internally looped back to the CS5376A MDATA inputs to test the digital filter and data collection circuitry.

Time Break

Timing information is recorded during data collection by strobing the TIMEB pin. A dedicated flag in the sample status bits, TB, is set high to indicate over which measurement the timing event occurred.

General Purpose I/O (GPIO)

Twelve general purpose pins are available on the CS5376A for system control. Each pin can be set as input or output, high or low, with an internal pull-up enabled or disabled. The CS3301A/02A, CS5371A/72A and CS4373A devices in Figure 9 are configured by simple pin settings controlled through the CS5376A GPIO pins.

Serial Peripheral Interface 2 (SPI 2)

A secondary master mode serial port to communicate with external serial peripherals.

JTAG Port

Boundary scan JTAG is IEEE 1149.1 compliant.

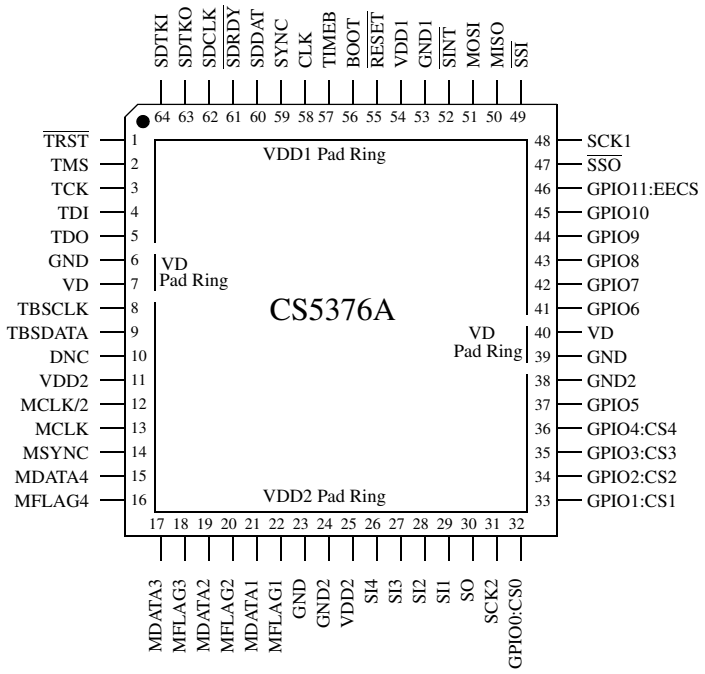


Figure 10. Power Supply Block Diagram

4. POWER SUPPLIES

The CS5376A has three sets of power supply inputs. Two sets supply power to the I/O pins of the device (VDD1, VDD2), and the third supplies power to the logic core (VD). The I/O pin power supplies determine the maximum input and output voltages when interfacing to peripherals, and the logic core power supply largely determines the power consumption of the CS5376A.

4.1 Pin Descriptions

VDD1, GND1 - Pins 54,53

Sets the interface voltage to a microcontroller and system telemetry. Can be driven with voltages from 3.3 V to 5 V.

VDD1 powers pins 1-5 and 41-64:

$\overline{\text{TRST}}$, TMS, TCK, TDI, TDO

GPIO6 - GPIO11:EECS

$\overline{\text{SSO}}$, SCK1, $\overline{\text{SSI}}$, MISO, MOSI, $\overline{\text{SINT}}$,

$\overline{\text{RESET}}$, BOOT, TIMEB, CLK, SYNC

SDDAT, $\overline{\text{SDRDY}}$, SDCLK, SDTKO, SDTKI

VDD2, GND2 - Pins 11, 25, 24, 38

Sets the interface voltage to the modulators, test DAC, and serial peripherals. Can be driven with voltages from 3.3 V to 5 V.

VDD2 powers pins 8-37:

TBSCLK, TBSDATA

MCLK/2, MCLK, MSYNC

MDATA1 - MDATA4

MFLAG1 - MFLAG4

SI1 - SI4, SO, SCK2

GPIO0:CS0 - GPIO5

VD, GND - Pins 7, 40, 6, 23, 39

Sets the operational voltage of the CS5376A logic core. Can be driven with voltages from 3 V to 5 V. A 3 V supply minimizes total power consumption.

4.2 Bypass Capacitors

Each power supply pin should be bypassed with parallel 1 µF and 0.01 µF caps, or by a single 0.1 µF cap, placed as close as possible to the CS5376A. Bypass capacitors should be ceramic (X7R, C0G), tantalum, or other good quality dielectric type.

4.3 Power Consumption

Power consumption of the CS5376A depends primarily on the power supply voltage of the logic core (VD) and the programmed digital filter clock rate. Digital filter clock rates are selected based on the required output word rate as explained in “Digital Filter Initialization” on page 41.

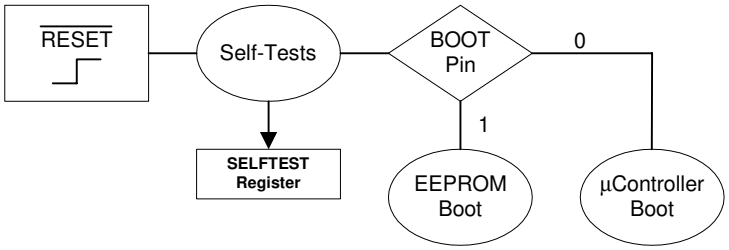


Figure 11. Reset Control Block Diagram

5. RESET CONTROL

The CS5376A reset signal is active low. When released, a series of self-tests are performed and the device either actively boots from an external EEPROM or enters an idle state waiting for microcontroller configuration.

5.1 Pin Descriptions

$\overline{\text{RESET}}$ - Pin 55

Reset input, active low.

BOOT - Pin 56

Boot mode select, latched following a $\overline{\text{RESET}}$ rising edge.

BOOT = 1 = EEPROM boot

BOOT = 0 = Microcontroller boot

5.2 Reset Self-Tests

After $\overline{\text{RESET}}$ is released but before booting, a series of digital filter self-tests are run. Results are combined into the SELFTEST register (0x2F), with 0x0AAAAA indicating all passed. Self-tests require 60 ms to complete, after which configuration commands are serviced.

Self-Test Type	Pass Code	Fail Code
Program ROM	0x00000A	0x00000F
Data ROM	0x0000A0	0x0000F0
Program RAM	0x000A00	0x000F00
Data RAM	0x00A000	0x00F000
Execution Unit	0x0A0000	0x0F0000

5.3 Boot Configurations

The logic state of the BOOT pin after reset determines if the CS5376A actively reads configuration information from EEPROM or enters an idle state waiting for a microcontroller to write configuration commands.

EEPROM Boot

When the BOOT pin is high after reset, the CS5376A actively reads data from an external serial EEPROM and then begins operation in the specified configuration. Configuration commands and data are encoded in the EEPROM as specified in the ‘Configuration By EEPROM’ section of this data sheet, starting on page 26.

Microcontroller Boot

When the BOOT pin is low after reset, the CS5376A enters an idle state waiting for a microcontroller to write configuration commands and initialize filter operation. Configuration commands and data are written as specified in the ‘Configuration By Microcontroller’ section of this data sheet, starting on page 32.

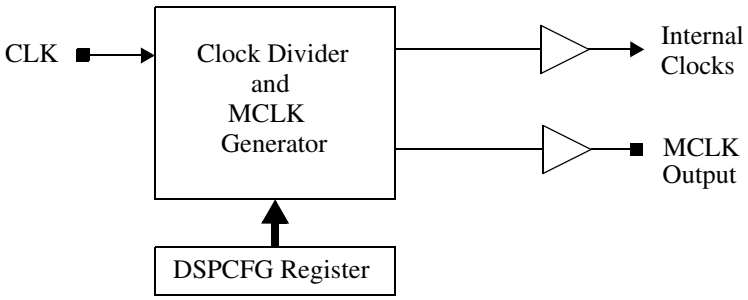


Figure 12. Clock Generation Block Diagram

6. CLOCK GENERATION

The CS5376A requires a 32.768 MHz master clock input, which is used to generate internal digital filter clocks and external modulator clocks.

6.1 Pin Description

CLK - Pin 58

Clock input, nominal frequency 32.768 MHz.

6.2 Synchronous Clocking

To guarantee synchronous measurements throughout a sensor network, the CS5376A master clock should be distributed to arrive at all nodes in phase. The 32.768 MHz master clock can either be directly distributed through the system telemetry, or reconstructed locally using a VCXO based PLL. To ensure recovered clocks have identical phase, system PLL designs should use a phase/frequency detector architecture.

6.3 Master Clock Jitter and Skew

Care must be taken to minimize jitter and skew in the received master clock as both parameters affect measurement performance.

Jitter in the master clock causes jitter in the generated modulator clocks, resulting in sample timing errors and increased noise.

Skew in the master clock from node to node creates a sample timing offset, resulting in systematic measurement errors in the reconstructed signal.

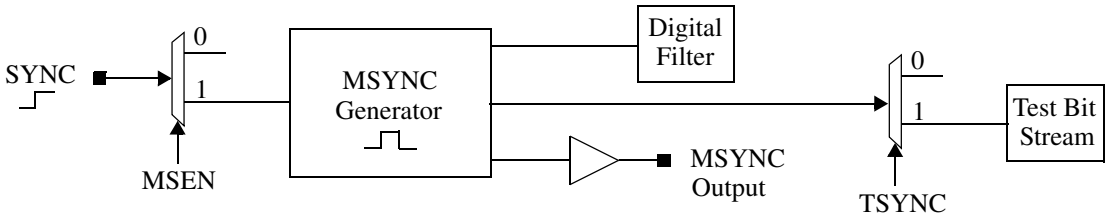


Figure 13. Synchronization Block Diagram

7. SYNCHRONIZATION

The CS5376A has a dedicated SYNC input that aligns the internal digital filter phase and generates an external signal for synchronizing modulator analog sampling. By providing simultaneous rising edges to the SYNC pins of multiple CS5376A devices, synchronous sampling across a network can be guaranteed.

7.1 Pin Description

SYNC - Pin 59

Synchronization input, rising edge triggered.

7.2 MSYNC Generation

The SYNC signal rising edge is used to generate a retimed synchronization signal, MSYNC. The MSYNC signal reinitializes internal digital filter phase and is driven onto the MSYNC output pin to phase align modulator analog sampling.

The MSEN bit in the digital filter CONFIG register (0x00) enables MSYNC generation. See "Modulator Interface" on page 39 for more information about MSYNC.

7.3 Digital Filter Synchronization

The internal MSYNC signal resets the digital filter state machine to establish a known digital filter phase. Filter convolutions restart, and the next output word is available one full sample period later.

Repetitive synchronization is supported when SYNC events occur at exactly the selected output word rate. In this case, re-synchronization occurs at the start of a convolution cycle when the digital filter state machine is already reset.

7.4 Modulator Synchronization

The external MSYNC signal phase aligns modulator analog sampling when connected to the CS5371A/72A MSYNC input. This ensures synchronous analog sampling relative to MCLK.

Repetitive synchronization of the modulators is supported when SYNC events occur at exactly the selected output word rate. In this case, synchronization will occur at the start of analog sampling.

7.5 Test Bit Stream Synchronization

When the test bit stream generator is enabled, an MSYNC signal can reset the internal data pointer. This restarts the test bit stream from the first data point to establish a known output signal phase.

The TSYNC bit in the digital filter TBSCFG register (0x2A) enables synchronization of the test bit stream by MSYNC. When TSYNC is disabled, the test bit stream phase is not affected by MSYNC.