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CS5378

Low-power Single-channel Decimation Filter

Features

- Single-channel Digital Decimation Filter
  - Multiple On-chip FIR and IIR Coefficient Sets
  - Programmable Coefficients for Custom Filters
  - Synchronous Operation
- Integrated PLL for Clock Generation
  - 1.024 MHz, 2.048 MHz, or 4.096 MHz Input
  - Standard Clock or Manchester Input
- Selectable Output Word Rate
  - 4000, 2000, 1000, 500, 333, 250 SPS
  - 200, 125, 100, 50, 40, 25, 20, 10, 5, 1 SPS
- Digital Gain and Offset Corrections
- Test DAC Bit-stream Generator
  - Digital Sine Wave Output
- Time Break Controller, General-purpose I/O
- Microcontroller or EEPROM Configuration
- Small-footprint, 28-pin SSOP Package
- Low Power Consumption
  - 16 mW at 500 SPS OWR
- Flexible Power Supplies
  - I/O Interface and PLL: 3.3 V or 5.0 V
  - Digital Logic Core: 2.5 V, 3.3 V or 5.0 V

Description

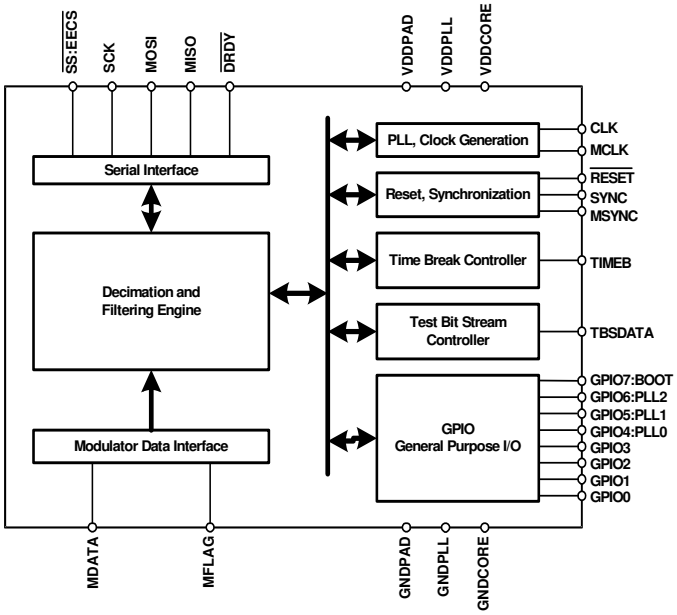
The CS5378 is a multi-function digital filter utilizing a low-power signal processing architecture to achieve efficient filtering for a delta-sigma-type modulator. By combining the CS5378 with a CS3301A/02A differential amplifier and a CS5373A modulator + test DAC, a synchronous high-resolution, self-testing, single-channel measurement system can be designed quickly and easily.

Digital filter coefficients for the CS5378 FIR and IIR filters are included on-chip for a simple setup, or they can be programmed for custom applications. Selectable digital filter decimation ratios produce output word rates from 4000 SPS to 1 SPS, resulting in measurement bandwidths ranging from 1600 Hz down to 400 mHz when using the on-chip coefficient sets.

The CS5378 includes integrated peripherals to simplify system design: a low-jitter PLL for standard clock or Manchester inputs, offset and gain corrections, a test DAC bit stream generator, a time break controller, and eight general-purpose I/O pins.

ORDERING INFORMATION

See page 86.



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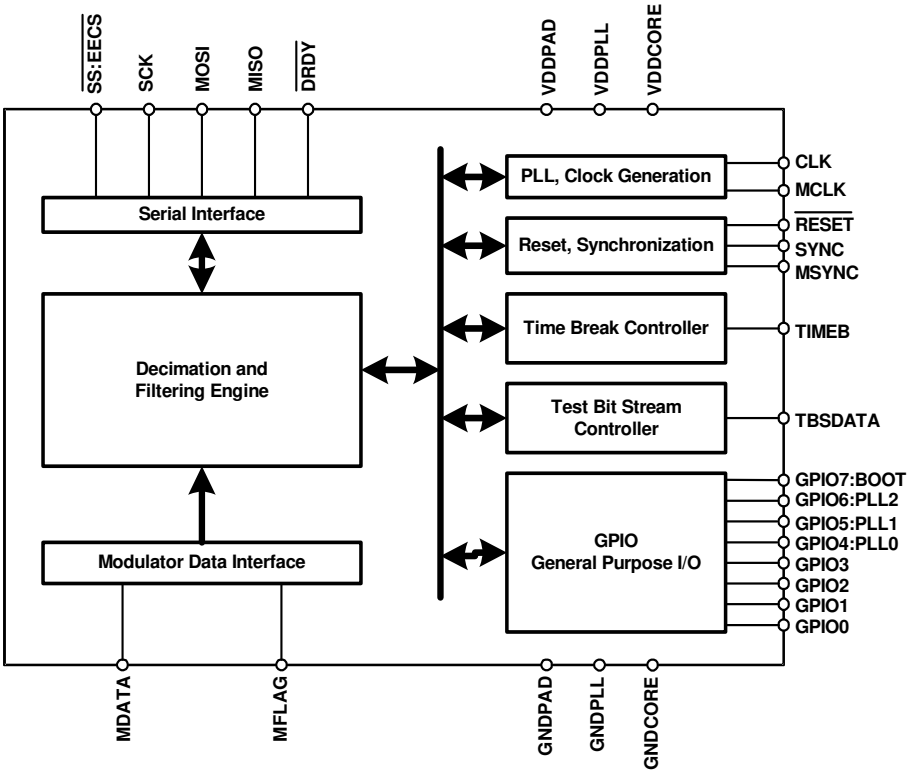


Figure 1. CS5378 Block Diagram

1. GENERAL DESCRIPTION

The CS5378 is a single channel digital filter with integrated system peripherals. Figure 1 illustrates a simplified block diagram of the CS5378.

1.1 Digital Filter Features

- Single channel decimation filter for CS5373A ΔΣ modulator.
- Synchronous operation for simultaneous sampling in multi-sensor systems.
  - Internal synchronization of digital filter phase to an external SYNC signal.
- Output word rates, including low bandwidth rates.
  - Standard output rates: 4000, 2000, 1000, 500, 333, 250 SPS.
  - Low bandwidth rates: 200, 125, 100, 50, 40, 25, 20, 10, 5, 1 SPS.
- Flexible digital filter configuration. (See Figure 2)
  - Cascaded SINC, FIR, and IIR filters with selectable output stage.
  - Linear and minimum phase FIR low-pass filter coefficients included.
  - 3 Hz Butterworth IIR high-pass filter coefficients included.
  - FIR and IIR coefficients programmable to create a custom filter response.
- Digital gain correction to normalize sensor gain.
- Digital offset correction and calibration.
  - Offset correction to remove measurement

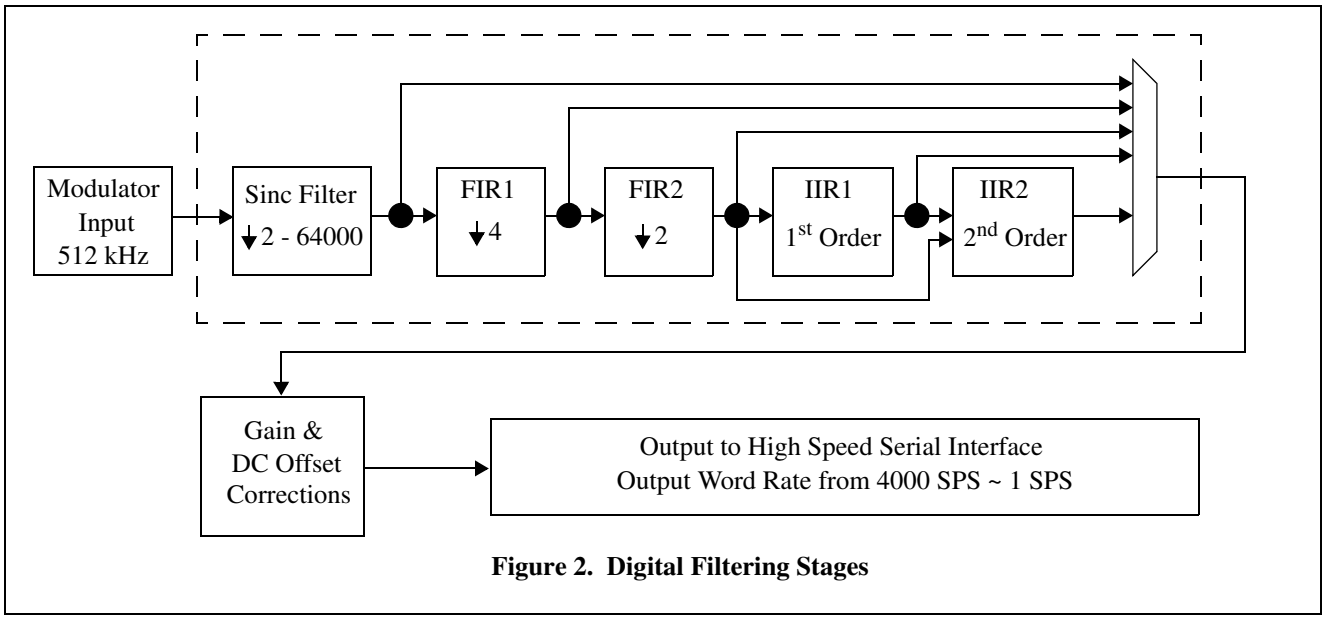


Figure 2. Digital Filtering Stages

DC offset.

- Calibration engine for automatic calculation of offset correction factor.

1.2 Integrated Peripheral Features

- Low jitter PLL to generate local clocks.
  - 1.024 MHz, 2.048 MHz, 4.096 MHz standard clock or Manchester encoded input.
- Synchronous operation for simultaneous sampling in multi-sensor systems.
  - MCLK / MSYNC output signals to synchronize external components.
- High speed serial data output.
  - Asynchronous operation to 4 MHz for direct connection to system telemetry.
  - Internal 8-deep data FIFO for flexible output timing.
  - Selectable 24-bit data only or 32-bit status+data output.
- Digital test bit stream signal generator suitable for CS5373A ΔΣ test DAC.
  - Sine wave output mode for testing total harmonic distortion.
- Time break controller to record system timing information.
  - Dedicated TB status bit in the output data stream.
  - Programmable output delay to match system group delay.
- 8 General Purpose I/O (GPIO) pins for local hardware control.

1.3 System Level Features

- Flexible configuration options.
  - Configuration 'on-the-fly' via microcontroller or system telemetry.
  - Fixed configuration via stand-alone boot EEPROM.
- Low power consumption.
  - 16 mW at 500 SPS OWR.
  - 100 µW standby mode.
- Flexible power supply configurations.
  - Separate digital logic core, telemetry I/O, and PLL power supplies.
  - Telemetry I/O and PLL interfaces operate

from 3.3 V or 5 V.

- Digital logic core operates from 2.5 V, 3.3 V or 5 V.

- Small 28-pin SSOP package.
  - Total footprint 8 mm x 10 mm plus three bypass capacitors.

1.4 Configuration Interface

- Configuration from microcontroller or stand-alone boot EEPROM.
  - Microcontroller boot permits reconfiguration during operation.
  - EEPROM boot sets a fixed operational configuration.
- Configuration commands written through the serial interface. (See Table 1)
  - Standardized microcontroller interface using SPI™ registers. (See Table 3)
  - Commands write digital filter registers and FIR / IIR filter coefficients.
  - Digital filter registers set hardware configuration options.

Microcontroller Boot Configuration Commands

Name	CMD 24-bit	DAT1 24-bit	DAT2 24-bit	Description
NOP	000000	-	-	No Operation
WRITE DF REGISTER	000001	REG	DATA	Write Digital Filter Register
READ DF REGISTER	000002	REG [DATA]	- -	Read Digital Filter Register
WRITE FIR COEFFICIENTS	000003	NUM FIR1 (FIR COEF)	NUM FIR2 (FIR COEF)	Write Custom FIR Coefficients
WRITE IIR COEFFICIENTS	000004	a11 b11 a22 b21	b10 a21 b20 b22	Write Custom IIR Coefficients
WRITE ROM COEFFICIENTS	000005	COEF SEL	-	Use On-Chip Coefficients
NOP	000006	-	-	No Operation
NOP	000007	-	-	No Operation
FILTER START	000008	-	-	Start Digital Filter Operation
FILTER STOP	000009	-	-	Stop Digital Filter Operation

EEPROM Boot Configuration Commands

Name	CMD 8-bit	DATA 24-bit	Description
NOP	00	-	No Operation
WRITE DF REGISTER	01	REG DATA	Write Digital Filter Register
WRITE FIR COEFFICIENTS	02	NUM FIR1 NUM FIR2 (FIR COEF)	Write Custom FIR Coefficients
WRITE IIR COEFFICIENTS	03	a11 b10 b11 a21 a22 b20 b21 b22	Write Custom IIR Coefficients
WRITE ROM COEFFICIENTS	04	COEF SEL	Use On-Chip Coefficients
NOP	05	-	No Operation
NOP	06	-	No Operation
FILTER START	07	-	Start Digital Filter Operation

[DATA] indicates data word returned from digital filter.

(DATA) indicates multiple words of this type are to be written.

Table 1. Microcontroller and EEPROM Configuration Commands

Bits	23:20	19:16	15:12	11:8	7:4	3:0
Selection	0000	0000	IIR2	IIR1	FIR2	FIR1

Bits 15:12	IIR2 Coefficients
0000	3 Hz @ 2000 SPS
0001	3 Hz @ 1000 SPS
0010	3 Hz @ 500 SPS
0011	3 Hz @ 333 SPS
0100	3 Hz @ 250 SPS

Bits 11:8	IIR1 Coefficients
0000	3 Hz @ 2000 SPS
0001	3 Hz @ 1000 SPS
0010	3 Hz @ 500 SPS
0011	3 Hz @ 333 SPS
0100	3 Hz @ 250 SPS

Bits 3:0	FIR1 Coefficients
0000	Linear Phase
0001	Minimum Phase

Bits 7:4	FIR2 Coefficients
0000	Linear Phase
0001	Minimum Phase

Figure 3. FIR and IIR Coefficient Set Selection Word

Test Bit Stream Characteristic Equation:

*(Signal Freq) * (# TBS Data) * (Interpolation + 1) = Output Rate*

Example: *(31.25 Hz) * (1024) * (0x07 + 1) = 256 kHz*

Signal Frequency (TBSDATA)	Output Rate (TBSCLK)	Output Rate Selection (RATE)	Interpolation Selection (INTP)
10.00 Hz	256 kHz	0x4	0x18
10.00 Hz	512 kHz	0x5	0x31
25.00 Hz	256 kHz	0x4	0x09
25.00 Hz	512 kHz	0x5	0x13
31.25 Hz	256 kHz	0x4	0x07
31.25 Hz	512 kHz	0x5	0x0F
50.00 Hz	256 kHz	0x4	0x04
50.00 Hz	512 kHz	0x5	0x09
125.00 Hz	256 kHz	0x4	0x01
125.00 Hz	512 kHz	0x5	0x03

Table 2. TBS Configurations Using On-Chip Data

SPI Registers

Name	Addr.	Type	# Bits	Description
SPICTRL	00 - 02	R/W	8, 8, 8	SPI Control
SPICMD	03 - 05	R/W	8, 8, 8	SPI Command
SPIDAT1	06 - 08	R/W	8, 8, 8	SPI Data 1
SPIDAT2	09 - 0B	R/W	8, 8, 8	SPI Data 2

Digital Filter Registers

Name	Addr.	Type	# Bits	Description
CONFIG	00	R/W	24	Hardware Configuration
RESERVED	01-0D	R/W	24	Reserved
GPCFG	0E	R/W	24	GPIO[7:0] Direction, Pull-up Enable, and Data
RESERVED	0F-1F	R/W	24	Reserved
FILTCFG	20	R/W	24	Digital Filter Configuration
GAIN	21	R/W	24	Gain Correction
RESERVED	22-24	R/W	24	Reserved
OFFSET	25	R/W	24	Offset Correction
RESERVED	26-28	R/W	24	Reserved
TIMEBRK	29	R/W	24	Time Break Delay
TBSCFG	2A	R/W	24	Test Bit Stream Configuration
TBSGAIN	2B	R/W	24	Test Bit Stream Gain
SYSTEM1	2C	R/W	24	User Defined System Register 1
SYSTEM2	2D	R/W	24	User Defined System Register 2
VERSION	2E	R/W	24	Hardware Version ID
SELFTEST	2F	R/W	24	Self-Test Result Code

Table 3. SPI and Digital Filter Registers

PLL[2:0]	Mode Selection on Reset
111	32.768 MHz clock input (PLL bypass).
110	1.024 MHz clock input.
101	2.048 MHz clock input.
100	4.096 MHz clock input.
011	32.768 MHz clock input (PLL bypass).
010	1.024 MHz Manchester input.
001	2.048 MHz Manchester input.
000	4.096 MHz Manchester input.

BOOT	Mode Selection on Reset
1	EEPROM boot
0	Microcontroller boot

Configuration Note:

States of the PLL[2:0] and BOOT pins are latched immediately after reset to select modes.

These pins have a weak (~100 kΩ) pull-up resistor enabled by default. An external 10 kΩ pull-down is required to set a low condition.

Table 4. PLL and BOOT Mode Reset Configurations

2. CHARACTERISTICS AND SPECIFICATIONS

- Min / Max characteristics and specifications are guaranteed over the Specified Operating Conditions.
- Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25°C.
- GND, GND1, GND2 = 0 V, all voltages with respect to 0 V.

SPECIFIED OPERATING CONDITIONS

Parameter		Symbol	Min	Nom	Max	Unit
Logic Core Power Supply		VDDCORE	2.375	2.5	5.25	V
PLL Power Supply		VDDPLL	3.135	3.3	5.25	V
I/O Power Supply		VDDPAD	3.135	3.3	5.25	V
Ambient Operating Temperature	Industrial (-IQ)	T_A	-40	-	85	°C

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Power Supplies	Logic Core	VDDCORE	-0.3	6.0	V
	PLL	VDDPLL	-0.3	6.0	V
	I/O	VDDPAD	-0.3	6.0	V
Input Current, Any Pin Except Supplies	(Note 1)	I_{IN}	-	±10	mA
Input Current, Power Supplies	(Note 1)	I_{IN}	-	±50	mA
Output Current	(Note 1)	I_{OUT}	-	±25	mA
Power Dissipation		P_{DN}	-	500	mW
Digital Input Voltages		V_{IND}	-0.3	VDD+0.3	V
Ambient Operating Temperature (Power Applied)		T_A	-40	85	°C
Storage Temperature Range		T_{STG}	-65	150	°C

1. Transient currents up to 100 mA will not cause SCR latch-up.

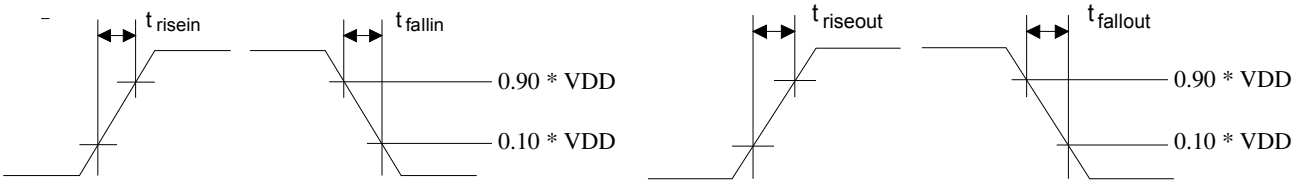
THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Allowable Junction Temperature	T_J	-	-	135	°C
Junction to Ambient Thermal Impedance (4-Layer PCB)	Θ_{JA}	-	50		°C / W
Ambient Operating Temperature (Power Applied)	T_A	-40	-	+85	°C

DIGITAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
High-Level Input Drive Voltage		V_{IH}	0.6 * VDD	-	VDD	V
Low-Level Input Drive Voltage		V_{IL}	0.0	-	0.8	V
High-Level Output Drive Voltage	I_{out} = -40 µA	V_{OH}	VDD - 0.3	-	VDD	V
Low-Level Output Drive Voltage	I_{out} = +40 µA	V_{OL}	0.0	-	0.3	V
Rise Times, Digital Inputs		t_{RISE}	-	-	100	ns
Fall Times, Digital Inputs		t_{FALL}	-	-	100	ns
Rise Times, Digital Outputs		t_{RISE}	-	-	100	ns
Fall Times, Digital Outputs		t_{FALL}	-	-	100	ns
Input Leakage Current	(Note 2)	I_{IN}	-	±	± 10	µA
3-State Leakage Current		I_{OZ}	-	-	± 10	µA
Digital Input Capacitance		C_{IN}	-	9	-	pF
Digital Output Pin Capacitance		C_{OUT}	-	9	-	pF

Notes: 2. Maximum leakage for pins with pull-up resistors ($\overline{\text{RESET}}$, $\overline{\text{SS:EECS}}$, GPIO, MOSI, SCK) is ±250 µA.



POWER CONSUMPTION

Parameter	Symbol	Min	Typ	Max	Unit
Operational Power Consumption					
1.024 MHz Digital Filter Clock	PWR_1	-	12	-	mW
2.048 MHz Digital Filter Clock	PWR_2	-	14	-	mW
4.096 MHz Digital Filter Clock	PWR_4	-	16	-	mW
8.192 MHz Digital Filter Clock	PWR_8	-	24	-	mW
Standby Power Consumption					
32 kHz Digital Filter Clock, Filter Stopped	PWR_S	-	100	-	µW

SWITCHING CHARACTERISTICS

Serial Configuration Interface Timing (External Master)

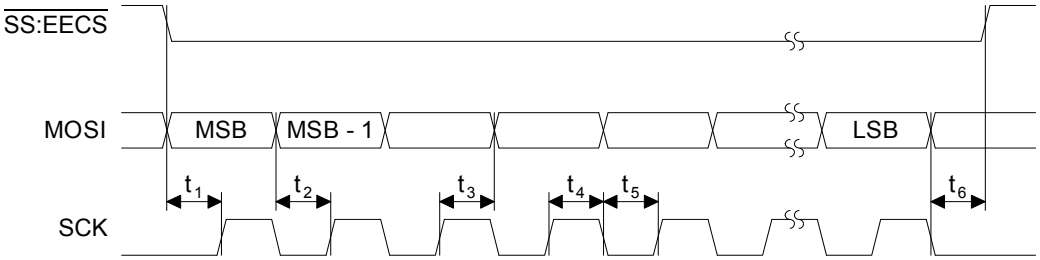


Figure 4. MOSI Write Timing in SPI Slave Mode

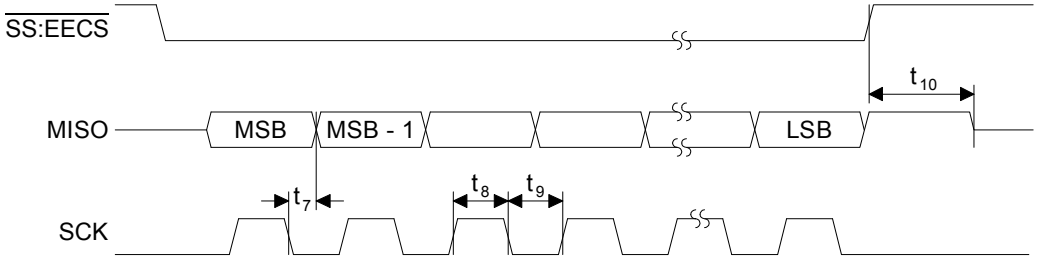


Figure 5. MISO Read Timing in SPI Slave Mode

Parameter	Symbol	Min	Typ	Max	Unit
MOSI Write Timing					
$\overline{\text{SS:EECS}}$ Enable to Valid Latch Clock	t_1	60	-	-	ns
Data Set-up Time Prior to SCK Rising	t_2	60	-	-	ns
Data Hold Time After SCK Rising	t_3	120	-	-	ns
SCK High Time	t_4	120	-	-	ns
SCK Low Time	t_5	120	-	-	ns
SCK Falling Prior to $\overline{\text{SS:EECS}}$ Disable	t_6	60	-	-	ns
MISO Read Timing					
SCK Falling to New Data Bit	t_7	-	-	60	ns
SCK High Time	t_8	120	-	-	ns
SCK Low Time	t_9	120	-	-	ns
$\overline{\text{SS:EECS}}$ Rising to MISO Hi-Z	t_{10}	-	-	150	ns

SWITCHING CHARACTERISTICS

Serial Data Interface Timing

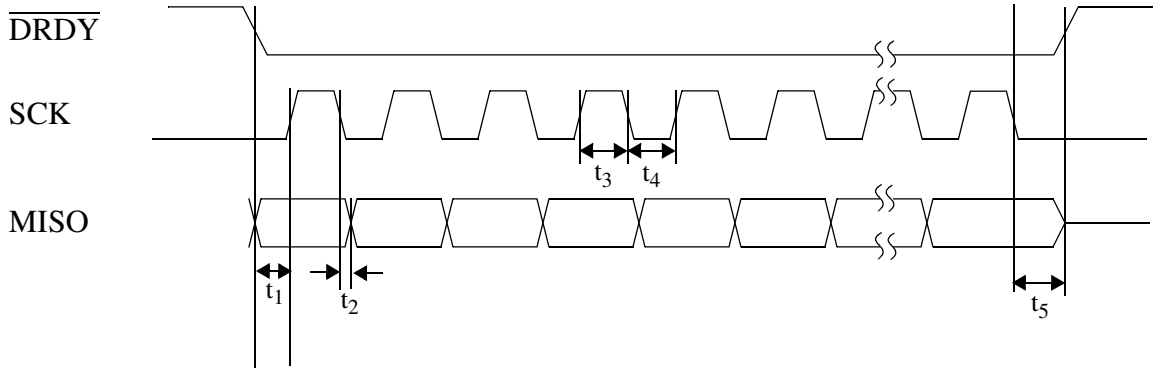
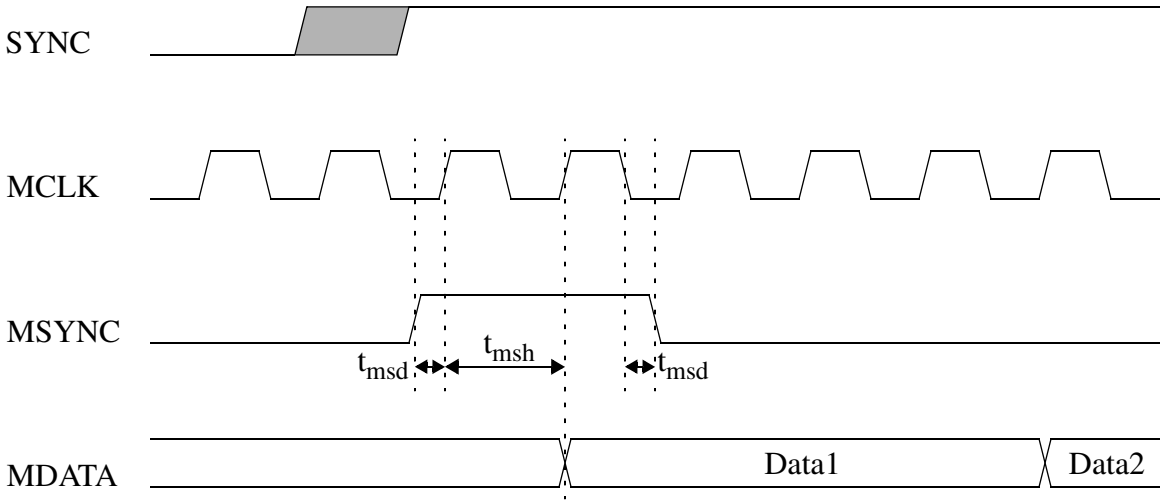


Figure 6. Serial Data Read Timing

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{DRDY}}$ Falling Edge to SCK Rising	t_1	60	-	-	ns
SCK Falling to New Data Bit	t_2	-	-	120	ns
SCK High Time	t_3	120	-	-	ns
SCK Low Time	t_4	120	-	-	ns
Final SCK Falling to $\overline{\text{DRDY}}$ Rising	t_5	60	-	-	ns

SWITCHING CHARACTERISTICS

CLK, SYNC, MCLK, MSYNC, and MDATA



Note: SYNC input latched on MCLK rising edge. MSYNC output triggered by MCLK falling edge.

f_{MCLK}	2.048 MHz	1.024 MHz
$t_{msd} = T_{MCLK} / 4$	t_{msd} = 122 ns	t_{msd} = 244 ns
$t_{msh} = T_{MCLK}$	t_{msh} = 488 ns	t_{msh} = 976 ns

Figure 7. SYNC, MCLK, MSYNC, MDATA Interface Timing

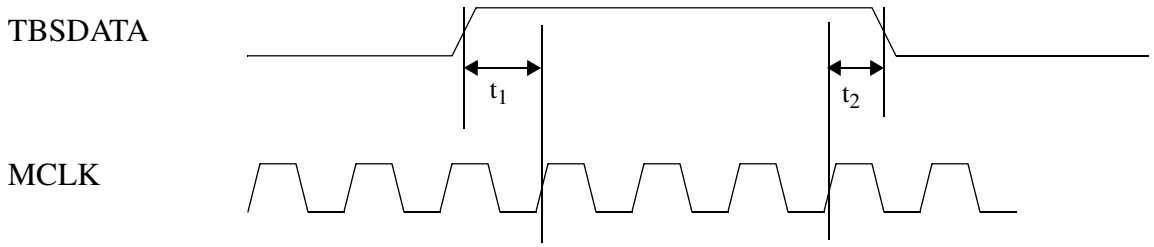
Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Frequency	(Note 3)	CLK	32	32.768	33	MHz
Master Clock Duty Cycle		DTY	40	-	60	%
Master Clock Rise Time		t_{RISE}	-	-	20	ns
Master Clock Fall Time		t_{FALL}	-	-	20	ns
Master Clock Jitter		JTR	-	-	300	ps
Synchronization after SYNC rising	(Note 4)	SYNC	-2	-	2	µs
MSYNC Setup Time to MCLK rising		t_{mss}	20	-	-	ns
MCLK rising to Valid MDATA		t_{mdv}	-	-	75	ns
MSYNC falling to MCLK rising		t_{msf}	20	-	-	ns

Notes: 3. PLL bypass mode. The PLL generates a 32.768 MHz master clock when enabled.

4. Sampling synchronization between multiple CS5378 devices receiving identical SYNC signals.

SWITCHING CHARACTERISTICS

Test Bit Stream (TBS)



Note: Example timing shown for a 256 kHz output rate and no programmable delays.

Figure 8. TBS Output Data Timing

Parameter	Symbol	Min	Typ	Max	Unit
TBS Data Output Timing					
TBS Data Bit Rate		-	256	-	kbps
TBS Data Rising to MCLK Rising Setup Time	t_1	60	-	-	ns
MCLK Rising to TBS Data Falling Hold Time (Note 5)	t_2	60	-	-	ns

5. TBSDATA can be delayed from 0 to 63 full bit periods. The timing diagram shows no TBSDATA delay.

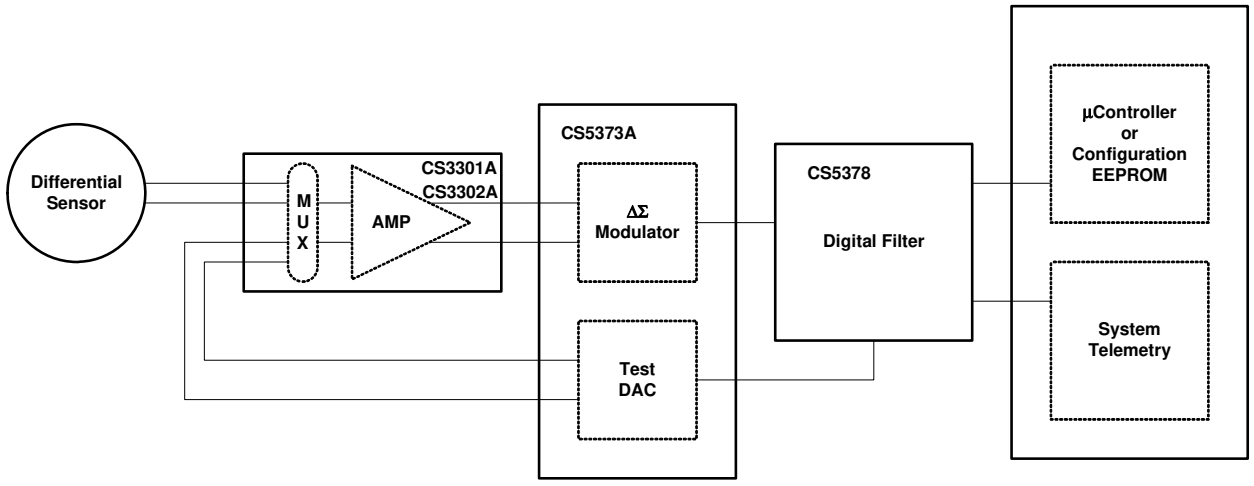


Figure 9. Single-Channel System Block Diagram

3. SYSTEM DESIGN WITH CS5378

Figure 9 illustrates a simplified block diagram of the CS5378 in a single channel measurement system.

A differential sensor is connected through the CS3301A/02A differential amplifiers to the CS5373A ΔΣ modulator, where analog to digital conversion occurs. The modulator's 1-bit output connects to the CS5378 MDATA input, where the oversampled ΔΣ data is decimated and filtered to 24-bit output samples at a programmed output rate. These output samples are buffered into an 8-deep data FIFO and then passed to the system telemetry.

System self tests are performed by connecting the CS5378 test bit stream (TBS) generator to the CS5373A test DAC. Analog tests drive differential signals from the CS5373A test DAC into the multiplexed inputs of the CS3301A/02A amplifiers or directly to the differential sensor. Digital loopback tests internally connect the TBS digital output directly to the CS5378 modulator input.

3.1 Power Supplies

The system shown in Figure 9 typically operates from a ±2.5 V analog power supply and a 3.3 V digital power supply. The CS5378 logic core can be powered from 2.5 V to minimize power consumption, if required.

3.2 Reset Control

System reset is required only for the CS5378 device, and is a standard active low signal that can be generated by a power supply monitor or microcontroller. Other system devices default to a power-down state when the CS5378 is reset.

3.3 PLL and Clock Generation

A PLL is included on the CS5378 to generate an internal 32.768 MHz master clock from a 1.024 MHz, 2.048 MHz, or 4.096 MHz standard clock or Manchester encoded input. Clock inputs for other system devices are driven by clock outputs from the CS5378.

3.4 Synchronization

Digital filter phase and analog sample timing of the ΔΣ modulator connected to the CS5378 are synchronized by a rising edge on the SYNC pin. If a synchronization signal is received identically by all CS5378 devices in a measurement network, synchronous sampling across the network is guaranteed.

3.5 System Configuration

Through the serial configuration interface, filter coefficients and digital filter register settings can either be programmed by a microcontroller or automatically loaded from an external EEPROM after reset. System configuration is only required for the CS5378 device, as other devices are configured via the CS5378 General Purpose I/O pins.

Two registers in the digital filter, SYSTEM1 and SYSTEM2 (0x2C, 0x2D), are provided for user defined system information. These are general purpose registers that will hold any 24-bit data values written to them.

3.6 Digital Filter Operation

After analog to digital conversion occurs in the modulator, the oversampled 1-bit ΔΣ data is read into the CS5378 through the MDATA pin. The digital filter then processes data through the enabled filter stages, decimating it to 24-bit words at a programmed output word rate. The final 24-bit samples are concatenated with 8-bit status words and placed into an output FIFO.

3.7 Data Collection

Data is collected from the CS5378 through the serial data interface. When data is available, serial transactions are automatically initiated to transfer 24-bit data or 32-bit status+data from the output FIFO to the system telemetry. The output FIFO has eight data locations to permit latency in data collection.

3.8 Integrated peripherals

Test Bit Stream (TBS)

A digital signal generator built into the CS5378 produces a 1-bit ΔΣ sine wave. This digital test bit stream is connected to the CS5373A test DAC to create high quality analog test signals or internally looped back to the CS5378 MDATA input to test the digital filter and data collection circuitry.

Time Break

Timing information is recorded during data collection by strobing the TIMEB pin. A dedicated flag in the sample status bits, TB, is set high to indicate during which measurement the timing event occurred.

General Purpose I/O (GPIO)

Eight general purpose pins are available on the CS5378 for system control. Each pin can be set as input or output, high or low, with an internal pull-up enabled or disabled. The CS3301A/02A and CS5373A devices in Figure 9 are configured by simple pin settings controlled through the CS5378 GPIO pins.

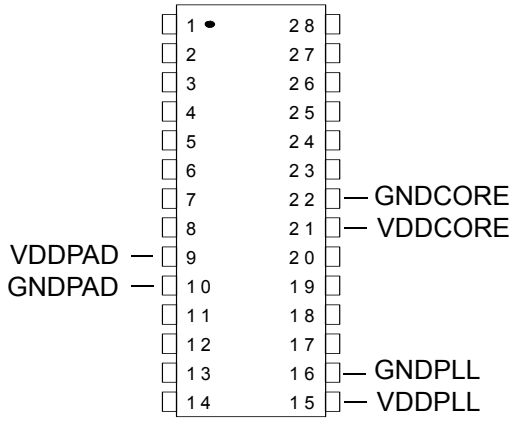


Figure 10. Power Supply Block Diagram

4. POWER SUPPLIES

The CS5378 has three sets of power supply inputs. One set supplies power to the I/O pins of the device (VDDPAD), another supplies power to the logic core (VDDCORE) and the third supplies power to the PLL (VDDPLL). The I/O pin power supplies determine the maximum input and output voltages when interfacing to peripherals, the logic core power supply largely determines the power consumption of the CS5378 and the PLL power supply powers the internal PLL circuitry.

4.1 Pin Descriptions

VDDPAD, GNDPAD - Pins 9, 10

Sets the interface voltage to a microcontroller, system telemetry, modulator, and test DAC. VDDPAD can be driven with voltages from 3.3 V to 5 V.

VDDPLL, GNDPLL - Pins 15, 16

Sets the operational voltage of the internal CS5378 PLL circuitry. Can be driven with voltages from 3.3 V to 5 V.

VDDCORE, GNDCORE - Pins 21, 22

Sets the operational voltage of the CS5378 logic core. VDDCORE can be driven with voltages from 2.5 V to 5 V. A 2.5 V supply will minimize total power consumption.

4.2 Bypass Capacitors

Each power supply pin should be bypassed with parallel 1 µF and 0.01 µF caps, or by a single 0.1 µF cap, placed as close as possible to the CS5378. Bypass capacitors should be ceramic (X7R, C0G), tantalum, or other good quality dielectric type.

4.3 Power Consumption

Power consumption of the CS5378 depends primarily on the power supply voltage of the logic core (VDDCORE) and the programmed digital filter clock rate. Digital filter clock rates are selected based on the required output word rate as explained in “Digital Filter Initialization” on page 38.

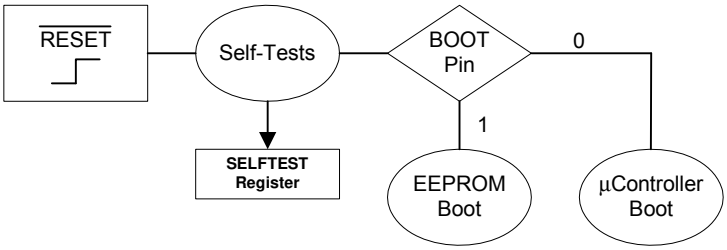


Figure 11. Reset Control Block Diagram

5. RESET CONTROL

The CS5378 reset signal is active low. When released, a series of self-tests are performed and the device either actively boots from an external EEPROM or enters an idle state waiting for microcontroller configuration.

5.1 Pin Descriptions

$\overline{RESET}$ - Pin 18

Reset input, active low.

GPIO7:BOOT - Pin 28

Boot mode select, latched immediately following reset. Weak (~100 kΩ) internal pull-up defaults high, external 10 kΩ pull-down required to set low.

BOOT	Reset Mode
1	EEPROM boot
0	Microcontroller boot

5.2 Reset Self-Tests

After $\overline{RESET}$ is released but before booting, a series of digital filter self-tests are run. Results are combined into the SELFTEST register (0x2F), with 0x0AAAAA indicating all passed. Self-tests require 60 ms to complete.

Self-Test Type	Pass Code	Fail Code
Program ROM	0x00000A	0x00000F
Data ROM	0x0000A0	0x0000F0
Program RAM	0x000A00	0x000F00
Data RAM	0x00A000	0x00F000
Execution Unit	0x0A0000	0x0F0000

5.3 Boot Configurations

The logic state of the BOOT pin after reset determines if the CS5378 actively reads configuration information from EEPROM or enters an idle state waiting for a microcontroller to write configuration commands.

EEPROM Boot

When the BOOT pin is high after reset, the CS5378 actively reads data from an external serial EEPROM and then begins operation in the specified configuration. Configuration commands and data are encoded in the EEPROM as specified in the 'Configuration By EEPROM' section of this data sheet, starting on page 25.

Microcontroller Boot

When the BOOT pin is low after reset, the CS5378 enters an idle state waiting for a microcontroller to write configuration commands and initialize filter operation. Configuration commands and data are written as specified in the 'Configuration By Microcontroller' section of this data sheet, starting on page 30.

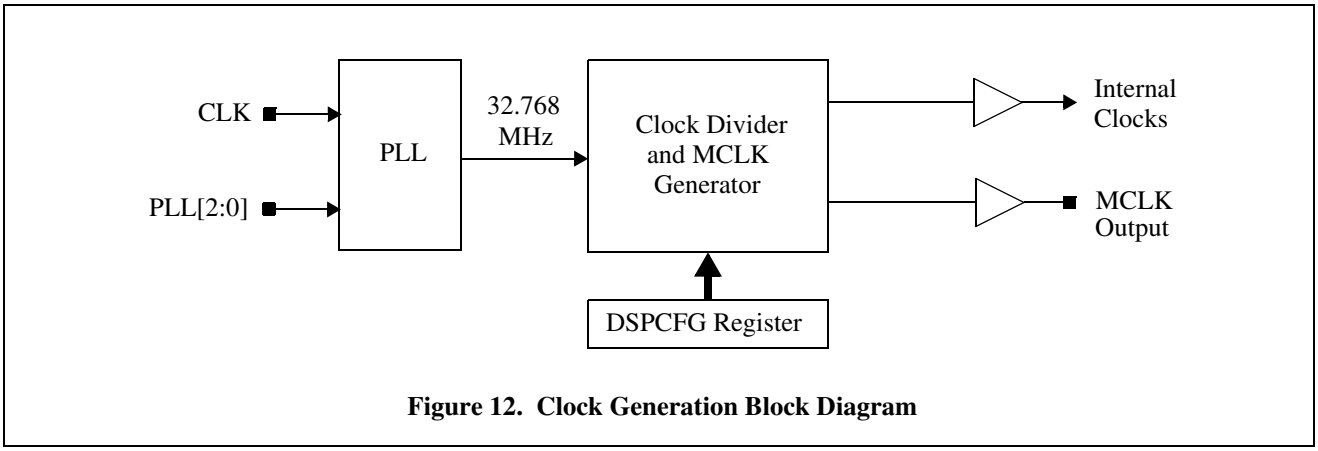


Figure 12. Clock Generation Block Diagram

6. PLL AND CLOCK GENERATION

The CS5378 requires a 32.768 MHz master clock, which can be supplied directly or from an internal phase locked loop. This master clock is used to generate an internal digital filter clock and an external modulator clock.

The internal PLL will lock to standard clock or Manchester encoded input signals. The input type and input frequency are selected by the reset state of the PLL mode select pins.

6.1 Pin Descriptions

CLK - Pin 17

Clock or PLL input, standard clock or Manchester.

GPIO[4:6]:PLL[0:2] - Pins 5, 6, 7

PLL mode select, latched immediately after reset. Weak (~100 kΩ) internal pull-ups default high, external 10 kΩ pull-downs required to set low.

6.2 PLL Mode Select

The CS5378 PLL operational mode and frequency are selected immediately after reset based on the state of the PLL[0:2] pins. On the rising edge of the reset signal, the digital high or low state of the PLL[0:2] pins is latched and used to program the clock input type and frequency.

A weak internal pull-up resistor (~100 kΩ) will hold the PLL mode select pins high by default. To force the pin low on reset, an external 10 kΩ pull-down resistor should be connected. Once the pin state is latched following reset, the GPIO[4:6] pins function without affecting PLL operation.

6.3 Synchronous Clocking

To guarantee synchronous measurements throughout a sensor network, a system clock should be distributed to arrive at all nodes in phase. The distributed system clock can either be the full 32.768 MHz master clock, or the CS5378 PLL can create a synchronous 32.768 MHz clock from a slower clock. To ensure the generated clock remains synchronous with the network, the CS5378 PLL uses a phase/frequency detector architecture.

PLL[2:0]	PLL Mode
111	32.768 MHz clock input (PLL bypass).
110	1.024 MHz clock input.
101	2.048 MHz clock input.
100	4.096 MHz clock input.
011	32.768 MHz clock input (PLL bypass).
010	1.024 MHz Manchester input.
001	2.048 MHz Manchester input.
000	4.096 MHz Manchester input.

Table 5. PLL Mode Selections

6.4 Master Clock Jitter and Skew

Care must be taken to minimize jitter and skew on the distributed system clock as both parameters affect measurement performance.

Jitter on the input clock causes jitter in the generated modulator clock, resulting in sample timing errors and increased noise.

Skew between input clocks from node to node creates a sample timing offset, resulting in systematic measurement errors in a reconstructed signal.

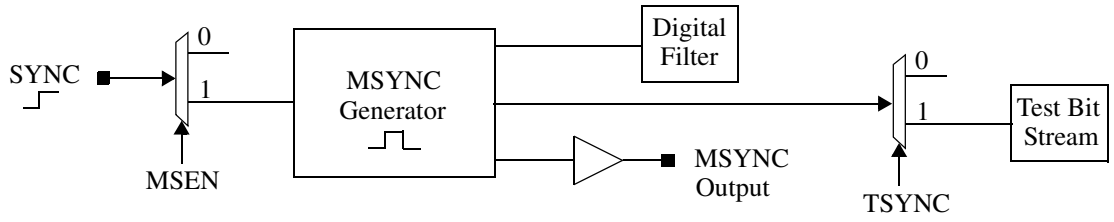


Figure 13. Synchronization Block Diagram

7. SYNCHRONIZATION

The CS5378 has a dedicated SYNC input that aligns the internal digital filter phase and generates an external signal for synchronizing modulator analog sampling. By providing simultaneous rising edges to the SYNC pins of multiple CS5378 devices, synchronous sampling across a network can be guaranteed.

7.1 Pin Description

SYNC - Pin 19

Synchronization input, rising edge triggered.

7.2 MSYNC Generation

The SYNC signal rising edge is used to generate a retimed synchronization signal, MSYNC. The MSYNC signal reinitializes internal digital filter phase and is driven onto the MSYNC output pin to phase align modulator analog sampling.

The MSEN bit in the digital filter CONFIG register (0x00) enables MSYNC generation. See "Modulator Interface" on page 36 for more information about MSYNC.

7.3 Digital Filter Synchronization

The internal MSYNC signal resets the digital filter state machine to establish a known digital filter phase. Filter convolutions restart, and the next output word is available one full sample period later.

Repetitive synchronization is supported when SYNC events occur at exactly the selected output rate. In this case, re-synchronization will occur at the start of a convolution cycle when the digital filter state machine is already reset.

7.4 Modulator Synchronization

The external MSYNC signal phase aligns modulator analog sampling when connected to the CS5373A MSYNC input. This ensures synchronous analog sampling relative to MCLK.

Repetitive synchronization of the modulators is supported when SYNC events occur at exactly the selected output rate. In this case, re-synchronization always occurs at the start of analog sampling.

7.5 Test Bit Stream Synchronization

When the test bit stream generator is enabled, an MSYNC signal can reset the internal data pointer. This restarts the test bit stream from the first data point to establish a known output signal phase.

The TSYNC bit in the digital filter TBSCFG register (0x2A) enables synchronization of the test bit stream by MSYNC. When TSYNC is disabled, the test bit stream phase is not affected by MSYNC.

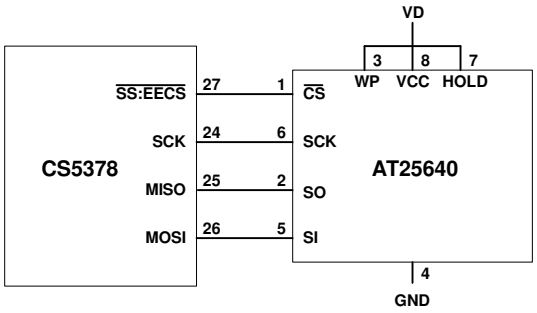


Figure 14. EEPROM Configuration Block Diagram

8. CONFIGURATION BY EEPROM

After reset, the CS5378 reads the state of the GPIO7:BOOT pin to determine a source for configuration commands. If BOOT is high, the CS5378 initiates serial transactions to read configuration information from an external EEPROM.

8.1 Pin Descriptions

Pins required for EEPROM boot are listed here, other serial pins are inactive.

SCK - Pin 24

Serial clock output, nominally 1.024 MHz.

MISO - Pin 25

Serial data input pin. Valid on rising edge of SCK, transition on falling edge.

MOSI - Pin 26

Serial data output pin. Valid on rising edge of SCK, transition on falling edge.

$\overline{\text{SS:EECS}}$ - Pin 27

EEPROM chip select output, active low.

8.2 EEPROM Hardware Interface

When booting from EEPROM the CS5378 actively performs serial transactions, as shown in Figure 15, to read configuration commands and data. 8-bit SPI opcodes and 16-bit addresses are combined to read back 8-bit configuration commands and 24-bit configuration data.

System design should include a connection to the configuration EEPROM for in-circuit reprogramming. The CS5378 serial pins tri-state when inactive to support external connections to the serial bus.

8.3 EEPROM Organization

The boot EEPROM holds the 8-bit commands and 24-bit data required to initialize the CS5378 into an operational state. Configuration information starts at memory location 0x10, with addresses 0x00 to 0x0F free for use as manufacturing header information.

The first serial transaction reads a 1-byte command from memory location 0x10 and then, depending on the command type, reads multiple 3-byte data words to complete the command. Command and data reads continue until the 'Filter Start' command is recognized.