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CS53L21

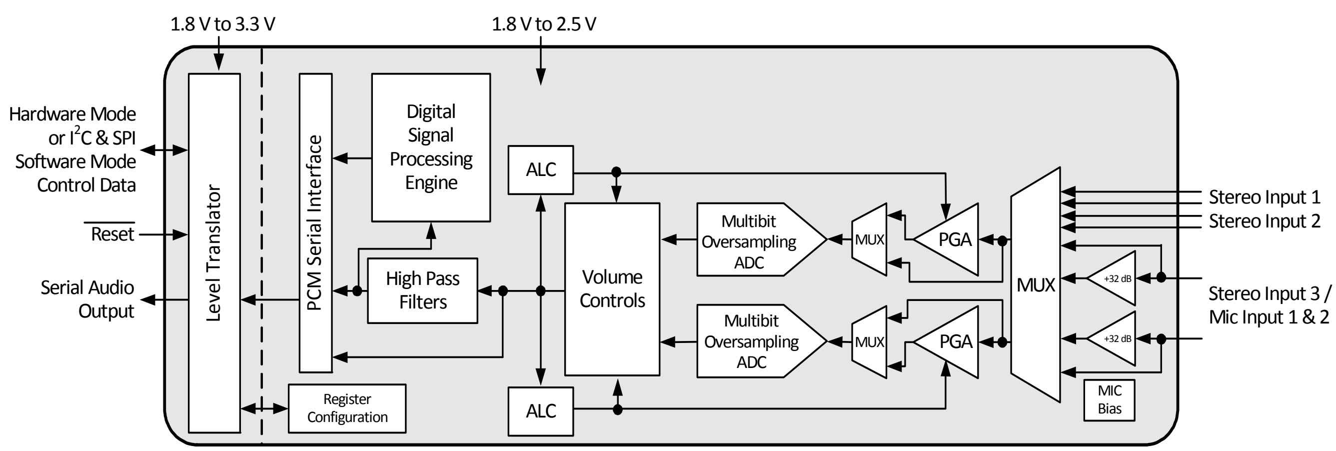
Low-Power, Stereo Analog-to-Digital Converter

FEATURES

- 98-dB dynamic range (A-weighted)
- –88-dB THD+N
- Analog gain controls
  - +32-dB or +16-dB mic preamps
  - Analog programmable gain amplifier (PGA)
- +20-dB digital boost
- Programmable automatic level control (ALC)
  - Noise gate for noise suppression
  - Programmable threshold and attack/release rates
- Independent left/right channel control
- Digital volume control
- High-pass filter disable for DC measurements
- Stereo 3:1 analog input MUX
- Dual mic inputs
  - Programmable, low noise mic bias levels
  - Differential mic mix for common mode noise rejection
- Very low 64 Fs oversampling clock reduces power consumption

SYSTEM FEATURES

- 24-bit conversion
- 4–96 kHz sample rate
- Multibit delta–sigma architecture
- Low power operation
  - Stereo record (ADC): 8.72 mW @ 1.8 V
  - Stereo record (mic to PGA and ADC): 13.73 mW @ 1.8 V
- Variable power supplies
  - 1.8–2.5-V digital and analog
  - 1.8–3.3-V interface logic
- Power down management
  - ADC, mic preamplifier, PGA
- Software Mode (I²C™ and SPI™ control)
- Hardware Mode (standalone control)
- Flexible clocking options
  - Master or slave operation
- Digital routing mixes
  - Mono mixes



APPLICATIONS

- Portable audio players
- Digital microphones
- Digital voice recorders
- Voice recognition systems
- Audio/video capture cards

GENERAL DESCRIPTION

The CS53L21 is a highly integrated, 24-bit, 96-kHz, low power stereo A/D. Based on multibit, delta–sigma modulation, it allows infinite sample rate adjustment between 4 kHz and 96 kHz. The ADC offers many features suitable for low power, portable system applications.

The ADC input path allows independent channel control of a number of features. An input multiplexer selects between line-level or microphone-level inputs for each channel. The microphone input path includes a selectable programmable-gain preamp stage and a low noise MIC bias voltage supply. A PGA is available for line or microphone inputs and provides analog gain with soft ramp and zero cross transitions. The ADC also features a digital volume attenuator with soft ramp transitions. A programmable ALC and Noise Gate monitor the input signals and adjust the volume levels appropriately.

The Signal Processing Engine (SPE) controls left/right channel volume mixing, channel swap and channel mute functions. All volume-level changes may be configured to occur on soft ramp and zero cross transitions.

The CS53L21 is available in a 32-pin QFN package in both Commercial (-10 to +70° C) and Automotive grades (-40 to +85° C). The CDB53L21 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please see “Ordering Information” on page 56 for complete details.

In addition to its many features, the CS53L21 operates from a low-voltage analog and digital core, making this A/D ideal for portable systems that require extremely low power consumption in a minimal amount of space.

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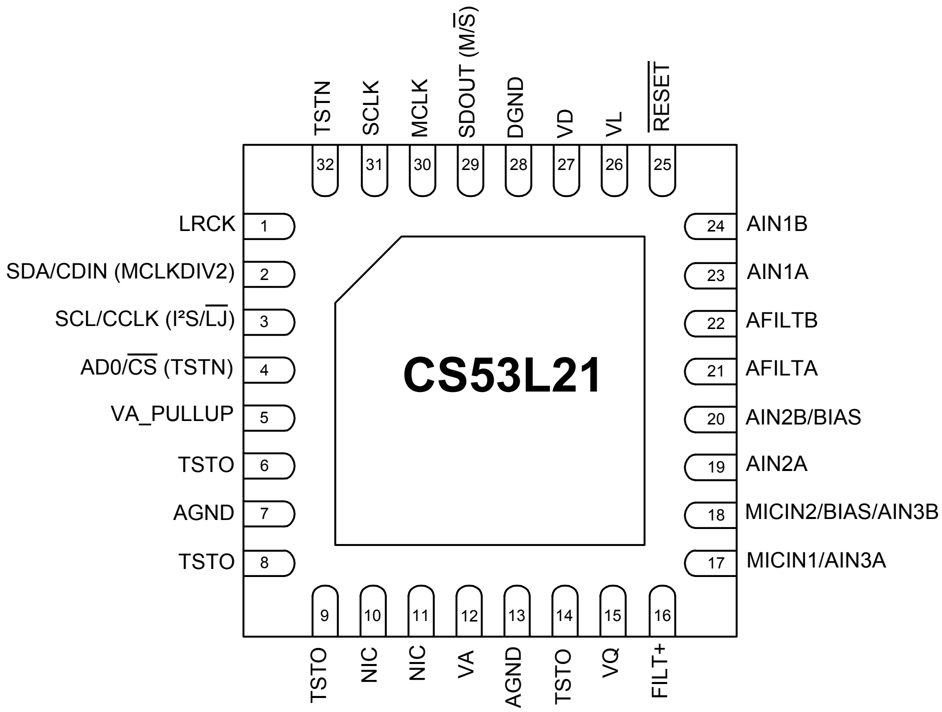
1. PIN DESCRIPTIONS - SOFTWARE (HARDWARE) MODE



Pin Name	#	Pin Description
LRCK	1	**Left Right Clock** (*Input/Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
SDA/CDIN (MCLKDIV2)	2	**Serial Control Data** (*Input/Output*) - SDA is a data I/O in I²C Mode. CDIN is the input data line for the control port interface in SPI Mode.
		MCLK Divide by 2 (*Input*) - Hardware Mode: Divides the MCLK by 2 prior to all internal circuitry.
SCL/CCLK (I²S/LJ)	3	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port.
		Interface Format Selection (*Input*) - Hardware Mode: Selects between I²S and left-Justified interface formats for the ADC.
AD0/CS (TSTN)	4	**Address Bit 0 (I²C) / Control Port Chip Select (SPI)** (*Input*) - AD0 is a chip address pin in I²C Mode; CS is the chip-select signal for SPI format.
		Test In (*Input*) - Hardware Mode: This pin is an input used for test purposes only and should be tied to DGND for normal operation.
VA_PULLUP	5	**Reference Pull-up** (*Input*) - This pin is an input used for test purposes only and must be pulled-up to VA using a 47 kΩ resistor.
TSTO	6	**Test Out** (*Output*) - This pin is an output used for test purposes only and must be left "floating" (no connection external to the pin).
AGND	7	**Analog Ground** (*Input*) - Ground reference for the internal analog section.
TSTO	8	**Test Out** (*Output*) - This pin is an output used for test purposes only and must be left "floating" (no connection external to the pin).

TSTO	9	**Test Out** (*Output*) - This pin is an output used for test purposes only and must be left “floating” (no connection external to the pin).
NIC NIC	10 11	.**Not Internally Connected** - This pin is not connected internal to the device and may be connected to ground or left “floating”. No other external connection should be made to this pin.
VA	12	**Analog Power** (*Input*) - Positive power for the internal analog section.
AGND	13	**Analog Ground** (*Input*) - Ground reference for the internal analog section.
TSTO	14	**Test Out** (*Output*) - This pin is an output used for test purposes only and must be left “floating” (no connection external to the pin).
VQ	15	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage.
FILT+	16	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits.
MICIN1/ AIN3A	17	**Microphone Input 1** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table.
MICIN2/ BIAS/AIN3B	18	**Microphone Input 2** (*Input/Output*) - The full-scale level is specified in the ADC Analog Characteristics specification table. This pin can also be configured as an output to provide a low noise bias supply for an external microphone. Electrical characteristics are specified in the DC Electrical Characteristics table.
AIN2A	19	**Analog Input** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table.
AIN2B/BIAS	20	**Analog Input** (*Input/Output*) - The full-scale level is specified in the ADC Analog Characteristics specification table. This pin can also be configured as an output to provide a low noise bias supply for an external microphone. Electrical characteristics are specified in the DC Electrical Characteristics table.
AFILTA AFILTB	21 22	**Filter Connection** (*Output*) - Filter connection for the ADC inputs.
AIN1A AIN1B	23 24	**Analog Input** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table.
$\overline{\text{RESET}}$	25	**Reset** (*Input*) - The device enters a low power mode when this pin is driven low.
VL	26	**Digital Interface Power** (*Input*) - Determines the required signal level for the serial audio interface and host control port. Refer to the Recommended Operating Conditions for appropriate voltages.
VD	27	**Digital Power** (*Input*) - Positive power for the internal digital section.
DGND	28	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
SDOUT (M/$\overline{\text{S}}$)	29	**Serial Audio Data Output** (*Output*) - Output for two’s complement serial audio data. **Serial Port Master/Slave** (*Input/Output*) - Hardware Mode Startup Option: Selects between Master and Slave Mode for the serial port.
MCLK	30	**Master Clock** (*Input*) - Clock source for the delta-sigma modulators.
SCLK	31	**Serial Clock** *(Input/Output)* -- Serial clock for the serial audio interface.
TSTN	32	**Test In** (*Input*) - This pin is an input used for test purposes only and should be tied to DGND for normal operation.
Thermal Pad	-	Thermal relief pad for optimized heat dissipation. See “QFN Thermal Pad” on page 53.

1.1 Digital I/O Pin Characteristics

The logic level for each input should not exceed the maximum ratings for the VL power supply.

Pin Name SW/(HW)	I/O	Driver	Receiver
$\overline{\text{RESET}}$	Input	-	1.8 V - 3.3 V
SCL/CCLK (I^2S/$\overline{\text{LJ}}$)	Input	-	1.8 V - 3.3 V, with Hysteresis
SDA/CDIN (MCLKDIV2)	Input/Output	1.8 V - 3.3 V, CMOS/Open Drain	1.8 V - 3.3 V, with Hysteresis
AD0/$\overline{\text{CS}}$ (DEM)	Input	-	1.8 V - 3.3 V
MCLK	Input	-	1.8 V - 3.3 V
LRCK	Input/Output	1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V
SCLK	Input/Output	1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V
SDOUT (M/$\overline{\text{S}}$)	Input/Output	1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V

Table 1. I/O Power Rails

2. TYPICAL CONNECTION DIAGRAMS

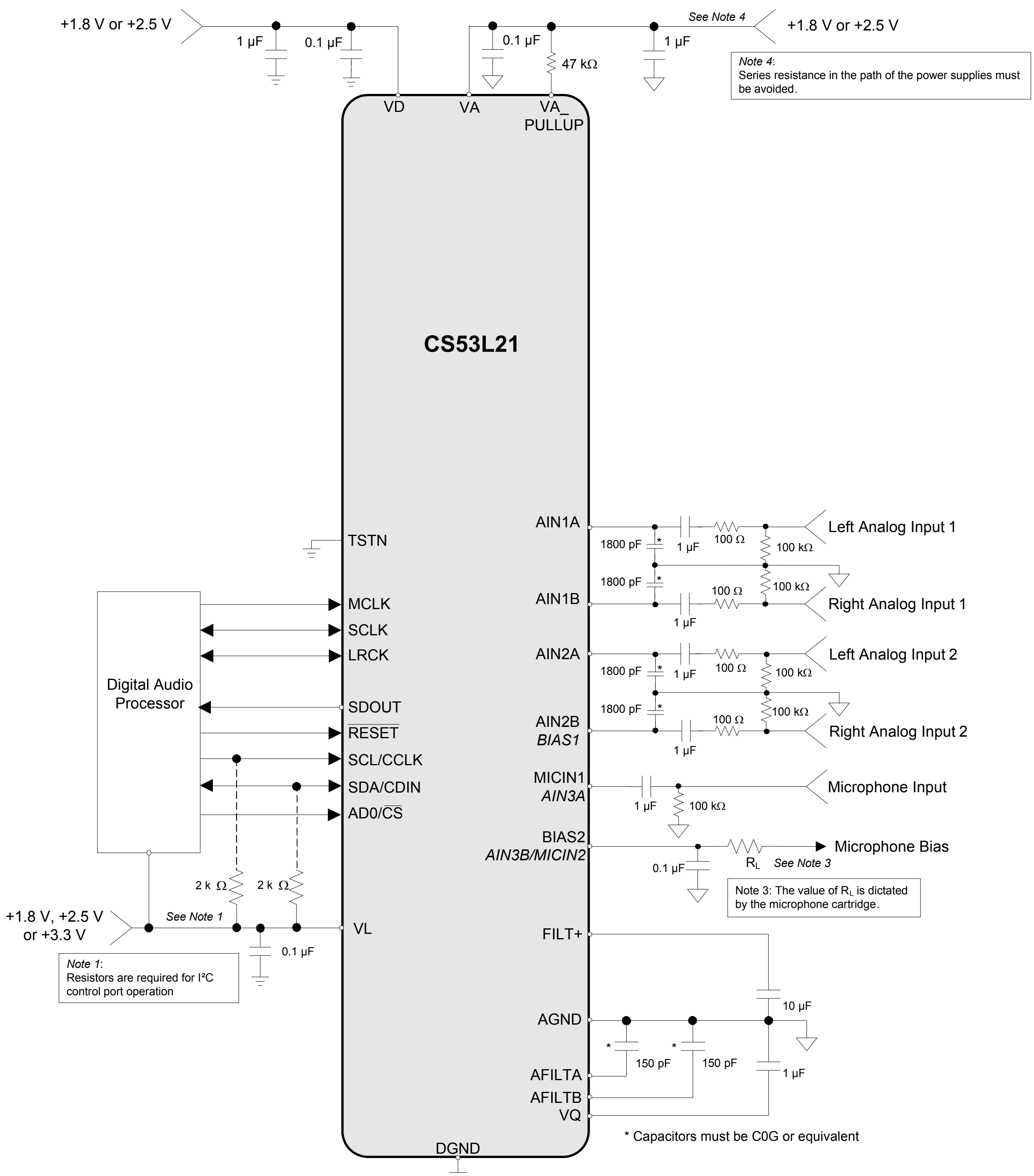


Figure 1. Typical Connection Diagram (Software Mode)

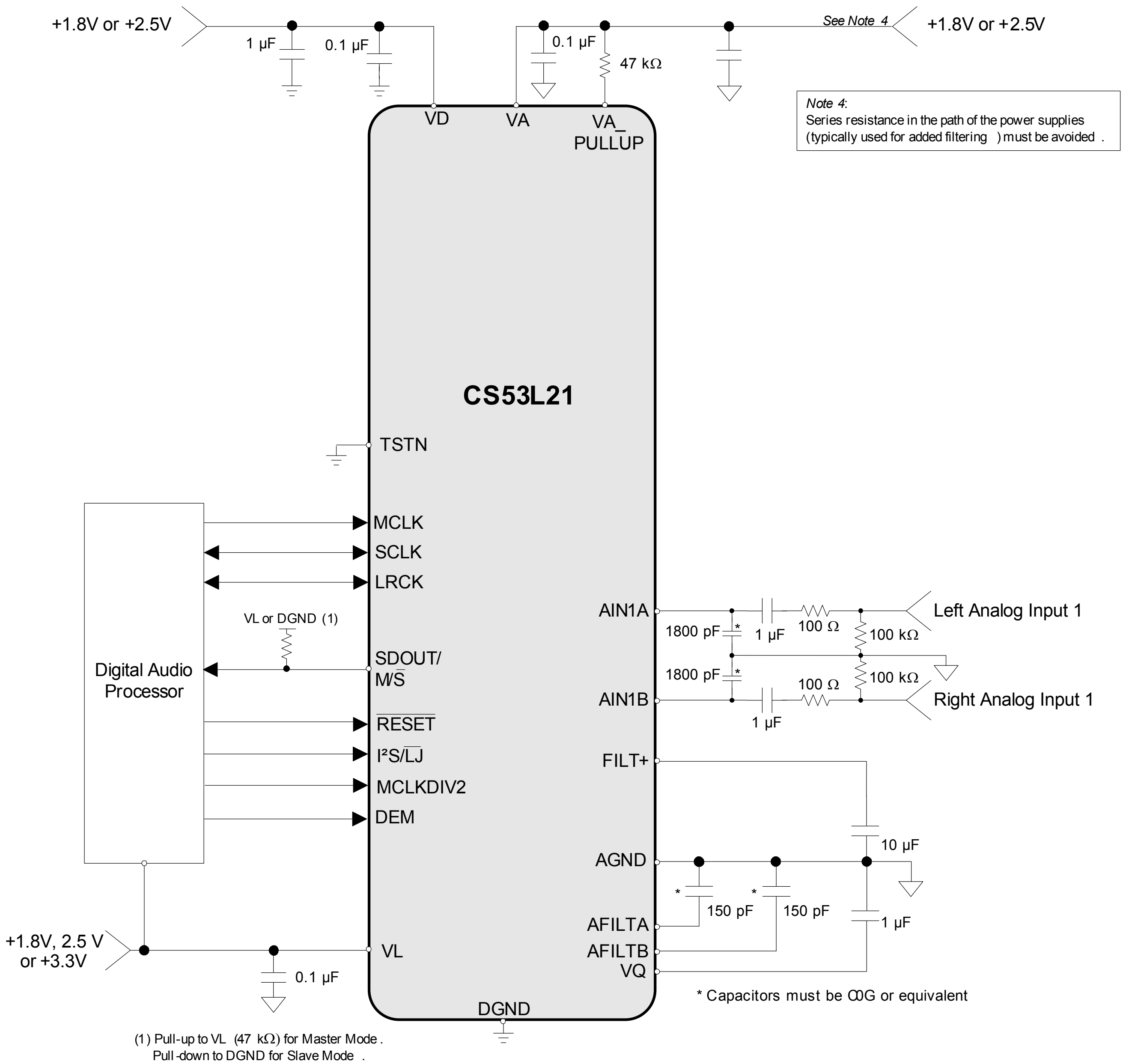


Figure 2. Typical Connection Diagram (Hardware Mode)

3. CHARACTERISTIC AND SPECIFICATION TABLES

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25° C.)

SPECIFIED OPERATING CONDITIONS

(AGND=DGND=0 V, all voltages with respect to ground.)

Parameters		Symbol	Min	Max	Units
DC Power Supply (Note 1)					
Analog Core		VA	1.65	2.63	V
Digital Core		VD	1.65	2.63	V
Serial/Control Port Interface		VL	1.65	3.47	V
Ambient Temperature	Commercial - CNZ Automotive - DNZ	T_A	-10 -40	+70 +85	°C °C

Note:

1. The device will operate properly over the full range of the analog, digital core and serial/control port interface supplies.

ABSOLUTE MAXIMUM RATINGS

(AGND = DGND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Max	Units
DC Power Supply	Analog Digital Serial/Control Port Interface	VA VD VL	-0.3 -0.3 -0.3	3.0 3.0 4.0	V V V
Input Current	(Note 2)	I_{in}	-	±10	mA
Analog Input Voltage	(Note 3)	V_{IN}	AGND-0.7	VA+0.7	V
Digital Input Voltage (Note 3)		V_{IND}	-0.3	VL+ 0.4	V
Ambient Operating Temperature (power applied)		T_A	-50	+115	°C
Storage Temperature		T_{stg}	-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:

2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.
3. The maximum over/under voltage is limited by the input current.

ANALOG CHARACTERISTICS (COMMERCIAL - CNZ)

(Test Conditions (unless otherwise specified): Input sine wave (relative to digital full scale): 1 kHz through passive input filter; Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. Sample Frequency = 48 kHz)

Parameter (Note 4)		VA = 2.5 V (nominal) Min	Typ	Max	VA = 1.8 V (nominal) Min	Typ	Max	Unit
Analog In to ADC (PGA bypassed)								
Dynamic Range	A-weighted	93	99	-	90	96	-	dB
	unweighted	90	96	-	87	93	-	dB
Total Harmonic Distortion + Noise	-1 dBFS	-	-86	-80	-	-84	-78	dB
	-20 dBFS	-	-76	-	-	-73	-	dB
	-60 dBFS	-	-36	-	-	-33	-	dB
Analog In to PGA to ADC								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	92	98	-	89	95	-	dB
	unweighted	89	95	-	86	92	-	dB
PGA Setting: +12 dB	A-weighted	85	91	-	82	88	-	dB
	unweighted	82	88	-	79	85	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-1 dBFS	-	-88	-81	-	-86	-80	dB
	-60 dBFS	-	-35	-	-	-32	-	dB
PGA Setting: +12 dB	-1 dBFS	-	-85	-79	-	-83	-77	dB
Analog In to MIC Pre-Amp (+16 dB) to PGA to ADC								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	-	86	-	-	83	-	dB
	unweighted	-	83	-	-	80	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-1 dBFS	-	-76	-	-	-74	-	dB
Analog In to MIC Pre-Amp (+32 dB) to PGA to ADC								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	-	78	-	-	75	-	dB
	unweighted	-	74	-	-	71	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-1 dBFS	-	-74	-	-	-71	-	dB
Other Characteristics								
DC Accuracy								
Interchannel Gain Mismatch		-	0.2	-	-	0.2	-	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Offset Error	SDOUT Code with HPF On	-	352	-	-	352	-	LSB
Input								
Interchannel Isolation		-	90	-	-	90	-	dB
Full-scale Input Voltage	ADC	0.74•VA	0.78•VA	0.82•VA	0.74•VA	0.78•VA	0.82•VA	Vpp
	PGA (0 dB)	0.75•VA	0.794•VA	0.83•VA	0.75•VA	0.794•VA	0.83•VA	Vpp
	MIC (+16 dB)		0.129•VA			0.129•VA		Vpp
	MIC (+32 dB)		0.022•VA			0.022•VA		Vpp
Input Impedance (Note 5)	ADC	-	20	-	-	20	-	kΩ
	PGA	-	39	-	-	39	-	kΩ
	MIC	-	50	-	-	50	-	kΩ

4. Referred to the typical full-scale voltage. Applies to all THD+N and Dynamic Range values in the table.
5. Measured between AINxx and AGND.

ANALOG CHARACTERISTICS (AUTOMOTIVE - DNZ)

(Test Conditions (unless otherwise specified): Input sine wave (relative to full scale): 1 kHz through passive input filter; Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. Sample Frequency = 48 kHz)

Parameter (Note 4)		VA = 2.5 V (nominal) Min	Typ	Max	VA = 1.8 V (nominal) Min	Typ	Max	Unit
Analog In to ADC								
Dynamic Range	A-weighted	91	99	-	88	96	-	dB
	unweighted	78	96	-	85	93	-	dB
Total Harmonic Distortion + Noise	-1 dBFS	-	-86	-78	-	-84	-76	dB
	-20 dBFS	-	-76	-	-	-73	-	dB
	-60 dBFS	-	-36	-	-	-33	-	dB
Analog In to PGA to ADC								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	90	98	-	87	95	-	dB
	unweighted	87	95	-	84	92	-	dB
PGA Setting: +12 dB	A-weighted	83	91	-	80	88	-	dB
	unweighted	80	88	-	77	85	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-1 dBFS	-	-88	-80	-	-86	-78	dB
	-60 dBFS	-	-35	-	-	-32	-	dB
PGA Setting: +12 dB	-1 dBFS	-	-85	-77	-	-83	-75	dB
Analog In to MIC Pre-Amp (+16 dB) to PGA to ADC								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	-	86	-	-	83	-	dB
	unweighted	-	83	-	-	80	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-1 dBFS	-	-76	-	-	-74	-	dB
Analog In to MIC Pre-Amp (+32 dB) to PGA to ADC								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	-	78	-	-	75	-	dB
	unweighted	-	74	-	-	71	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-1 dBFS	-	-74	-	-	-71	-	dB
Other Characteristics								
DC Accuracy								
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Offset Error	SDOUT Code with HPF On	-	352	-	-	352	-	LSB
Input								
Interchannel Isolation		-	90	-	-	90	-	dB
Full-scale Input Voltage	ADC	0.74•VA	0.78•VA	0.82•VA	0.74•VA	0.78•VA	0.82•VA	Vpp
	PGA (0 dB)	0.75•VA	0.794•VA	0.83•VA	0.75•VA	0.794•VA	0.83•VA	Vpp
	MIC (+16 dB)		0.129•VA			0.129•VA		Vpp
	MIC (+32 dB)		0.022•VA			0.022•VA		Vpp
Input Impedance (Note 5)	ADC	18	-	-	18	-	-	kΩ
	PGA	40	-	-	40	-	-	kΩ
	MIC	50	-	-	50	-	-	kΩ

ADC DIGITAL FILTER CHARACTERISTICS

Parameter (Note 6)		Min	Typ	Max	Unit
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.46	Fs
Passband Ripple		-0.09	-	0.17	dB
Stopband		0.6	-	-	Fs
Stopband Attenuation		33	-	-	dB
Total Group Delay		-	7.6/Fs	-	s
High-Pass Filter Characteristics (48 kHz Fs)					
Frequency Response	-3.0 dB -0.13 dB	- -	3.7 24.2	- -	Hz Hz
Phase Deviation	@ 20 Hz	-	10	-	Deg
Passband Ripple		-	-	0.17	dB
Filter Settling Time		-	10^5/Fs	0	s

6. Response is clock-dependent and will scale with Fs. Note that the response plots (Figures 23 to 26) have been normalized to Fs and can be denormalized by multiplying the X-axis scale by Fs. HPF parameters are for Fs = 48 kHz.

SWITCHING SPECIFICATIONS - SERIAL PORT

(Inputs: Logic 0 = DGND, Logic 1 = VL, SDOUT C_{LOAD} = 15 pF.)

Parameters		Symbol	Min	Max	Units
$\overline{\text{RESET}}$ pin Low Pulse Width	(Note 7)		1	-	ms
MCLK Frequency			1.024	38.4	MHz
MCLK Duty Cycle	(Note 8)		45	55	%
Slave Mode					
Input Sample Rate (LRCK)	Quarter-Speed Mode Half-Speed Mode Single-Speed Mode Double-Speed Mode	F_s F_s F_s F_s	4 8 4 50	12.5 25 50 100	kHz kHz kHz kHz
LRCK Duty Cycle			45	55	%
SCLK Frequency		$1/t_P$	-	$64 \cdot F_s$	Hz
SCLK Duty Cycle			45	55	%
LRCK Setup Time Before SCLK Rising Edge		$t_{s(LK-SK)}$	40	-	ns
LRCK Edge to SDOUT MSB Output Delay		$t_{d(MSB)}$	-	52	ns
SDOUT Setup Time Before SCLK Rising Edge		$t_{s(SDO-SK)}$	20	-	ns
SDOUT Hold Time After SCLK Rising Edge		$t_{h(SK-SDO)}$	30	-	ns

Parameters		Symbol	Min	Max	Units
Master Mode (Note 9)					
Output Sample Rate (LRCK)	All Speed Modes (Note 10)	F_s	-	$\frac{MCLK}{128}$	Hz
LRCK Duty Cycle			45	55	%
SCLK Frequency		$1/t_P$	-	$64 \cdot F_s$	Hz
SCLK Duty Cycle			45	55	%
LRCK Edge to SDOUT MSB Output Delay		$t_{d(MSB)}$	-	52	ns
SDOUT Setup Time Before SCLK Rising Edge		$t_{s(SDO-SK)}$	20	-	ns
SDOUT Hold Time After SCLK Rising Edge		$t_{h(SK-SDO)}$	30	-	ns

7. After powering up the CS53L21, $\overline{\text{RESET}}$ should be held low after the power supplies and clocks are settled.
8. See "Example System Clock Frequencies" on page 51 for typical MCLK frequencies.
9. See "Master" on page 29.
10. "MCLK" refers to the external master clock applied.

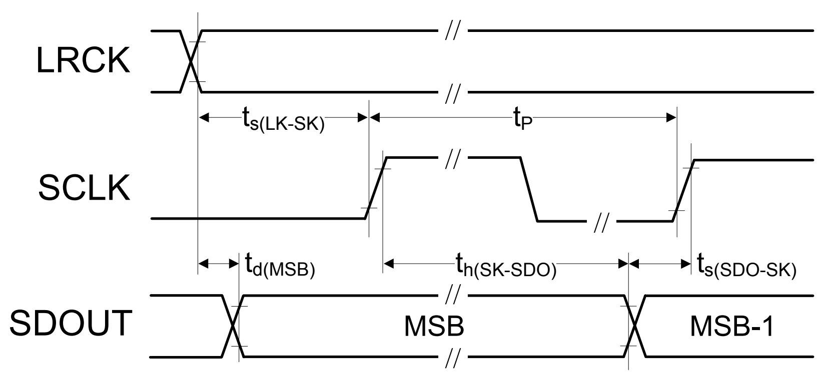


Figure 3. Serial Audio Interface Slave Mode Timing

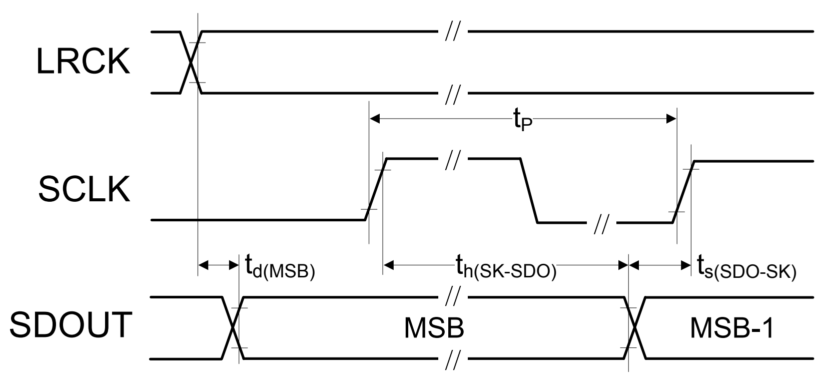


Figure 4. Serial Audio Interface Master Mode Timing

SWITCHING SPECIFICATIONS - I²C CONTROL PORT

(Inputs: Logic 0 = DGND, Logic 1 = VL, SDA C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{\text{RESET}}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 11)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}	-	1	µs
Fall Time SCL and SDA	t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	3450	ns

11. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

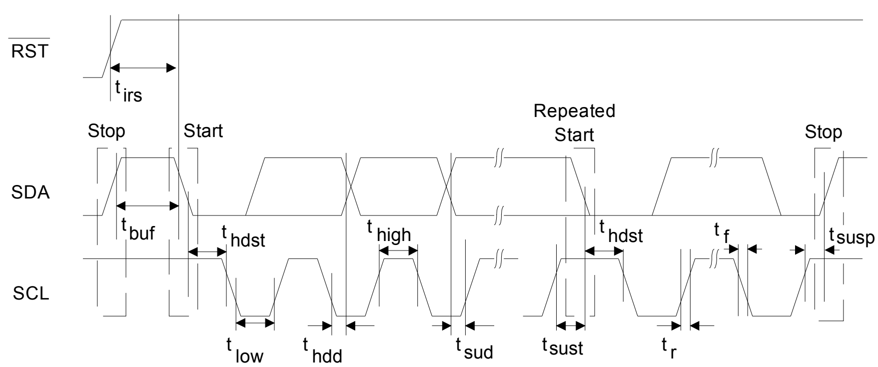


Figure 5. Control Port Timing - I²C

SWITCHING CHARACTERISTICS - SPI CONTROL PORT

(Inputs: Logic 0 = DGND, Logic 1 = VL)

Parameter	Symbol	Min	Max	Units
CCLK Clock Frequency	f_{sck}	0	6.0	MHz
RESET Rising Edge to CS Falling	t_{srs}	20	-	ns
CS Falling to CCLK Edge	t_{css}	20	-	ns
CS High Time Between Transmissions	t_{csh}	1.0	-	µs
CCLK Low Time	t_{scl}	66	-	ns
CCLK High Time	t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time	t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time (Note 12)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN (Note 13)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN (Note 13)	t_{f2}	-	100	ns

12. Data must be held for sufficient time to bridge the transition time of CCLK.
13. For f_{sck} <1 MHz.

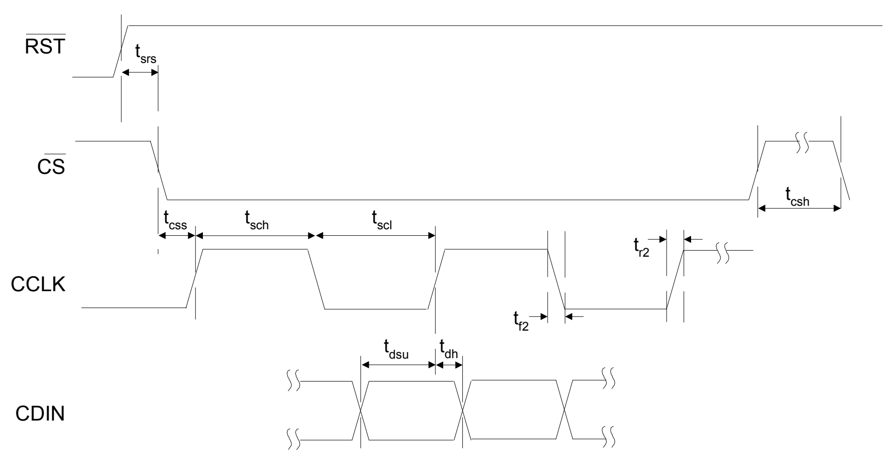


Figure 6. Control Port Timing - SPI Format

DC ELECTRICAL CHARACTERISTICS

(AGND = 0 V; all voltages with respect to ground.)

Parameters		Min	Typ	Max	Units
VQ Characteristics					
Nominal Voltage		-	0.5•VA	-	V
Output Impedance		-	23	-	kΩ
DC Current Source/Sink (Note 14)		-	-	10	µA
FILT+		-	VA	-	V
MIC BIAS Characteristics					
Nominal Voltage	MICBIAS_LVL[1:0] = 00	-	0.8•VA	-	V
	MICBIAS_LVL[1:0] = 01	-	0.7•VA	-	V
	MICBIAS_LVL[1:0] = 10	-	0.6•VA	-	V
	MICBIAS_LVL[1:0] = 11	-	0.5•VA	-	V
DC Current Source		-	-	1	mA
Power Supply Rejection Ratio (PSRR)	1 kHz	-	50	-	dB
Power Consumption (Normal Operation Worse Case)	1 kHz	-	-	30	mW
Power Supply Rejection Ratio (PSRR) (Note 15)	1 kHz	-	60	-	dB

14. The DC current draw represents the allowed current draw from the VQ pin due to typical leakage through electrolytic de-coupling capacitors.
15. Valid with the recommended capacitor values on FILT+ and VQ. Increasing the capacitance will also increase the PSRR.

DIGITAL INTERFACE SPECIFICATIONS AND CHARACTERISTICS

Parameters (Note 16)	Symbol	Min	Max	Units
Input Leakage Current	I_{in}	-	±10	µA
Input Capacitance		-	10	pF
1.8 V - 3.3 V Logic				
High-Level Output Voltage (I_{OH} = -100 µA)	V_{OH}	VL - 0.2	-	V
Low-Level Output Voltage (I_{OL} = 100 µA)	V_{OL}	-	0.2	V
High-Level Input Voltage	V_{IH}	0.68•VL	-	V
Low-Level Input Voltage	V_{IL}	-	0.32•VL	V

16. See “Digital I/O Pin Characteristics” on page 8 for serial and control port power rails.

POWER CONSUMPTION

See (Note 17)

	Operation	Power Control. Registers 02h: Reserved bit 6	02h: Reserved bit 5	02h: PDN_PGAB	02h: PDN_PGAA	02h: PDN_ADCB	02h: PDN_ADCA	02h: PDN	03h: PDN_MICB	03h: PDN_MICA	03h: PDN_MICBIAS	V	Typical Current (mA)	i_{VA}	i_{VD}	i_{VL} (Note 18)	Total Power (mW_{rms})
1	Off (Note 19)	x	x	x	x	x	x	x	x	x	x	1.8		0	0	0	0
												2.5		0	0	0	0
2	Standby (Note 20)	x	x	x	x	x	x	1	x	x	x	1.8		0.01	0.02	0	0.05
												2.5		0.01	0.03	0	0.10
3	Mono Record ADC	1	1	1	1	1	0	0	1	1	1	1.8		1.85	2.03	0.03	7.05
												2.5		2.07	3.05	0.05	12.94
	PGA to ADC	1	1	1	0	1	0	0	1	1	1	1.8		2.35	2.03	0.03	7.95
												2.5		2.58	3.08	0.05	14.29
	MIC to PGA to ADC (with Bias)	1	1	1	0	1	0	0	1	0	0	1.8		3.67	2.05	0.03	10.36
												2.5		3.95	3.09	0.05	17.71
	MIC to PGA to ADC (no Bias)	1	1	1	0	1	0	0	1	0	1	1.8		3.27	2.03	0.03	9.61
												2.5		3.52	3.08	0.05	16.62
4	Stereo Record ADC	1	1	1	1	0	0	0	1	1	1	1.8		2.69	2.12	0.03	8.72
												2.5		2.93	3.18	0.04	15.40
	PGA to ADC	1	1	0	0	0	0	0	1	1	1	1.8		3.65	2.12	0.03	10.45
												2.5		3.91	3.17	0.04	17.84
	MIC to PGA to ADC (no Bias)	1	1	0	0	0	0	0	0	0	1	1.8		5.48	2.11	0.03	13.73
												2.5		5.76	3.17	0.04	22.45

17. Unless otherwise noted, test conditions are as follows: All zeros input, slave mode, sample rate = 48 kHz; No load. Digital (VD) and logic (VL) supply current will vary depending on speed mode and master/slave operation.
18. VL current will slightly increase in master mode.
19. $\overline{\text{RESET}}$ pin 25 held LO, all clocks and data lines are held LO.
20. $\overline{\text{RESET}}$ pin 25 held HI, all clocks and data lines are held HI.

4. APPLICATIONS

4.1 Overview

4.1.1 Architecture

The CS53L21 is a highly integrated, low power, 24-bit audio A/D. The ADC operates at 64Fs, where Fs is equal to the system sample rate. The different clock rates maximize power savings while maintaining high performance. The A/D operates in one of four sample rate speed modes: Quarter, Half, Single and Double. It accepts and is capable of generating serial port clocks (SCLK, LRCK) derived from an input Master Clock (MCLK).

4.1.2 Line and MIC Inputs

The analog input portion of the A/D allows selection from and configuration of multiple combinations of stereo and microphone (MIC) sources. Six line inputs with configuration for two MIC inputs (or one MIC input with common mode rejection), two MIC bias outputs and independent channel control (including a high-pass filter disable function) are available. A Programmable Gain Amplifier (PGA), MIC boost, and Automatic Level Control (ALC), with noise gate settings, provide analog gain and adjustment. Digital volume controls, including gain, boost, attenuation and inversion are also available.

4.1.3 Signal Processing Engine

The ADC data has independent volume controls and mixing functions such as mono mixes and left/right channel swaps.

4.1.4 Device Control (Hardware or Software Mode)

In Software Mode, all functions and features may be controlled via a two-wire I²C or three-wire SPI control port interface. In Hardware Mode, a limited feature set may be controlled via stand-alone control pins.

4.1.5 Power Management

Two Software Mode control registers provide independent power-down control of the ADC, PGA, MIC preamp and MIC bias, allowing operation in select applications with minimal power consumption.

4.2 Hardware Mode

A limited feature set is available when the A/D powers up in Hardware Mode (see "Recommended Power-Up Sequence" on page 30) and may be controlled via stand-alone control pins. Table 2 shows a list of functions/features, the default configuration and the associated stand-alone control available.

Hardware Mode Feature/Function Summary				
Feature/Function		**Default Configuration**	**Stand-Alone Control**	**Note**
Power Control	Device PGAx ADCx MIC Bias MICx Preamp	Powered Up Powered Up Powered Up Powered Down Powered Down	-	-
Auto-Detect		Enabled	-	-
Speed Mode	Serial Port Slave Serial Port Master	Auto-Detect Speed Mode Single-Speed Mode	-	-
MCLK Divide		(Selectable)	"MCLKDIV2" pin 2	see Section 4.5 on page 28
Serial Port Master / Slave Selection		(Selectable)	"M/$\overline{\text{S}}$" pin 29	see Section 4.5 on page 28
Interface Control	ADC	(Selectable)	"I²S/$\overline{\text{LJ}}$" pin 3	see Section 4.6 on page 30
ADC Volume and Gain	Digital Boost Soft Ramp Zero Cross Invert PGAx Attenuator ALC Noise Gate	Disabled Disabled Disabled Disabled 0 dB 0 dB Disabled Disabled	-	-
ADCx High-Pass Filter ADCx High-Pass Filter Freeze		Enabled Continuous DC Subtraction	-	-
Line/MIC Input Select		AIN1A to PGAA AIN1B to PGAB	-	-
ADC mix Volume and Gain	Invert Soft Ramp Zero Cross	Disabled Enabled Enabled	-	-
Signal Processing Engine (SPE)	MIX	Disabled	-	-
Data Selection (SPE Enable)		ADC Data to SPE	-	-
Channel Swap	ADC	ADCA = L; ADCB = R	-	-

Table 2. Hardware Mode Feature Summary

4.3 Analog Inputs

AINxA and AINxB are the analog inputs, internally biased to VQ, that accepts line-level and MIC-level signals, allowing various gain and signal adjustments for each channel.

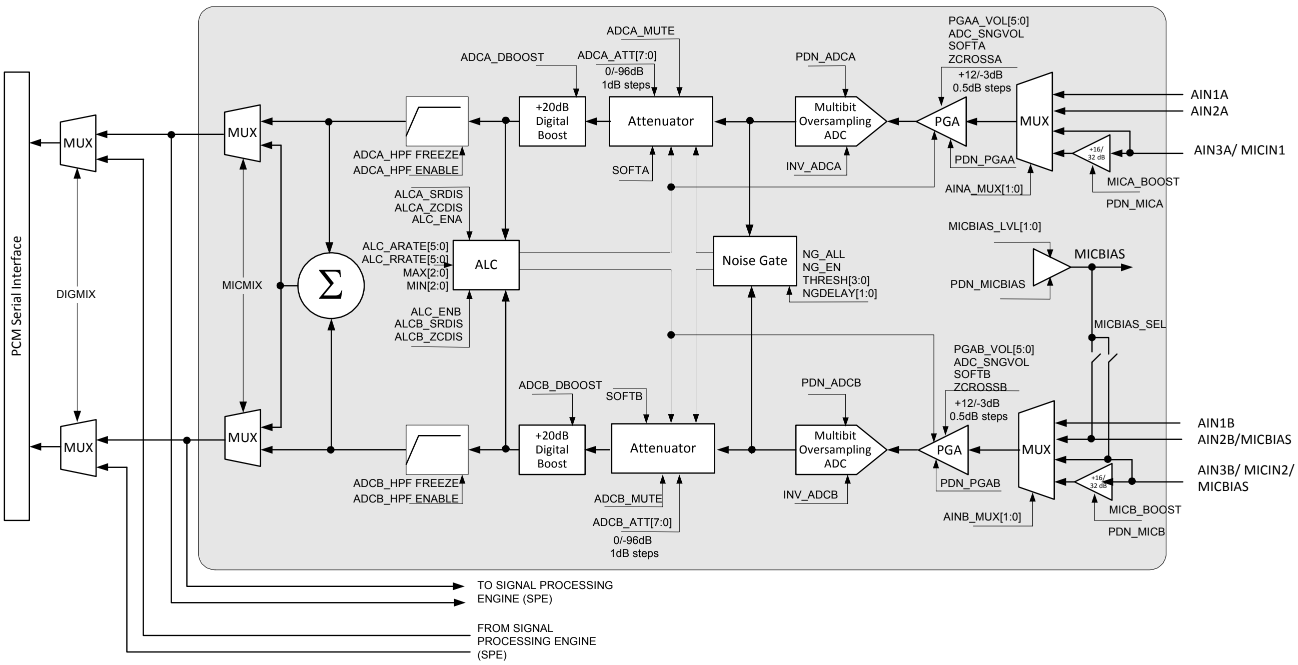


Figure 7. Analog Input Architecture

4.3.1 Digital Code, Offset and DC Measurement

The ADC output data is in two's complement binary format. For inputs above positive full scale or below negative full scale, the ADC will output 7FFFFFH or 800000H, respectively and cause the ADC overflow bit to be set to a '1'.

Given the two's complement format, low-level signals may cause the MSB of the serial data to periodically toggle between '1' and '0', possibly introducing noise into the system as the bit switches back and forth. To prevent this phenomena, a constant DC offset is added to the serial data bringing the low-level signal just above the point at which the MSB would normally toggle, thus reducing the noise introduced. Note that this offset is not removed (refer to "Analog Characteristics (Commercial - CNZ)" on page 12 and/or "Analog Characteristics (Automotive - DNZ)" on page 13 for the specified offset level).

The A/D may be used to measure DC voltages by disabling the high-pass filter for the designated channel. DC levels are measured relative to VQ and will be decoded as positive two's complement binary numbers above VQ and negative two's complement binary numbers below VQ.

Software Controls:	"Status (Address 20h) (Read Only)" on page 50, "ADC Control (Address 06h)" on page 41.

4.3.2 High-Pass Filter and DC Offset Calibration

The high-pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. If the high-pass filter is “frozen” during normal operation, the current value of the DC offset for the corresponding channel is held. It is this DC offset that will continue to be subtracted from the conversion result. This feature makes it possible to perform a system DC offset calibration by:

1. Running the A/D with the high-pass filter enabled and the DC offset not “frozen” until the filter settles. See the Digital Filter Characteristics for filter settling time.
2. Freezing the DC offset.

The high-pass filters are controlled using the ADCx_HPFRZ and ADCx_HPFEN bits.

If a particular ADC channel is used to measure DC voltages, the high-pass filter may be disabled using the ADCx_HPFEN bit.

Software Controls:	“ADC Control (Address 06h)” on page 41.

4.3.3 Digital Routing

The digital output of the ADC may be internally routed to the Signal Processing Engine (SPE). ADC output volume may be controlled using the ADCMIX [6:0] bits, and channel swaps can be done using the ADCA[1:0] and ADCB[1:0] bits. This “processed” ADC data can be selected for output in place of the ADC output data using the DIGMIX bit.

Software Controls:	“ADCx Mixer Volume Control: ADCA (Address 0Eh) and ADCB (Address 0Fh)” on page 46, “Interface Control (Address 04h)” on page 39.

4.3.4 Differential Inputs

The stereo pair inputs act as a single differential input when the MICMIX bit is enabled. This provides common mode rejection of noise in digitally intense PCBs, where the microphone signal traverses long traces, or across long microphone cables as illustrated in Figure 8.

Since the mixer provides a differential combination of the two signals, the potential input mix may exceed the maximum full-scale input and result in clipping. The level out of the mixer, therefore, is automatically attenuated 6 dB. Gain may be applied using either the analog PGA or MIC preamp or the digital ADCMIX volume control to readjust a small signal to desired levels.

The analog inputs may also be used as a differential input pair as illustrated in Figure 9. The two channels are differentially combined when the MICMIX bit is enabled.

4.3.4.1 External Passive Components

The microphone input is internally biased to VQ. Input signals must be AC coupled using external capacitors with values consistent with the desired high-pass filter design. The MICINx input resistance of 50 kW may be combined with an external capacitor of 1 mF to achieve the cutoff frequency defined by the equation,

$$fc = \frac{1}{2\pi(50\ k\Omega)(1\ \mu F)} = 3.18\ Hz$$

An electrolytic capacitor must be placed such that the positive terminal is positioned relative to the side with the greater bias voltage. The MICBIAS voltage level is controlled by the MICBIAS_LVL[1:0] bits.

The MICBIAS series resistor must be selected based on the requirements of the particular microphone used. The MICBIAS output pin is selected using the MICBIAS_SEL bit.

Software Controls:	"Interface Control (Address 04h)" on page 39, "MIC Control (Address 05h)" on page 40.

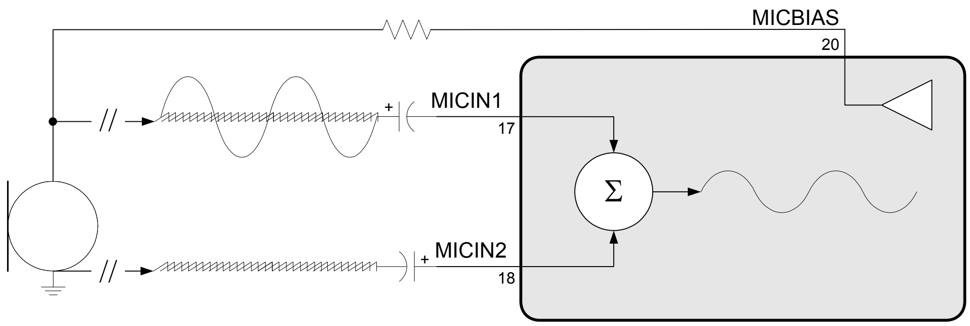


Figure 8. MIC Input Mix w/Common Mode Rejection

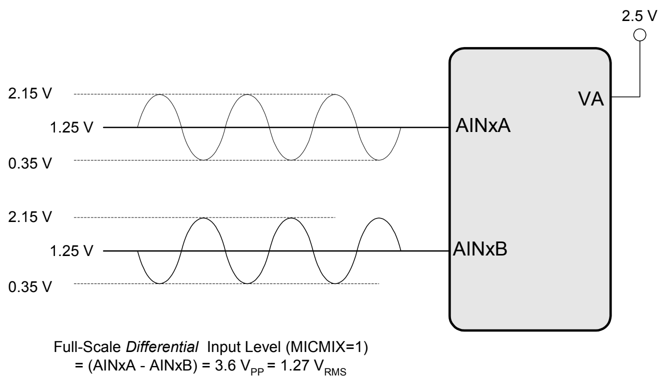


Figure 9. Differential Input

4.3.5 Analog Input Multiplexer

A stereo 4-to-1 analog input multiplexer selects between a line-level input source, or a mic-level input source, depending on the PDN_PGAx and AINx_MUX[1:0] bit settings. Signals may be routed to or bypassed around the PGA. To conserve power, the PGAs may be powered down allowing the user to select from multiple line-level sources and route the stereo signal directly to the ADC. When using the MIC preamp, however, the PGA must be powered up.

Analog input channel B may also be used as an output for the MIC bias voltage. The MICBIAS_SEL bit routes the bias voltage to either of two pins. The multiplexer must then select from the remainder of the two input channels.

Each ADC, PGA and MIC preamp has an associated input resistance. When selecting between these paths, the input resistance to the A/D will change accordingly. Refer to the input resistance characteristics in the Characteristic and Specification Tables for the input resistance of each path.

Software Controls:	"Power Control 1 (Address 02h)" on page 36, "MIC Control (Address 05h)" on page 40 "ADCx Input Select, Invert and Mute (Address 07h)" on page 42.

4.3.6 MIC and PGA Gain

The MIC-level input passes through a +16 dB or +32 dB analog gain stage prior to the input multiplexer, allowing it to be used for microphone level signals without the need for any external gain. The PGA must be powered up when using the MIC preamp.

The PGA stage provides an additional +12 dB to -3 dB of analog gain in 0.5 dB steps.

Software Controls:	"Power Control 1 (Address 02h)" on page 36, "ADCx Input Select, Invert and Mute (Address 07h)" on page 42, "ALCX and PGAX Control: ALCA, PGAA (Address 0Ah) and ALCB, PGAB (Address 0Bh)" on page 45, "MIC Control (Address 05h)" on page 40.

4.3.7 Automatic Level Control (ALC)

When enabled, the ALC monitors the analog input signal after the digital attenuator, detects when peak levels exceed the maximum threshold settings and lowers, first, the PGA gain settings and then increases the digital attenuation levels at a programmable attack rate and maintains the resulting level below the maximum threshold.

When input signal levels fall below the minimum threshold, digital attenuation levels are decreased first and the PGA gain is then increased at a programmable release rate and maintains the resulting level above the minimum threshold.

Attack and release rates are affected by the ADC soft ramp/zero cross settings and sample rate, Fs. ALC soft ramp and zero cross dependency may be independently enabled/disabled.

Recommended settings: Best level control may be realized with the fastest attack and slowest release setting with soft ramp enabled in the control registers. **Note: 1.)** The maximum realized gain must be set in the PGAx_VOL register. The ALC will only apply the gain set in the PGAx_VOL. **2.)** The ALC maintains the output signal between the MIN and MAX thresholds. As the input signal level changes, the level-controlled output may not always be the same but will always fall within the thresholds.

Software Controls:	"ALC Enable and Attack Rate (Address 1Ch)" on page 47, "ALC Release Rate (Address 1Dh)" on page 48, "ALC Threshold (Address 1Eh)" on page 48, "ALCX and PGAX Control: ALCA, PGAA (Address 0Ah) and ALCB, PGAB (Address 0Bh)" on page 45.

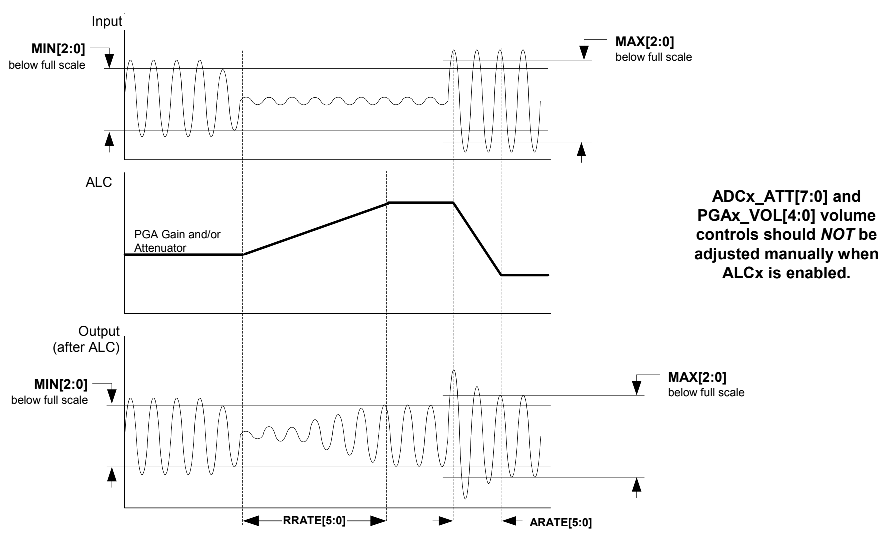


Figure 10. ALC