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CS53L30

Low-Power Quad-Channel Microphone ADC with TDM Output

Analog Input and ADC Features

- 91-dB dynamic range (A-weighted) @ 0-dB gain
- –84-dB THD+N @ 0-dB gain
- Four fully differential inputs: Four analog mic/line inputs
- Four analog programmable gain amplifiers
  - –6 to +12 dB, in 0.5-dB steps
  - +10 or +20 dB boost for mic input
- Four mic bias generators
- MUTE pin for quick mic mute and programmable quick power down

Digital Processing Features

- Volume control, mute, programmable high-pass filter, noise gate
- Two digital mic (DMIC) interfaces

Digital Output Features

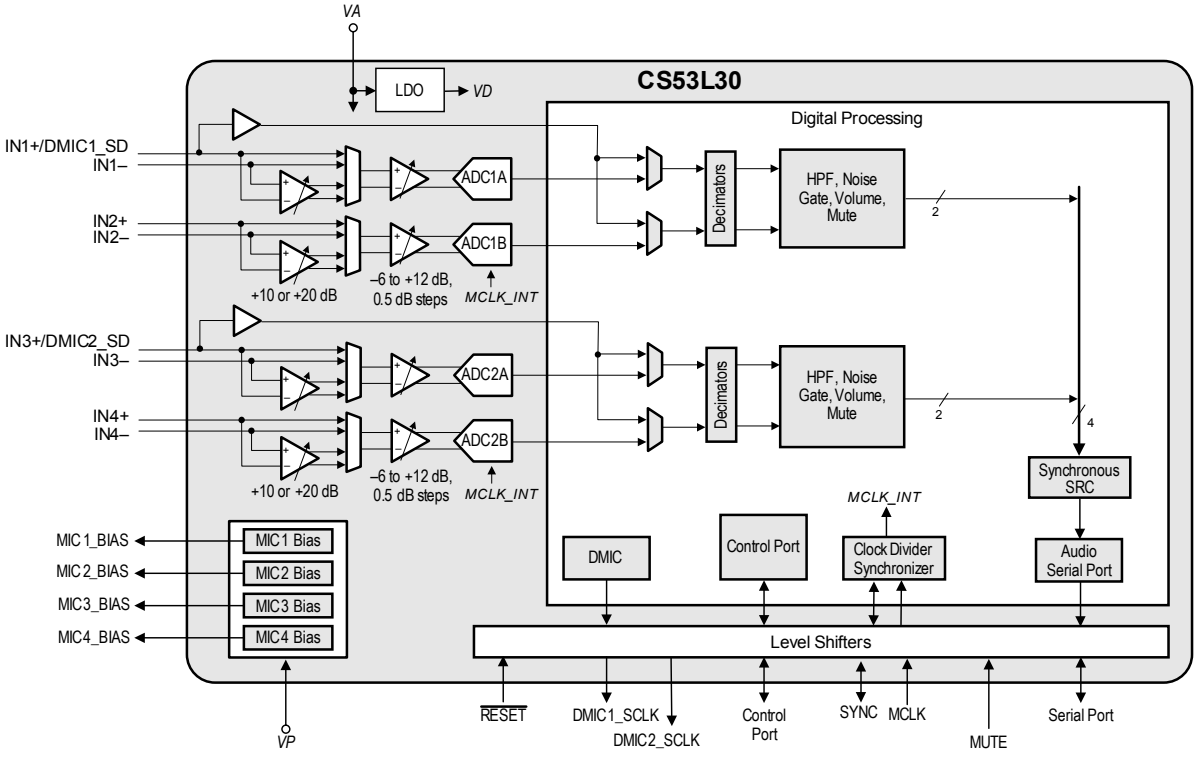
- Two DMIC SCLK generators
- Four-channel I²S output or TDM output. Four CS53L30s can be used to output 16 channels of 24-bit 16-kHz sample rate data on a single TDM line.

System Features

- Native (no PLL required) support for 6-/12-MHz, 6.144-/12.288-MHz, 5.6448-/11.2896-MHz, or 19.2-MHz master clock rates and 8- to 48-kHz audio sample rates
- Master or Slave Mode. Clock dividers can be used to generate common audio clocks from single-master clock input.
- Low power consumption
  - Less than 4.5-mW stereo (16 kHz) analog mic record
  - Less than 2.5-mW mono (8 kHz) analog mic record
- Selectable mic bias and digital interface logic voltages
- High-speed (400-kHz) I²C control port
- Available in 30-ball WLCSP and 32-pin QFN

Applications

- Voice-recognition systems
- Advanced headsets and telephony systems
- Voice recorders
- Digital cameras and video cameras



General Description

The CS53L30 is a high-performance, low-power, quad-channel ADC. It is designed for use in multiple-mic applications while consuming minimal board space and power.

The flexible ADC inputs can accommodate four channels of analog mic or line-input data in differential, pseudodifferential, or single-ended mode, or four channels of digital mic data. The analog input path includes a +10- to +20-dB boost and a –6- to +12-dB PGA. Digital mic data bypasses the analog gain circuits and is fed directly to the decimators.

Four mic bias generators are integrated into the device. The device also includes two digital mic serial clock outputs.

The CS53L30 includes several digital signal processing features such as high-pass filters, noise gate, and volume control.

The device can output its four channels of audio data over two I^2S ports or a single TDM port. Additionally, up to four CS53L30s can be used to output up to 16 channels of data over a single TDM line. This is done by setting the appropriate frame slots for each device, and each device then alternates between outputting data and setting the output pin to high impedance.

The CS53L30 can operate as a serial port clock master or slave. In Master Mode, clock dividers are used to generate the internal master clock and audio clocks from either the 6-/12-MHz, 6.144-/12.288-MHz, 5.6448-/11.2896-MHz, or 19.2-MHz master clock.

The device is powered from VA, a 1.8-V nominal supply and VP, a typical battery supply. An internal LDO on the VA supply powers the device's digital core. The VP supply powers the mic bias generators and the AFE.

The CS53L30 is controlled by an I^2C control port. A reset pin is also included. The device is available in a 30-ball 0.4-mm pitch WLCSP package and 32-pin 5 x 5-mm QFN package.

Table of Contents

1 Pin Descriptions

1.1 WLCSP

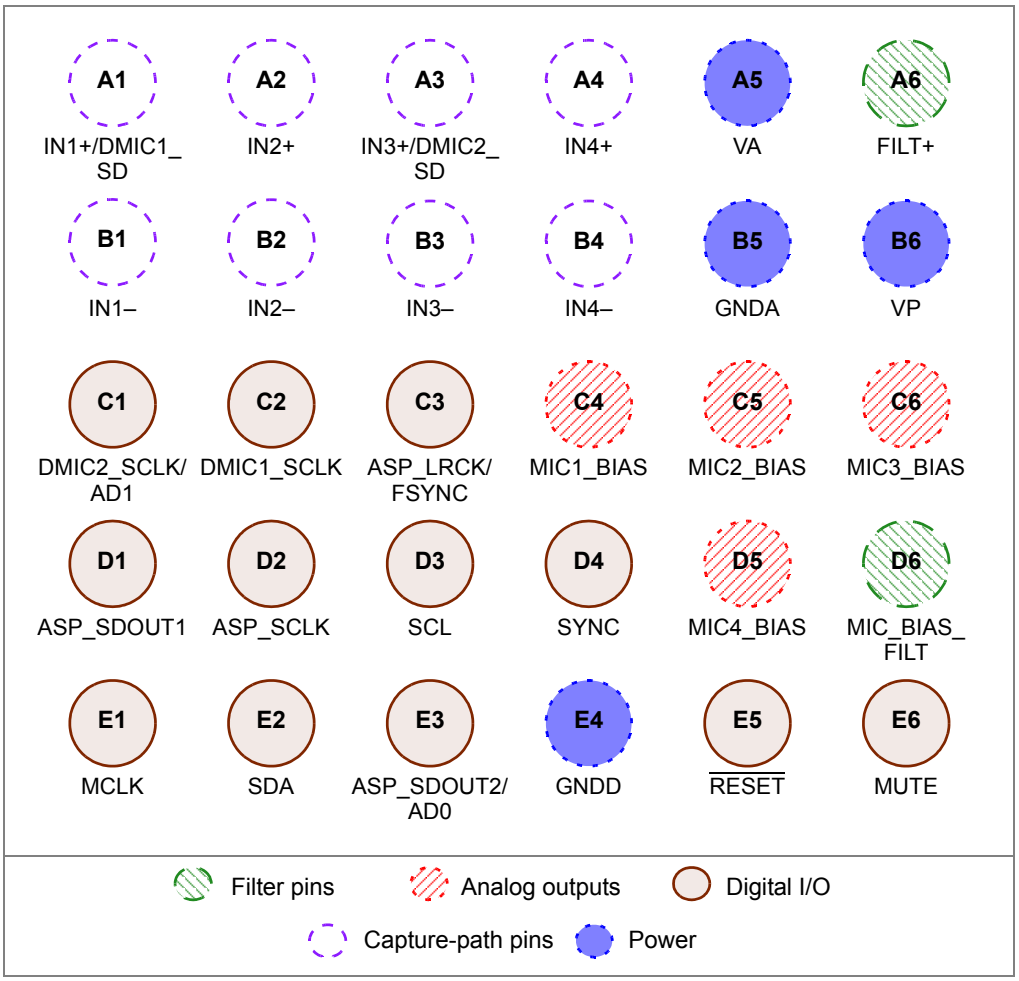


Figure 1-1. Top-Down (Through-Package) View—30-Ball WLCSP Package

1.2 QFN

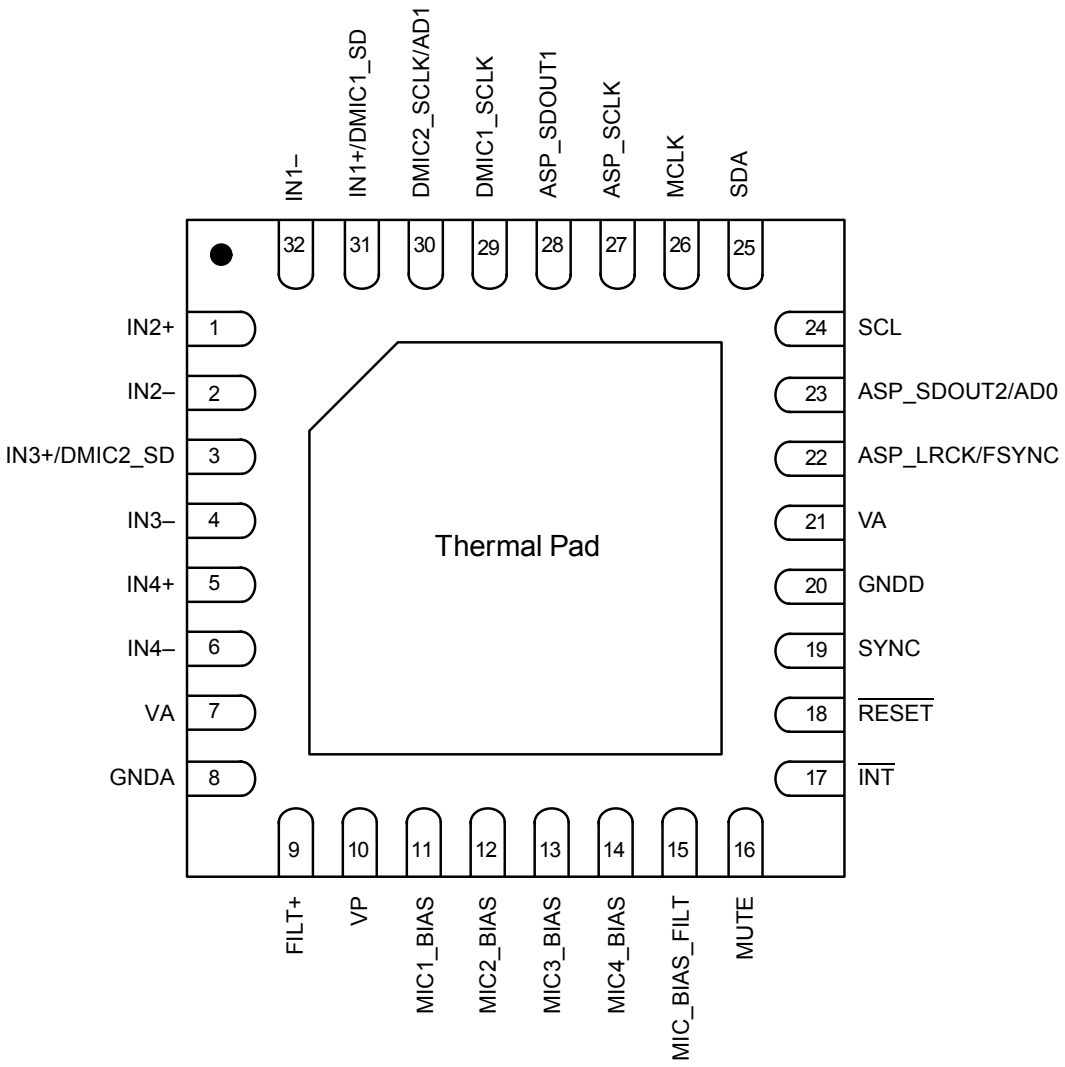


Figure 1-2. Top-Down (Through-Package) View—32-Pin QFN Package

1.3 Pin Descriptions

Table 1-1. Pin Descriptions

Name	Ball #	Pin #	Power Supply	I/O	Description	Internal Connection	Driver	Receiver	State at Reset
Capture-Path Pins									
IN1+/DMIC1_SD IN2+ IN3+/DMIC2_SD IN4+	A1 A2 A3 A4	31 1 3 5	VA	I	**Noninverting Inputs/DMIC Inputs.** Positive analog inputs for the stereo ADCs when CH_TYPE = 0 (default) or DMIC inputs when CH_TYPE = 1.	Programmable	—	Hysteresis on CMOS input	—
IN1– IN2– IN3– IN4–	B1 B2 B3 B4	32 2 4 6	VA	I	**Inverting Inputs.** Negative analog inputs for the stereo ADCs when CH_TYPE = 0 (default) or unused when CH_TYPE = 1.	Programmable	—	Hysteresis on CMOS input	—

Table 1-1. Pin Descriptions *(Cont.)*

Name	Ball #	Pin #	Power Supply	I/O	Description	Internal Connection	Driver	Receiver	State at Reset
					Filter pins				
MIC_BIAS_FILT	D6	15	VP	I	**Microphone Bias Voltage Filter.** Filter connection for the internal quiescent voltage used for the MICx_BIAS outputs.	—	—	—	—
FILT+	A6	9	VA	O	**Positive Reference Filter.** Positive reference voltage filter for internal sampling circuits.	—	—	—	—
					Analog Outputs				
MIC1_BIAS MIC2_BIAS MIC3_BIAS MIC4_BIAS	C4 C5 C6 D5	11 12 13 14	VP	O	**Microphone Bias Voltage.** Low-noise bias supply for an external mic.	—	—	—	Hi-Z
					Digital I/O				
$\overline{\text{INT}}$	—	17	VA	O	**Interrupt.** Outgoing interrupt signal generated upon registering an error (fault).	—	CMOS open-drain output	—	Hi-Z
$\overline{\text{RESET}}$	E5	18	VA	I	**Reset.** The device enters a low power mode when this pin is driven low.	—	—	Hysteresis on CMOS input	—
SYNC	D4	19	VA	I/O	**Multidevice Synchronization Signal.** Synchronization output when SYNC_EN is set, otherwise it is a synchronization input. Defaults to input.	Weak pulldown	CMOS output	Hysteresis on CMOS input	Hi-Z
SCL	D3	24	VA	I	**Serial Control Port Clock.** Serial clock for the I²C port.	—	—	Hysteresis on CMOS input	—
SDA	E2	25	VA	I/O	**Serial Control Data.** Bidirectional data pin for the I²C port.	—	CMOS open-drain output	Hysteresis on CMOS input	—
MCLK	E1	26	VA	I	**Master Clock.** Clock source for device's core.	Weak pulldown	—	Hysteresis on CMOS input	—
ASP_SCLK	D2	27	VA	I/O	**Audio Serial Clock.** Audio bit clock. Input in Slave Mode, output in Master Mode.	Weak pulldown	CMOS output	Hysteresis on CMOS input	Hi-Z
ASP_LRCK/ FSYNC	C3	22	VA	I/O	**Audio Left/Right Clock/Frame SYNC.** Identifies the start of each serialized PCM data word and indicates the active channel on each serial PCM audio data line. Input in Slave Mode, output in Master Mode.	Weak pulldown	CMOS output	Hysteresis on CMOS input	Hi-Z
ASP_SDOUT1	D1	28	VA	O	**Audio Data Output.** Output for the two's complement serial PCM data. Channels 1 and 2 are output in I²S Mode, while all four channels of data are output on this single pin in TDM Mode.	Weak pulldown	Tristateable CMOS output	—	Hi-Z
ASP_SDOUT2/ AD0	E3	23	VA	I/O	**Audio Data Output/Address Select.** Output for the two's-complement serial PCM data. Channels 3 and 4 are output in I²S Mode. Along with DMIC2_SCLK/AD1, immediately sets the I²C address when $\overline{\text{RESET}}$ is deasserted. Default is 0.	Weak pulldown	Tristateable CMOS output	—	Hi-Z
DMIC1_SCLK	C2	29	VA	O	**Digital MIC Interface 1 Serial Clock.** High speed clock output to the digital mics.	Weak pulldown	CMOS output	—	Hi-Z

Table 1-1. Pin Descriptions *(Cont.)*

Name	Ball #	Pin #	Power Supply	I/O	Description	Internal Connection	Driver	Receiver	State at Reset
DMIC2_SCLK/ AD1	C1	30	VA	I/O	**Digital MIC Interface 2 Serial Clock/ Address Select.** High speed clock output to the digital mics. Along with ASP_ SDOUT2/AD0, immediately sets the I²C address when RESET is deasserted. Default is 0.	Weak pulldown	CMOS output	—	Hi-Z
MUTE	E6	16	VA	I	**Mute.** Asserting this pin mutes all four channels. Also can be programmed to power down modules as configured in the MUTE pin control registers.	Weak pulldown	—	Hysteresis on CMOS input	—
					Power				
VA	A5	7 21	N/A	I	**Analog/Digital Power.** Power supply for analog circuitry and digital circuitry via internal LDO.	—	—	—	—
VP	B6	10	N/A	I	**Analog Power.** Power supply for mic bias.	—	—	—	—
GNDA	B5	8	N/A	I	**Analog Ground.** Ground reference.	—	—	—	—
GNDD	E4	20	N/A	I	**Digital Ground.** Ground reference.	—	—	—	—

2 Typical Connection Diagram

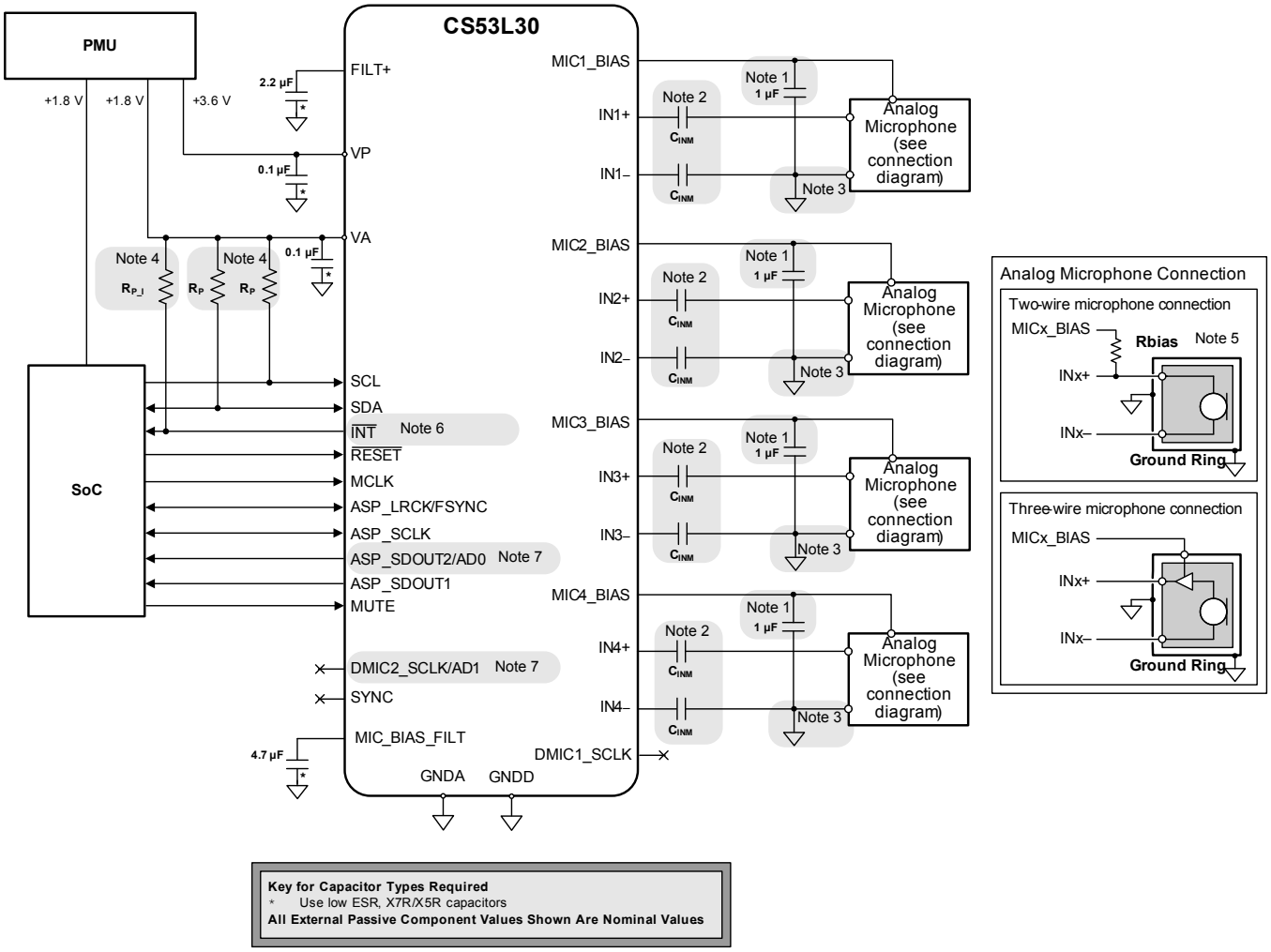


Figure 2-1. Typical Connection Diagram—Analog Microphone Connections

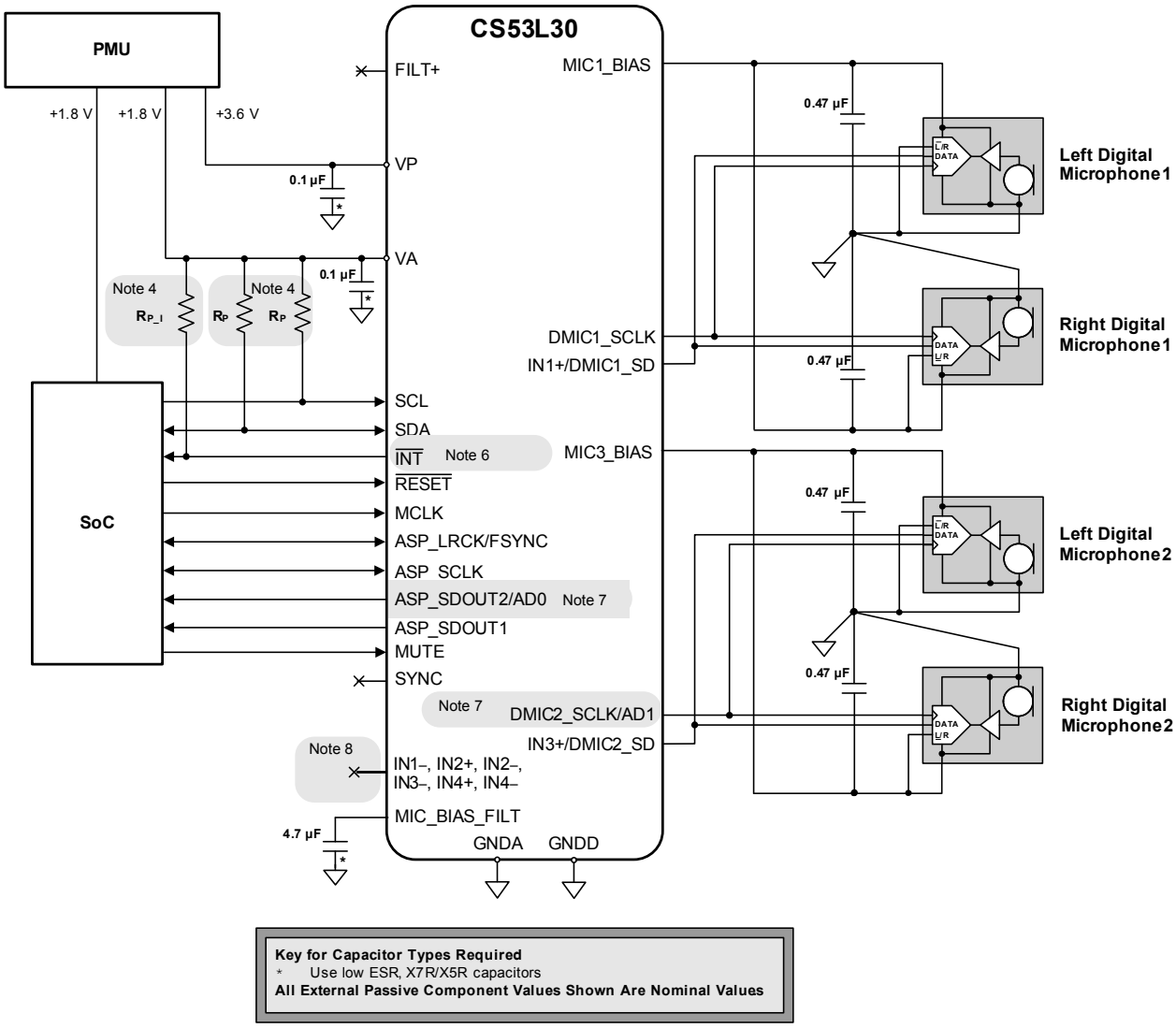


Figure 2-2. Typical Connection Diagram—Digital Microphone Connections

1. The MICx_BIAS compensation capacitor must be 1 µF (nominal values indicated, can vary from the nominal by ±20%). This value is bounded by the stability of the amplifier and the maximum rise-time specification of the output.
2. The DC-blocking capacitor, C_{INM}, forms a high-pass filter whose corner frequency is determined by the capacitor value and the input impedance. See Table 3-5 and Section 4.4.2.
3. The reference terminal of the INx inputs connects to the ground pin of the mic cartridge in the pseudodifferential case. In a fully differential configuration, the reference terminal of the INx inputs connects to the inverting output terminal of differential mic.
4. R_{P_I} and R_P can be calculated by using the values in Table 3-14.
5. The value of R_{BIAS}, the bias resistor for electret condenser mics, is dictated by the mic cartridge.
6. The $\overline{INT}$ pin is provided only on the QFN package.
7. ASP_SDOUT2/AD0 and DMIC2_SCLK/AD1 have internal pull-downs that allow for the default I^2C address with no external components. See Table 3-14 for typical and maximum pull-down values. If an I^2C physical address other than the default is desired, then external resistor termination to VA is required. The minimum value resistor allowed on these I/O pins is 10 kΩ. The time constant resulting from the pull-up/pull-down resistor and the total net capacitance should be considered when determining the time required for the pin voltage to settle before $\overline{RESET}$ is deasserted.
8. Unconnected INx pins can be terminated with an internal weak_vcm or weak pull-down by setting the termination in the INxy_BIAS bits. See Section 5.7, Section 7.19, and Section 7.20.

3 Characteristics and Specifications

Section 8 provides additional details about parameter definitions.

Table 3-1. Recommended Operating Conditions

Test conditions: GNDA = GNDD = 0 V; all voltages are with respect to ground.

Parameters [1]		Symbol	Min	Max	Unit
DC power supply	Analog/Digital	VA	1.71	1.89	V
	VP_MIN = 1	VP	3.2	5.25	V
	VP_MIN = 0		3.0	5.25	V
External voltage applied to pin [2]	VA domain pins	V_{IN-AI}	–0.3	VA + 0.3	V
	VP domain pins	V_{IN-PI}	–0.3	VP + 0.3	V
Ambient temperature	Commercial	T_A	–10	+70	°C

1. Device functional operation is guaranteed within these limits; operation outside them is not guaranteed or implied and may reduce device reliability.
2. The maximum over/under voltage is limited by the input current.

Table 3-2. Absolute Maximum Ratings

Test conditions: GNDA = GNDD = 0 V; all voltages are with respect to ground.

Parameters		Symbol	Min	Max	Units
DC power supply	Analog/digital	VA	–0.3	2.22	V
	Mic bias	VP	–0.3	5.6	V
Input current [1]		I_{in}	—	±10	mA
Ambient operating temperature (power applied)		T_A	–50	+115	°C
Storage temperature (no power applied)		T_{stg}	–65	+150	°C

CAUTION: Operation at or beyond these limits may permanently damage the device.

1. Any pin except supplies. Transient currents of up to ±100 mA on the capture-path pins do not cause SCR latch-up.

Table 3-3. Combined ADC On-Chip Analog, Digital Filter, SRC, and DMIC Characteristics

Test conditions (unless otherwise specified): T_A = +25°C; MCLK = 12.288 MHz; characteristics do not include the effects of external AC-coupling capacitors. Path is INx to SDOUT. Analog and digital gains are all set to 0 dB; HPF disabled.

Parameters [1]				Min	Typ	Max	Units
$Fs_{int} = Fs_{ext} =$ Fs = 48 kHz [2]	ADC notch filter on (ADCx_NOTCH_DIS = 0)	Passband	–0.05-dB corner	—	0.391	—	Fs
			–3.0-dB corner	—	0.410	—	Fs
		Passband ripple (0 Hz to 0.394 Fs; normalized to 0 Hz)		–0.13	—	0.14	dB
		Stopband @ –70 dB		—	0.492	—	Fs
		Total group delay		—	$15.3/Fs_{int} + 6.5/Fs_{ext}$	—	s
	ADC notch filter off (ADCx_NOTCH_DIS = 1)	Passband	–0.05-dB corner	—	0.445	—	Fs
			–3.0-dB corner	—	0.470	—	Fs
		Passband ripple (0 Hz to 0.447 Fs; normalized to 0 Hz)		–0.09	—	0.14	dB
		Stopband @ –70 dB		—	0.639	—	Fs
		Total group delay		—	$15.5/Fs_{int} + 6.6/Fs_{ext}$	—	s

1. Specifications are normalized to Fs and can be denormalized by multiplying by Fs.
2. See Section 5.6 for information about combined filter response when Fs_{int} is not equal to Fs_{ext}.

Table 3-4. ADC High-Pass Filter (HPF) Characteristics

Test conditions (unless specified otherwise): Analog and digital gains are all set to 0 dB; ADCx_HPF_CF = 00.

Parameters [1]		Min	Typ	Max	Units
Passband [2]	–0.05-dB corner	—	$3.57x10^{-4}$	—	Fs_{int}
	–3.0-dB corner	—	$3.88x10^{-5}$	—	Fs_{int}
Passband ripple ($0.417x10^{-3}$ Fs to 0.417 Fs; normalized to 0.417 Fs)		—	—	0.01	dB
Phase deviation @ 0.453 x 10^{-3} Fs		—	4.896	—	°
Filter settling time [3]	ADCx_HPF_CF = 00 ($3.88 \times 10^{-5} \times Fs_{int}$ mode)	—	$12260/Fs_{int}$	—	s
	ADCx_HPF_CF = 01 ($2.5 \times 10^{-3} \times Fs_{int}$ mode)	—	$200/Fs_{int}$	—	s
	ADCx_HPF_CF = 10 ($4.9 \times 10^{-3} \times Fs_{int}$ mode)	—	$100/Fs_{int}$	—	s
	ADCx_HPF_CF = 11 ($9.7 \times 10^{-3} \times Fs_{int}$ mode)	—	$50/Fs_{int}$	—	s

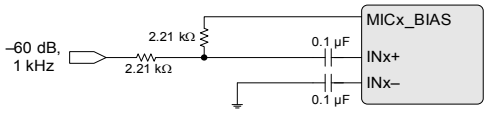
1. Response scales with Fs_{int}. Specifications are normalized to Fs_{int} and are denormalized by multiplying by Fs_{int}.
2. Characteristics do not include effects of the analog HPF filter formed by the external AC-coupling capacitors and the input impedance.
3. Required time for the magnitude of the DC component present at the output of the HPF to reach 5% of the applied DC signal.

Table 3-5. Analog-Input-to-Serial-Port Characteristics

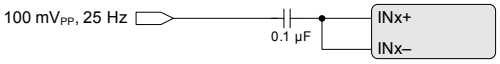
Test conditions (unless otherwise specified): Fig. 2-1 shows CS53L30 connections; input is a full-scale 1-kHz sine wave; ADCx_PREAMP = +10 dB; ADCx_PGA_VOL = 0 dB; GNDA = GNDD = 0; voltages are with respect to ground; parameters can vary with VA, typical performance data taken with VA = 1.8 V, VP = 3.6 V, min/max performance data taken with **V**A = 1.8 V, VP = 3.6 V; T_A = +25°C; measurement bandwidth is 20 Hz–20 kHz; LRCK = Fs = 48 kHz.

Parameters [1]			Min	Typ	Max	Units
Dynamic range [2]	Preamp setting: Bypass, PGA setting: 0 dB	A-weighted unweighted	87 85	93 91	— —	dB dB
	Preamp setting: Bypass, PGA setting: +12 dB	A-weighted unweighted	80 78	86 84	— —	dB dB
	Preamp setting: +10 dB, PGA setting: 0 dB	A-weighted unweighted	84 82	90 88	— —	dB dB
	Preamp setting: +10 dB, PGA setting: +12 dB	A-weighted unweighted	74 72	80 78	— —	dB dB
	Preamp setting: +20 dB, PGA setting: 0 dB	A-weighted unweighted	78 76	84 82	— —	dB dB
	Preamp setting: +20 dB, PGA setting: +12 dB	A-weighted unweighted	66 64	72 70	— —	dB dB
Total harmonic distortion + noise [3]	Preamp setting: Bypass, PGA setting: 0 dB	–1 dB	—	–84	–78	dB
	Preamp setting: Bypass, PGA setting: +12 dB	–1 dB	—	–80	–74	dB
	Preamp setting: +10 dB, PGA setting: 0 dB	–1 dB	—	–76	–70	dB
	Preamp setting: +10 dB, PGA setting: +12 dB	–1 dB	—	–63	–57	dB
	Preamp setting: +20 dB, PGA setting: 0 dB	–1 dB	—	–70	–64	dB
	Preamp setting: +20 dB, PGA setting: +12 dB	–1 dB	—	–62	–56	dB
Common-mode rejection [4]			—	70	—	dB
DC accuracy	Interchannel gain mismatch [5]		—	±0.2	—	dB
	Gain drift [5]		—	±100	—	ppm/°C
	PGA A/B gain	G_{MIN} G_{MAX} ΔG	–6.25 11.75 0.375	–6 12 0.5	–5.75 12.25 0.625	dB dB dB
	Preamp A/B gain	G_{MIN} G_{MAX}	9.5 19.9	10 20	10.5 20.5	dB dB
	Offset error [6]		—	128	—	LSB
Phase accuracy	Multichip interchannel phase mismatch [7]		—	0.5	—	°
	Interchannel phase mismatch [8]		—	0.5	—	°
Input	Interchannel isolation [8]	217 Hz 1 kHz 20 kHz	— — —	90 90 80	— — —	dB dB dB
	Full-scale signal input voltage [9]	Preamp setting: 0 dB, PGA setting: 0 dB Preamp setting: +10 dB, PGA setting: 0 dB Preamp setting: +10 dB, PGA setting: +12 dB Preamp setting: +20 dB, PGA setting: 0 dB Preamp setting: +20 dB, PGA setting: +12 dB	0.78•VA — — — —	0.82•VA 0.258•VA 0.064•VA 0.081•VA 0.020•VA	0.88•VA — — — —	Vpp Vpp Vpp Vpp Vpp
	Input impedance [10]	Preamp setting: 0 dB Preamp setting: +10 or +20 dB;	45 0.9	50 1	— —	kΩ MΩ
DC voltage at INx (pin floating) [11,12]	Preamp setting: Bypass	ADCx_PDN = 0 ADCx_PDN = 1	— —	0.42•VA 0.50•VA	— —	V V
	Preamp setting: +10 dB or +20 dB	ADCx_PDN = 0 ADCx_PDN = 1	— —	0.39•VA 0.50•VA	— —	V V

1. Measures are referred to the applicable typical full-scale voltages. Applies to all THD+N and dynamic range values in the table.
2. INx dynamic range test configuration (pseudodifferential) Includes noise from MICx_BIAS output (2.7-V setting) through a series 2.21-kΩ resistor connected to INx. Input signal is –60 dB down from the corresponding full-scale signal input voltage.



3. Input signal amplitude is relative to typical full-scale signal input voltage.
4. INx CMRR test configuration



5. Measurements taken at all defined full-scale signal input voltages.
6. SDOUT code with ADC_HPF_EN = 1, DIG_BOOSTx = 0. The offset is added at the ADC output; if two ADC sources are mixed, their offsets add.
7. Measured between two CS53L30 chips with input pairs IN1 selected and driven from same source with an MCLK of 19.2 MHz, 16-kHz sample rate, and 8-kHz full-scale sine wave with preamp gain of +20 dB and PGA gain of +12 dB.
8. Measured between input pairs (IN1 to INx, IN2 to INx, IN3 to INx, IN4 to INx) with +20 dB preamp gain and +12 dB PGA gain.
9. ADC full-scale input voltage is measured between INx+ and INx– with the preamp set to bypass and the PGA set to 0-dB gain. Maximum input signal level for INx depends on the preamp and PGA gain settings described in Section 5.4.1. The digital output level corresponding to ADC full-scale input is less than 0 dBFS due to signal attenuation through the SRC; see Table 4-4.
10. Measured between INx+ and INx–.
11. INx pins are biased as specified when weak VCM is selected in the input bias control registers; see Section 7.19 and Section 7.20.
12. Changing gain settings to Bypass Mode may cause audible artifacts due to the difference in DC operating points between modes.

Table 3-6. MIC BIAS Characteristics

Test conditions (unless otherwise specified): Fig. 2-1 shows CS53L30 connections; GNDA = GNDD = 0; all voltages are with respect to ground; VA = 1.8 V, VP = 3.6 V, T_A = +25°C; only one bias output is powered up at a time; MCLK_INT_SCALE = 0.

Parameters		Min	Typ	Max	Units
Output voltage [1]	MIC_BIAS_CTRL = 01 (1.8-V mode) MIC_BIAS_CTRL = 10 (2.7-V mode)	1.71 2.61	1.80 2.75	1.89 2.86	V V
Mic bias startup delay [2]		—	10	—	ms
Rise time [3]	I_{OUT} = 500 µA, MIC_BIAS_CTRL = 01 (1.8-V mode) I_{OUT} = 500 µA, MIC_BIAS_CTRL = 10 (2.7-V mode) I_{OUT} = 2 mA	— — —	0.2 0.5 —	— — 3	ms ms ms
DC output current (I_{OUT})	Per output	—	—	2	mA
Integrated output noise	f = 100 Hz–20 kHz	—	3	—	µVrms
Dropout voltage [4]		—	—	340	mV
PSRR reduction voltage [5]		—	—	500	mV
Output resistance (R_{OUT})	I_{OUT} = 2-mA	—	30	—	Ω

1. The output voltage includes attenuation due to the MIC BIAS output resistance (R_{OUT}).
2. Startup delay times are approximate and vary with $MCLK_{INT}$ frequency. If MCLK_INT_SCALE = 1, the startup delay time is scaled up by the $MCLK_{INT}$ scaling factor. The $MCLK_{INT}$ scaling factor is 1, 2, or 4, depending on Fs_{EXT}. See Table 4-2.
3. From 10% to 90% of typical output voltage. External capacitor on MICx_BIAS is as shown in Fig. 2-1.
4. Dropout voltage indicates the point where an output's voltage starts to vary significantly with reductions to its supply voltage. When the VP supply voltage drops below the programmed MICx_BIAS output voltage plus the dropout voltage, the MICx_BIAS output voltage progressively decreases as its supply decreases.
   Dropout voltage is measured by reducing the VP supply until MICx_BIAS drops 10 mV from its initial voltage with the default typical test condition VP voltage (= 3.6 V, as in test conditions listed above). The difference between the VP supply voltage and the MICx_BIAS voltage at this point is the dropout voltage. For instance, if the initial MICx_BIAS output is 2.86 V when VP = 3.6 V and VP = 3.19 V when MICx_BIAS drops to 2.85 V (–10 mV), the dropout voltage is 340 mV (3.19 V – 2.85 V).
5. PSRR voltage indicates the point where an output's supply PSRR starts to degrade significantly with supply voltage reductions. When the VP supply voltage drops below the programmed MICx_BIAS output voltage plus the PSRR reduction voltage, the MICx_BIAS output's PSRR progressively decreases as its supply decreases.
   PSRR reduction voltage is measured by reducing the VP supply until MICx_BIAS PSRR @ 217 Hz falls below 100 dB. The difference between the VP supply voltage and the MICx_BIAS voltage at this point is the PSRR reduction voltage. For instance, if the MICx_BIAS PSRR falls to 99.9 dB when VP is reduced to 3.25 V and the MICx_BIAS output voltage is 2.75 V at that point, PSRR reduction voltage is 500 mV (3.25 V – 2.75 V).

Table 3-7. Power-Supply Rejection Ratio (PSRR) Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows CS53L30 connections; input test signal held low (all zero data); GNDA = GNDD = 0; voltages are with respect to ground; VA = 1.8 V, VP = 3.6 V; T_A = +25°C.

Parameters [1]		Min	Typical	Max	Units
INx (32-dB analog gain) PSRR with 100-mVpp signal AC coupled to VA supply	217 Hz 1 kHz 20 kHz	— — —	70 70 55	— — —	dB dB dB
MICx_BIAS (MICx_BIAS = 2.7-V mode, I_{OUT} = 500 µA) PSRR with 100 mVpp signal AC coupled to VA supply VP_MIN = 0 (3.0 V)	217 Hz 1 kHz 20 kHz	— — —	105 100 95	— — —	dB dB dB
MICx_BIAS (MICx_BIAS = 2.7-V mode, I_{OUT} = 500 µA) PSRR with 100 mVpp signal AC coupled to VA supply VP_MIN = 1 (3.2 V)	217 Hz 1 kHz 20 kHz	— — —	105 100 95	— — —	dB dB dB
MICx_BIAS (MICx_BIAS = 2.7-V mode, I_{OUT} = 500 µA) PSRR with 100 mVpp signal AC coupled to VP supply VP_MIN = 0 (3.0 V)	217 Hz 1 kHz 20 kHz	— — —	90 90 70	— — —	dB dB dB
MICx_BIAS (MICx_BIAS = 2.7-V mode, I_{OUT} = 500 µA) PSRR with 1 Vpp signal AC coupled to VP supply VP_MIN = 1 (3.2 V)	217 Hz 1 kHz 20 kHz	— — —	120 115 105	— — —	dB dB dB

1. PSRR test configuration: Typical PSRR can vary by approximately 6 dB below the indicated values.

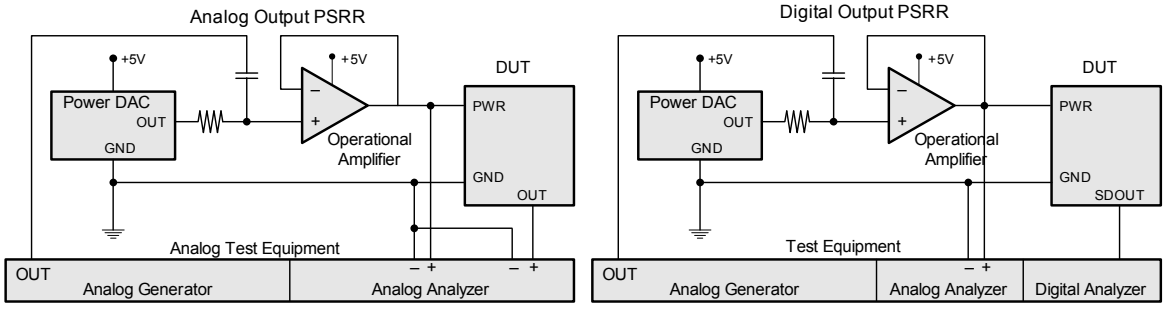
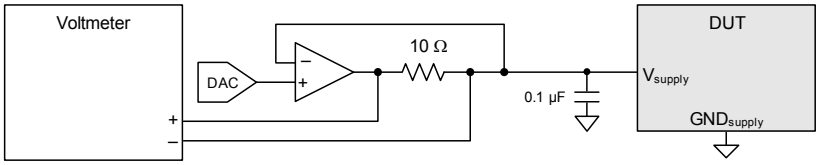


Table 3-8. Power Consumption

Test conditions (unless specified otherwise): Fig. 2-1 shows CS53L30 connections; GNDA = GNDD = 0 V; voltages are with respect to ground; performance data taken with VA = 1.8 V, VP = 3.6 V; T_A = +25°C; MCLK = 12.288 MHz; serial port set to Slave Mode; digital volume = 0 dB; no signal on any input; control port inactive; MCLK_INT_SCALE = 1.

Use Cases [1] (See Table 3-9 for register field settings.)				Typical Current (µA)		Total Power (µW)
				i_{VA}	i_{VP}	
1		Standby [2]		2	0	4
2	A	Quiescent [3]	MCLK low, MCLK_DIS = x, PDN_ULP = 1, PDN_LP = x	7	1	17
	B		MCLK active, MCLK_DIS = 1, PDN_ULP = 1, PDN_LP = x	54	1	101
	C		MCLK low, MCLK_DIS = x, PDN_ULP = 0, PDN_LP = 1	103	19	253
	D		MCLK active, MCLK_DIS = 1, PDN_ULP = 0, PDN_LP = 1	134	19	308
3	A	Capture, analog mic input, ADCx_PREAMP = +20 dB, ADCx_PGA_VOL = +12 dB	Fs_{ext} = 48 kHz, mono input, MICx_BIAS_PDN = 1	1998	58	3805
	B		Fs_{ext} = 48 kHz, mono input, MICx_BIAS_PDN = 0	2003	147	4136
	C		Fs_{ext} = 16 kHz, mono input, MICx_BIAS_PDN = 1	1423	58	2770
	D		Fs_{ext} = 16 kHz, mono input, MICx_BIAS_PDN = 0	1432	147	3107
	E		Fs_{ext} = 8 kHz, mono input, MICx_BIAS_PDN = 1	1046	58	2092
	F		Fs_{ext} = 8 kHz, mono input, MICx_BIAS_PDN = 0	1053	147	2425
	G		Fs_{ext} = 48 kHz, stereo input, MICx_BIAS_PDN = 1	2697	81	5147
	H		Fs_{ext} = 48 kHz, stereo input, MICx_BIAS_PDN = 0	2702	243	5739
	I		Fs_{ext} = 16 kHz, stereo input, MICx_BIAS_PDN = 1	1955	81	3811
	J		Fs_{ext} = 16 kHz, stereo input, MICx_BIAS_PDN = 0	1960	243	4405
	K		Fs_{ext} = 8 kHz, stereo input, MICx_BIAS_PDN = 1	1494	81	2981
	L		Fs_{ext} = 8 kHz, stereo input, MICx_BIAS_PDN = 0	1498	243	3573
	M		Fs_{ext} = 48 kHz, four-channel input, MICx_BIAS_PDN = 1	4138	145	7969
	N		Fs_{ext} = 48 kHz, four-channel input, MICx_BIAS_PDN = 0	4141	454	9087
	O		Fs_{ext} = 16 kHz, four-channel input, MICx_BIAS_PDN = 1	3033	145	5981
	P		Fs_{ext} = 16 kHz, four-channel input, MICx_BIAS_PDN = 0	3040	454	7106
	Q		Fs_{ext} = 8 kHz, four-channel input, MICx_BIAS_PDN = 1	2397	145	4836
	R		Fs_{ext} = 8 kHz, four-channel input, MICx_BIAS_PDN = 0	2403	454	5959
4	A	Capture, analog line input, ADCx_PREAMP = 0 dB, ADCx_PGA_VOL = 0 dB	Fs_{ext} = 48 kHz, four-channel input, MICx_BIAS_PDN = 1	3151	145	6193
	B		Fs_{ext} = 16 kHz, four-channel input, MICx_BIAS_PDN = 1	2059	145	4227
	C		Fs_{ext} = 8 kHz, four-channel input, MICx_BIAS_PDN = 1	1429	145	3092
5	A	Capture, digital mic input	Fs_{ext} = 48 kHz, four-channel input, MICx_BIAS_PDN = 0	2433	352	5645
	B		Fs_{ext} = 16 kHz, four-channel input, MICx_BIAS_PDN = 0	1366	352	3725
	C		Fs_{ext} = 8 kHz, four-channel input, MICx_BIAS_PDN = 0	881	352	2852

1. Power consumption test configuration.
   The current draw on the power supply pins is derived from the measured voltage drop across a 10-Ω series resistor between the associated supply source and the voltage supply pin.



2. Standby configuration: Clock/data lines are held low; $\overline{\text{RESET}}$ = LOW; VA = 1.8 V, VP = 3.6 V
3. Quiescent configuration: data lines held low; $\overline{\text{RESET}}$ = HIGH

Table 3-9. Register Field Settings

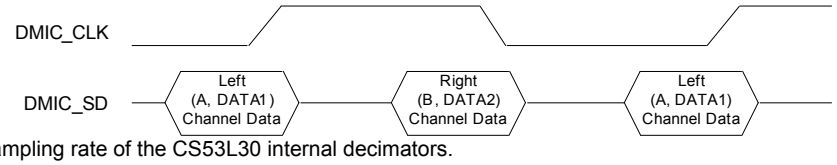
Use Cases		PDN_ULP	PDN_LP	MCLK_DIS	MCLK_INT_SCALE	MIC1_BIAS_PDN	MIC2_BIAS_PDN	MIC3_BIAS_PDN	MIC4_BIAS_PDN	MIC_BIAS_CTRL	ASP_RATE[3:0]	ASP_SDOUT1_PDN	ASP_SDOUT2_PDN	ASP_3ST	ADC1A_PDN	ADC1B_PDN	ADC2A_PDN	ADC2B_PDN	ADC1A_PREAMP[1:0]	ADC1A_PGA_VOL[5:0]	ADC1B_PREAMP[1:0]	ADC1B_PGA_VOL[5:0]	ADC2A_PREAMP[1:0]	ADC2A_PGA_VOL[5:0]	ADC2B_PREAMP[1:0]	ADC2B_PGA_VOL[5:0]	DMIC1_PDN	DMIC2_PDN	ASP_M/S
1		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
2	A	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	B	1	—	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	C	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	D	0	1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
3	A	0	0	0	—	1	1	1	1	—	1100	0	1	0	0	1	1	1	10	011000	10	011000	10	011000	10	011000	1	1	0
	B	0	0	0	—	0	1	1	1	10	1100	0	1	0	0	1	1	1	10	011000	10	011000	10	011000	10	011000	1	1	0
	C	0	0	0	1	1	1	1	1	—	0101	0	1	0	0	1	1	1	10	011000	10	011000	10	011000	10	011000	1	1	0
	D	0	0	0	1	0	1	1	1	10	0101	0	1	0	0	1	1	1	10	011000	10	011000	10	011000	10	011000	1	1	0
	E	0	0	0	1	1	1	1	1	—	0001	0	1	0	0	1	1	1	10	011000	10	011000	10	011000	10	011000	1	1	0
	F	0	0	0	1	0	1	1	1	10	0001	0	1	0	0	1	1	1	10	011000	10	011000	10	011000	10	011000	1	1	0
	G	0	0	0	—	1	1	1	1	—	1100	0	1	0	0	0	1	1	10	011000	10	011000	10	011000	10	011000	1	1	0
	H	0	0	0	—	0	0	1	1	10	1100	0	1	0	0	0	1	1	10	011000	10	011000	10	011000	10	011000	1	1	0
	I	0	0	0	1	1	1	1	1	—	0101	0	1	0	0	0	1	1	10	011000	10	011000	10	011000	10	011000	1	1	0
	J	0	0	0	1	0	0	1	1	10	0101	0	1	0	0	0	1	1	10	011000	10	011000	10	011000	10	011000	1	1	0
	K	0	0	0	1	1	1	1	1	—	0001	0	1	0	0	0	1	1	10	011000	10	011000	10	011000	10	011000	1	1	0
	L	0	0	0	1	0	0	1	1	10	0001	0	1	0	0	0	1	1	10	011000	10	011000	10	011000	10	011000	1	1	0
	M	0	0	0	—	1	1	1	1	—	1100	0	0	0	0	0	0	0	10	011000	10	011000	10	011000	10	011000	1	1	0
	N	0	0	0	—	0	0	0	0	10	1100	0	0	0	0	0	0	0	10	011000	10	011000	10	011000	10	011000	1	1	0
	O	0	0	0	1	1	1	1	1	—	0101	0	0	0	0	0	0	0	10	011000	10	011000	10	011000	10	011000	1	1	0
	P	0	0	0	1	0	0	0	0	10	0101	0	0	0	0	0	0	0	10	011000	10	011000	10	011000	10	011000	1	1	0
	Q	0	0	0	1	1	1	1	1	—	0001	0	0	0	0	0	0	0	10	011000	10	011000	10	011000	10	011000	1	1	0
	R	0	0	0	1	0	0	0	0	10	0001	0	0	0	0	0	0	0	10	011000	10	011000	10	011000	10	011000	1	1	0
4	A	0	0	0	—	1	1	1	1	—	1100	0	0	0	0	0	0	0	00	000000	00	000000	00	000000	00	000000	1	1	0
	B	0	0	0	1	1	1	1	1	—	0101	0	0	0	0	0	0	0	00	000000	00	000000	00	000000	00	000000	1	1	0
	C	0	0	0	1	1	1	1	1	—	0001	0	0	0	0	0	0	0	00	000000	00	000000	00	000000	00	000000	1	1	0
5	A	0	0	0	—	0	0	0	0	10	1100	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—	0	0	0
	B	0	0	0	1	0	0	0	0	10	0101	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—	0	0	0
	C	0	0	0	1	0	0	0	0	10	0001	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—	0	0	0

Table 3-10. Switching Specifications—Digital Mic Interface

Test conditions (unless specified otherwise): Fig. 2-1 shows CS53L30 connections; GNDA = GNDD = 0 V; voltages are with respect to ground; parameters can vary with VA, typical performance data taken with VA = 1.8 V, VP = 3.6 V, min/max performance data taken with VA = 1.8 V, VP = 3.6 V; T_A = +25°C; logic 0 = ground, logic 1 = VA; DMIC_DRIVE = 0 (normal); input timings are measured at V_{IL} and V_{IH} thresholds, and output timings are measured at V_{OL} and V_{OH} thresholds (see Table 3-14).

Parameters [1,2]	Symbol	Min	Max	Units
Output clock (DMICx_SCLK) frequency	$1/t_P$	—	3.2[3]	MHz
DMICx_SCLK duty cycle[4]	—	45	55	%
DMICx_SCLK rise time (10% to 90% of VA) [4]	t_r	—	21	ns
DMICx_SCLK fall time (90% to 10% of VA) [4]	t_f	—	13	ns
DMICx_SD setup time before DMICx_SCLK rising edge	$t_{s(SD-CLKR)}$	10	—	ns
DMICx_SD hold time after DMICx_SCLK rising edge	$t_{h(CLKR-SD)}$	4	—	ns
DMICx_SD setup time before DMICx_SCLK falling edge	$t_{s(SD-CLKF)}$	10	—	ns
DMICx_SD hold time after DMICx_SCLK falling edge	$t_{h(CLKF-SD)}$	4	—	ns

1. Digital mic interface timing



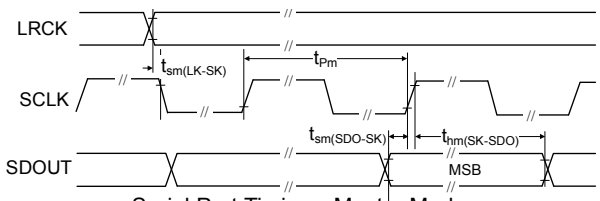
2. Oversampling rate of the digital mic must match the oversampling rate of the CS53L30 internal decimators.
3. The output clock frequency follows the internal MCLK rate divided by 2 or 4, as set in the ADCx/DMICx control registers (see DMIC1_SCLK_DIV on p. 53 and DMIC2_SCLK_DIV on p. 55). DMICx_SCLK is further divided by up to a factor of 4 when MCLK_INT_SCALE is set (see p. 48). MCLK source deviation from nominal supported rates is applied directly to the output clock rate by the same factor (e.g., a +100-ppm offset in the frequency of MCLK becomes a +100-ppm offset of DMICx_SCLK.
4. Timing guaranteed with pull-up or pull-down resistor, with a minimum value 10 kΩ tied to DMIC2_SCLK/AD1 for I²C address determination.

Table 3-11. Specifications—I²S

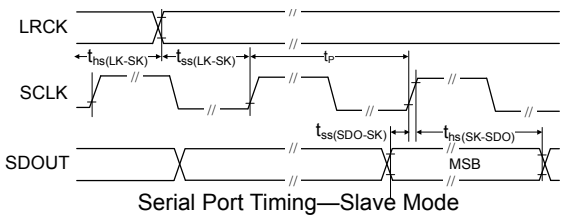
Test conditions (unless specified otherwise): Fig. 2-1 shows CS53L30 connections; GNDA = GNDD = 0 V; all voltages are with respect to ground; parameters can vary with VA; typical performance data taken with VA = 1.8 V, VP = 3.6 V; min/max performance data taken with VA = 1.8 V, VP = 3.6 V; T_A = +25°C; Test load for ASP_LRCK/FSYNC, ASP_SCLK, and ASP_SDOUTx C_L = 60 pF; logic 0 = ground, logic 1 = VA; ASPx_DRIVE = 0; input timings are measured at V_{IL} and V_{IH} thresholds, and output timings are measured at V_{OL} and V_{OH} thresholds (see Table 3-14).

Parameters [1,2]		Symbol	Min	Max	Units
MCLK frequency		—	1.024	19.2	MHz
MCLK duty cycle		—	45	55	%
Slave mode	Input sample rate (LRCK)	Fs	(See Table 4-2)		kHz
	LRCK duty cycle	—	45	55	%
	SCLK frequency	$1/t_{Ps}$	—	$64•Fs_{ext}$	Hz
	SCLK duty cycle	—	45	55	%
	SCLK rising edge to LRCK edge	$t_{hs(LK-SK)}$	10	—	ns
	LRCK setup time before SCLK rising edge	$t_{ss(LK-SK)}$	40	—	ns
	SDOUT setup time before SCLK rising edge	$t_{ss(SDO-SK)}$	20	—	ns
	SDOUT hold time after SCLK rising edge	$t_{hs(SK-SDO)}$	30	—	ns
Master mode	Output sample rate (LRCK) All speed modes	Fs_{ext}	(See Table 4-2)		kHz
	LRCK duty cycle	—	45	55	%
	SCLK frequency	$1/t_{Pm}$	—	$64•Fs_{ext}$	Hz
	SCLK duty cycle	—	33	67	%
	LRCK time before SCLK falling edge	$t_{sm(LK-SK)}$	–2	+2	ns
	SDOUT setup time before SCLK rising edge	$t_{sm(SDO-SK)}$	20	—	ns
	SDOUT hold time after SCLK rising edge	$t_{hm(SK-SDO)}$	30	—	ns

1. Serial port interface timing



Serial Port Timing—Master Mode



Serial Port Timing—Slave Mode

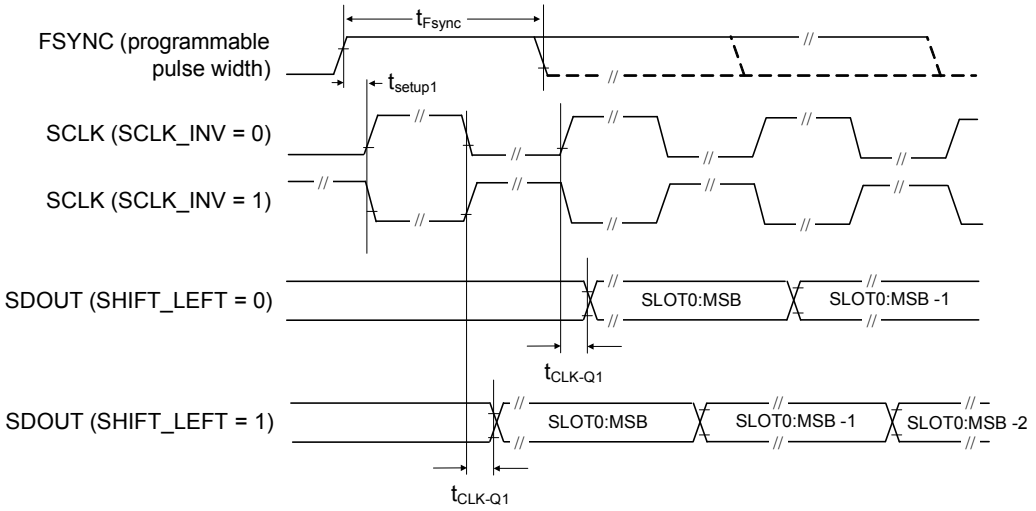
2. MCLK must be stable before powering up the device. In Slave Mode, ASP_LRCK/FSYNC and ASP_SCLK must be stable before powering up the device. Before making changes to any clock setting, the device must be powered down by setting either the PDN_ULP or PDN_LP bit.

Table 3-12. Switching Specifications—Time-Division Multiplexed (TDM) Mode

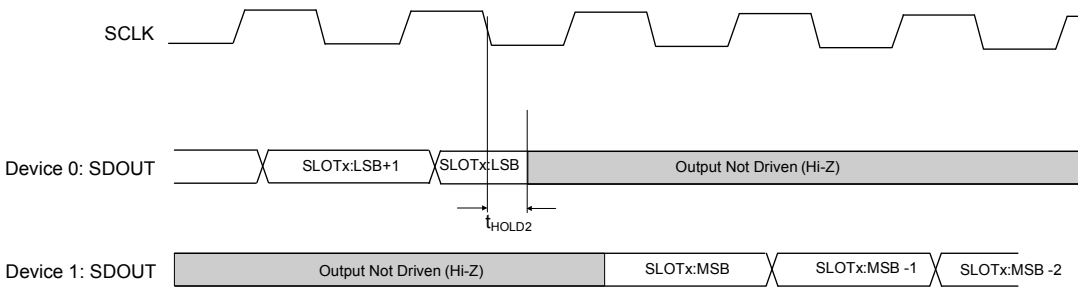
Test conditions (unless specified otherwise): Fig. 2-1 shows CS53L30 connections; GNDA = GNDD = 0 V; all voltages are with respect to ground; parameters can vary with VA; typical performance data taken with VA = 1.8 V, VP = 3.6 V; min/max performance data taken with VA = 1.8 V, VP = 3.6 V; T_A = +25°C; Test load for ASP_LRCK/FSYNC, ASP_SCLK, and ASP_SDOUT1 C_L = 60 pF; logic 0 = ground, logic 1 = VA; ASPx_DRIVE = 0; input timings are measured at V_{IL} and V_{IH} thresholds, and output timings are measured at V_{OL} and V_{OH} thresholds (see Table 3-14).

Parameters			Symbol	Min	Max	Units
MCLK frequency			—	1.024	19.2	MHz
MCLK duty cycle			—	45	55	%
Slave mode	Input sample rate (FSYNC) [1,2]		Fs_{ext}	—	48	kHz
	FSYNC high time pulse [3]		t_{FSYNC}	$1/f_{SCLK}$	$(n–1)/f_{SCLK}$	s
	FSYNC setup time before SCLK rising edge		t_{SETUP1}	20	—	ns
	SCLK frequency [4,5]		f_{SCLK}	—	12.288	MHz
	SCLK duty cycle		—	45	55	%
	SDOUT delay time after SCLK rising edge [6]	SHIFT_LEFT = 0	t_{CLK-Q1}	—	25	ns
		SHIFT_LEFT = 1	t_{CLK-Q1}	—	45	ns
	SDOUT hold time of LSB before transition to Hi-Z	SHIFT_LEFT = 0 [7]	t_{HOLD2}	10	30	ns
		SHIFT_LEFT = 1 [8]	t_{HOLD2}	10	40	ns
Master mode	Output sample rate (FSYNC) [1]		Fs_{ext}	—	[9]	kHz
	FSYNC high time pulse [10]		t_{FSYNC}	$1/f_{SCLK}$	$(n–1)/f_{SCLK}$	s
	FSYNC setup time before SCLK rising edge		t_{SETUP1}	15	—	ns
	SCLK frequency		f_{SCLK}	(See Table 4-3)		MHz
	SCLK duty cycle		—	45	55	%
	SDOUT delay time after SCLK rising edge	SHIFT_LEFT = 0	t_{CLK-Q1}	—	25	ns
	SDOUT delay time after SCLK rising edge [6]	SHIFT_LEFT = 1	t_{CLK-Q2}	—	45	ns
	SDOUT hold time of LSB before transition to Hi-Z	SHIFT_LEFT = 0 [7]	t_{HOLD2}	10	30	ns
		SHIFT_LEFT = 1 [8]	t_{HOLD2}	10	40	ns

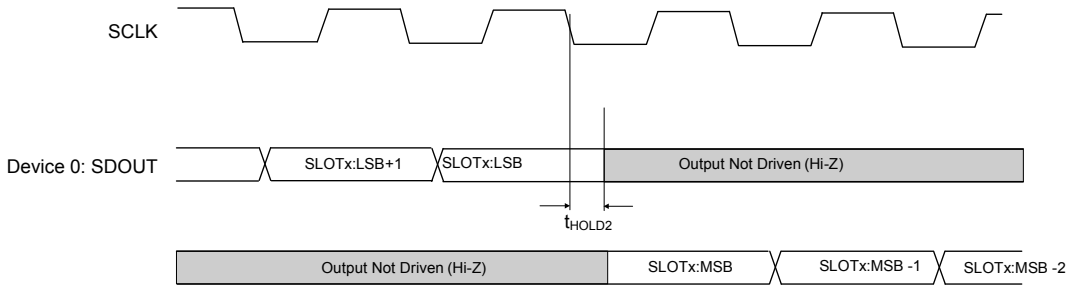
1. Clock rates must be stable when the device is powered up and the serial port is not powered down. Therefore, the appropriate serial port must be powered down before any clock rates are changed.
2. Maximum frequency for the highest supported nominal rate is indicated. Table 4-2 shows nominal MCLK rates and their associated configurations.
3. "n" refers to the total number of SCLKs in one FSYNC frame.
4. If MCLK_19MHZ_EN is set, the maximum SCLK frequency is 6.4 MHz. If SHIFT_LEFT is set, the maximum SCLK frequency is 6.4 MHz.
5. SCLK frequency must be high enough to provide the necessary SCLK cycles to capture all the serial audio port bits.
6. Single-device TDM timings



7. Hand-off timing for multidevice systems (SHIFT_LEFT = 0.



8. Hand-off timing for multidevice systems (SHIFT_LEFT = 1). When SHIFT_LEFT = 1, it is recommended to insert an empty slot between devices on the TDM bus to prevent contention possibilities.



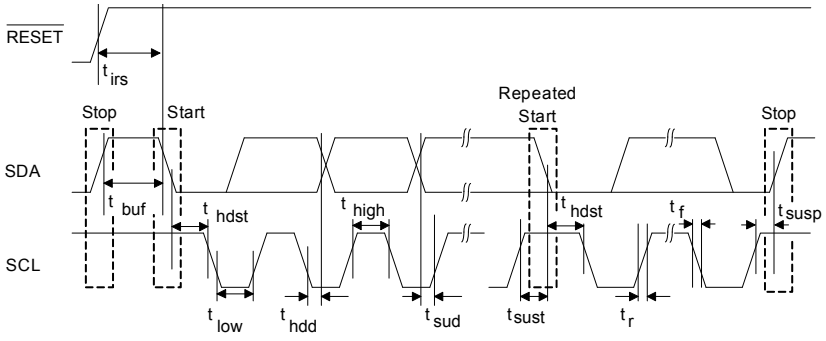
9. In Master Mode, the output sample rate follows the MCLK rate, per Section 4.6.5. MCLK deviations from the nominal supported rates are passed directly to the output sample rate by the same factor (e.g., a +100 ppm offset in the frequency of MCLK becomes a +100 ppm offset in FSYNC).
10. "n" refers to number of SCLK cycles programmed in LRCK_TPWH[10:3] | LRCK_TPWH[2:0] (see p. 51) when LRCK_50_NPW (see p. 51) is set; otherwise, t_{FSYNC} has a 50% duty cycle.

Table 3-13. Switching Specifications—I²C Control Port

Test conditions (unless specified otherwise): Fig. 2-1 shows CS53L30 connections; GNDA = GNDD = 0 V; all voltages are with respect to ground; Parameters can vary with VA, typical performance data taken with VA = 1.8 V, VP = 3.6 V, min/max performance data taken with VA = 1.8 V, VP = 3.6 V; T_A = +25°C; logic 0 = ground, logic 1 = VA; input timings are measured at V_{IL} and V_{IH} thresholds, and output timings are measured at V_{OL} and V_{OH} thresholds (see Table 3-14).

Parameter [1,2]	Symbol	Min	Max	Unit
$\overline{\text{RESET}}$ rising edge to start	t_{irs}	500	—	ns
SCL clock frequency	f_{scl}	—	550	kHz
Start condition hold time (prior to first clock pulse)	t_{hdst}	0.6	—	µs
Clock low time	t_{low}	1.3	—	µs
Clock high time	t_{high}	0.6	—	µs
Setup time for repeated start condition	t_{sust}	0.6	—	µs
SDA input hold time from SCL falling [3]	t_{hddi}	0	0.9	µs
SDA output hold time from SCL falling	t_{hddo}	0.2	0.9	µs
SDA setup time to SCL rising	t_{sud}	100	—	ns
Rise time of SCL and SDA	t_{rc}	—	300	ns
Fall time SCL and SDA	t_{fc}	—	300	ns
Setup time for stop condition	t_{susp}	0.6	—	µs
Bus free time between transmissions	t_{buf}	1.3	—	µs
SDA bus capacitance	C_L	—	400	pF
SDA pull-up resistance	R_p	500	—	Ω

1. All specifications are valid for the signals at the pins of the CS53L30 with the specified load capacitance.
2. I²C control port timing.



3. Data must be held for sufficient time to bridge the transition time, t_f, of SCL.

Table 3-14. Digital Interface Specifications and Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows CS53L30 connections; GNDA = GNDD = 0 V; all voltages are with respect to ground; VA =1.8 V, VP = 3.6 V; T_A = +25°C

Parameters [1]	Symbol	Min	Max	Units
Input leakage current [2] MCLK, SYNC, MUTE, all serial port inputs	I_{in}	—	±4000	nA
All control port inputs, INT, RESET		—	±100	nA
Internal weak pulldown	—	550	2450	kΩ
Input capacitance [2]	—	—	10	pF
$\overline{INT}$ current sink (V_{OL} = 0.3 V max)	—	825	—	µA
High-level output voltage [3]	V_{OH}	VA – 0.2	—	V
Low-level output voltage [4]	V_{OL}	—	0.2	V
High-level input voltage	V_{IH}	0.70•VA	—	V
Low-level input voltage	V_{IL}	—	0.30•VA	V

1.See Table 1-1 for serial and control port power rails.
2.Specification is per pin. Includes current through internal pull-down resistors on serial port.
3.I_{OH} = –100 µA for x_DRIVE = 0; I_{OH} = –67 µA for x_DRIVE = 1
4.I_{OL} = 100 µA for x_DRIVE = 0; I_{OL} = 67 µA for x_DRIVE = 1

Table 3-15. Thermal Overload Detection Characteristics

Test conditions (unless otherwise specified): GNDA = GNDD = 0; all voltages are with respect to ground; VA = 1.8 V, VP = 3.6 V.

Parameters	Min	Typ	Max	Units
Thermal overload detection threshold	—	150	—	°C

4 Functional Description

This section provides a general description of the CS53L30 architecture and detailed functional descriptions of the various blocks that comprise the CS53L30.

4.1 Overview

Fig. 4-1 is a block diagram of the CS53L30 with links to descriptions of major subblocks.

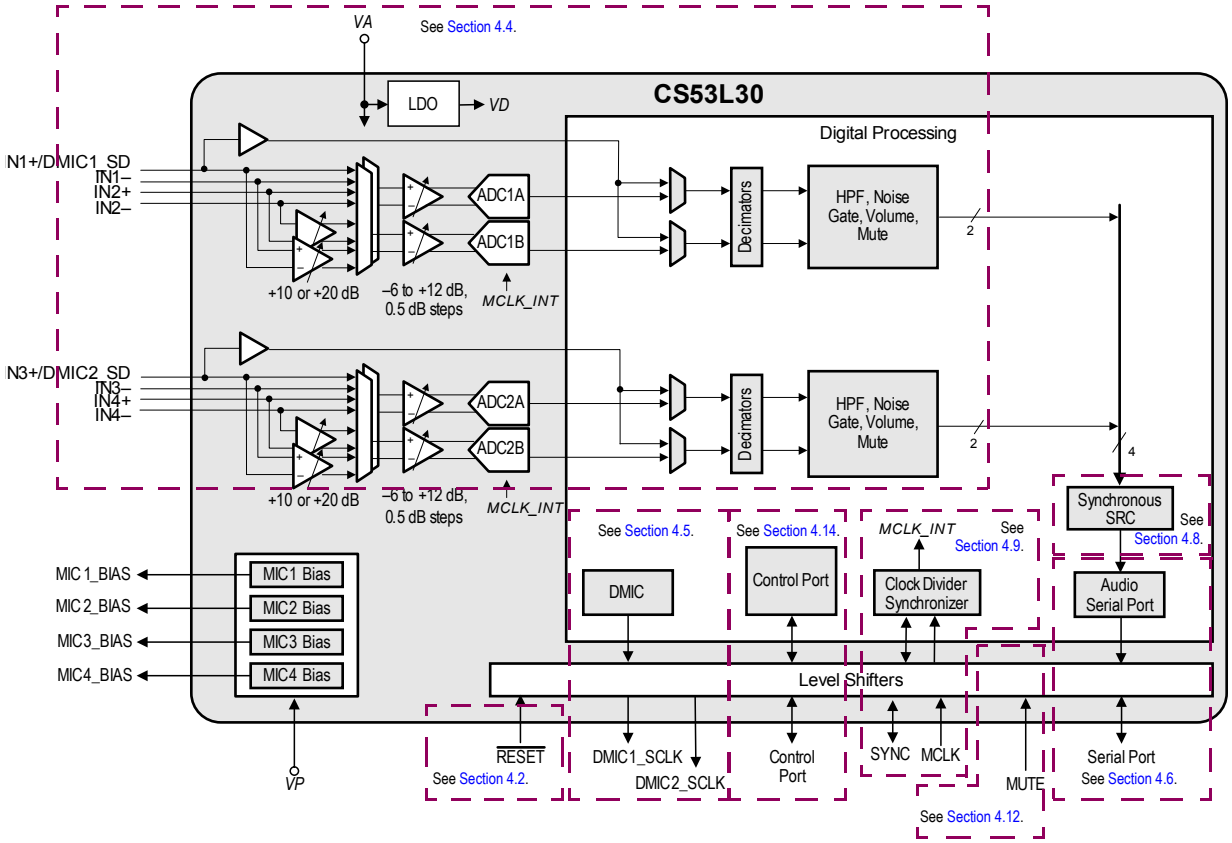


Figure 4-1. Overview of Signal Flow

The CS53L30 is a low-power, four-channel, 24-bit audio ADC. The ADCs are fed by fully differential analog inputs that support mic and line-level input signals. The ADCs are designed using multibit delta-sigma techniques. The ADCs operate at an optimal oversampling ratio balancing performance with power savings. Enhanced power savings are possible when the internal MCLK is scaled by setting MCLK_INT_SCALE (see p. 45). Table 4-2 lists supported sample rates with scaled internal MCLK.

The serial data port operates at a selectable range of standard audio sample rates as either timing master or slave. Core timing is flexibly sourced, without the need of a PLL, by clocks with typical audio clock rates (N x 5.6448, or N x 6.1440 MHz; where N = 1 or 2), USB rates (6 or 12 MHz), or 3G and DVB rates (19.2 MHz).

The integrated LDO regulator allows the digital core to operate at a very low voltage, significantly reducing the CS53L30's overall power consumption.

The CS53L30 can operate in a system with multiple CS53L30s to increase the number of channels available. The CS53L30s may be connected in a multidrop configuration in TDM Mode. Up to four CS53L30s can operate simultaneously on the same TDM bus. Connecting together the SYNC pins of multiple CS53L30s allows operation with minimal channel-to-channel phase mismatch across devices.

The signal to be converted can be either mic/line-level. The digital mic inputs (IN1+/DMIC1_SD, IN3+/DMIC2_SD) connect directly to the decimators.

The CS53L30 consists of the following blocks:

- Interrupts. The CS53L30 QFN package includes an open-drain, active-low interrupt output, $\overline{\text{INT}}$. Section 4.3 describes interrupts.
- Capture-path inputs. The analog input block, described in Section 4.4, allows selection from either analog line-level, or analog mic sources. The selected analog source is fed into a mic preamplifier (when applicable) and then into a PGA, before entering the ADC. The pseudodifferential input configuration can provide noise rejection for single-ended analog inputs. The digital mic inputs (IN1+/DMIC1_SD, IN3+/DMIC2_SD) connect directly to the decimators.
- Serial ports. The CS53L30 has either two I²S output ports or one TDM output port allowing communication to other devices in the system such as applications processors. The serial data ports are described in Section 4.6.1. The TDM port allows multidrop operation (i.e., tristate capable SDOUT driver) for sharing the TDM bus between multiple devices, and flexible data structuring via control port registers.
- Synchronous sample rate converter (SRC). The SRC, described in Section 4.8, is used to bridge different sample rates at the serial port within the digital-processing core.
- Multichip synchronization protocol. Some applications require more than four simultaneous audio channels requiring multiple CS53L30s. In a subset of these multidevice applications, special attention to phase alignment of audio channels is required. The CS53L30 has a synchronization protocol to align all audio channels and minimize interchannel phase mismatch. Section 4.9 describes the synchronization protocol.
- Thermal overload notification. The CS53L30 can be configured to notify the system processor that its die temperature is too high. This functionality is described in Section 4.11.
- Mute pin. The CS53L30 audio outputs can be muted with the assertion of the register-programmable MUTE pin. The MUTE pin function can also be programmed to power-down ADCs, MICx_BIAS, etc., by setting the appropriate bits in Section 7.17 and Section 7.18. Section 4.12 describes the MUTE pin functionality.
- Power management. Several registers provide independent power-down control of the analog and digital sections of the CS53L30, allowing operation in select applications with minimal power consumption. Power management considerations are described in Section 4.13.
- Control port operation. The control port is used to access the registers allowing the CS53L30 to be configured for the desired operational modes and formats. The operation of the control port may be completely asynchronous with respect to the audio sample rates. To avoid interference problems, the control port pins must remain static if no operation is required. Control port operation is described in Section 4.14.

4.2 Resets

The CS53L30 can be reset only by asserting $\overline{\text{RESET}}$. When $\overline{\text{RESET}}$ is asserted, all registers and all state machines are immediately set to their default values/states. No operation can begin until $\overline{\text{RESET}}$ is deasserted. Before normal operation can begin, $\overline{\text{RESET}}$ must be asserted at least once after the VA supply is brought up. The VP supply should be brought up before the VA supply.

4.3 Interrupts

The status of events that may require special attention is recorded in the interrupt status register (see Section 7.36). Interrupt status bits are sticky and read-to-clear: That is, once set, they remain set until the status register is read and the associated interrupt condition is no longer present.

4.3.1 Interrupt Handling with the WLCSP Package

If the WLCSP package is used, events and conditions are detected in software by polling the interrupt status register. The mask register can be ignored (see Section 7.35). Status register bits are cleared when read, as Fig. 4-2 shows. If the underlying condition remains valid, the bit remains set even after the status register is read.

4.3.2 Interrupt Handling with the QFN Package

The interrupt pin ($\overline{INT}$) is implemented on the QFN package. Interrupt status bits can be individually masked by setting corresponding bits in the interrupt mask register (see Section 7.35). The configuration of mask bits determines which events cause the assertion of $\overline{INT}$:

- When an unmasked interrupt status event is detected, the status bit is set and $\overline{INT}$ is asserted.
- When a masked interrupt status event is detected, the interrupt status bit is set, but $\overline{INT}$ is not affected.

Once $\overline{INT}$ is asserted, it remains asserted until all status bits that are unmasked and set have been read. If a condition remains present and the status bit is read, although $\overline{INT}$ is deasserted, the status bit remains set.

To clear any status bits set due to the initiation of a path or block, all interrupt status bits should be read after reset and before normal operation begins. Otherwise, unmasking any previously set status bits causes $\overline{INT}$ to assert.

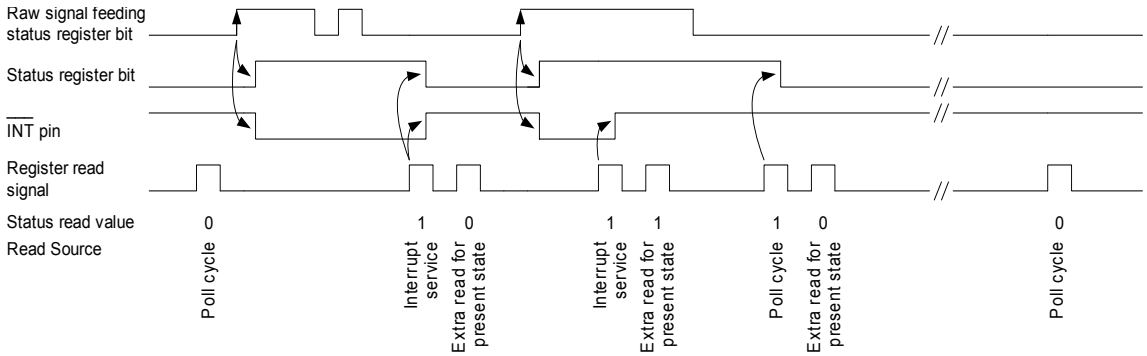


Figure 4-2. Example of Rising-Edge Sensitive, Sticky, Interrupt Status Bit Behavior ($\overline{INT}$ Pin in QFN only)

4.4 Capture-Path Inputs

This section describes the line in and mic inputs. Fig. 4-3 shows the capture-path signal flow.

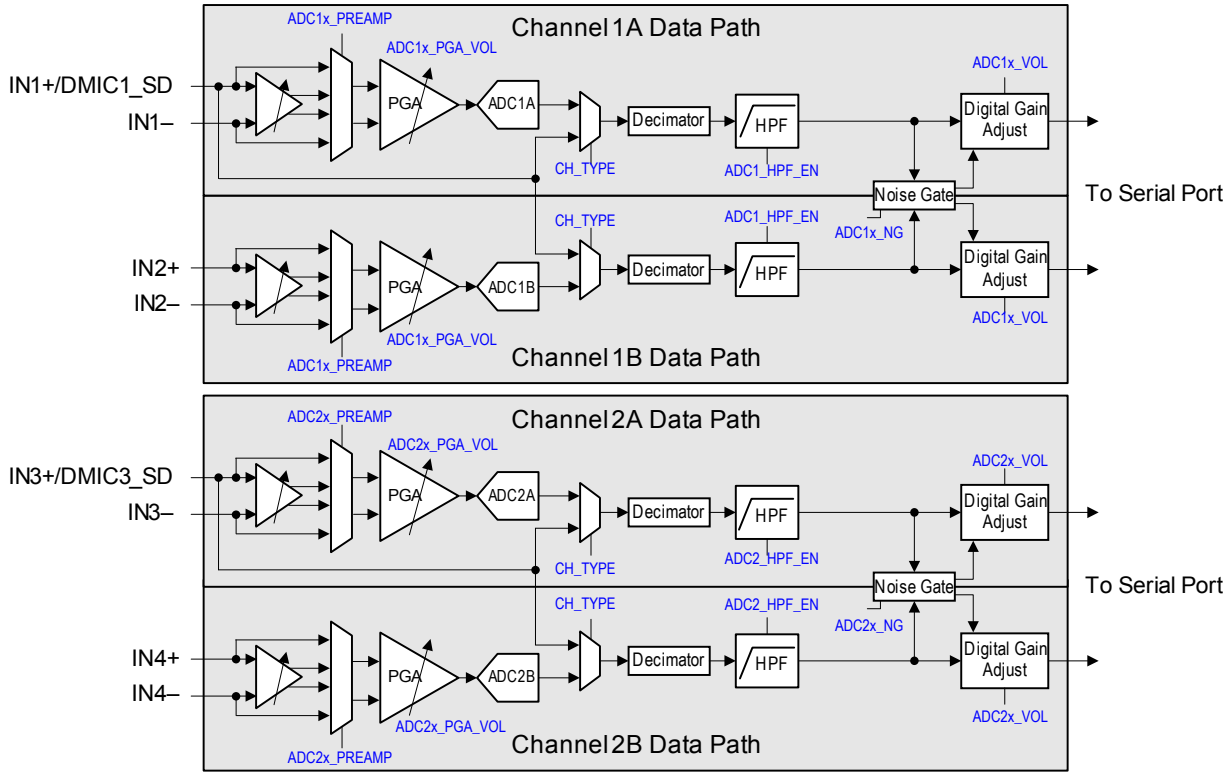
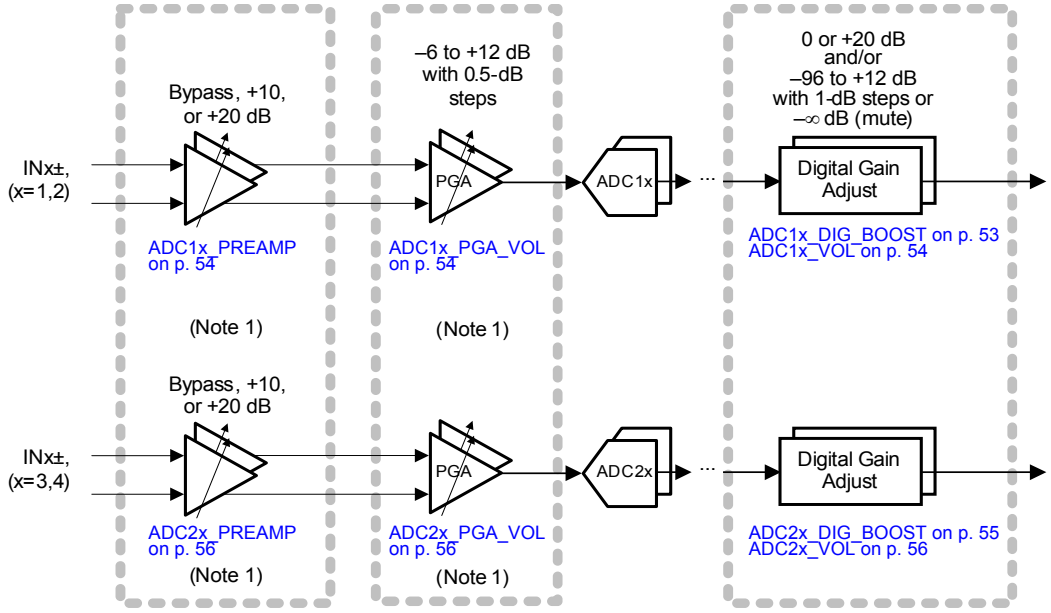


Figure 4-3. Capture-Path Signal Flow

Fig. 4-4 shows details of the various analog input gain settings, including control register fields.



1. Gains within analog blocks vary with supply voltage, with temperature, and from part to part. The gain values listed for these blocks are typical values with nominal parts and conditions.

Figure 4-4. Input Gain Paths

4.4.1 Analog Input Configurations

The CS53L30 implements fully differential analog input stages, as shown in Fig. 4-5. In addition to accepting fully differential input signals, the inputs can be used in a pseudodifferential configuration to improve common mode noise rejection with single-ended signals. In this configuration, a low-level reference signal is sensed at the ground point of the internal mic or external mic jack and used as a pseudodifferential reference for the internal input amplifiers. Sitting between the preamp and the PGA is an internal antialias filter with a first-order pole at 95 kHz and a first-order pole at 285 kHz.

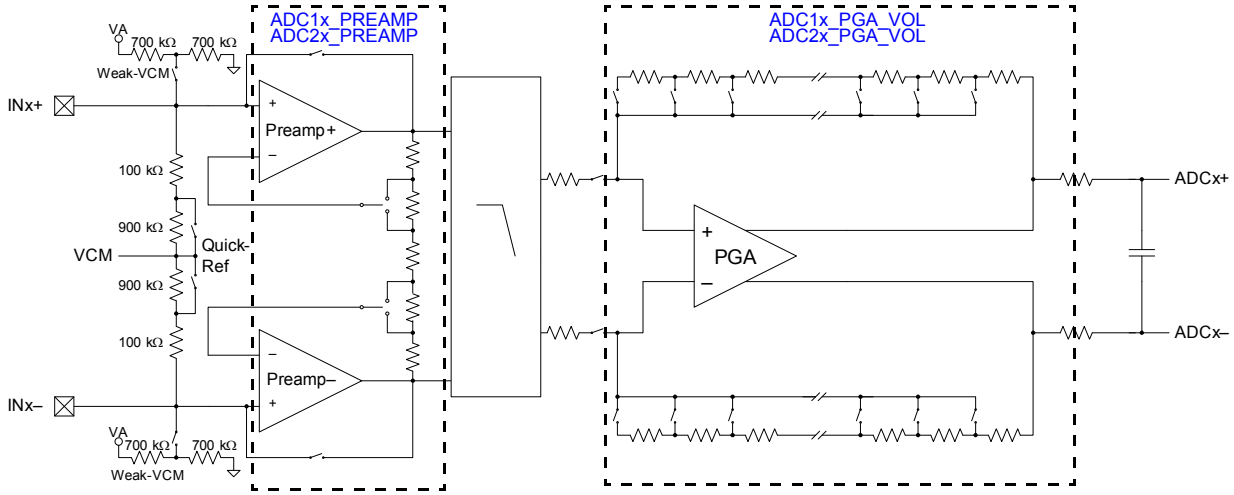


Figure 4-5. Op-Amp Level Schematic—Analog Inputs

Fig. 4-6 shows the INx interface and the related connections recommended for a fully differential internal mic. These connections are truncated in Fig. 4-6.

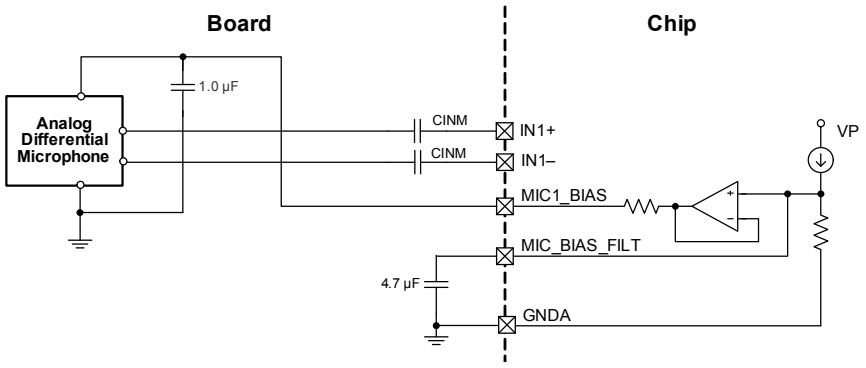


Figure 4-6. Fully Differential Mic Input Connections Example

Fig. 4-7 shows the IN1–IN4 interfaces and the related pseudodifferential connections recommended to achieve the best common-mode rejection for single-ended internal mics.

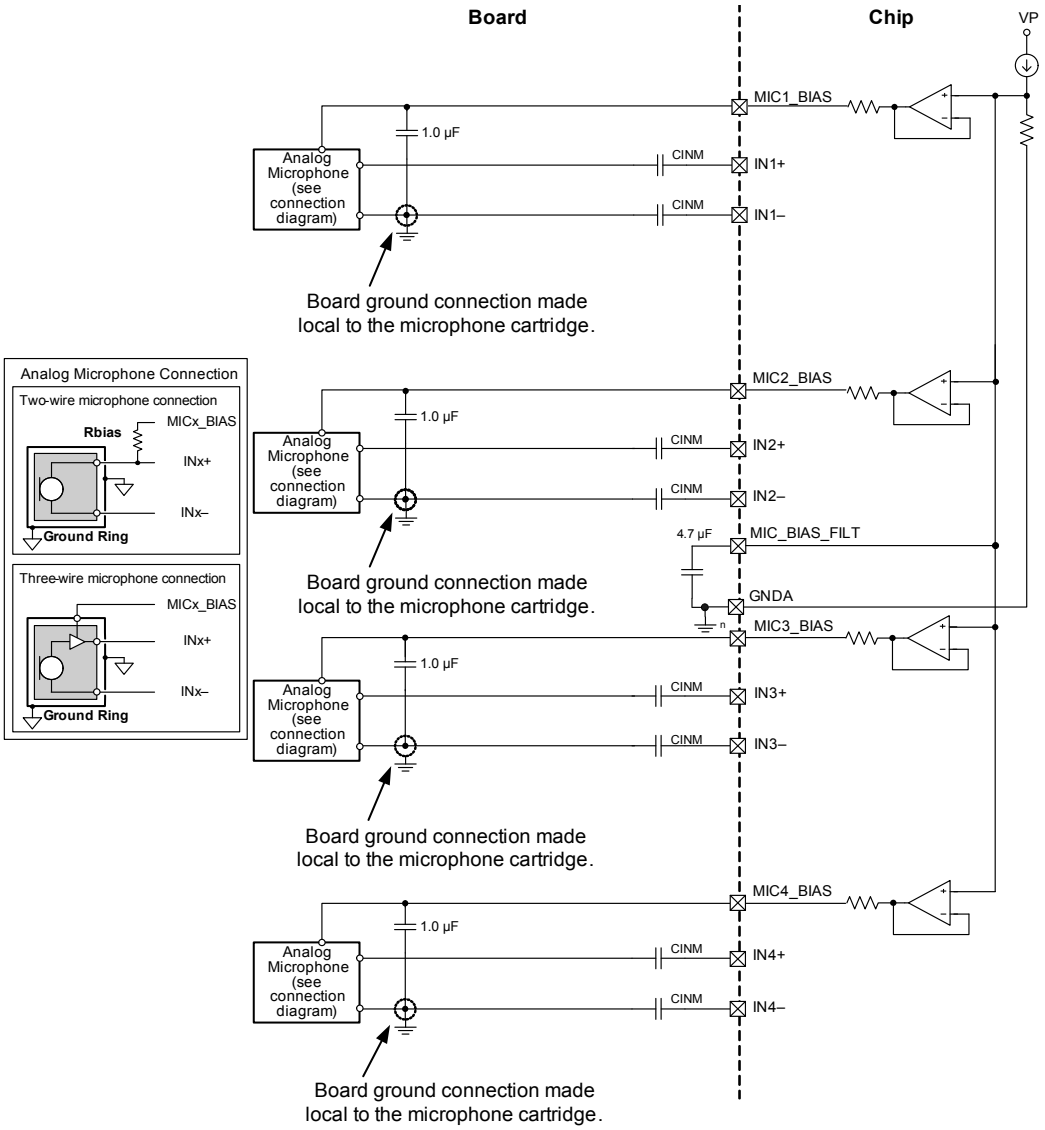


Figure 4-7. Pseudodifferential Mic Input Connections Example

4.4.2 External Coupling Capacitors

The analog inputs are internally biased to the internally generated common-mode voltage (VCM). Input signals must be AC coupled using external capacitors (C_{INM}) with values consistent with the desired HPF design. The analog input resistance may be combined with an external capacitor to achieve the desired cutoff frequency.

Eq. 4-1 provides an example for mic inputs.

$$f_c = \frac{1}{2\pi(1\ M\Omega)(0.01\ \mu F)} = 15.9\ Hz$$

Equation 4-1. External Coupling Capacitors—Mic Inputs

Eq. 4-2 provides an example for line inputs.

$$f_c = \frac{1}{2\pi(50\ k\Omega)(0.1\ \mu F)} = 31.83\ Hz$$

Equation 4-2. External Coupling Capacitors—Line Inputs

4.4.3 Capture-Path Pin Biasing

Capture-path pins are internally biased during normal operation. When connecting analog sources to the CS53L30, the input must be AC-coupled with an external capacitor. These sources may bias the analog inputs:

- Quick-Ref. After an analog input is powered up, the Quick-Ref buffer charges the external capacitor with a low-impedance bias source to minimize startup time.
- Weak VCM. When ADCx is powered up, the weak VCM biases unselected inputs to minimize coupling conditions.
- ADCx_PREAMP. When ADCx is powered up, ADCx_PREAMP biases the selected channel.

See Fig. 4-5 for the location of each bias source.

4.4.4 Soft Ramping (DIGSFT)

DIGSFT (see p. 50) controls whether digital volume updates are applied slowly by stepping through each volume control setting with a delay between steps equal to an integer number of FS_{int} periods. The amount of delay between steps is fixed at 8 FS_{int} periods. The step size is fixed at 0.125 dB.

When enabled, soft ramping is applied to all digital volume changes. Digital volume is affected by the following:

1. Writing directly to the ADC digital volume registers, ADC1x_VOL or ADC2x_VOL (see p. 54 and p. 56)
2. Enabling or disabling mute by driving a signal to the MUTE pin
3. Muting that is applied automatically by the noise gate
4. Muting that is applied automatically during power up and power down

If digital boost is disabled and the ADC digital volume is set to any value from 0x0C to 0x7F (all equivalent to +12 dB), the soft ramp first steps through the +12-dB settings in the same manner as the remainder of the volume settings. Soft ramp timing calculations must include these additional steps. For example, if the ADC digital volume setting is changed from 0x10 (+12 dB) to 0x00 (0 dB), the first 32 soft ramp steps from 0x10 to 0x0C do not produce any changes in digital volume, while each of the remaining 96 steps from 0x0C (+12 dB) to 0x00 (0 dB) causes a 0.125-dB reduction in digital volume. If digital boost is enabled, the soft ramp does not step through the +12-dB settings.

4.5 Digital Microphone (DMIC) Interface

The digital mic interface can be used to collect pulse-E (PDM) audio data from the integrated ADCs of one or two digital mics. The following sections describe how to use the interface.

4.5.1 DMIC Interface Description

The DMIC interface consists of a serial-data shift clock output (DMICx_SCLK) and a serial data input (DMICx_SD). Fig. 2-2 shows how to connect two digital mics (“Left” and “Right”) to the CS53L30. The clock is fanned out to both digital mics, and both digital mics’ data outputs share a single signal line to the CS53L30. To share a single line, the digital mics tristate their output during one phase of the clock (high or low part of cycle, depending on how they are configured via their L/R input). The CS53L30 defaults to mono digital mic input (left channel or rising edge of DMICx_SCLK data only). When DMIC1_STEREO_ENB or DMIC2_STEREO_ENB (see p. 52) is cleared, then both edges of DMICx_SCLK are used to capture stereo data; Alternating between one digital mic outputting a bit of data and then the other mic outputting a bit of data, the digital mics time domain multiplex on the signal data line. Contention on the data line is avoided by entering the high-impedance tristate faster than removing it.

The DMICx_SD signal can be held low through a weak pulldown (per Section 7.19 and Section 7.20) by its CS53L30 input. When the DMIC interface is active, this pulling is not strong enough to affect the multiplexed data line significantly while it is in tristate between data slots. While the interface is disabled and the data line is not driven, the weak pulling ensures that the CS53L30 input avoids any power-consuming midrail voltage.

4.5.2 DMIC Interface Signaling

Fig. 4-8 shows the signaling on the DMIC interface. Notice how the left channel (A, or DATA1 channel) data from the “Left” mic is sampled on the rising edge of the clock and the right channel (B, or DATA2 channel) data from the “Right” mic is sampled on the falling edge.

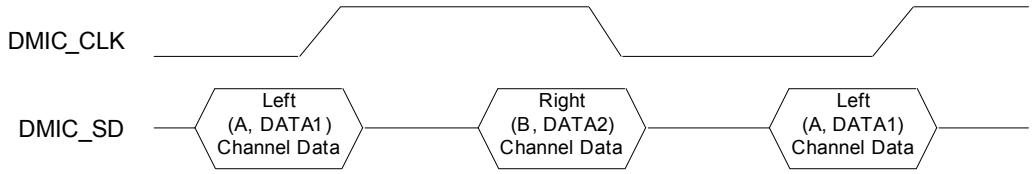


Figure 4-8. Digital Mic Interface Signalling

4.5.3 DMIC Interface Clock Generation

Table 4-1 lists DMIC interface serial clock (DMICx_SCLK) nominal frequencies and their derivation from the internal master clock.

Table 4-1. Digital Mic Interface Clock Generation

Post-MCLK_DIV MCLK Rate (MHz)	MCLK_INT_ SCALE	ASP_RATE (kHz) [1]	Divide Ratio	DMICx_SCLK Rate (MHz)	DMICx_SCLK_DIV Programming
5.6448	0	X	2	2.8224	0
			4	1.4112	1
	1	11.025	2	0.7056	0
			4	0.3528	1
		22.050	2	1.4112	0
			4	0.7056	1
		44.1	2	2.8224	0
			4	1.4112	1
6.0000	0	X	2	3.0000	0
			4	1.5000	1
	1	8,11.025,12	2	0.7500	0
			4	0.3750	1
		16, 22.050, 24	2	1.5000	0
			4	0.7500	1
		32, 44.1, 48	2	3.0000	0
			4	1.5000	1

Table 4-1. Digital Mic Interface Clock Generation *(Cont.)*

Post-MCLK_DIV MCLK Rate (MHz)	MCLK_INT_ SCALE	ASP_RATE (kHz) [1]	Divide Ratio	DMICx_SCLK Rate (MHz)	DMICx_SCLK_DIV Programming
6.1440	0	X	2	3.0720	0
			4	1.5360	1
	1	8, 11.025, 12	2	0.7680	0
			4	0.3840	1
		16, 22.050, 24	2	1.5360	0
			4	0.7680	1
		32, 44.1, 48	2	3.0720	0
			4	1.5360	1
6.4000	0	X	2	3.2000	0
			4	1.6000	1
	1	8, 11.025, 12	2	0.8000	0
			4	0.4000	1
		16, 22.050, 24	2	1.6000	0
			4	0.8000	1
		32, 44.1, 48	2	3.2000	0
			4	1.6000	1

1.An X indicates that the sample rate setting does not affect DMICx_SCLK rate.

4.6 Serial Ports

The CS53L30 has a highly configurable serial port to communicate audio and voice data to and from other devices in the system such as application processors and Bluetooth™ transceivers.

4.6.1 I/O

The serial port interface consists of four signals:

- ASP_SCLK. Serial data shift clock
- ASP_LRCK/FSYNC. Left/right (I²S) or frame sync clock (TDM)
  - LRCK identifies the start of each serialized data word and locates the left and right channels within the data word when I²S format is used (see Section 4.6.6).
  - FSYNC identifies the start of each TDM frame.
  - Toggles at external sample rate (Fs_{ext}).
- ASP_SDOUTx. Serial data outputs

4.6.2 Serial Port Power-Up, Power-Down, and Tristate

The ASP has separate power-down and tristate controls for its output data paths. The serial port power, tristate, and TDM control is done through ASP_3ST, ASP_TDM_PDN, and the respective ASP_SDOUTx_PDN bit. Separating power state controls helps minimize power consumption when the output port is not in use.

- ASP_SDOUTx_PDN. If the SDOUT functionality of a serial port is not required, the SDOUT data path can be powered down by setting ASP_SDOUTx_PDN. The ASP_SDOUTx pin is Hi-Z when ASP_SDOUTx_PDN is set; it does not tristate the serial port clock.
- ASP_3ST. See Section 4.6.3 for details.
- ASP_TDM_PDN. When ASP_TDM_PDN = 1, the ASP serial port is configured to operate in I²S Mode. When ASP_TDM_PDN = 0, ASP is configured to operate in TDM Mode and ASP_SDOUT2 is Hi-Z.

  To facilitate clock mastering in TDM Mode, while not sending data, ASP_TDM_PDN and all ASP_TX_ENABLEy bits must be cleared to prevent wasting power to drive the output nets. To save power when no TDM TX slots are used, ASP_SDOUT1 is automatically tristated.

Master/slave operation is controlled only by the M/$\overline{S}$ bit setting and is done irrespective of the setting of the ASP_SDOUTx_PDN, and ASP_3ST bits.