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CS5460A

Single Phase, Bi-directional Power/Energy IC

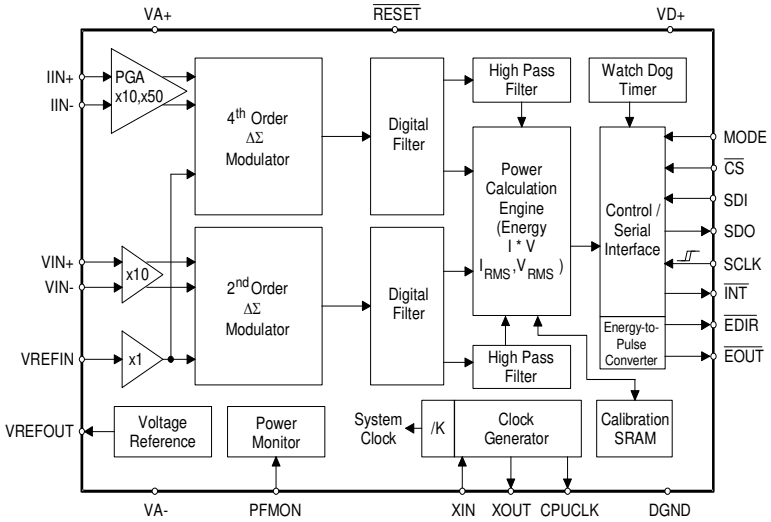
Features

- Energy Data Linearity: ±0.1% of Reading over 1000:1 Dynamic Range.
- On-Chip Functions: (Real) Energy, I ∗ V, I_{RMS} and V_{RMS}, Energy-to-Pulse Conversion
- Smart "Auto-boot" Mode from Serial EEPROM Enables Use without MCU.
- AC or DC System Calibration
- Mechanical Counter/Stepper Motor Driver
- Meets Accuracy Spec for IEC 687/1036, JIS
- Typical Power Consumption <12 mW
- Interface Optimized for Shunt Sensor
- *V* vs. *I* Phase Compensation
- Ground-Referenced Signals with Single Supply
- On-chip 2.5 V Reference (MAX 60 ppm/°C drift)
- Simple Three-wire Digital Serial Interface
- Watch Dog Timer
- Power Supply Monitor
- Power Supply Configurations
  VA+ = +5 V; VA- = 0 V; VD+ = +3.3 V to +5 V

Description

The CS5460A is a highly integrated power measurement solution which combines two ΔΣ Analog-to-digital Converters (ADCs), high-speed power calculation functions, and a serial interface on a single chip. It is designed to accurately measure and calculate: Real (True) Energy, Instantaneous Power, I_{RMS}, and V_{RMS} for single phase 2- or 3-wire power metering applications. The CS5460A interfaces to a low-cost shunt resistor or transformer to measure current, and to a resistive divider or potential transformer to measure voltage. The CS5460A features a bi-directional serial interface for communication with a microcontroller and a pulse output engine for which the average pulse frequency is proportional to the real power. The CS5460A has on-chip functionality to facilitate AC or DC system-level calibration.

The "Auto-boot" feature allows the CS5460A to function 'stand-alone' and to initialize itself on system power-up. In Auto-boot Mode, the CS5460A reads the calibration data and start-up instructions from an external EEPROM. In this mode, the CS5460A can operate without a microcontroller, in order to lower the total bill-of-materials cost.



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1. CHARACTERISTICS & SPECIFICATIONS

ANALOG CHARACTERISTICS

(T_A = -40 °C to +85 °C; VA+ = VD+ = +5 V ±10%; VREFIN = +2.5 V; VA- = AGND = 0 V; MCLK = 4.096 MHz, K = 1; N = 4000 ==> OWR = 4000 Sps.)(See Notes 1, 2, 3, 4, and 5.)

Parameter		Symbol	Min	Typ	Max	Unit
Accuracy (Both Channels)						
Common Mode Rejection	(DC, 50, 60 Hz)	CMRR	80	-	-	dB
Offset Drift (Without the High Pass Filter)			-	5	-	nV/°C
Analog Inputs (Current Channel)						
Maximum Differential Input Voltage Range {(V_{IIN+}) - (V_{IIN-})}	(Gain = 10) (Gain = 50)	I_{IN}	- -	- -	500 100	mV_{P-P} mV_{P-P}
Total Harmonic Distortion		THD_I	80	-	-	dB
Common Mode + Signal on IIN+ or IIN-	(Gain = 10 or 50)		-0.25	-	VA+	V
Crosstalk with Voltage Channel at Full Scale	(50, 60 Hz)		-	-	-115	dB
Input Capacitance	(Gain = 10) (Gain = 50)	C_{in}	- -	25 25	- -	pF pF
Effective Input Impedance	(Note 6) (Gain = 10) (Gain = 50)	 Z_{inI} Z_{inI}	 - -	 30 30	 - -	 kΩ kΩ
Noise (Referred to Input)	(Gain = 10) (Gain = 50)		- -	- -	20 4	μV_{rms} μV_{rms}
Accuracy (Current Channel)						
Bipolar Offset Error	(Note 1)	VOS_I	-	±0.001	-	%F.S.
Full-Scale Error	(Note 1)	FSE_I	-	±0.001	-	%F.S.
Analog Inputs (Voltage Channel)						
Maximum Differential Input Voltage Range	{(V_{VIN+}) - (V_{VIN-})}	V_{IN}	-	-	500	mV_{P-P}
Total Harmonic Distortion		THD_V	62	-	-	dB
Common Mode + Signal on VIN+ or VIN-			VA-	-	VA+	V
Crosstalk with Current Channel at Full Scale	(50, 60 Hz)		-	-	-70	dB
Input Capacitance		C_{inV}	-	0.2	-	pF
Effective Input Impedance	(Note 6)	Z_{inV}	-	5	-	MΩ
Noise (Referred to Input)			-	-	250	μV_{rms}
Accuracy (Voltage Channel)						
Bipolar Offset Error	(Note 1)	VOS_V	-	±0.01	-	%F.S.
Full-Scale Error	(Note 1)	FSE_V	-	±0.01	-	%F.S.

Notes:
1. Bipolar Offset Errors and Full-Scale Gain Errors for the current and voltage channels refer to the respective Irms Register and Vrms Register output, when the device is operating in 'continuous computation cycles' data acquisition mode, *after* offset/gain system calibration sequences have been executed. These specs do *not* apply to the error of the Instantaneous Current/Voltage Register output.
2. Specifications guaranteed by design, characterization, and/or test.
3. Analog signals are relative to VA- and digital signals to DGND unless otherwise noted.
4. In requiring VA+ = VD+ =5 V ±10%, note that it is allowable for VA+, VD+ to differ by as much as ±200 mV, as long as VA+ > VD+.
5. Note that "Sps" is an abbreviation for units of "samples per second".
6. Effective Input Impedance (Zin) is determined by clock frequency (DCLK) and Input Capacitance (IC). Zin = 1/(IC*DCLK/4). Note that DCLK = MCLK / K.

ANALOG CHARACTERISTICS (Continued)

Parameter		Symbol	Min	Typ	Max	Unit
Dynamic Characteristics						
Phase Compensation Range (Voltage Channel, 60 Hz)			-2.4	-	+2.5	°
High Rate Filter Output Word Rate (Both Channels)		OWR	-	DCLK/1024	-	Sps
Input Sample Rate DCLK = MCLK/K			-	DCLK/8	-	Sps
Full Scale DC Calibration Range (Note 7)		FSCR	25	-	100	%F.S.
Channel-to-Channel Time-Shift Error (when PC[6:0] bits are set to "0000000")				1.0		µs
High Pass Filter Pole Frequency -3 dB			-	0.5	-	Hz
Power Supplies						
Power Supply Currents (Active State)	I_{A+}	PSCA	-	1.3	-	mA
	I_{D+} (VD+ = 5 V)	PSCD	-	2.9	-	mA
	I_{D+} (VD+ = 3.3 V)	PSCD	-	1.7	-	mA
Power Consumption (Note 8)	Active State (VD+ = 5 V)	PC	-	21	25	mW
	Active State (VD+ = 3.3 V)		-	11.6	-	mW
	Stand-By State		-	6.75	-	mW
	Sleep State		-	10	-	µW
Power Supply Rejection Ratio for Current Channel (Note 9)	(50, 60 Hz) (Gain = 10)	PSRR	56	-	-	dB
	(50, 60 Hz) (Gain = 50)	PSRR	75	-	-	dB
Power Supply Rejection Ratio for Voltage Channel	(50, 60 Hz) (Note 9)	PSRR	-	65	-	dB
PFMON Power-Fail Detect Threshold (Note 10)		PMLO	2.3	2.45	-	V
PFMON "Power-Restored" Detect Threshold (Note 11)		PMHI	-	2.55	2.7	V

Notes:
7. The minimum FSCR is limited by the maximum allowed gain register value.
8. All outputs unloaded. All inputs CMOS level.
9. Definition for PSRR: VREFIN tied to VREFOUT, VA+ = VD+ = 5 V, a 150 mV zero-to-peak sinewave (frequency = 60 Hz) is imposed onto the +5 V supply voltage at VA+ and VD+ pins. The "+" and "-" input pins of both input channels are shorted to VA-. Then the CS5460A is commanded to 'continuous computation cycles' data acquisition mode, and digital output data is collected for the channel under test. The zero-peak value of the digital sinusoidal output signal is determined, and this value is converted into the zero-peak value of the sinusoidal voltage that would need to be applied at the channel's inputs, in order to cause the same digital sinusoidal output. This voltage is then defined as Veq. PSRR is then (in dB):

$$PSRR = 20 \cdot \log\left\{\frac{0.150V}{V_{eq}}\right\}$$

10. When voltage level on PFMON is sagging, and LSD bit is 0, the voltage at which LSD bit is set to 1.
11. Assuming that the LSD bit has been set to 1 (because PFMON voltage fell below PMLO), then if/when the PFMON voltage starts to rise again, PMHI is the voltage level (on PFMON pin) at which the LSD bit can be permanently reset back to 0 (without instantaneously changing back to 1). Attempts to reset the LSD bit before this condition is true will not be successful. This condition indicates that power has been restored. Typically, for a given sample, the PMHI voltage will be ~100 mV above the PMLO voltage.

VREFOUT REFERENCE OUTPUT VOLTAGE

Parameter	Symbol	Min	Typ	Max	Unit
Reference Output					
Output Voltage	REFOUT	+2.4	-	+2.6	V
VREFOUT Temperature Coefficient (Note 12)	$T_{VREFOUT}$	-	30	60	ppm/°C
Load Regulation (Output Current 1 µA Source or Sink)	ΔV_R	-	6	10	mV
Reference Input					
Input Voltage Range	VREFIN	+2.4	+2.5	+2.6	V
Input Capacitance		-	4	-	pF
Input CVF Current		-	25	-	nA

Notes: 12. The voltage at VREFOUT is measured across the temperature range. From these measurements the following formula is used to calculate the VREFOUT Temperature Coefficient:.

$$T_{VREFOUT} = \left(\frac{(VREFOUT_{MAX} - VREFOUT_{MIN})}{VREFOUT_{AVG}}\right)\cdot\left(\frac{1}{T_{A}MAX - T_{A}MIN}\right)\cdot\left(1.0 \times 10^{6}\right)$$

5V DIGITAL CHARACTERISTICS

(T_A = -40 °C to +85 °C; VA+ = VD+ = 5 V ±10% VA-, DGND = 0 V) (See Notes 3, 4, and 13)

Parameter	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	V_{IH}				
All Pins Except XIN, SCLK and $\overline{RESET}$		0.6 VD+	-	-	V
XIN		(VD+) - 0.5	-	-	V
SCLK and $\overline{RESET}$		0.8 VD+	-	-	V
Low-Level Input Voltage	V_{IL}				
All Pins Except XIN, SCLK, and $\overline{RESET}$		-	-	0.8	V
XIN		-	-	1.5	V
SCLK and $\overline{RESET}$		-	-	0.2 VD+	V
High-Level Output Voltage (except XOUT) I_{out} = +5 mA	V_{OH}	(VD+) - 1.0	-	-	V
Low-Level Output Voltage (except XOUT) I_{out} = -5 mA	V_{OL}	-	-	0.4	V
Input Leakage Current (Note 14)	I_{in}	-	±1	±10	µA
High Impedance State Leakage Current	I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance	C_{out}	-	5	-	pF

13. Note that the 5 V characteristics are guaranteed by characterization. Only the more rigorous 3.3 V digital characteristics are actually verified during production test.
14. Applies to all INPUT pins except XIN pin (leakage current < 50 µA) and MODE pin (leakage current < 25 µA).

3.3 V DIGITAL CHARACTERISTICS

(T_A = -40 °C to +85 °C; VA+ = 5 V ±10%, VD+ = 3.3 V ±10%; VA-, DGND = 0 V) (See Notes 3, 4, and 13)

Parameter	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	V_{IH}				
All Pins Except XIN, XOUT, SCLK, and $\overline{\text{RESET}}$		0.6 VD+	-	-	V
XIN		(VD+) - 0.5	-	-	V
SCLK and $\overline{\text{RESET}}$		0.8 VD+	-	-	V
Low-Level Input Voltage	V_{IL}				
All Pins Except XIN, XOUT, SCLK, and $\overline{\text{RESET}}$		-	-	0.48	V
XIN		-	-	0.3	V
SCLK and $\overline{\text{RESET}}$		-	-	0.2 VD+	V
High-Level Output Voltage (except XIN, XOUT) I_{out} = +5 mA	V_{OH}	(VD+) - 1.0	-	-	V
Low-Level Output Voltage (except XIN, XOUT) I_{out} = -5 mA	V_{OL}	-	-	0.4	V
Input Leakage Current (Note 14)	I_{in}	-	±1	±10	µA
3-State Leakage Current	I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance	C_{out}	-	5	-	pF

Notes: 15. All measurements performed under static conditions.

16. If VD+ = 3 V and if XIN input is generated using crystal, then XIN frequency must remain between 2.5 MHz - 5.0 MHz. If using oscillator, full XIN frequency range is available, see *Switching Characteristics*.

ABSOLUTE MAXIMUM RATINGS

(DGND = 0 V; See Note 17) WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Parameter	Symbol	Min	Typ	Max	Unit
DC Power Supplies (Notes 18 and 19)					
Positive Digital	VD+	-0.3	-	+6.0	V
Positive Analog	VA+	-0.3	-	+6.0	V
Negative Analog	VA-	+0.3	-	-6.0	V
Input Current, Any Pin Except Supplies (Note 20, 21, and 22)	I_{IN}	-	-	±10	mA
Output Current	I_{OUT}	-	-	±25	mA
Power Dissipation (Note 23)	P_D	-	-	500	mW
Analog Input Voltage All Analog Pins	V_{INA}	(VA-) - 0.3	-	(VA+) + 0.3	V
Digital Input Voltage All Digital Pins	V_{IND}	DGND - 0.3	-	(VD+) + 0.3	V
Ambient Operating Temperature	T_A	-40	-	85	°C
Storage Temperature	T_{stg}	-65	-	150	°C

Notes: 17. All voltages with respect to ground.

18. VA+ and VA- must satisfy {(VA+) - (VA-)} ≤ +6.0 V.
19. VD+ and VA- must satisfy {(VD+) - (VA-)} ≤ +6.0 V.
20. Applies to all pins including continuous over-voltage conditions at the analog input (AIN) pins.
21. Transient current of up to 100 mA will not cause SCR latch-up.
22. Maximum DC input current for a power supply pin is ±50 mA.
23. Total power dissipation, including all input currents and output currents.

SWITCHING CHARACTERISTICS

(T_A = -40 °C to +85 °C; VA+ = 5.0 V ±10%; VD+ = 3.0 V ±10% or 5.0 V ±10%; VA- = 0.0 V; Logic Levels: Logic 0 = 0.0 V, Logic 1 = VD+; CL = 50 pF))

Parameter	Symbol	Min	Typ	Max	Unit
Master Clock Frequency Crystal/Internal Gate Oscillator (Note 24)	MCLK	2.5	4.096	20	MHz
Master Clock Duty Cycle		40	-	60	%
CPUCLK Duty Cycle (Note 25)		40		60	%
Rise Times Any Digital Input Except SCLK (Note 26)	t_{rise}	-	-	1.0	µs
SCLK		-	-	100	µs
Any Digital Output		-	50	-	ns
Fall Times Any Digital Input Except SCLK (Note 26)	t_{fall}	-	-	1.0	µs
SCLK		-	-	100	µs
Any Digital Output		-	50	-	ns
Start-up					
Oscillator Start-Up Time XTAL = 4.096 MHz (Note 27)	t_{ost}	-	60	-	ms
Serial Port Timing					
Serial Clock Frequency	SCLK	-	-	2	MHz
Serial Clock Pulse Width High	t_1	200	-	-	ns
Pulse Width Low	t_2	200	-	-	ns
SDI Timing					
$\overline{CS}$ Falling to SCLK Rising	t_3	50	-	-	ns
Data Set-up Time Prior to SCLK Rising	t_4	50	-	-	ns
Data Hold Time After SCLK Rising	t_5	100	-	-	ns
SCLK Falling Prior to $\overline{CS}$ Disable	t_6	100	-	-	ns
SDO Timing					
$\overline{CS}$ Falling to SDI Driving	t_7	-	20	50	ns
SCLK Falling to New Data Bit	t_8	-	20	50	ns
$\overline{CS}$ Rising to SDO Hi-Z	t_9	-	20	50	ns
Auto-boot Timing					
Serial Clock Pulse Width High	t_{10}		8		MCLK
Pulse Width Low	t_{11}		8		MCLK
MODE setup time to RESET Rising	t_{12}	50			ns
RESET rising to $\overline{CS}$ falling	t_{13}	48			MCLK
$\overline{CS}$ falling to SCLK rising	t_{14}	100	8		MCLK
SCLK falling to $\overline{CS}$ rising	t_{15}		16		MCLK
CS rising to driving MODE low (to end auto-boot sequence).	t_{16}	50			ns
SDO guaranteed setup time to SCLK rising	t_{17}	100			ns

Notes: 24. Device parameters are specified with a 4.096 MHz clock, yet, clocks between 3 MHz to 20 MHz can be used. However, for input frequencies over 5 MHz, an external oscillator must be used.

25. If external MCLK is used, then duty cycle must be between 45% and 55% to maintain this specification.

26. Specified using 10% and 90% points on wave-form of interest. Output loaded with 50 pF.

27. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.

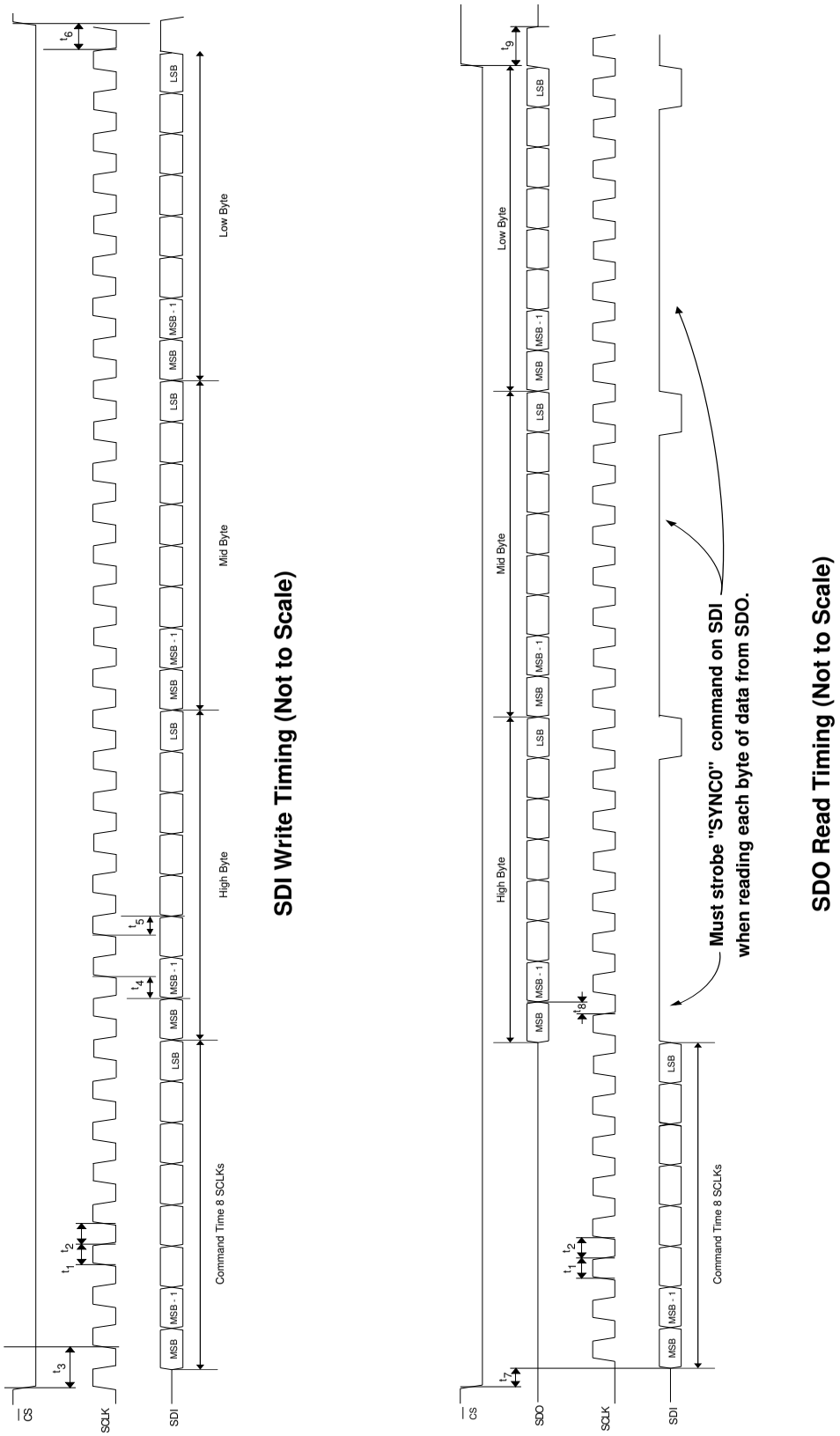

Figure 1. CS5460A Read and Write Timing Diagrams

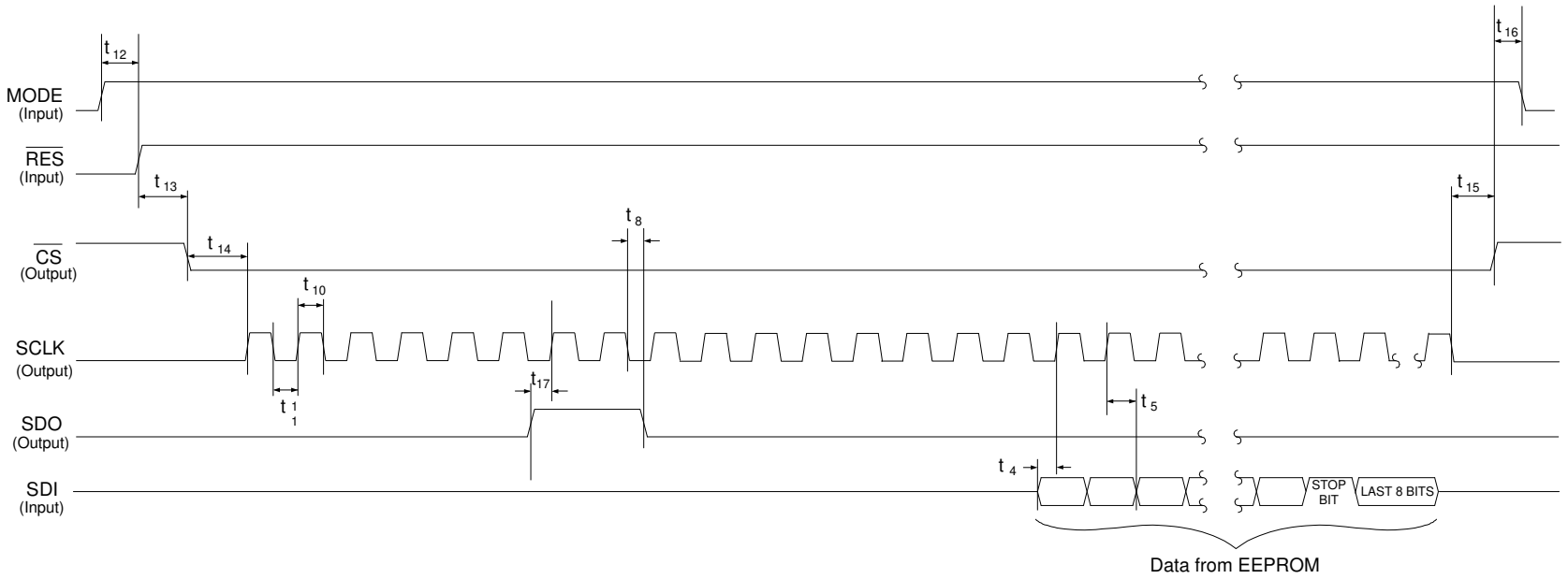

Figure 2. CS5460A Auto-boot Sequence Timing

2. OVERVIEW

The CS5460A is a CMOS monolithic power measurement device with a real power/energy computation engine. The CS5460A combines two programmable gain amplifiers, two ΔΣ modulators, two high rate filters, system calibration, and rms/power calculation functions to provide instantaneous voltage/current/power data samples as well as periodic computation results for real (billable) energy, V_{RMS}, and I_{RMS}. In order to accommodate lower cost metering applications, the CS5460A can also generate pulse-train signals on certain output pins, for which the number of pulses emitted on the pins is proportional to the quantity of real (billable) energy registered by the device.

The CS5460A is optimized for power measurement applications and is designed to interface to a shunt or current transformer to measure current, and to a resistive divider or potential transformer to measure voltage. To accommodate various input voltage levels, the current channel includes a programmable gain amplifier (PGA) which provides two full-scale input levels, while the voltage channel's PGA provides a single input voltage range. With a single +5 V supply on VA+/-, both of the CS5460A's input channels can accomodate common mode + signal levels between -0.25 V and VA+.

The CS5460A includes two high-rate digital filters (one per channel), which decimate/integrate the output from the 2 ΔΣ modulators. The filters yield 24-bit output data at a (MCLK/K)/1024 output word rate (OWR). The OWR can be thought of as the effective sample frequency of the voltage channel and the current channel.

To facilitate communication to a microcontroller, the CS5460A includes a simple three-wire serial interface which is SPI™ and Microwire™ compatible. The serial port has a Schmitt Trigger input on its SCLK (serial clock) and $\overline{\text{RESET}}$ pins to allow for slow rise time signals.

2.1 Theory of Operation

A computational flow diagram for the two data paths is shown in Fig. 3. The reader should refer to this diagram while reading the following data processing description, which is covered block-by-block.

2.1.1 ΔΣ Modulators

The analog waveforms at the voltage/current channel inputs are subject to the gains of the input PGAs (not shown in Figure 3). These waveforms are then sampled by the delta-sigma modulators at a rate of (MCLK/K)/8 Sps.

2.1.2 High-rate Digital Low-pass Filters

The data is then low-pass filtered, to remove high-frequency noise from the modulator output. Referring to Figure 3, the high rate filter on the voltage channel is implemented as a fixed $Sinc^2$ filter. The current channel uses a $Sinc^4$ filter, which allows the current channel to make accurate measurements over a wider span of the total input range, in comparison to the accuracy range of the voltage channel. (This subject is discussed more in *Section 2.2.1*)

Also note from Figure 3 that the digital data on the voltage channel is subjected to a variable time-delay filter. The amount of delay depends on the value of the seven phase compensation bits (see *Phase Compensation*). Note that when the phase compensation bits PC[6:0] are set to their default setting of "0000000" (and if MCLK/K = 4.096 MHz) then the nominal time delay that is imposed on the original analog voltage input signal, with respect to the original analog current input signal, is ~1.0 µs. This translates into a delay of ~0.0216 degrees at 60 Hz.

2.1.3 Digital Compensation Filters

The data from both channels is then passed through two FIR compensation filters, whose purpose is to compensate for the magnitude roll-off of the low-pass filtering operation (mentioned earlier).

2.1.4 Digital High-pass Filters

Both channels provide an optional high-pass filter (denoted as "HPF" in Figure 3) which can be engaged into the signal path, to remove the DC content from the current/voltage signal before the RMS/energy calculations are made. These filters are activated by enabling certain bits in the Configuration Register.

If the high-pass filter is engaged in only one of the two channels, then the all-pass filter (see "APF" in

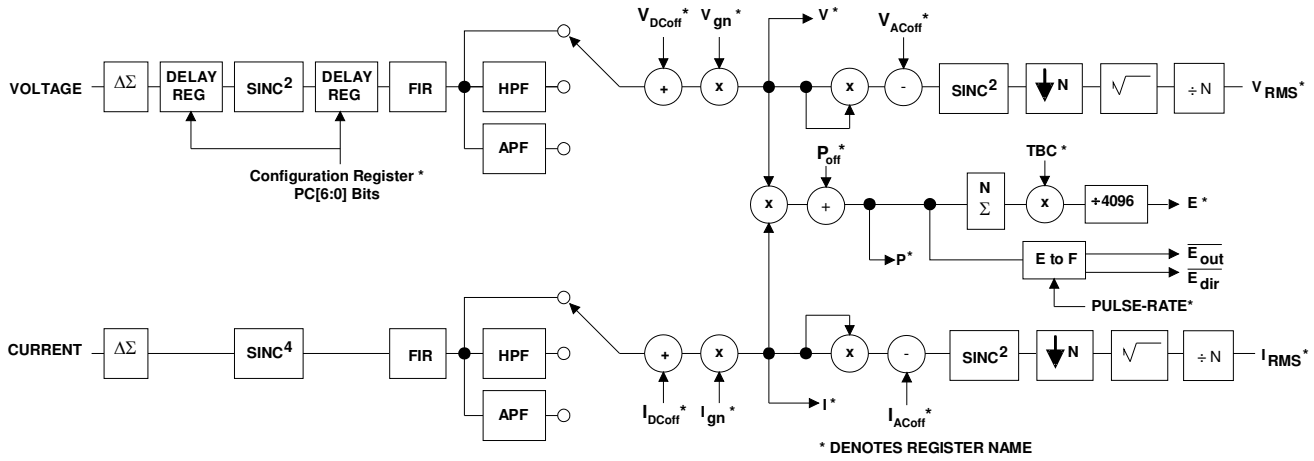

Figure 3. Data Flow.

Figure 3) will be enabled on the other channel; in order to preserve the relative phase relationship between the voltage-sense and current-sense input signals. For example, if the HPF is engaged for the voltage channel, but not the current channel, then the APF will be engaged in the current channel, to nullify the additional phase delay introduced by the high-pass filter in the current channel.

2.1.5 Overall Filter Response

When the CS5460A is driven with a 4.096 MHz clock (K = 1), the composite magnitude response (over frequency) of the voltage channel's input filter network is shown in Figure 4, while the composite magnitude response of the current channel's input filter network is given in Figure 5. Note that the composite filter response of both channels scales with MCLK frequency and K.

2.1.6 Gain and DC Offset Adjustment

After filtering, the instantaneous voltage and current digital codes are subjected to offset/gain adjustments, based on the values in the DC offset registers (additive) and the gain registers (multiplicative). These registers are used for calibration of the device (see *Section 3.8, Calibration*). After offset and gain, the 24-bit instantaneous data sample values are stored in the Instantaneous Voltage and Current Registers.

2.1.7 Real Energy and RMS Computations

The digital instantaneous voltage and current data is then processed further. Referring to Figure 3, the instantaneous voltage/current data samples are multiplied together (one multiplication for each pair of voltage/current samples) to form instantaneous (real) power samples. After each A/D conversion cycle, the new instantaneous power sample is stored in the Instantaneous Power Register.

The instantaneous power samples are then grouped into sets of N samples (where N = value in Cycle Count Register). The cumulative sum of each successive set of N instantaneous power is used to compute the result stored in the Energy Register, which will be proportional to the amount of real energy registered by the device during the most recent N A/D conversion cycles. Note from Figure 3 that the bits in this running energy sum are right-shifted 12 times (divided by 4096) to avoid overflow in the Energy Register. RMS calculations are also performed on the data using the last N instantaneous voltage/current samples, and these results can be read from the RMS Voltage Register and the RMS Current Register.

2.2 Performing Measurements

To summarize Section 2.1, the CS5460A performs measurements of instantaneous current and instantaneous voltage, and from this, performs computations of the corresponding instantaneous power, as well as periodic calculations of real energy, RMS current, and RMS voltage. These measurement/calculation results are available in the form of 24-bit signed and unsigned words. The scaling of all output words is normalized to unity

full-scale. Note that the 24-bit *signed* output words are expressed in two's complement format. The 24-bit data words in the CS5460A output registers represent values between 0 and 1 (for unsigned output registers) or between -1 and +1 (for signed output registers). A register value of 1 represents the maximum possible value. Note that a value of 1.0 is never actually obtained in the registers of the CS5460A. As an illustration, in any of the signed output registers, the maximum register value is [(2^23 - 1) / (2^23)] = 0.999999880791. After each A/D conversion, the CRDY bit will be asserted in the Status Register, and the $\overline{\text{INT}}$ pin will also become active if the CRDY bit is unmasked (in the Mask Register). The assertion of the CRDY bit indicates that new instantaneous 24-bit voltage and current samples have been collected, and these two samples have also been multiplied together to provide a corresponding instantaneous 24-bit power sample.

Table 1 conveys the typical relationship between the differential input voltage (across the "+" and "-" input pins of the voltage channel input) and the corresponding output code in the Instantaneous Voltage Register. Note that this table is applicable for the current channel if the current channel's PGA gain is set for the "10x" gain mode.

Input Voltage (DC)	Output Code (hexidecimal)	Output Code (decimal)
+250 mV	7FFFFF	8388607
14.9 nV to 44.7 nV	000001	1
-14.9 nV to 14.9 nV	000000	0
-44.7 nV to -14.9 nV	FFFFFF	-1
-250 mV	800000	-8388608

Table 1. Differential Input Voltage vs. Output Code

The V_{RMS}, I_{RMS}, and energy calculations are updated every N conversions (which is known as 1 "*computation cycle*"), where N is the value in the Cycle Count Register. At the end of each computation cycle, the DRDY bit in the Mask Register will be set, and the $\overline{\text{INT}}$ pin will become active if the DRDY bit is unmasked.

DRDY is set only after each computation cycle has completed, whereas the CRDY bit is asserted after each individual A/D conversion. Bits asserted by the CS5460A must be cleared before being asserted again. If the Cycle Count Register value (N) is set to 1, all output calculations are instantaneous, and DRDY will indicate when instantaneous calculations are finished, just like the CRDY bit. For the RMS results to be valid, the Cycle-Count Register must be set to a value greater than 10.

The computation cycle frequency is derived from the master clock, and has a value of (MCLK/K)/(1024*N). Under default conditions, with

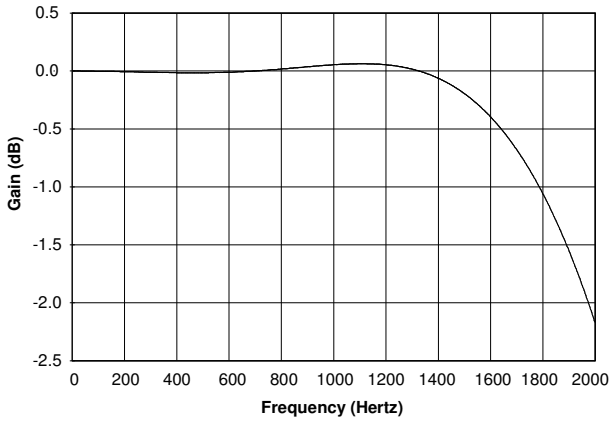

Figure 4. Voltage Input Filter Characteristics

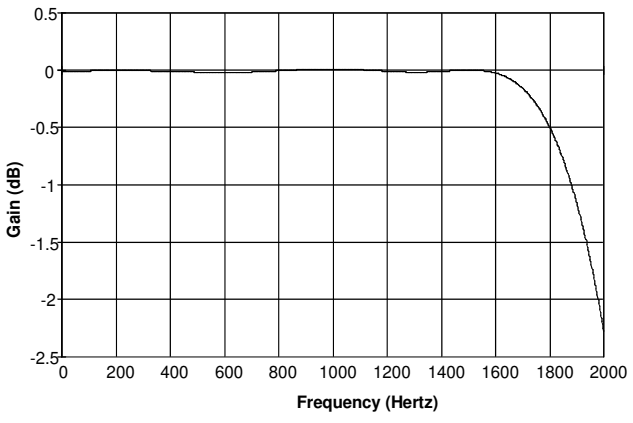

Figure 5. Current Input Filter Characteristics

a 4.096 MHz clock at XIN, and K = 1, instantaneous A/D conversions for voltage, current, and power are performed at a 4000 Sps rate, whereas I_{RMS}, V_{RMS}, and energy calculations are performed at a 1 Sps rate.

2.2.1 CS5460A Linearity Performance

Table 2 lists the range of input levels (as a percentage of full-scale) over which the (linearity + variation) of the results in the Vrms, Irms and Energy Registers are guaranteed to be within ±0.1 % of reading after the completion of each successive computation cycle. Note that until the CS5460A is calibrated (see Calibration) the *accuracy* of the CS5460A with respect to a reference line-voltage and line-current level on the power mains is not guaranteed to within ±0.1%. After both channels of the device are calibrated for offset/gain, the ±0.1% of reading spec will also reflect accuracy of the Vrms, Irms, and Energy Register results. Finally, observe that the maximum (full-scale) differential input voltage for the voltage channel (and current channel, when its PGA is set for 10x gain) is 250 mV (nominal). **If the gain registers of both channels are set to 1 (default) and the two DC offset registers are set to zero (default), then a 250mV DC signal applied to the voltage/current inputs will measure at (or near) the maximum value of 0.9999... in the RMS Current/Voltage Registers.** Remember that the RMS value of a 250 mV (DC) signal is also 250 mV. However, for either input channel, it would not be practical to inject a sinusoidal voltage with RMS value of 250 mV. This is because when the instantaneous value of such a sine wave is at or near the level of its positive/negative peak regions (over each cycle), the voltage level of this signal would exceed the maximum differential input voltage range of the input channels. The largest sine wave voltage signal that can be presented across the inputs, with no saturation of the inputs, is:

250 mV / sqrt(2) = ~176.78 mV (RMS),

which is ~70.7% of full-scale. This would imply that for the current channel, the (linearity+variation) tolerance of the RMS measurements for a purely sinusoidal 60 Hz input signal could be measured to within ±0.1% of reading over a magnitude range of 0.2% - 70.7% of the maximum full-scale differential input voltage level.

The range over which the (linearity + variation) will remain within ±0.1% can often be increased by selecting a value for the Cycle-Count Register such that the time duration of one computation cycle is equal to (or very close to) a *whole-number* of power-line cycles (and N must be greater than or equal to 4000). For example, with the cycle count set to 4200, the ±0.1% of reading (linearity + variation) range for measurement of a 60 Hz sinusoidal current-sense voltage signal can be increased beyond the range of 0.2% - 70.7%. The accuracy range will be increased because (4200 samples / 60 Hz) is a whole number of cycles (70). Note that this increase in the measurement range refers to an extension of the *low* end of the input scale (i.e., this does *not* extend the high-end of the range above 100% of full-scale). This enables accurate measurement of even smaller power-line current levels, thereby extending the load range over which the power meter can make accurate energy measurements. Increasing the accuracy range can be beneficial for power metering applications which require accurate power metering over a very large load range.

	Energy	Vrms	Irms
Range (% of FS)	0.1% - 100%	50% - 100%	0.2% - 100%
Max. Differential Input	*not applicable*	V-channel: ±250 mV	I-channel: ±250 mV 10x ±50 mV 50x
Linearity	0.1% of reading	0.1% of reading	0.1% of reading

Table 2. Available range of ±0.1% output linearity, with default settings in the gain/offset registers.

2.2.2 Single Computation Cycle (C=0)

Note that 'C' refers to the value of the C bit, contained in the 'Start Conversions' command (see Section 4.1). This commands instructs the CS5460A to perform conversions in 'single computation cycle' data acquisition mode. Based on the value in the Cycle Count Register, a single computation cycle is performed after a 'Start Conversions' command is sent to the serial interface. After the computations are complete, DRDY is set. 32 SCLKs are then needed to read out a calculation

result from one of several result registers. The first 8 SCLKs are used to clock in the command to determine which register is to be read. The last 24 SCLKs are used to read the desired register. After reading the data, the serial port remains in the *active state*, and waits for a new command to be issued. (See Section 3 for more details on reading register data from the CS5460A).

2.2.3 Continuous Computation Cycles (C=1)

When C = 1, the CS5460A will perform conversions in 'continuous computation cycles' data acquisition mode. Based on the information provided in the Cycle Count Register, computation cycles are repeatedly performed on the voltage and current channels (after every N conversions). Computation cycles cannot be started/stopped on a 'per-channel' basis. After each computation cycle is completed, DRDY is set. Thirty-two SCLKs are then needed to read a register. The first 8 SCLKs are used to clock in the command to determine which results register is to be read. The last 24 SCLKs are used to read out the 24-bit calculation result. While in this acquisition mode, the designer/programmer may choose to acquire (read) only those calculations required for their particular application, as DRDY repeatedly indicates the availability of new data. Note again that the MCU firmware must reset the DRDY bit to "0" before it can be asserted again.

Referring again to Figure 3, note that within the Irms and Vrms data paths, prior to the square-root operation, the instantaneous voltage/current data is low-pass filtered by a $Sinc^2$ filter. Then the data is decimated to every Nth sample. Because of the $Sinc^2$ filter operation, the first output for each channel will be invalid (i.e. all RMS calculations are invalid in the 'single computation cycle' data acquisition mode and the first RMS calculation results will be invalid in the 'continuous computation cycles' data acquisition mode). However, all energy calculations will be valid since energy calculations do not require this $Sinc^2$ operation.

If the 'Start Conversions' command is issued to the CS5460A (see *Section 4.1, Commands (Write Only)*), and if the 'C' bit in this command is set to a value of '1', the device will remain in its *active state*. Once commanded into *continuous computation cycles* data acquisition mode, the CS5460A will continue to perform A/D conversions on the voltage/current channels, as well as all subsequent calculations, until:

1) the 'Power-Up/Halt' command is received through the serial interface, or
2) loss of power, or
3) the RS bit in the Configuration Register is asserted ('software reset'), or
4) the /RESET pin is asserted and then de-asserted ('hardware reset').

2.3 Basic Application Circuit Configurations

Figure 6 shows the CS5460A connected to a service to measure power in a single-phase 2-wire system operating from a single power supply. Note that in this diagram the shunt resistor used to monitor the line current is connected on the "Line" (hot) side of the power mains. In most residential power metering applications, the power meter's current-sense shunt resistor is intentionally placed on the 'hot' side of the power mains in order to help detect any attempt by the subscriber to steal power. In this type of shunt-resistor configuration, note that the common-mode level of the CS5460A must be referenced to the hot side of the power line. This means that the common-mode potential of the CS5460A will typically oscillate to very high positive voltage levels, as well as very high negative voltage levels, with respect to earth ground potential. *The designer must therefore be careful* when attempting to interface the CS5460A's digital output lines to an external digital interface (such as a LAN connection or other communication network). Such digital communication networks may require that the CMOS-level digital interface to the meter is referenced to an earth-ground. In such cases, the CS5460A's digital serial interface pins *must be isolated* from the external digital interface, so that there is no conflict between the ground references of the meter and the external interface. The CS5460A and associate circuitry should be enclosed in a protective insulated case when used in this configuration, to avoid risk of harmful electric shock to humans/animals/etc.

Figure 7 shows how the same single-phase two-wire system can be metered while achieving

complete isolation from the power lines. This isolation is achieved using three transformers. One transformer is a general-purpose voltage transformer, used to supply the on-board DC power to the CS5460A. A second transformer is a high-precision, low-impedance voltage transformer (often called a 'potential transformer') with very little roll-off/phase delay, even at the higher harmonics. A current transformer is then used to sense the line current. A burden resistor placed across the secondary of the current transformer creates the current-sense voltage signal, for the CS5460A's current channel inputs. Because the CS5460A is not directly connected to the power mains, isolation is not required for the CS5460A's digital interface.

Figure 8 shows the CS5460A configured to measure power in a single-phase 3-wire system. In many 3-wire residential power systems within the United States, only the two Line terminals are available (neutral is not available). Figure 9 shows how the CS5460A can be configured to meter a 3-wire system when no neutral is available.

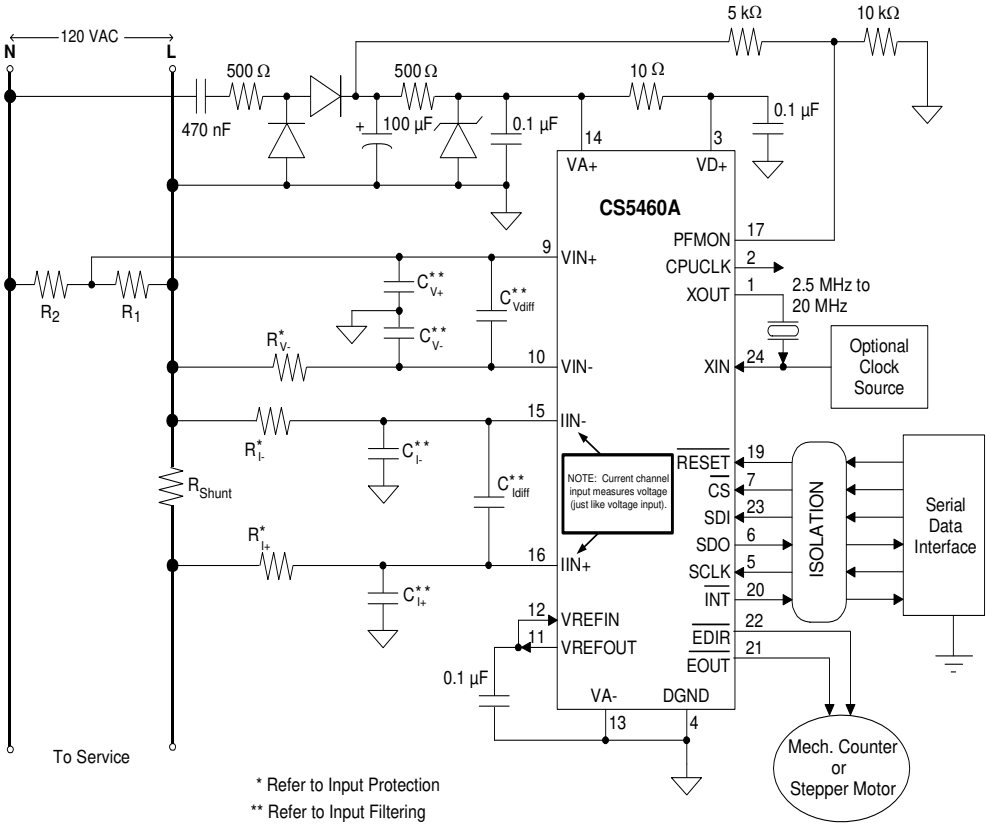

Figure 6. Typical Connection Diagram (One-Phase 2-Wire, Direct Connect to Power Line)

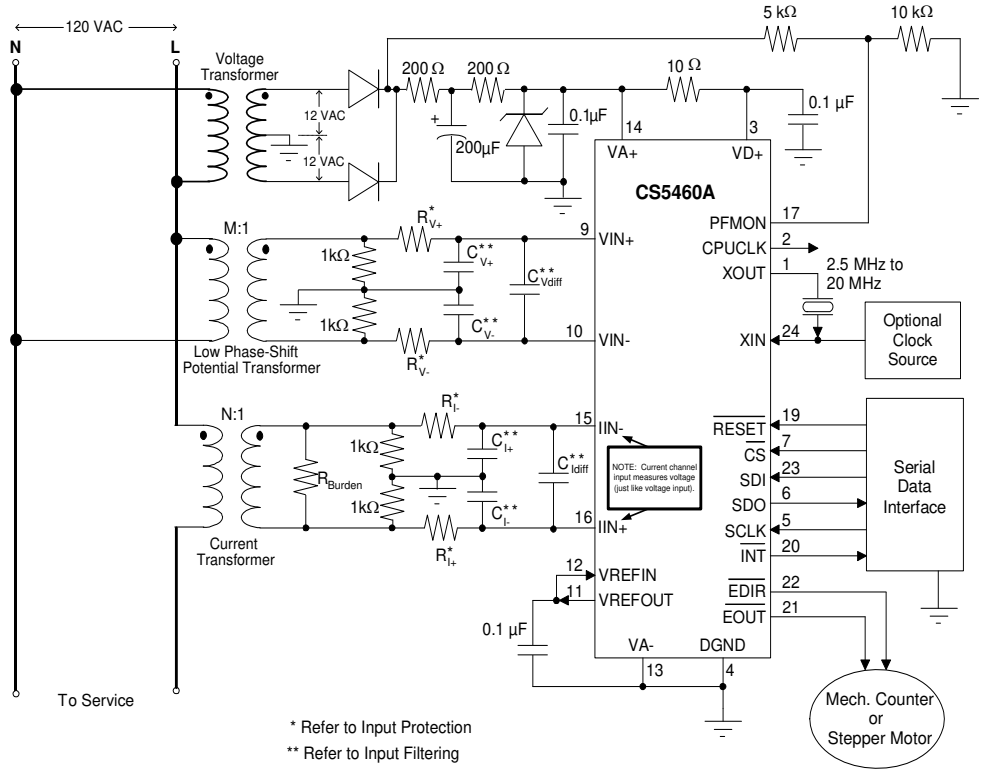

Figure 7. Typical Connection Diagram (One-Phase 2-Wire, Isolated from Power Line)

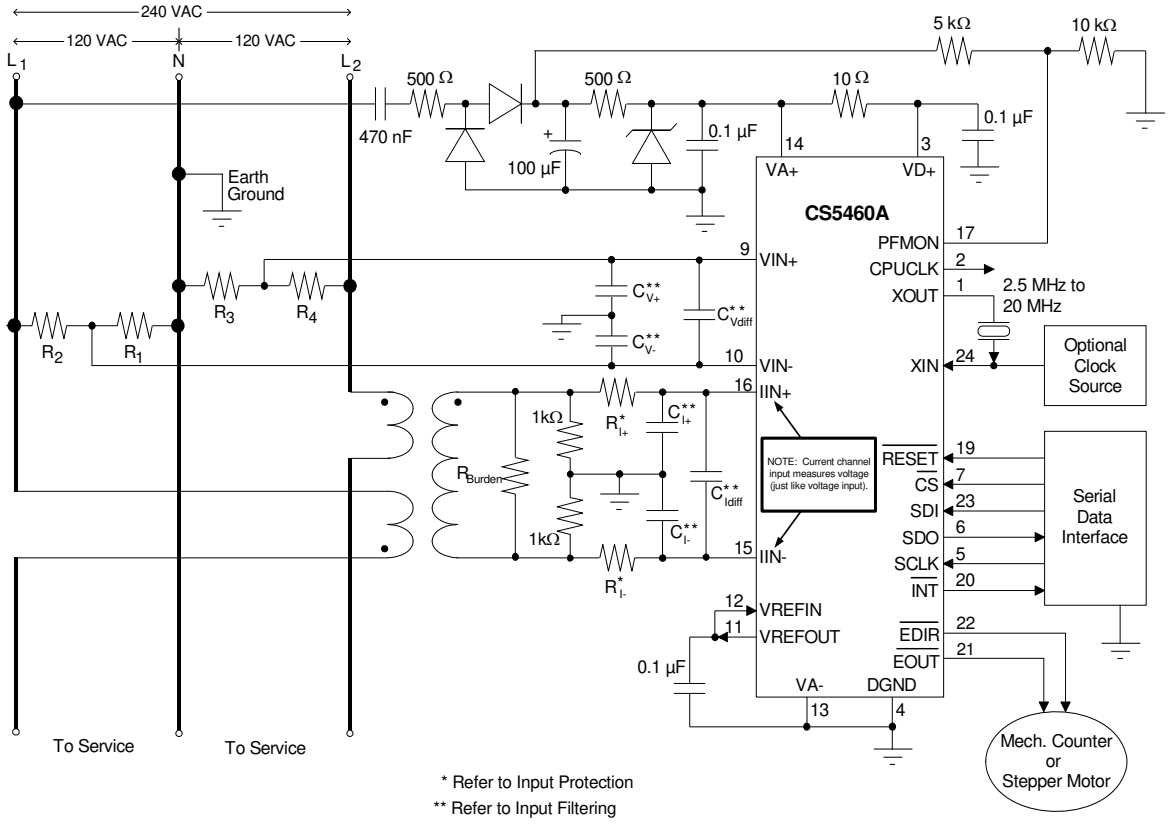

Figure 8. Typical Connection Diagram (One-Phase 3-Wire)

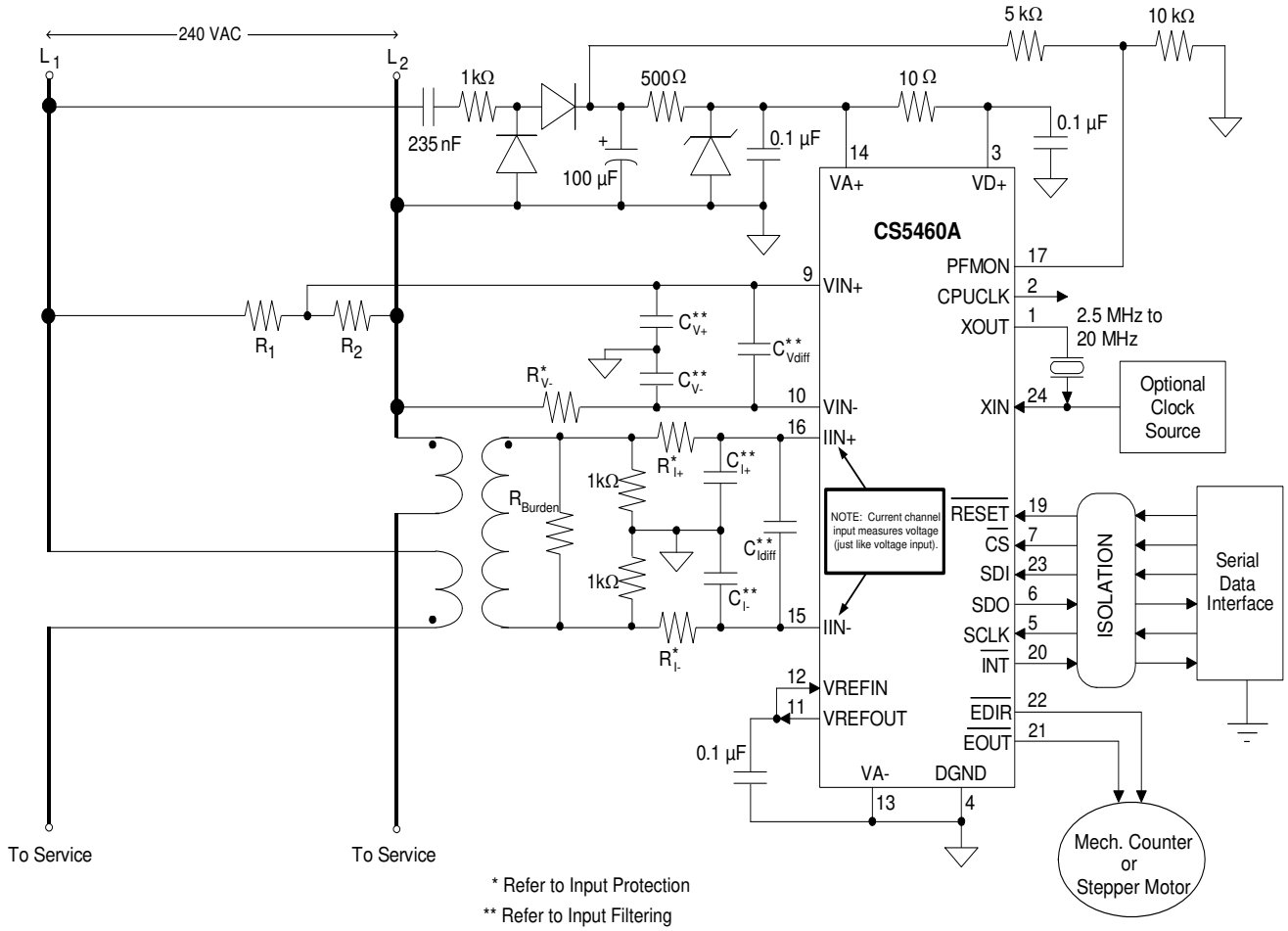

Figure 9. Typical Connection Diagram (One-Phase 3-Wire - No Neutral Available)

3. FUNCTIONAL DESCRIPTION

3.1 Pulse-Rate Output

As an alternative to reading the real energy through the serial port, the EOUT and EDIR pins provide a simple interface with which signed energy can be accumulated. Each EOUT pulse represents a predetermined quantity of energy. The quantity of energy represented in one pulse can be varied by adjusting the value in the Pulse-Rate Register. Corresponding pulses on the EDIR output pin signify that the sign of the energy is negative. Note that these pulses are not influenced by the value of the Cycle-Count Register, and they have no reliance on the computation cycle, described earlier. With MCLK = 4.096 MHz, K = 1, the pulses will have an average frequency (in Hz) equal to the frequency setting in the Pulse Rate Register when the input signals into the voltage and current channels cause full-scale readings in the Instantaneous Voltage and Current Registers. When MCLK/K is not equal to 4.096 MHz, the pulse-rate should be scaled by a factor of 4.096 MHz / (MCLK/K) to get the actual output pulse-rate.

EXAMPLE #1: For a power line with maximum rated levels of 250 V (RMS) and 20 A (RMS), the pulse-frequency on the EOUT pin needs to be 'IR' = 100 pulses-per-second (100 Hz) when the RMS-voltage and RMS-current levels on the power line are 220 V and 15 A respectively. To meet this requirement, the pulse-rate frequency ('PR') in the Pulse-Rate Register must be set accordingly.

After calibration, the first step to finding the value of 'PR' is to set the voltage and current sensor gain constants, K_V and K_I, such that there will be acceptable voltage levels on the CS5460A inputs when the power line voltage and current levels are at the maximum values of 250 V and 20 A. K_V and K_I are needed to determine the appropriate ratios of the voltage/current transformers and/or shunt resistor values to use in the front-end voltage/current sensor networks.

For a sinewave, the largest RMS value that can be accurately measured (without over-driving the inputs) will register ~0.7071 of the maximum DC input level. Since power signals are often not perfectly sinusoidal in real-world situations, and to provide for some over-range capability, the RMS Voltage Register and RMS Current Register is set to measure 0.6 when the RMS-values of the line-voltage and line-current levels are 250 V and 20 A. Therefore, when the RMS registers measure 0.6, the voltage level at the inputs will be 0.6 x 250 mV = 150 mV. The sensor gain constants, K_V and K_I, are determined by demanding that the voltage and current channel inputs should be 150 mV RMS when the power line voltage and current are at the maximum values of 250 V and 20 A.

K_V = 150 mV / 250 V = 0.0006

K_I = 150 mV / 20 A = 0.0075 Ω

These sensor gain constants are used to calculate what the input voltage levels will be on the CS5460A inputs when the line-voltage and line-current are 220 V and 15 A. These values are V_{Vnom} and V_{Inom}.

$V_{Vnom} = K_V * 220\ V = 132\ mV$

$V_{Inom} = K_I * 15\ A = 112.5\ mV$

The pulse rate on EOUT will be at 'PR' pulses per second (Hz) when the RMS-levels of voltage/current inputs are at 250 mV. When the voltage/current inputs are set at V_{Vnom} and V_{Inom}, the pulse rate needs to be 'IR' = 100 pulses per second. IR will be some percentage of PR. The percentage is defined by the ratios of V_{Vnom}/250 mV and V_{Inom}/250 mV with the following formula:

$$PulseRate = IR = PR \cdot \frac{V_{Vnom}}{250mV} \cdot \frac{V_{Inom}}{250mV}$$

From this equation the value of 'PR' is shown as:.

$$PR = \frac{IR}{\frac{V_{Vnom}}{250mV} \times \frac{V_{Inom}}{250mV}} = \frac{100Hz}{\frac{132mV}{250mV} \times \frac{112.5mV}{250mV}}$$

Therefore the Pulse-Rate Register is set to ~420.875 Hz, or 0x00349C.

The above equation is valid when current channel is set to x10 gain. If current channel gain is set to x50, then the equation becomes:

$$PR = \frac{IR}{\frac{V_{Vnom}}{250mV} \times \frac{V_{Inom}}{50mV}}$$

EXAMPLE #2: The required number of pulses per unit energy present at EOUT is specified to be 500 pulses/kW-hr; given that the maximum line-voltage is 250 V (RMS) and the maximum line-current is 20 A (RMS). In such a situation, the nominal line voltage and current do not determine the appropriate pulse-rate setting. Instead, the maximum line levels must be considered. As before, the given maximum line-voltage and line-current levels are used to determine K_V and K_I:

K_V = 150 mV / 250 V = 0.0006

K_I = 150 mV / 20 A = 0.0075 Ω

Again the sensor gains are calculated such that the maximum line-voltage and line-current levels will measure as 0.6 in the RMS Voltage Register and RMS Current Register.

The required Pulse-Rate Register setting is now determined by using the following equation:

$$PR = 500\frac{pulses}{kW \cdot hr} \cdot \frac{1hr}{3600s} \cdot \frac{1kW}{1000W} \cdot \frac{250mV}{K_V} \cdot \frac{250mV}{K_I}$$

Therefore PR = ~1.929 Hz.

Note that the Pulse-Rate Register cannot be set to a frequency of exactly 1.929 Hz. The closest setting that the Pulse-Rate Register can obtain is 0x00003E = 1.9375 Hz. To improve the accuracy, either gain register can be programmed to correct for the round-off error in PR. This value would be calculated as

$$Ign \text{ or } Vgn = \frac{PR}{1.929} \cong 1.00441 = 0x404830$$

In the last example, suppose a value for MCLK/K of 3.05856 MHz. When MCLK/K is not equal to 4.096 MHz, the result for 'PR' that is calculated for the Pulse-Rate Register must be scaled by a correction factor of: 4.096 MHz / (MCLK/K). In this case the result is scaled by 4.096/3.05856 to get a final PR result of ~2.583 Hz.

3.2 Pulse Output for Normal Format, Stepper Motor Format and Mechanical Counter Format

The duration and shape of the pulse outputs at the EOUT and EDIR pins can be set for three different output formats. The default setting is for *Normal* output pulse format. When the pulse is set to either of the other two formats, the time duration and/or the relative timing of the EOUT and EDIR pulses is increased/varied such that the pulses can drive either an electro-mechanical counter or a stepper motor. The EOUT and EDIR output pins are capable of driving certain low-voltage/low-power counters/stepper motors directly. This depends on the drive current and voltage level requirements of the counter/motor. The ability to set the pulse output format to one of the three available formats is controlled by setting certain bits in the Control Register.

3.2.1 Normal Format

Referring to the description of the Control Register in *Section 5., Register Descriptions*, if both the MECH and STEP bits are set to '0', the pulse output format at the EOUT and EDIR pins is illustrated in Figure 10. These are active-low pulses with very short duration. The pulse duration is an integer multiple of MCLK cycles, approximately equal to 1/16 of the period of the contents of the Pulse-Rate Register. However for Pulse-Rate Register settings less than the sampling rate (which is [MCLK/8]/1024), the pulse duration will remain at a constant duration, which is equal to the duration of the pulses when the Pulse-Rate Register is set to [MCLK/K]/1024. The maximum pulse frequency from the EOUT pin is therefore [MCLK/K]/16. When energy is positive, EDIR is always high. When energy is negative, EDIR has the same output as EOUT. When MCLK/K is not equal to 4.096 MHz, the true pulse-rate can be found by first calculating what the pulse-rate would be if a 4.096 MHz crystal is used (with K = 1) and then scaling the result by a factor of (MCLK/K) / 4.096 MHz.

When set to run in *Normal* pulse output format, the pulses may be sent out in "bursts" depending on both the value of the Pulse-Rate Register as well as the amount of billable energy that was registered by the CS5460A over the most recent A/D sampling period, which is (in Hz): 1 / [(MCLK/K) / 1024]. A running total of the energy accumulation is maintained in an internal register (not accessible to the user) inside the CS5460A. If the amount of energy that has accumulated in this register over the most recent A/D sampling period is equal to or greater than the amount of energy that is repre-

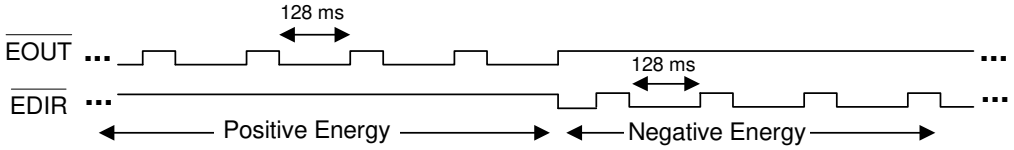

Figure 11. Mechanical Counter Format on $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$

sented by one pulse, the CS5460A will issue a "burst" of one or more pulses on $\overline{\text{EOUT}}$ (and also possibly on $\overline{\text{EDIR}}$). The CS5460A will issue as many pulses as are necessary to reduce the running energy accumulation value in this register to a value that is less than the energy represented in one pulse. If the amount of energy that has been registered over the most recent sampling period is large enough that it cannot be expressed with only one pulse, then a burst of pulses will be issued, possibly followed by a period of time during which there will be no pulses, until the next A/D sampling period occurs. After the pulse or pulses are issued, a certain residual amount of energy may be left over in this internal energy accumulation register, which is always less (in magnitude) than the amount of energy represented by one pulse. In this situation, the residual energy is not lost or discarded, but rather it is maintained and added to the energy that is accumulated during the next A/D conversion cycle. The amount of residual energy that can be left over becomes larger as the Pulse-Rate Register is set to lower and lower values, because lower Pulse-Rate Register values correspond to a higher amount of energy per pulse (for a given calibration).

3.2.2 Mechanical Counter Format

Setting the MECH bit in the Control Register to '1' and the STEP bit to '0' enables wide-stepping pulses for mechanical counters and similar discrete counter instruments. In this format, active-low pulses are 128 ms wide when using a 4.096 MHz crystal and K = 1. When energy is positive, the pulses appear on $\overline{\text{EOUT}}$. When energy is negative, pulses appear on $\overline{\text{EDIR}}$. To insure that pulses will not occur at a rate faster than the 128 ms pulse duration, or faster than the mechanical counter can accommodate, the Pulse-Rate Register should be set to an appropriate value. Because the duration of each pulse is set to 128 ms, the maximum output pulse frequency is limited to ~7.8 Hz (for MCLK/K = 4.096 MHz). For values of MCLK / K different than 4.096 MHz, the duration of one pulse is (128 * 4.096 MHz) / (MCLK / K) milliseconds. See Figure 11 for a diagram of the typical pulse output.

3.2.3 Stepper Motor Format

Setting the STEP bit in the Control Register to '1' and the MECH bit to '0' transforms the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins into two stepper motor phase outputs. When enough energy has been registered by the CS5460A to register one positive/negative energy

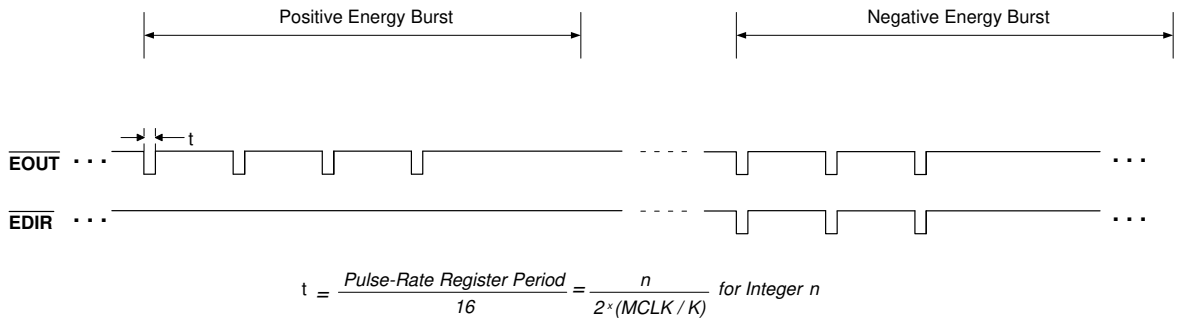

Figure 10. Time-plot representation of pulse output for a typical burst of pulses (Normal Format)

pulse, one of the output pins (either $\overline{\text{EOUT}}$ or $\overline{\text{EDIR}}$) changes state. When the CS5460A must issue another energy pulse, the other output changes state. The direction the motor will rotate is determined by the order of the state changes. When energy is positive, $\overline{\text{EOUT}}$ will lead $\overline{\text{EDIR}}$ such that the $\overline{\text{EOUT}}$ pulse train will lead the $\overline{\text{EDIR}}$ pulse train by ~1/4 of the periods of these two pulse train signal. When energy is negative, $\overline{\text{EDIR}}$ will lead $\overline{\text{EOUT}}$ in a similar manner. See Figure 12.

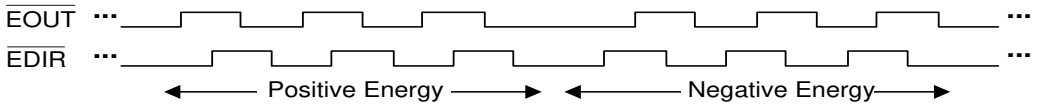

Figure 12. Stepper Motor Format on $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$

3.3 Auto-boot Mode Using EEPROM

The CS5460A has a MODE pin. When the MODE pin is set to logic low, the CS5460A is in normal operating mode, called *host mode*. This mode denotes the normal operation of the part, that has been described so far. But when this pin is set to logic high, the CS5460A *auto-boot mode* is enabled. In auto-boot mode, the CS5460A is configured to request a memory download from an external serial EEPROM. The download sequence is initiated by driving the $\overline{\text{RESET}}$ pin to logic high. Auto-boot mode allows the CS5460A to operate without the need for a microcontroller. Note that if the MODE pin is left unconnected, it will default to logic low because of an internal pull-down on the pin.

3.3.1 Auto-boot Configuration

Figure 13 shows the typical connections between the CS5460A and a serial EEPROM for proper auto-boot operation. In this mode, $\overline{\text{CS}}$ and SCLK are driven outputs. SDO is always an output. During the auto-boot sequence, the CS5460A drives $\overline{\text{CS}}$ low, provides a clock output on SCLK, and drives out-commands on SDO. It receives the EEPROM data on SDI. The serial EEPROM must be programmed with the user-specified commands and register data that will be used by the CS5460A to change any of the default register values (if desired) and begin conversions.

Figure 13 also shows the external connections that would be made to a calibrator device, such as a PC

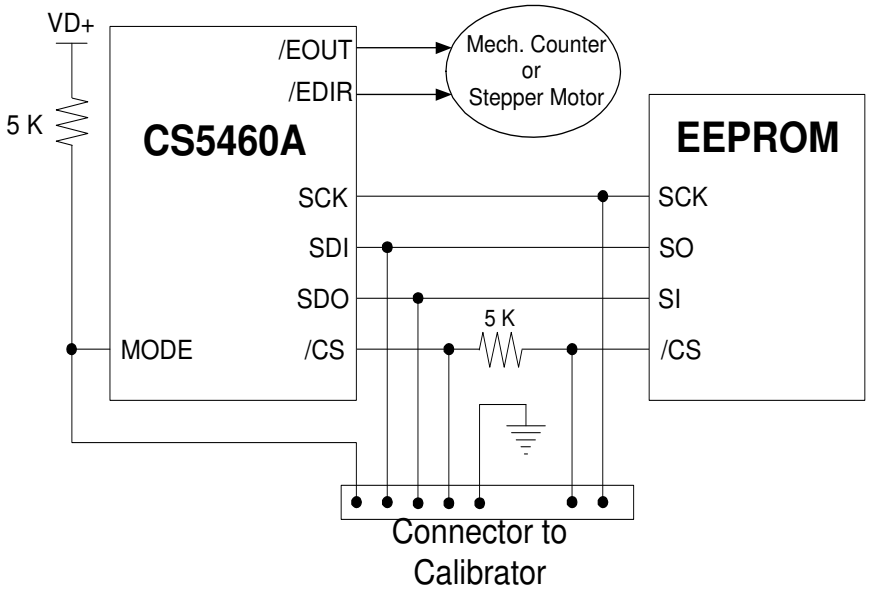

Figure 13. Typical Interface of EEPROM to CS5460A

or custom calibration board. When the metering system is installed, the calibrator would be used to control calibration and/or to program user-specified commands and calibration values into the EEPROM. The commands/data will determine the CS5460A's exact operation, when the auto-boot initialization sequence is running. Any of the valid commands can be used.

3.3.2 Auto-boot Data for EEPROM

This section illustrates what a typical set of code would look like for an auto-boot sequence. This code is what would be written into the EEPROM. In the sequence below, the EEPROM is programmed so that it will first send out commands that write calibration values to the calibration registers inside the CS5460A. This is followed by the commands used to set (write) the desired Pulse-Rate Register value, and also to un-mask the 'LSD' status bit in the Mask Register. Finally, the EEPROM code will initiate 'continuous computation cycles' data acquisition mode and select one of the alternate pulse-output formats (e.g., set the MECH bit in the Control Register). The serial data for such a sequence is shown below in single-byte hexidecimal notation:

40 00 00 61	;Write to Configuration Register, turn high-pass filters on, set K = 1.
44 7F C4 A9	;Write value of 0x7FC4A9 to Current Channel Gain Register.
46 7F B2 53	;Write value of 0x7FB253 to Voltage Channel DC Offset Register.
4C 00 00 14	;Set Pulse Rate Register to 0.625 Hz.
74 00 00 04	;Unmask bit #2 ("LSD" bit in the Mask Register).
E8	;Start performing continuous computation cycles.
78 00 01 40	;Write STOP bit to Control Register, to terminate auto-boot initialization sequence, and also set the $\overline{\text{EOUT}}$ pulse output to Mechanical Counter Format.

This data from the EEPROM will drive the SDI pin of the CS5460A during the auto-boot sequence.

The following sequence of events will cause the CS5460A to execute the auto-boot mode initialization sequence: (A simple timing diagram for this sequence is shown below in Figure 14.) If the MODE pin is set to logic high (or if the MODE pin was set/tied to logic high during/after the CS5460A has been powered on), then changing the $\overline{\text{RESET}}$ pin from active state to inactive state (low to high) will cause the CS5460A to drive the $\overline{\text{CS}}$ pin low, and after this, to issue the standard EEPROM block-read command on the CS5460A's SDO line. Once these events have completed, the CS5460A will continue to issue SCLK pulses, to accept data/commands from the EEPROM. The serial port will become a *master*-mode interface. For a more detailed timing diagram, see *Switching Characteristics* (in *Section 1.*)

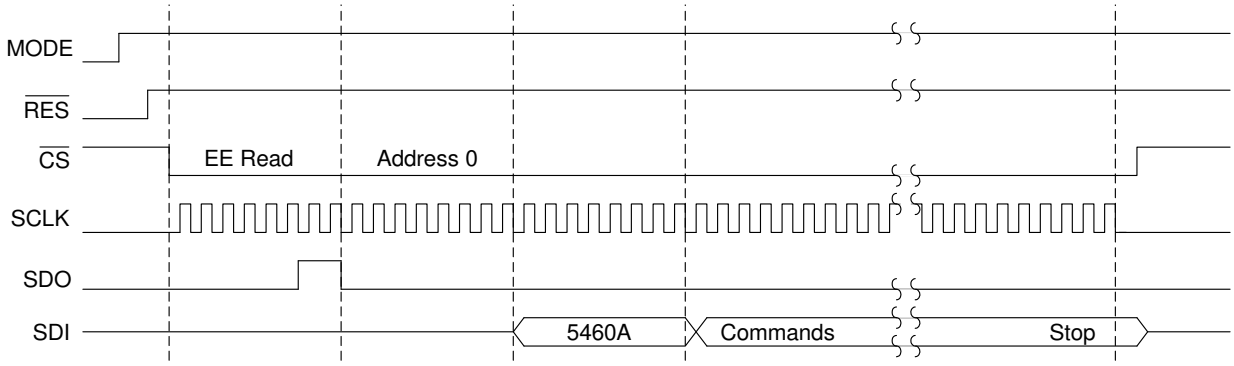

Figure 14. Timing Diagram for Auto-boot Sequence