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CS5461A

Single Phase, Bi-directional Power/Energy IC

Features

- Energy Data Linearity: ±0.1% of Reading over 1000:1 Dynamic Range
- On-chip Functions:
  - Instantaneous Voltage, Current, and Power
  - I_{RMS} and V_{RMS}, Apparent and Active (Real) Power
  - Energy-to-pulse Conversion for Mechanical Counter/Stepper Motor Drive
  - System Calibrations and Phase Compensation
  - Temperature Sensor
  - Voltage Sag Detect
- Meets Accuracy Spec for IEC, ANSI, & JIS.
- Low Power Consumption
- Current Input Optimized for Sense Resistor.
- GND-referenced Signals with Single Supply
- On-chip 2.5 V Reference (25 ppm/°C typ)
- Power Supply Monitor
- Simple Three-wire Digital Serial Interface
- "Auto-boot" Mode from Serial E^2PROM.
- Power Supply Configurations:
  VA+ = +5 V; AGND = 0 V; VD+ = +3.3 V to +5 V

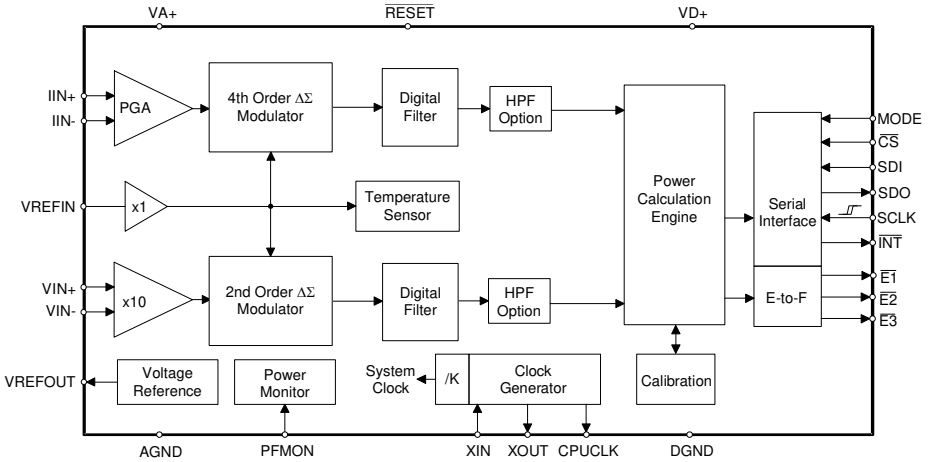
Description

The CS5461A is an integrated power measurement device which combines two ΔΣ analog-to-digital converters, power calculation engine, energy-to-frequency converter, and a serial interface on a single chip. It is designed to accurately measure instantaneous current and voltage, and calculate V_{RMS}, I_{RMS}, instantaneous power, apparent power, and active power for single-phase, 2- or 3-wire power metering applications.

The CS5461A is optimized to interface to shunt resistors or current transformers for current measurement, and to resistive dividers or potential transformers for voltage measurement.

The CS5461A features a bi-directional serial interface for communication with a processor, and a programmable energy-to-pulse output function. Additional features include on-chip functionality to facilitate system-level calibration, temperature sensor, voltage sag detection, and phase compensation.

ORDERING INFORMATION:
See Page 43.



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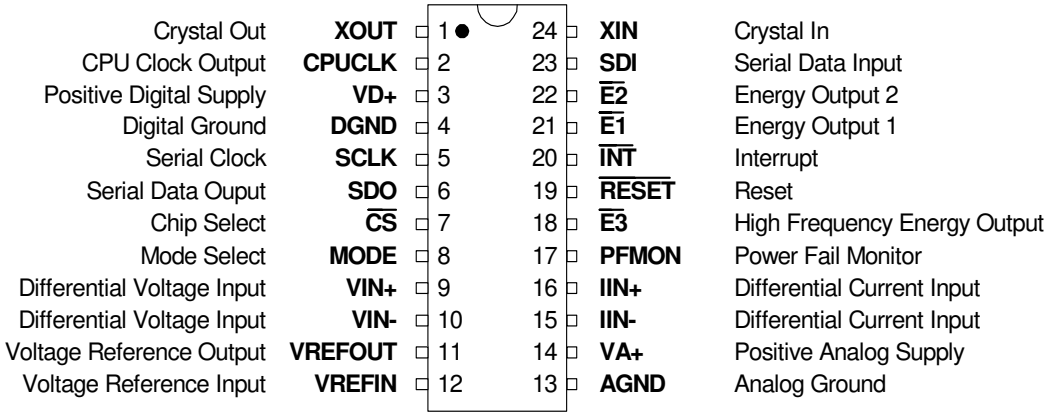
1. OVERVIEW

The CS5461A is a CMOS monolithic power measurement device with a computation engine and an energy-to-frequency pulse output. The CS5461A combines a programmable-gain amplifier, two ΔΣ analog-to-digital converters (ADCs), system calibration and a computation engine on a single chip.

The CS5461A is designed for power measurement applications and is optimized to interface to a current-sense resistor or transformer for current measurement, and to a resistive divider or potential transformer for voltage measurement. The voltage and current channels provide programmable gains to accommodate various input levels from a wide variety of sensing elements. With single +5 V supply on VA+/AGND, both of the CS5461A's input channels can accommodate common mode as well as signal levels between (AGND - 0.25 V) and VA+.

Additionally, the CS5461A is equipped with a computation engine that calculates I_{RMS}, V_{RMS}, apparent power and active (real) power. To facilitate communication to a microprocessor, the CS5461A includes a simple three-wire serial interface which is SPI™ and Microwire™ compatible. The CS5461A provides three outputs for energy registration. $\overline{E1}$ and $\overline{E2}$ are designed to directly drive a mechanical counter or stepper motor, or interface to a microprocessor. The pulse output $\overline{E3}$ is designed to assist with meter calibration.

2. PIN DESCRIPTION



Clock Generator		
Crystal Out **Crystal In**	1,24	**XOUT, XIN** - The output and input of an inverting amplifier. Oscillation occurs when connected to a crystal, providing an on-chip system clock. Alternatively, an external clock can be supplied to the XIN pin to provide the system clock for the device.
CPU Clock Output	2	**CPUCLK** - Output of on-chip oscillator which can drive one standard CMOS load.
Control Pins and Serial Data I/O		
Serial Clock Input	5	**SCLK** - A Schmitt Trigger input pin. Clocks data from the SDI pin into the receive buffer and out of the transmit buffer onto the SDO pin when $\overline{CS}$ is low.
Serial Data Output	6	**SDO** -Serial port data output pin.SDO is forced into a high impedance state when $\overline{CS}$ is high.
Chip Select	7	**$\overline{CS}$** - Low, activates the serial port interface.
Mode Select	8	**MODE** - High, enables the “auto-boot” mode. The mode pin is pulled low by an internal resistor.
High Frequency Energy Output	18	**E3** - Active low pulses with an output frequency proportional to the active power. Used to assist in system calibration.
Reset	19	**$\overline{RESET}$** - A Schmitt Trigger input pin. Low activates Reset, all internal registers (some of which drive output pins) are set to their default states.
Interrupt	20	**$\overline{INT}$** - Low, indicates that an enabled event has occurred.
Energy Output	21,22	**E1, $\overline{E2}$** - Active low pulses with an output frequency proportional to the active power. Indicates if the measured energy is negative.
Serial Data Input	23	**SDI** - Serial port data input pin. Data will be input at a rate determined by SCLK.
Analog Inputs/Outputs		
Differential Voltage Inputs	9,10	**VIN+, VIN-** - Differential analog input pins for the voltage channel.
Differential Current Inputs	15,16	**IIN+, IIN-** - Differential analog input pins for the current channel.
Voltage Reference Output	11	**VREFOUT** - The on-chip voltage reference output. The voltage reference has a nominal magnitude of 2.5 V and is referenced to the AGND pin on the converter.
Voltage Reference Input	12	**VREFIN** - The input to this pin establishes the voltage reference for the on-chip modulator.
Power Supply Connections		
Positive Digital Supply	3	**VD**+ - The positive digital supply.
Digital Ground	4	**DGND** - Digital Ground.
Positive Analog Supply	14	**VA+** - The positive analog supply.
Analog Ground	13	**AGND** - Analog ground.
Power Fail Monitor	17	**PFMON** - The power fail monitor pin monitors the analog supply. If PFMON’s voltage threshold is not met, a Low-Supply Detect (LSD) bit is set in the status register.

3. CHARACTERISTICS & SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Positive Digital Power Supply	VD+	3.135	5.0	5.25	V
Positive Analog Power Supply	VA+	4.75	5.0	5.25	V
Voltage Reference	VREFIN	-	2.5	-	V
Specified Temperature Range	T_A	-40	-	+85	°C

ANALOG CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all *Recommended Operating Conditions*.
- Typical characteristics and specifications are measured at nominal supply voltages and TA = 25 °C.
- VA+ = VD+ = 5 V ±5%; AGND = DGND = 0 V; VREFIN = +2.5 V. All voltages with respect to 0 V.
- MCLK = 4.096 MHz.

Parameter		Symbol	Min	Typ	Max	Unit
Linearity Performance						
Active Power Accuracy (All Gain Ranges) (Note 1)	Input Range 0.1% - 100%	P_{Active}	-	±0.1	-	%
Current RMS Accuracy (All Gain Ranges) (Note 1) (Note 1)	Input Range 0.2% - 100% Input Range 0.1% - 0.2%	I_{RMS}	- -	±0.2 ±1.5	- -	% %
Voltage RMS Accuracy (All Gain Ranges) (Note 1)	Input Range 5% - 100%	V_{RMS}	-	±0.1	-	%
Analog Inputs (Both Channels)						
Common Mode Rejection	(DC, 50, 60 Hz)	CMRR	80	-	-	dB
Common Mode + Signal (All Gain Ranges)			-0.25	-	VA+	V
Analog Inputs (Current Channel)						
Differential Input Range [(IIN+) - (IIN-)]	(Gain = 10) (Gain = 50)	IIN	- -	500 100	- -	mV_{P-P} mV_{P-P}
Total Harmonic Distortion	(Gain = 50)	THD	80	94	-	dB
Crosstalk with Voltage Channel at Full Scale	(50, 60 Hz)		-	-115	-	dB
Input Capacitance	(Gain = 10) (Gain = 50)	IC	- -	32 52	- -	pF pF
Effective Input Impedance		EII	30	-	-	kΩ
Noise (Referred to Input)	(Gain = 10) (Gain = 50)	N_I	- -	22.5 4.5	- -	μV_{rms} μV_{rms}
Offset Drift (Without the high-pass filter)		OD	-	4.0	-	µV/°C
Gain Error	(Note 2)	GE	-	±0.4		%
Analog Inputs (Voltage Channel)						
Differential Input Range	{(VIN+) - (VIN-)}	VIN	-	500	-	mV_{P-P}
Total Harmonic Distortion		THD	65	75	-	dB
Crosstalk with Current Channel at Full Scale	(50, 60 Hz)		-	-70	-	dB
Input Capacitance	All Gain Ranges	IC	-	0.2	-	pF
Effective Input Impedance		EII	2	-	-	MΩ
Noise (Referred to Input)		N_V	-	140	-	μV_{rms}
Offset Drift (Without the high-pass Filter)		OD	-	16.0	-	µV/°C
Gain Error	(Note 2)	GE	-	±3.0		%

ANALOG CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
Temperature Channel					
Temperature Accuracy	T	-	±5	-	°C
Power Supplies					
Power Supply Currents (Active State) I_{A+}	PSCA	-	1.1	-	mA
I_{D+} (VA+ = VD+ = 5 V)	PSCD	-	2.9	-	mA
I_{D+} (VA+ = 5 V, VD+ = 3.3 V)	PSCD	-	1.7	-	mA
Power Consumption Active State (VA+ = VD+ = 5 V) (Note 3)	PC	-	21	28	mW
Active State (VA+ = 5 V, VD+ = 3.3 V)		-	12	16.5	mW
Stand-By State		-	8	-	mW
Sleep State		-	10	-	µW
Power Supply Rejection Ratio (DC, 50 and 60 Hz) (Note 4)					
Voltage Channel	PSRR	45	65	-	dB
Current Channel		70	75	-	dB
PFMON Low-voltage Trigger Threshold (Note 5)	PMLO	2.3	2.45	-	V
PFMON High-voltage Power-On Trip Point (Note 6)	PMHI	-	2.55	2.7	V

1. Applies when the HPF option is enabled.
2. Applies before system calibration.
3. All outputs unloaded. All inputs CMOS level.
4. Measurement method for PSRR: VREFIN tied to VREFOUT, VA+ = VD+ = 5 V, a 150 mV (zero-to-peak) (60 Hz) sinewave is imposed onto the +5 V DC supply voltage at VA+ and VD+ pins. The "+" and "-" input pins of both input channels are shorted to AGND. Then the CS5461A is commanded to continuous conversion acquisition mode, and digital output data is collected for the channel under test. The (zero-to-peak) value of the digital sinusoidal output signal is determined, and this value is converted into the (zero-to-peak) value of the sinusoidal voltage (measured in mV) that would need to be applied at the channel's inputs, in order to cause the same digital sinusoidal output. This voltage is then defined as Veq. PSRR is then (in dB):

$$PSRR = 20 \cdot \log\left\{\frac{150}{V_{eq}}\right\}$$

5. When voltage level on PFMON is sagging, and LSD bit is at 0, the voltage at which LSD bit is set to 1.
6. If the LSD bit has been set to 1 (because PFMON voltage fell below PMLO), this is the voltage level on PFMON at which the LSD bit can be permanently reset back to 0.

VOLTAGE REFERENCE

Parameter	Symbol	Min	Typ	Max	Unit
Reference Output					
Output Voltage	VREFOUT	+2.4	+2.5	+2.6	V
Temperature Coefficient (Note 7)	TC_{VREF}	-	25	60	ppm/°C
Load Regulation (Note 8)	ΔV_R	-	6	10	mV
Reference Input					
Input Voltage Range	VREFIN	+2.4	+2.5	+2.6	V
Input Capacitance		-	4	-	pF
Input CVF Current		-	25	-	nA

Notes: 7. The voltage at VREFOUT is measured across the temperature range. From these measurements the following formula is used to calculate the VREFOUT Temperature Coefficient:.

$$TC_{VREF} = \left(\frac{(VREFOUT_{MAX} - VREFOUT_{MIN})}{VREFOUT_{AVG}}\right)\left(\frac{1}{T_{AMAX} - T_{AMIN}}\right)\left(1.0 \times 10^{6}\right)$$

8. Specified at maximum recommended output of 1 µA, source or sink.

DIGITAL CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all *Recommended Operating Conditions*.
- Typical characteristics and specifications are measured at nominal supply voltages and TA = 25 °C.
- VA+ = VD+ = 5V ±5%; AGND = DGND = 0 V. All voltages with respect to 0 V.
- MCLK = 4.096 MHz.

Parameter	Symbol	Min	Typ	Max	Unit
Master Clock Characteristics					
Master Clock Frequency Internal Gate Oscillator (Note 10)	MCLK	2.5	4.096	20	MHz
Master Clock Duty Cycle		40	-	60	%
CPUCLK Duty Cycle (Note 11 and 12)		40		60	%
Filter Characteristics					
Phase Compensation Range (Voltage Channel, 60 Hz)		-2.8	-	+2.8	°
Input Sampling Rate DCLK = MCLK/K		-	DCLK/8	-	Hz
Digital Filter Output Word Rate (Both Channels)	OWR	-	DCLK/1024	-	Hz
High-pass Filter Corner Frequency -3 dB		-	0.5	-	Hz
Full Scale Calibration Range (Referred to Input) (Note 13)	FSCR	25	-	100	%F.S.
Channel-to-channel Time-shift Error (Note 14)			1.0		µs
Input/Output Characteristics					
High-level Input Voltage All Pins Except XIN and SCLK and $\overline{\text{RESET}}$ XIN SCLK and $\overline{\text{RESET}}$	V_{IH}	 0.6 VD+ (VD+) - 0.5 0.8 VD+	 - - -	 - - -	 V V V
Low-level Input Voltage (VD = 5 V) All Pins Except XIN and SCLK and $\overline{\text{RESET}}$ XIN SCLK and $\overline{\text{RESET}}$	V_{IL}	 - - -	 - - -	 0.8 1.5 0.2 VD+	 V V V
Low-level Input Voltage (VD = 3.3 V) All Pins Except XIN and SCLK and $\overline{\text{RESET}}$ XIN SCLK and $\overline{\text{RESET}}$	V_{IL}	 - - -	 - - -	 0.48 0.3 0.2 VD+	 V V V
High-level Output Voltage I_{out} = +5 mA	V_{OH}	(VD+) - 1.0	-	-	V
Low-level Output Voltage I_{out} = -5 mA	V_{OL}	-	-	0.4	V
Input Leakage Current (Note 15)	I_{in}	-	±1	±10	µA
3-state Leakage Current	I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance	C_{out}	-	5	-	pF

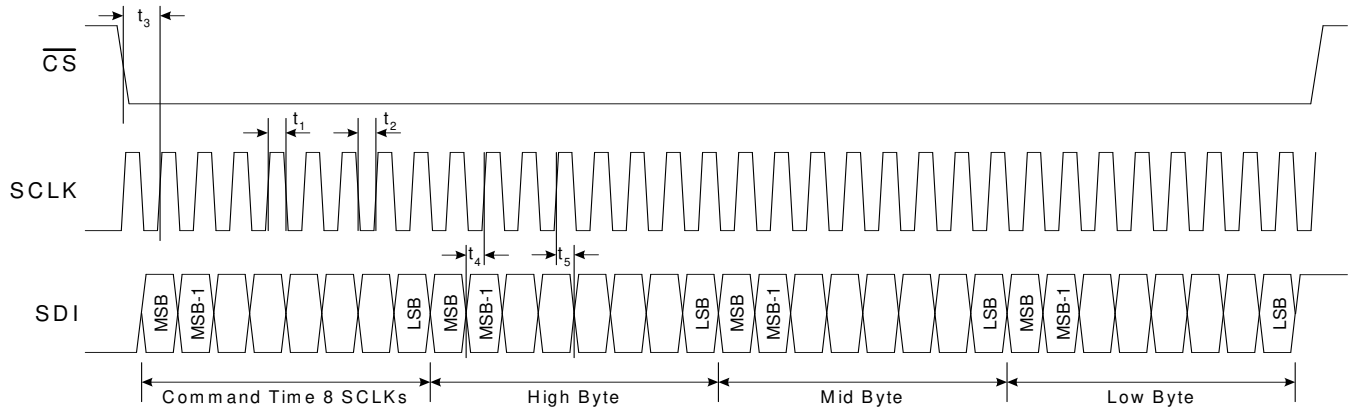
Notes:
9. All measurements performed under static conditions.
10. If a crystal is used, then XIN frequency must remain between 2.5 MHz - 5.0 MHz. If an external oscillator is used, XIN frequency range is 2.5 MHz - 20 MHz, but K must be set so that MCLK is between 2.5 MHz - 5.0 MHz.
11. If external MCLK is used, then the duty cycle must be between 45% and 55% to maintain this specification.
12. The frequency of CPUCLK is equal to MCLK.
13. The minimum FSCR is limited by the maximum allowed gain register value. The maximum FSCR is limited by the full-scale signal applied to the channel input.
14. Configuration Register bits PC[6:0] are set to “0000000”.
15. The MODE pin is pulled low by an internal resistor.

SWITCHING CHARACTERISTICS

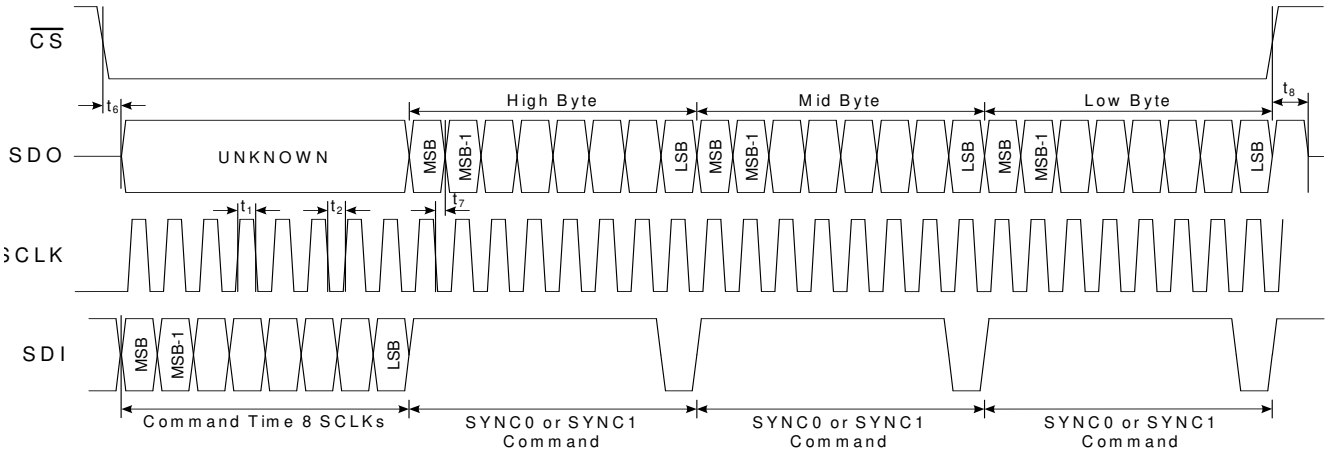
- Min / Max characteristics and specifications are guaranteed over all *Recommended Operating Conditions*.
- Typical characteristics and specifications are measured at nominal supply voltages and TA = 25 °C.
- VA+ = 5 V ±5% VD+ = 3.3 V ±5% or 5 V ±5%; AGND = DGND = 0 V. All voltages with respect to 0 V.
- Logic Levels: Logic 0 = 0 V, Logic 1 = VD+.

Parameter		Symbol	Min	Typ	Max	Unit
Rise Times (Note 16)	Any Digital Input Except SCLK SCLK Any Digital Output	t_{rise}	- - -	- - 50	1.0 100 -	µs µs ns
Fall Times (Note 16)	Any Digital Input Except SCLK SCLK Any Digital Output	t_{fall}	- - -	- - 50	1.0 100 -	µs µs ns
Start-up						
Oscillator Start-Up Time	XTAL = 4.096 MHz (Note 17)	t_{ost}	-	60	-	ms
Serial Port Timing						
Serial Clock Frequency		SCLK	-	-	2	MHz
Serial Clock	Pulse Width High Pulse Width Low	t_1 t_2	200 200	- -	- -	ns ns
SDI Timing						
$\overline{CS}$ Falling to SCLK Rising		t_3	50	-	-	ns
Data Set-up Time Prior to SCLK Rising		t_4	50	-	-	ns
Data Hold Time After SCLK Rising		t_5	100	-	-	ns
SDO Timing						
$\overline{CS}$ Falling to SDO Driving		t_6	-	20	50	ns
SCLK Falling to New Data Bit (hold time)		t_7	-	20	50	ns
$\overline{CS}$ Rising to SDO Hi-Z		t_8	-	20	50	ns
Auto-Boot Timing						
Serial Clock	Pulse Width Low Pulse Width High	t_9 t_{10}		8 8		MCLK MCLK
MODE setup time to $\overline{RESET}$ Rising		t_{11}	50			ns
$\overline{RESET}$ rising to $\overline{CS}$ falling		t_{12}	48			MCLK
$\overline{CS}$ falling to SCLK rising		t_{13}	100	8		MCLK
SCLK falling to $\overline{CS}$ rising		t_{14}		16		MCLK
$\overline{CS}$ rising to driving MODE low (to end auto-boot sequence).		t_{15}	50			ns
SDO guaranteed setup time to SCLK rising		t_{16}	100			ns

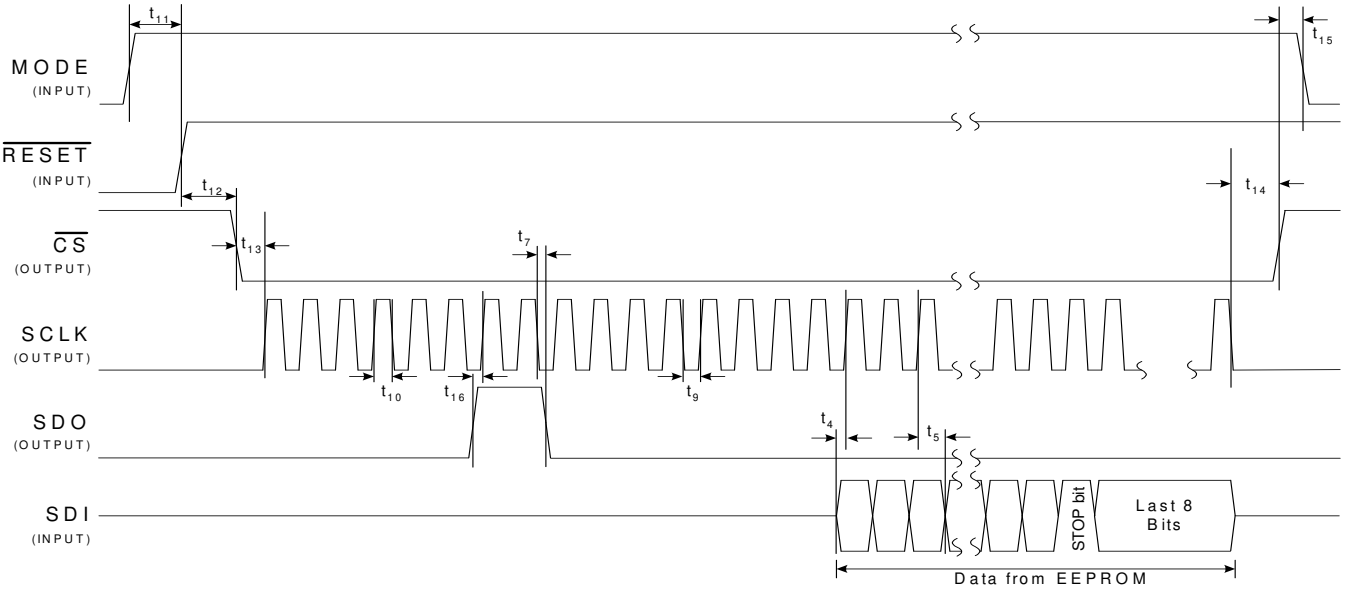
Notes: 16. Specified using 10% and 90% points on wave-form of interest. Output loaded with 50 pF.
17. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.



SDI Write Timing (Not to Scale)



SDO Read Timing (Not to Scale)



Auto-Boot Sequence Timing (Not to Scale)

Figure 1. CS5461A Read and Write Timing Diagrams

ABSOLUTE MAXIMUM RATINGS

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	(Notes 18 and 19)					
Positive Digital		VD+	-0.3	-	+6.0	V
Positive Analog		VA+	-0.3	-	+6.0	V
Input Current, Any Pin Except Supplies	(Notes 20, 21, 22)	I_{IN}	-	-	±10	mA
Output Current, Any Pin Except VREFOUT		I_{OUT}	-	-	100	mA
Power Dissipation	(Note 23)	P_D	-	-	500	mW
Analog Input Voltage	All Analog Pins	V_{INA}	- 0.3	-	(VA+) + 0.3	V
Digital Input Voltage	All Digital Pins	V_{IND}	-0.3	-	(VD+) + 0.3	V
Ambient Operating Temperature		T_A	-40	-	85	°C
Storage Temperature		T_{stg}	-65	-	150	°C

Notes:
18. VA+ and AGND must satisfy {(VA+) - (AGND)} ≤ + 6.0 V.
19. VD+ and AGND must satisfy {(VD+) - (AGND)} ≤ + 6.0 V.
20. Applies to all pins including continuous over-voltage conditions at the analog input pins.
21. Transient current of up to 100 mA will not cause SCR latch-up.
22. Maximum DC input current for a power supply pin is ±50 mA.
23. Total power dissipation, including all input currents and output currents.

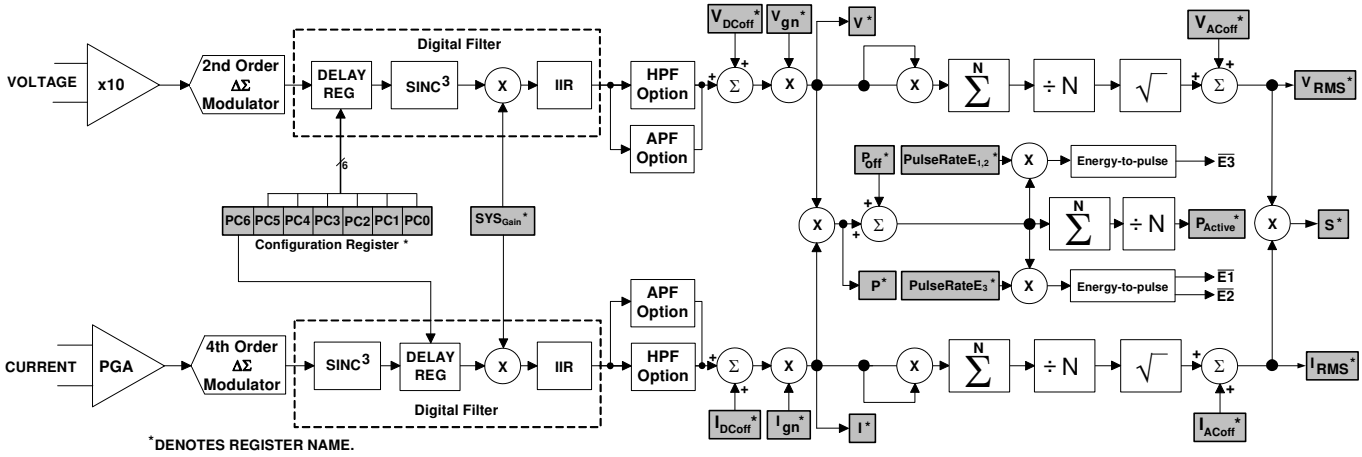


Figure 2. Data Flow.

4. THEORY OF OPERATION

The CS5461A is a dual-channel analog-to-digital converter (ADC) followed by a computation engine that performs power calculations and energy-to-pulse conversion. The flow diagram for the two data paths is depicted in Figure 2. The analog inputs are structured with two dedicated channels, voltage and current, then optimized to simplify interfacing to sensing elements.

The voltage-sensing element introduces a voltage waveform on the voltage channel input VIN± and is subject to a gain of 10x. A second-order, delta-sigma modulator samples the amplified signal for digitization.

Simultaneously, the current-sensing element introduces a voltage waveform on the current channel input IIN± and is subject to the two selectable gains of the programmable gain amplifier (PGA). The amplified signal is sampled by a fourth-order, delta-sigma modulator for digitization. Both converters sample at a rate of MCLK/8, the over-sampling provides a wide dynamic range and simplified anti-alias filter design.

4.1 Digital Filters

The decimating digital filters on both channels are $Sinc^3$ filters followed by 4th-order, IIR filters. The single-bit data is passed to the low-pass decimation filter and output at a fixed word rate. The output word is passed to the IIR filter to compensate for the magnitude roll-off of the low-pass filtering operation.

An optional digital High-pass Filter (*HPF* in Figure 2) removes any DC component from the selected signal path. By removing the DC component from the voltage and/or the current channel, any DC content will also be removed from the calculated active power as well. With both HPFs enabled, the DC component will be removed from the calculated V_{RMS} and I_{RMS} as well as the apparent power.

When the HPF option is used in only one channel, the APF (all pass filter) option can be applied to the other channel to preserve the phase match between the two channels.

4.2 Voltage and Current Measurements

The digital filter output word is then subject to a DC offset adjustment and a gain calibration (See Section 7. *System Calibration* on page 35). The calibrated measurement is available to the user by reading the instantaneous voltage and current registers.

The Root Mean Square (RMS) calculations are performed on N instantaneous voltage and current samples, V_n and I_n respectively (where N is the cycle count), using the formula:

$$I_{RMS} = \sqrt{\frac{\sum_{n=0}^{N-1} I_n}{N}}$$

and likewise for V_{RMS}, using V_n. I_{RMS} and V_{RMS} are accessible by register reads, which are updated once every cycle count (referred to as a computational cycle).

4.3 Power Measurements

The instantaneous voltage and current samples are multiplied to obtain the instantaneous power (see Figure 2). The product is then averaged over N conversions to compute active power and used to drive energy pulse outputs **E1, E2 and E3**. Output $\overline{E3}$ provides a uniform pulse stream that is proportional to the active power and is designed for system calibration.

To generate a value for the accumulated active energy over the last computation cycle, the active power can be multiplied by the time duration of the computation cycle.

The apparent power is the combination of the active power and reactive power, without reference to an impedance phase angle, and is calculated by the CS5461A using the following formula:

$$S = V_{RMS} \times I_{RMS}$$

The apparent power is registered once every computation cycle.

4.4 Linearity Performance

The linearity of the V_{RMS}, I_{RMS}, and active power measurements (before calibration) will be within ±0.1% of reading over the ranges specified, with respect to the input voltage levels required to cause full-scale readings in the I_{RMS} and V_{RMS} registers. Refer to *Linearity Performance Specifications* on page 7.

Until the CS5461A is calibrated, the *accuracy* of the CS5461A (with respect to a reference line-voltage and line-current level on the power mains) is not guaranteed to within ±0.1%. See Section 7. *System Calibration* on page 35. The accuracy of the internal calculations can often be improved by selecting a value for the *Cycle Count Register* that will cause the time duration of one computation cycle to be equal to (or very close to) a whole-number of power-line cycles (and N must be greater than or equal to 4000).

5. FUNCTIONAL DESCRIPTION

5.1 Analog Inputs

The CS5461A is equipped with two fully differential input channels. The inputs VIN± and IIN± are designated as the voltage and current channel inputs, respectively. The full-scale differential input voltage for the current and voltage channel is ±250 mV_P.

5.1.1 Voltage Channel

The output of the line-voltage resistive divider or transformer is connected to the VIN+ and VIN- input pins of the CS5461A. The voltage channel is equipped with a 10x, fixed-gain amplifier. The full-scale signal level that can be applied to the voltage channel is ±250 mV. If the input signal is a sine wave the maximum RMS voltage at a gain 10x is:

$$\frac{250\,mV_P}{\sqrt{2}} \cong 176.78\,mV_{RMS}$$

which is approximately 70.7% of maximum peak voltage. The voltage channel is also equipped with a *Voltage Gain Register*, allowing for an additional programmable gain of up to 4x.

5.1.2 Current Channel

The output of the current-sense resistor or transformer is connected to the IIN+ and IIN- input pins of the CS5461A. To accommodate different current-sensing elements, the current channel incorporates a Programmable Gain Amplifier (PGA) with two programmable input gains. *Configuration Register* bit Igain (See Table 1) defines the two gain selections and corresponding maximum input-signal level.

Igain	Maximum Input Range	
0	±250 mV	10x
1	±50 mV	50x

Table 1. Current Channel PGA Configuration

For example, if Igain=0, the current channel's PGA gain is set to 10x. If the input signals are pure sinusoids with zero phase shift, the maximum peak differential signal on the current or voltage channel is ±250 mV_P. The input-signal levels are approximately 70.7% of maximum peak voltage producing a full-scale energy pulse registration equal to 50% of absolute maximum energy pulse registration. This will be discussed further in Section 5.4 *Energy Pulse Output* on page 16.

The *Current Gain Register* also allows for an additional programmable gain of up to 4x. If an additional gain is applied to the voltage and/or current channel, the maximum input range should be adjusted accordingly.

5.2 High-pass Filters

By removing the offset from either channel, no error component will be generated at DC when computing the active power. By removing the offset from both channels, no error component will be generated at DC when computing V_{RMS}, I_{RMS}, and apparent power. *Configuration Register* bits VHPF and IHPF activate the HPF in the voltage and current channel respectively.

5.3 Performing Measurements

The CS5461A performs measurements of instantaneous voltage (V_n) and current (I_n), and calculates instantaneous power (P_n) at an Output Word Rate (OWR) of

$$OWR = \frac{(MCLK/K)}{1024}$$

where K is the clock divider setting in the *Configuration Register*.

The RMS voltage (V_{RMS}), RMS current (I_{RMS}), and active power (P_{Active}) are computed using N instantaneous samples of V_n, I_n and P_n respectively, where N is the value in the *Cycle Count Register* (N) and is referred to as a *"computation cycle"*. The apparent power (S) is the product of V_{RMS} and I_{RMS}. A computation cycle is derived from the master clock (MCLK), with frequency:

$$\text{Computation Cycle} = \frac{OWR}{N}$$

Under default conditions & with K = 1, N = 4000, and MCLK = 4.096 MHz – the OWR = 4000 Hz and the Computation Cycle = 1 Hz.

All measurements are available as a percentage of full scale. The format for *signed* registers is a two's complement, normalized value between -1 and +1. The format for *unsigned* registers is a normalized value between 0 and 1. A register value of

$$\frac{(2^{23}-1)}{2^{23}} = 0.99999988$$

represents the maximum possible value.

At each instantaneous measurement, the CRDY bit will be set (logic 1) in the *Status Register*, and the $\overline{INT}$ pin will become active if the CRDY bit is unmasked in the *Mask Register*. At the end of each computation cycle, the DRDY bit will be set in the *Status Register*, and the

$\overline{INT}$ pin will become active if the DRDY bit is unmasked in the *Mask Register*. When these bits are set, they must be cleared (logic 0) by the user before they can be asserted again.

If the *Cycle Count Register* (N) is set to 1, all output calculations are instantaneous, and DRDY, like CRDY, will indicate when instantaneous measurements are finished. Some calculations are inhibited when the cycle count is less than 2.

5.4 Energy Pulse Output

The CS5461A provides three output pins for energy registration. The $\overline{E1}$ and $\overline{E2}$ pins provide a simple interface which energy can be registered. These pins are designed to directly connect to a stepper motor or electromechanical counter. $\overline{E1}$ and $\overline{E2}$ pins can be set to one of four pulse output formats, Normal, Alternate, Stepper Motor, or Mechanical Counter. Table 2 defines the pulse output format, which is controlled by bits ALT in the *Configuration Register*, and MECH and STEP in the *Control Register.*

ALT	STEP	MECH	FORMAT
0	0	0	Normal
0	X	1	Mechanical Counter
0	1	0	Stepper Motor
1	X	1	Alternate Pulse

Table 2. E1 and E2 Pulse Output Format

The $\overline{E3}$ pin is designated for system calibration, the pulse rate can be selected to reach a frequency of 512 kHz.

The pulse output frequency of $\overline{E1}$ and $\overline{E2}$ is directly proportional to the active power calculated from the input signals. To calculate the output frequency on $\overline{E1}$ and $\overline{E2}$, the following transfer function can be utilized:

$$FREQ_E = \frac{VIN \times VGAIN \times IIN \times IGAIN \times PF \times PulseRateE_{1,2}}{VREFIN^2}$$

$FREQ_E$ = Average frequency of $\overline{E1}$ and $\overline{E2}$ pulses [Hz]
VIN = rms voltage across VIN+ and VIN- [V]
VGAIN = Voltage channel gain
IIN = rms voltage across IIN+ and IIN- [V]
IGAIN = Current channel gain
PF = Power Factor
$PulseRateE_{1,2}$ = Maximum frequency on $\overline{E1}$ and $\overline{E2}$ [Hz]
VREFIN = Voltage at VREFIN pin [V]

With MCLK = 4.096 MHz, PF = 1, and default settings, the pulses will have an average frequency equal to the frequency setting in the *$PulseRateE_{1,2}$ Register* when the input signals applied to the voltage and current channels cause full-scale readings in the instantaneous voltage and current registers. When MCLK/K is not equal to 4.096 MHz, the user should scale the *$PulseRateE_{1,2}$ Register* by a factor of 4.096 MHz/(MCLK/K) to get the actual pulse rate output.

5.4.1 Normal Format

The Normal format is the default. Figure 3 illustrates the output format on pins $\overline{E1}$ and $\overline{E2}$. The $\overline{E1}$ pin outputs active-low pulses with a frequency proportional to the active power. The $\overline{E2}$ pin is the energy direction indicator. Positive energy is represented by a pulse on the $\overline{E1}$ pin while the $\overline{E2}$ pin remains high. Negative energy is represented by synchronous pulses on both the $\overline{E1}$ pin and the $\overline{E2}$ pin.

The *$PulseRateE_{1,2}$ Register* defines the average frequency on output pin $\overline{E1}$, when full-scale input signals are applied to the voltage and current channels. The maximum pulse frequency from the $\overline{E1}$ pin

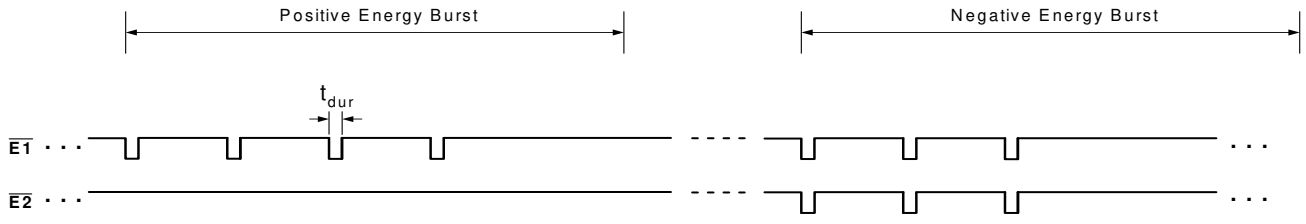


Figure 3. Normal Format on pulse outputs E1 and E2

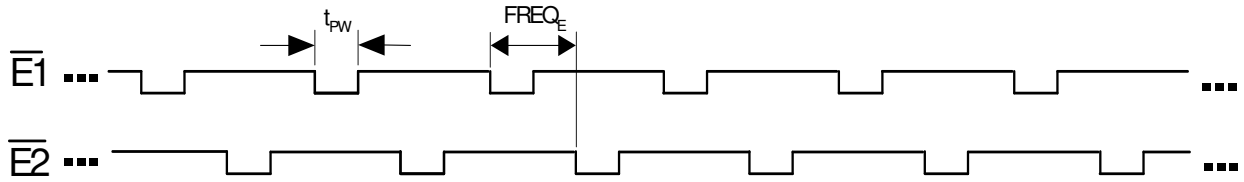


Figure 4. Alternate Pulse Format on E1 and E2

is (MCLK/K)/16. The pulse duration (t_{dur}) is an integer multiple of MCLK cycles, approximately equal to:

$$t_{dur}(sec) \cong \frac{1}{PulseRateE_{1,2} \times 8}$$

The maximum pulse duration (t_{dur}) is determined by the sampling rate and the minimum is defined by the maximum pulse frequency. The t_{dur} limits are:

$$\frac{1}{(MCLK/K)/16 \times 8} < t_{dur}(sec) < \frac{1}{(MCLK/K)/1024 \times 8}$$

The *Pulse Width Register* (PW) does not affect the normal format.

5.4.2 Alternate Pulse Format

Setting bits MECH = 1 and STEP = 0 in the *Control Register* and ALT = 1 in the *Configuration Register* configures the $\overline{E1}$ and $\overline{E2}$ pins for alternating pulse format output (see Figure 4). Each pin produces alternating active-low pulses with a pulse duration (t_{PW}) defined by the *Pulse Width Register* (PW):

$$t_{PW}(ms) = \frac{PW}{(MCLK/K)/1024}$$

If MCLK = 4.096 MHz, K = 1, and PW = 1 then t_{PW} = 0.25 ms. To ensure that pulses occur on the $\overline{E1}$ and $\overline{E2}$ output pins when full-scale input signals are applied to the voltage and current channels, then:

$$PulseRateE_{1,2} < \frac{1}{t_{PW}}$$

The pulse frequency ($FREQ_E$) is determined by the *PulseRateE$_{1,2}$ Register* and can be calculated using the transfer function. The energy direction is not defined in the alternate pulse format.

5.4.3 Mechanical Counter Format

Setting bits MECH = 1 and STEP = 0 in the *Control Register* and bit ALT = 0 in the *Configuration Register* enables $\overline{E1}$ and $\overline{E2}$ for mechanical counters and similar discrete counting instruments. When energy is negative, pulses appear on $\overline{E2}$ (see Figure 5). When energy is positive, the pulses appear on $\overline{E1}$. The pulse width is defined by the *Pulsewidth Register* and will limit the output pulse frequency ($FREQ_E$). By default, PW = 512 samples, if MCLK = 4.096 MHz and K = 1 then t_{PW} = 128 ms. To ensure that pulses will occur, the *PulseRateE$_{1,2}$ Register* must be set to an appropriate value.

5.4.4 Stepper Motor Format

Setting bits STEP = 1 and MECH = 0 in the *Control Register* and bit ALT = 0 in the *Configuration Register* configures the $\overline{E1}$ and $\overline{E2}$ pins for stepper motor format. When the accumulated active power equals the defined

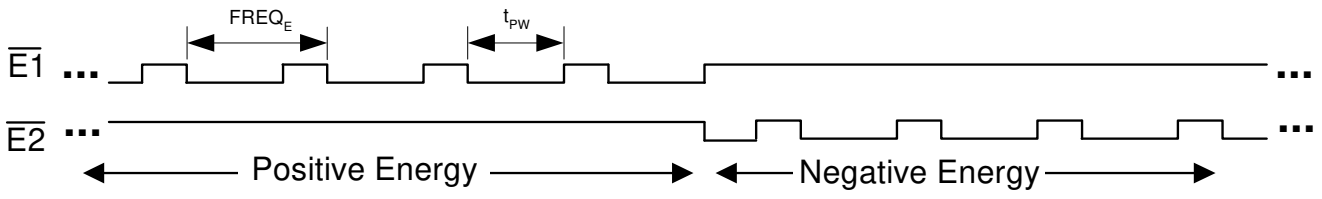


Figure 5. Mechanical Counter Format on E1 and E2

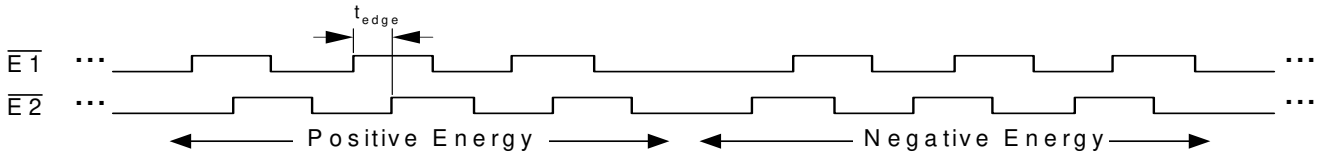


Figure 6. Stepper Motor Format on E1 and E2

energy level, the energy output pins ($\overline{E1}$ and $\overline{E2}$) alternate changing states (see Figure 6). The duration (t_{edge}) between the alternating states is defined by the transfer function:

$$t_{edge}(sec) = \frac{1}{FREQ_E}$$

The direction the motor will rotate is determined by the order of the state changes. When energy is positive, $\overline{E1}$ will lead $\overline{E2}$. When energy is negative, $\overline{E2}$ will lead $\overline{E1}$. The *Pulse Width Register* (PW) does not affect the stepper motor format.

5.4.5 Pulse Output $\overline{E3}$

The pulse output $\overline{E3}$ is designed to assist with meter calibration. The pulse-output frequency of $\overline{E3}$ is directly proportional to the active power calculated from the input signals. $\overline{E3}$ pulse frequency is derived using a simular transfer function as $\overline{E1}$, but is set by the value in the *PulseRateE$_3$ Register*.

The $\overline{E3}$ pin outputs negative and positive energy, but has no energy direction indicator.

The pulse width of $\overline{E3}$ is configurable. The *PulseWidth* register defines the pulse width of $\overline{E3}$ in units of 1/OWR or:

$$t_{pw} = \frac{PulseWidth}{((MCLK)/K)/1024}$$

The default value is 0.

5.4.6 Anti-creep for the Pulse Outputs

Anti-creep allows the measurement element to maintain an energy level, such that when the magnitude of the accumulated active power is below this level, no energy pulses are output. Anti-creep is enabled by setting bit FAC in the *Control Register* for $\overline{E3}$ and bit EAC in the *Control Register* for $\overline{E1}$ and $\overline{E2}$.

For low-frequency pulse output formats (i.e. mechanical counter and stepper motor formats), the active power is accumulated over time. When a designated energy level is reached (determined by the transfer function) a pulse is generated on $\overline{E1}$ and/or $\overline{E2}$. If active power with alternating polarity occurs during the accumulation period (e.g. random noise at zero power levels), the accuracy of the registered energy will be maintained.

For high-frequency pulse output formats (i.e. normal and alternate pulse formats), the active power is accumulated over time until a ±8x buffer is defined. Then, when the designated energy level is reached, a pulse is generated on $\overline{E1}$ and/or $\overline{E2}$. For pulse outputs with high frequencies and power levels close to zero, the extended buffer prevents random noise from being registered as active energy.

5.4.7 Design Examples

EXAMPLE #1:

The maximum rated levels for a power line meter are 250 V rms and 20 A rms. The required number of pulses per second on $\overline{E1}$ is 100 pulses per second (100 Hz), when the levels on the power line are 220 V rms and 15 A rms.

With a 10x gain on the voltage and current channel the maximum input signal is 250 mV_P (see Section 5.1 *Analog Inputs* on page 15). To prevent over-driving the channel inputs, the maximum rated rms input levels will register 0.6 in V_{RMS} and I_{RMS} by design. Therefore the voltage level at the channel inputs will be 150 mV rms when the maximum rated levels on the power lines are 250 V rms and 20 A rms.

Solving for PulseRateE$_{1,2}$ using the transfer function:

$$PulseRateE_{1,2} = \frac{FREQ_E \times VREFIN^2}{VIN \times VGAIN \times IIN \times PF}$$

Therefore with PF = 1 and

$$VIN = 220V \times ((150mV)/(250V)) = 132mV$$

$$IIN = 15A \times ((150mV)/(20A)) = 112.5mV$$

the *PulseRateE$_{1,2}$ Register* is set to:

$$PulseRateE = \frac{100 \times 2.5^2}{0.132 \times 10 \times 0.1125 \times 10} = 420.8754Hz$$

EXAMPLE #2:

The required number of pulses per unit energy present on $\overline{E1}$ is specified to be 500 pulses per kWhr, given that the line voltage is 250 Vrms and the line current is 20 Arms. In such a situation, the stated line voltage and current do not determine the appropriate $PulseRateE_{1,2}$ setting. To achieve full-scale readings in the instantaneous voltage and current registers, a 250 mV, DC-level signal is applied to the channel inputs.

As in example #1, the voltage and current channel gains are 10x, and the voltage level at the channel inputs will be 150 mV rms when the levels on the power lines are 250 V rms and 20 A rms. In order to achieve 500 pulse-per-kW Hr per unit-energy, the *PulseRateE$_{1,2}$ Register* setting is determined using the following equation:

$$PulseRateE_{1,2} = \frac{500pulses}{kWHr} \times \frac{1Hr}{3600s} \times \frac{1kW}{1000W} \times \frac{250mV}{\left(\frac{150mV}{250V}\right)} \times \frac{250mV}{\left(\frac{150mV}{20A}\right)}$$

Therefor, the *PulseRateE$_{1,2}$ Register* is approximately 1.929 Hz. The *PulseRateE$_{1,2}$ Register* cannot be set to a frequency of exactly 1.929 Hz. The closest setting is 0x00003E = 1.9375 Hz.

To improve the accuracy, either gain register can be programmed to correct for the round-off error. This value would be calculated as

$$Vgn \text{ or } Ign = \frac{PulseRateE}{1.929} \cong 1.00441 = 0x404830$$

If (MCLK/K) is not equal to 4.096 MHz, the *PulseRateE$_{1,2}$ Register* must be scaled by a correction factor of:

$$\frac{4.096MHz}{(MCLK/K)} \times PulseRateE_{1,2}$$

Therefore if (MCLK/K) = 3.05856 MHz the value of *PulseRateE$_{1,2}$ Register* is

$$PulseRateE_{1,2} = \frac{4.096}{3.05856} \times 1.929Hz \cong 2.583Hz$$

5.5 Voltage Sag-detect Feature

Status bit VSAG in the *Status Register,* indicates a voltage sag occurred in the power line voltage. For a voltage sag condition to be identified, the absolute value of the instantaneous voltage must be less than the voltage sag level for more than half of the voltage sag duration (see Figure 7).

To activate Voltage Sag detect, a voltage sag level must be specified in the *Voltage Sag Level Register* (VSAGLevel), and a voltage sag duration must be specified in the *Voltage Sag Duration Register* (VSAGDuration). The voltage sag level is specified as the average of the absolute instantaneous voltage. Voltage sag duration is specified in terms of ADC cycles.

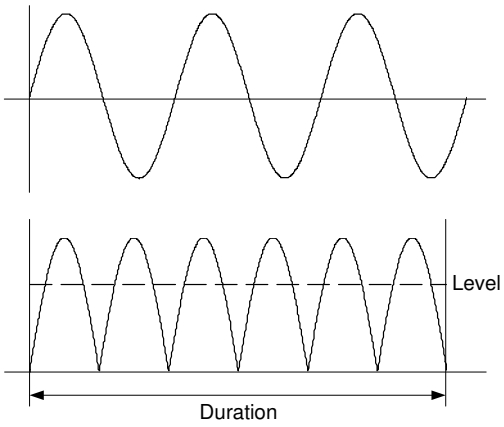


Figure 7. Voltage Sag Detect

5.6 No Load Threshold

The CS5461A includes the *LoadIntv* (No Load Detection Interval) register and the *LoadMin* register to implement the no load threshold function. When the accumulated energy measured within the time defined by the *LoadIntv* register does not reach the value in the *LoadMin* register, the pulse outputs will be disabled.

5.7 On-chip Temperature Sensor

The on-chip temperature sensor is designed to assist in characterizing the measurement element over a desired temperature range. Once a temperature characterization is performed, the temperature sensor can then be utilized to assist in compensating for temperature drift.

Temperature measurements are performed during continuous conversions and stored in the *Temperature Register*. The *Temperature Register* (T) default is Celsius scale (°C). The *Temperature Gain Register* (T_{gain}) and *Temperature Offset Register* (T_{off}) are constant values allowing for temperature scale conversions.

The temperature update rate is a function of the number of ADC samples. With MCLK = 4.096 MHz and K = 1 the update rate is:

$$\frac{2240 \text{ samples}}{(MCLK/K)/1024} = 0.56 \text{ sec}$$

The *Cycle Count Register* (N) must be set to a value greater than one. Status bit TUP in the *Status Register,* indicates when the *Temperature Register* is updated.

The *Temperature Offset Register* sets the zero-degree measurement. To improve temperature measurement accuracy, the zero-degree offset should be adjusted after the CS5461A is initialized. Temperature offset calibration is achieved by adjusting the *Temperature Offset Register* (T_{off}) by the differential temperature (ΔT) measured from a calibrated digital thermometer and the CS5461A temperature sensor. A one-degree adjustment to the *Temperature Register* (T) is achieved by adding 2.737649×10^{-4} to the *Temperature Offset Register* (T_{off}). Therefore,

$$T_{off} = T_{off} + (\Delta T \times 2.737649 \cdot 10^{-4})$$

if T_{off} = -0.0951126 and ΔT = -2.0 (°C), then

$$T_{off} = -0.0951126 + (-2.0 \times 2.737649 \cdot 10^{-4}) = -0.09566$$

or 0xF3C168 (2's compliment notation) is stored in the *Temperature Offset Register* (T_{off}).

To convert the *Temperature Register* (T) from a Celsius scale (°C) to a Fahrenheit scale (°F) utilize the formula

$$^{o}F = \frac{9}{5}(^{o}C + 17.7778)$$

Applying the above relationship to the CS5461A temperature measurement algorithm

$$T\langle^{o}F\rangle = (\frac{9}{5} \times T_{gain})[T\langle^{o}C\rangle + (T_{off} + (17.7778 \times 2.737649 \cdot 10^{-4}))]$$

If T_{off} = -0.09566 and T_{gain} = 23.507 for a Celsius scale, then the modified values are T_{off} = -0.0907935 (0xF460E1) and T_{gain} = 42.3132 (0x54A05E) for a Fahrenheit scale.

5.8 Voltage Reference

The CS5461A is specified for operation with a +2.5 V reference between the VREFIN and AGND pins. To utilize the on-chip 2.5 V reference, connect the VREFOUT pin to the VREFIN pin of the device. The VREFIN pin can be used to connect external filtering and/or references.

5.9 System Initialization

Upon powering up, the digital circuitry is held in reset until the analog voltage reaches 4.0 V. At that time, an eight-XIN-clock-period delay is enabled to allow the oscillator to stabilize. The CS5461A will then initialize.

A hardware reset is initiated when the $\overline{\text{RESET}}$ pin is asserted with a minimum pulse width of 50 ns. The $\overline{\text{RESET}}$ signal is asynchronous, with a Schmitt-trigger input. Once the $\overline{\text{RESET}}$ pin is de-asserted, an eight-XIN-clock-period delay is enabled.

A software reset is initiated by writing the command of 0x80. After a hardware or software reset, the internal registers (some of which drive output pins) will be reset to their *default* values. Status bit DRDY in the *Status Register,* indicates the CS5461A is in its *active* state and ready to receive commands.

5.10 Power-down States

The CS5461A has two power-down states, stand-by and sleep. In the stand-by state all circuitry except the voltage reference and crystal oscillator is turned off. To return the device to the active state a power-up command is sent to the device.

In sleep state all circuitry except the instruction decoder is turned off. When the power-up command is sent to the device, a system initialization is performed (see Section 5.9 *System Initialization* on page 20).

5.11 Oscillator Characteristics

The XIN and XOUT pins are the input and output of an inverting amplifier configured as an on-chip oscillator, as shown in Figure 8. The oscillator circuit is designed

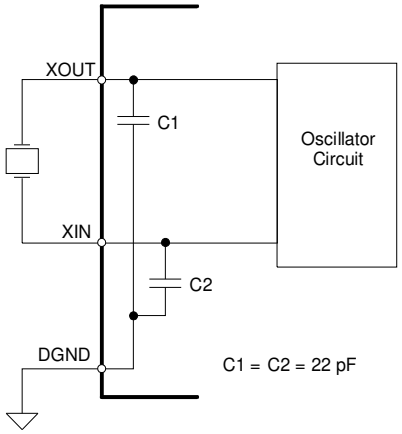


Figure 8. Oscillator Connection

to work with a quartz crystal. To reduce circuit cost, two load capacitors C1 and C2 are integrated in the device, from XIN to DGND, and XOUT to DGND. PCB trace lengths should be minimized to reduce stray capacitance. To drive the device from an external clock source, XOUT should be left unconnected while XIN is driven by the external circuitry. There is an amplifier between XIN and the digital section which provides CMOS-level signals. This amplifier works with sinusoi-

dal inputs so there are no problems with slow edge times.

The CS5461A can be driven by an external oscillator ranging from 2.5 to 20 MHz, but the K divider value must be set such that the internal MCLK will run somewhere between 2.5 MHz and 5 MHz. The K divider value is set with the K[3:0] bits in the *Configuration Register*. As an example, if XIN = MCLK = 15 MHz, and K is set to 5, then DCLK is 3 MHz, which is a valid value for DCLK.

5.12 Event Handler

The $\overline{\text{INT}}$ pin is used to indicate that an internal error or event has taken place in the CS5461A. Writing a logic 1 to any bit in the *Mask Register* allows the corresponding bit in the *Status Register* to activate the $\overline{\text{INT}}$ pin. The interrupt condition is cleared by writing a logic 1 to the bit that has been set in the *Status Register*.

The behavior of the $\overline{\text{INT}}$ pin is controlled by the IMODE and IINV bits of the *Configuration Register*.

IMODE	IINV	$\overline{\text{INT}}$ Pin
0	0	Active-low Level
0	1	Active-high Level
1	0	Low Pulse

Table 3. Interrupt Configuration

IMODE	IINV	$\overline{\text{INT}}$ Pin
1	1	High Pulse

Table 3. Interrupt Configuration

If the interrupt output signal format is set for either falling or rising edge, the duration of the $\overline{\text{INT}}$ pulse will be at least one DCLK cycle (DCLK = MCLK/K).

5.12.1 Typical Interrupt Handler

The steps below show how interrupts can be handled.

INITIALIZATION:

1) All Status bits are cleared by writing 0xFFFFFF to the Status Register.
2) The condition bits which will be used to generate interrupts are then set to logic 1 in the Mask Register.
3) Enable interrupts.

INTERRUPT HANDLER ROUTINE:

4) Read the Status Register.
5) Disable all interrupts.
6) Branch to the proper interrupt service routine.
7) Clear the Status Register by writing back the read value in step 4.
8) Re-enable interrupts.
9) Return from interrupt service routine.

5.13 Serial Port Overview

The CS5461A incorporates a serial port transmit and receive buffer with a command decoder that interprets one-byte (8 bits) commands as they are received. There are four types of commands; instructions, synchronizing, register writes and register reads (See Section 5.14 *Commands* on page 23).

Instructions are one byte in length and will interrupt any instruction currently executing. Instructions do not affect register reads currently being transmitted.

Synchronizing commands are one byte in length and only affect the serial interface. Synchronizing commands do not affect operations currently in progress.

Register writes must be followed by three bytes of data. register reads can return up to four bytes of data.

Commands and data are transferred most-significant bit (MSB) first. Figure 1 on page 11, defines the serial port timing and required sequence necessary to write to and read from the serial port receive and transmit buffer, respectively. While reading data from the serial port, commands and data can be simultaneously written. Starting a new register read command while data is being read will terminate the current read in progress. This is acceptable if the remainder of the current read data is not needed. During data reads, the serial port requires input data. If a new command and data is not sent, SYNC0 or SYNC1 must be sent.

5.13.1 Serial Port Interface

The serial port interface is a “4-wire” synchronous serial communications interface. The interface is enabled to start excepting SCLKs when $\overline{CS}$ (Chip Select) is asserted. SCLK (Serial bit-clock) is a Schmitt-trigger input that is used to strobe the data on SDI (Serial Data In) into the receive buffer and out of the transmit buffer onto SDO (Serial Data Out).

If the serial port interface becomes unsynchronized with respect to the SCLK input, any attempt to clock valid commands into the serial interface may result in unexpected operation. The serial port interface must then be re-initialized by one of the following actions:

- Drive the $\overline{CS}$ pin high, then low.
- Hardware Reset (drive $\overline{RESET}$ pin low, for at least 10 µs).
- Issue the *Serial Port Initialization Sequence*, which is 3 (or more) SYNC1 command bytes (0xFF) followed by one SYNC0 command byte (0xFE).

If a resynchronization is necessary, it is best to re-initialize the part either by hardware or software reset (0x80), as the state of the part may be unknown.

5.14 Commands

All commands are 8-bits in length. Any byte that is not listed in this section is invalid. Commands that write to registers must be followed by 3 bytes of data. Commands that read data can be chained with other commands (e.g., while reading data, a new command can be sent which can execute during the original read). All commands except register reads, register writes, and SYNC0 & SYNC1 will abort any currently executing commands.

5.14.1 Start Conversions

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	0	C3	C2	0	0

Initiates acquiring measurements and calculating results. The device has three modes of acquisition.

C[3:2] Modes of acquisition/measurement
00 = Perform a single computation cycle
01 = Not Used
10 = Perform continuous computation cycles
11 = Perform continuous computation cycles with APF enabled on the other channel

5.14.2 SYNC0 and SYNC1

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	1	1	1	1	SYNC

The serial port can be initialized by asserting $\overline{CS}$ or by sending three or more consecutive SYNC1 commands followed by a SYNC0 command. The SYNC0 or SYNC1 can also be sent while sending data out.

SYNC 0 = Last byte of a serial port re-initialization sequence.
1 = Used during reads and serial port initialization.

5.14.3 Power-Up/Halt

B7	B6	B5	B4	B3	B2	B1	B0
1	0	1	0	0	0	0	0

If the device is powered-down, Power-Up/Halt will initiate a power on reset. If the part is already powered-on, all computations will be halted.

5.14.4 Power-down and Software Reset

B7	B6	B5	B4	B3	B2	B1	B0
1	0	0	S1	S0	0	0	0

To conserve power the CS5461A has two power-down states. In stand-by state all circuitry, except the analog/digital clock generators, is turned off. In the sleep state all circuitry, except the instruction decoder, is turned off. Bringing the CS5461A out of sleep state requires more time than out of stand-by state, because of the extra time needed to re-start and re-stabilize the analog oscillator.

S[1:0] Power-down state
00 = Software Reset
01 = Halt and enter stand-by power saving state. This state allows quick power-on
10 = Halt and enter sleep power saving state.
11 = Reserved

5.14.5 Register Read/Write

B7	B6	B5	B4	B3	B2	B1	B0
0	W/R	RA4	RA3	RA2	RA1	RA0	0

The Read/Write informs the command decoder that a register access is required. During a read operation, the addressed register is loaded into an output buffer and clocked out by SCLK. During a write operation, the data is clocked into an input buffer and transferred to the addressed register upon completion of the 24th SCLK.

W/$\overline{R}$ Write/Read control
0 = Read
1 = Write

RA[4:0] Register address bits (bits 5 through 1) of the read/write command.

Address	RA[4:0]	Name	Description
0	00000	Config	Configuration
1	00001	I_{DCoff}	Current DC Offset
2	00010	I_{gn}	Current Gain
3	00011	V_{DCoff}	Voltage DC Offset
4	00100	V_{gn}	Voltage Gain
5	00101	Cycle Count	Number of A/D conversions used in one computation cycle (N)).
6	00110	$PulseRateE_{1,2}$	Sets the $\overline{E1}$ and $\overline{E2}$ energy-to-frequency output pulse rate.
7	00111	I	Instantaneous Current
8	01000	V	Instantaneous Voltage
9	01001	P	Instantaneous Power
10	01010	P_{Active}	Active (Real) Power
11	01011	I_{RMS}	RMS Current
12	01100	V_{RMS}	RMS Voltage
14	01110	P_{off}	Power Offset
15	01111	Status	Status
16	10000	I_{ACoff}	Current AC (RMS) Offset
17	10001	V_{ACoff}	Voltage AC (RMS) Offset
18	10010	$PulseRateE_3$	Sets the $\overline{E3}$ energy-to-frequency output pulse rate.
19	10011	T	Temperature
20	10100	SYS_{Gain}	System Gain
21	10101	PW	Pulse width register for mechanical counter output mode
22	10110	PulseWidth	Pulse width register for $\overline{E3}$ energy pulse output
23	10111	$VSAG_{Duration}$	Voltage Sag Duration
24	11000	$VSAG_{Level}$	Voltage Sag Level Threshold
25	11001	LoadIntv	No load threshold interval (detection window)
26	11010	Mask	Interrupt Mask
27	11011	LoadMin	No Load Threshold
28	11100	Ctrl	Control
29	11101	T_{Gain}	Temperature Sensor Gain
30	11110	T_{off}	Temperature Sensor Offset
31	11111	S	Apparent Power

Note: For proper operation, *do not* attempt to write to unspecified registers.

5.14.6 Calibration

B7	B6	B5	B4	B3	B2	B1	B0
1	1	0	CAL4	CAL3	CAL2	CAL1	CAL0

The CS5461A can perform system calibrations. Proper input signals must be applied to the current and voltage channel before performing a designated calibration.

CAL[4:0]* Designates calibration to be performed
01001 = Current channel DC offset
01010 = Current channel DC gain
01101 = Current channel AC offset
01110 = Current channel AC gain
10001 = Voltage channel DC offset
10010 = Voltage channel DC gain
10101 = Voltage channel AC offset
10110 = Voltage channel AC gain
11001 = Current and Voltage channel DC offset
11010 = Current and Voltage channel DC gain
11101 = Current and Voltage channel AC offset
11110 = Current and Voltage channel AC gain

*Values for CAL[4:0] not specified should not be used.