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CS5463

Single Phase, Bi-directional Power/Energy IC

Features

- Energy Data Linearity: ±0.1% of Reading over 1000:1 Dynamic Range
- On-chip Functions:
  - Instantaneous Voltage, Current, and Power
  - I_{RMS} and V_{RMS}, Apparent, Reactive, and Active (Real) Power
  - Active Fundamental and Harmonic Power
  - Reactive Fundamental, Power Factor, and Line Frequency
  - Energy-to-pulse Conversion
  - System Calibrations and Phase Compensation
  - Temperature Sensor
- Meets accuracy spec for IEC, ANSI, JIS.
- Low Power Consumption
- Current Input Optimized for Sense Resistor.
- GND-referenced Signals with Single Supply
- On-chip 2.5 V Reference (25 ppm/°C typ)
- Power Supply Monitor
- Simple Three-wire Digital Serial Interface
- "Auto-boot" Mode from Serial E^2PROM
- Power Supply Configurations:
  VA+ = +5 V; AGND = 0 V; VD+ = +3.3 V to +5 V

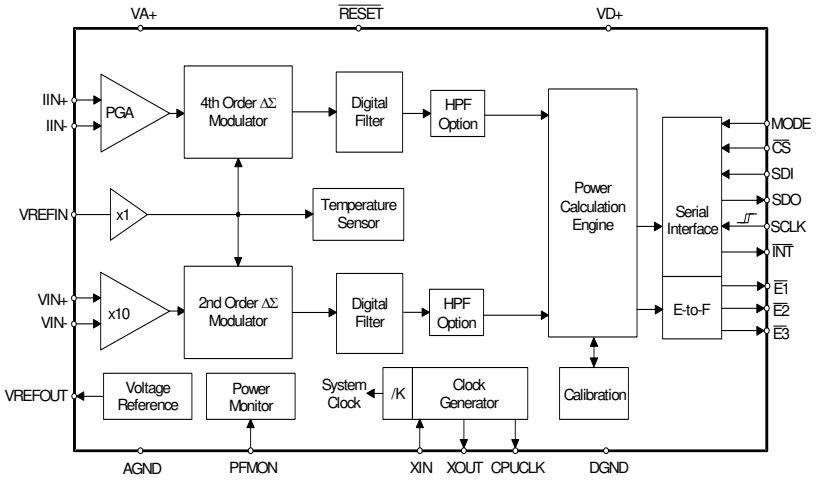
Description

The CS5463 is an integrated power measurement device which combines two ΔΣ analog-to-digital converters, power calculation engine, energy-to-frequency converter, and a serial interface on a single chip. It is designed to accurately measure instantaneous current and voltage, and calculate V_{RMS}, I_{RMS}, instantaneous power, apparent power, active power, and reactive power for single-phase, 2- or 3-wire power metering applications.

The CS5463 is optimized to interface to shunt resistors or current transformers for current measurement, and to resistive dividers or potential transformers for voltage measurement.

The CS5463 features a bi-directional serial interface for communication with a processor and a programmable energy-to-pulse output function. Additional features include on-chip functionality to facilitate system-level calibration, temperature sensor, voltage sag detection, and phase compensation.

ORDERING INFORMATION:
See Page 45.



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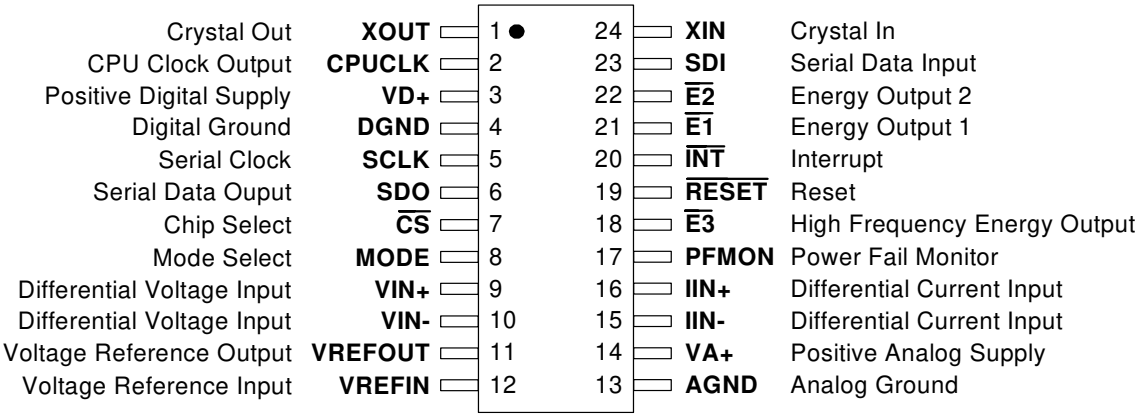
1. OVERVIEW

The CS5463 is a CMOS monolithic power measurement device with a computation engine and an energy-to-frequency pulse output. The CS5463 combines a programmable gain amplifier, two ΔΣ Analog-to-Digital Converters (ADCs), system calibration, and a computation engine on a single chip.

The CS5463 is designed for power measurement applications and is optimized to interface to a current sense resistor or transformer for current measurement, and to a resistive divider or potential transformer for voltage measurement. The current channel provides programmable gains to accommodate various input levels from a multitude of sensing elements. With single +5 V supply on VA+/AGND, both of the CS5463's input channels can accommodate common mode plus signal levels between (AGND - 0.25 V) and VA+.

The CS5463 also is equipped with a computation engine that calculates instantaneous power, I_{RMS}, V_{RMS}, apparent power, active (real) power, reactive power, harmonic active power, active and reactive fundamental power, and power factor. The CS5463 additional features include line frequency, current and voltage sag detection, zero-cross detection, positive-only accumulation mode, and three programmable pulse output pins. To facilitate communication to a microprocessor, the CS5463 includes a simple three-wire serial interface which is SPI™ and Microwire™ compatible. The CS5463 provides three outputs for energy registration. $\overline{E1}$, $\overline{E2}$, and $\overline{E3}$ are designed to interface to a microprocessor.

2. PIN DESCRIPTION



Clock Generator		
Crystal Out **Crystal In**	1,24	**XOUT, XIN** – The output and input of an inverting amplifier. Oscillation occurs when connected to a crystal, providing an on-chip system clock. Alternatively, an external clock can be supplied to the XIN pin to provide the system clock for the device.
CPU Clock Output	2	**CPUCLK** – Output of on-chip oscillator which can drive one standard CMOS load.
Control Pins and Serial Data I/O		
Serial Clock Input	5	**SCLK** – A Schmitt-trigger input pin. Clocks data from the SDI pin into the receive buffer and out of the transmit buffer onto the SDO pin when $\overline{CS}$ is low.
Serial Data Output	6	**SDO** – Serial port data output pin.SDO is forced into a high-impedance state when $\overline{CS}$ is high.
Chip Select	7	**$\overline{CS}$** – Low, activates the serial port interface.
Mode Select	8	**MODE** - High, enables the “auto-boot” mode. The mode pin has an internal pull-down resistor.
Energy Output	18,21,22	**$\overline{E3}$, $\overline{E1}$, $\overline{E2}$** – Active-low pulses with an output frequency proportional to the selected power. Configurable outputs for active, apparent, and reactive power, negative energy indication, zero cross detection, and power failure monitoring. $\overline{E1}$, $\overline{E2}$, $\overline{E3}$ outputs are configured in the Operational Modes Register.
Reset	19	**$\overline{RESET}$** – A Schmitt-trigger input pin. Low activates Reset, all internal registers (some of which drive output pins) are set to their default states.
Interrupt	20	**$\overline{INT}$** - Low, indicates that an enabled event has occurred.
Serial Data Input	23	**SDI** - Serial port data input pin. Data will be input at a rate determined by SCLK.
Analog Inputs/Outputs		
Differential Voltage Inputs	9,10	**VIN+, VIN-** – Differential analog input pins for the voltage channel.
Differential Current Inputs	15,16	**IIN+, IIN-** – Differential analog input pins for the current channel.
Voltage Reference Output	11	**VREFOUT** – The on-chip voltage reference output. The voltage reference has a nominal magnitude of 2.5 V and is referenced to the AGND pin on the converter.
Voltage Reference Input	12	**VREFIN** – The input to this pin establishes the voltage reference for the on-chip modulator.
Power Supply Connections		
Positive Digital Supply	3	**VD+** – The positive digital supply.
Digital Ground	4	**DGND** – Digital Ground.
Positive Analog Supply	14	**VA+** – The positive analog supply.
Analog Ground	13	**AGND** – Analog ground.
Power Fail Monitor	17	**PFMON** – The power fail monitor pin monitors the analog supply. If the analog supply does not meet or falls below PFMON’s voltage threshold, a Low-supply Detect (LSD) event is set in the status register.

3. CHARACTERISTICS & SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Positive Digital Power Supply	VD+	3.135	5.0	5.25	V
Positive Analog Power Supply	VA+	4.75	5.0	5.25	V
Voltage Reference	VREFIN	-	2.5	-	V
Specified Temperature Range	T_A	-40	-	+85	°C

ANALOG CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all *Recommended Operating Conditions*.
- Typical characteristics and specifications are measured at nominal supply voltages and TA = 25 °C.
- VA+ = VD+ = 5 V ±5%; AGND = DGND = 0 V; VREFIN = +2.5 V. All voltages with respect to 0 V.
- MCLK = 4.096 MHz.

Parameter		Symbol	Min	Typ	Max	Unit
Accuracy						
Active Power (Note 1)	All Gain Ranges Input Range 0.1% - 100%	P_{Active}	-	±0.1	-	%
Average Reactive Power (Note 1 and 2)	All Gain Ranges Input Range 0.1% - 100%	Q_{Avg}	-	±0.2	-	%
Power Factor (Note 1 and 2)	All Gain Ranges Input Range 1.0% - 100% Input Range 0.1% - 1.0%	PF	- -	±0.2 ±0.27	- -	% %
Current RMS (Note 1)	All Gain Ranges Input Range 0.2% - 100% Input Range 0.1% - 0.2%	I_{RMS}	- -	±0.2 ±1.5	- -	% % %
Voltage RMS (Note 1)	All Gain Ranges Input Range 5% - 100%	V_{RMS}	-	±0.1	-	%
Analog Inputs (Both Channels)						
Common Mode Rejection	(DC, 50, 60 Hz)	CMRR	80	-	-	dB
Common Mode + Signal	All Gain Ranges		-0.25	-	VA+	V
Analog Inputs (Current Channel)						
Differential Input Range [(IIN+) - (IIN-)]	(Gain = 10) (Gain = 50)	IIN	- -	500 100	- -	mV_{P-P} mV_{P-P}
Total Harmonic Distortion	(Gain = 50)	THD	80	94	-	dB
Crosstalk with Voltage Channel at Full Scale	(50, 60 Hz)		-	-115	-	dB
Input Capacitance	(Gain = 10) (Gain = 50)	IC	- -	32 52	- -	pF pF
Effective Input Impedance		EII	30	-	-	kΩ
Noise (Referred to Input)	(Gain = 10) (Gain = 50)	N_I	- -	22.5 4.5	- -	μV_{rms} μV_{rms}
Offset Drift (Without the High Pass Filter)		OD	-	4.0	-	µV/°C
Gain Error	(Note 3)	GE	-	±0.4		%

Notes: 1. Applies when the HPF option is enabled.

2. Applies when the line frequency is equal to the product of the Output Word Rate (OWR) and the value of epsilon (ε).

ANALOG CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
Analog Inputs (Voltage Channel)					
Differential Input Range [(VIN+) - (VIN-)]	VIN	-	500	-	mV_{P-P}
Total Harmonic Distortion	THD	65	75	-	dB
Crosstalk with Current Channel at Full Scale (50, 60 Hz)		-	-70	-	dB
Input Capacitance All Gain Ranges	IC	-	0.2	-	pF
Effective Input Impedance	EII	2	-	-	MΩ
Noise (Referred to Input)	N_V	-	140	-	μV_{rms}
Offset Drift (Without the High Pass Filter)	OD	-	16.0	-	µV/°C
Gain Error (Note 3)	GE	-	±3.0		%
Temperature Channel					
Temperature Accuracy	T	-	±5	-	°C
Power Supplies					
Power Supply Currents (Active State) I_{A+}	PSCA	-	1.1	-	mA
I_{D+} (VA+ = VD+ = 5 V)	PSCD	-	2.9	-	mA
I_{D+} (VA+ = 5 V, VD+ = 3.3 V)	PSCD	-	1.7	-	mA
Power Consumption Active State (VA+ = VD+ = 5 V)	PC	-	21	29	mW
(Note 4) Active State (VA+ = 5 V, VD+ = 3.3 V)		-	11.6	17.5	mW
Stand-by State		-	8	-	mW
Sleep State		-	10	-	µW
Power Supply Rejection Ratio (50, 60 Hz)			-	-	
(Note 5) Voltage Channel	PSRR	45	65	-	dB
Current Channel		70	75	-	dB
PFMON Low-voltage Trigger Threshold (Note 6)	PMLO	2.3	2.45	-	V
PFMON High-voltage Power-on Trip Point (Note 7)	PMHI	-	2.55	2.7	V

Notes:
3. Applies before system calibration.
4. All outputs unloaded. All inputs CMOS level.
5. Measurement method for PSRR: VREFIN tied to VREFOUT, VA+ = VD+ = 5 V, a 150 mV (zero-to-peak) (60 Hz) sinewave is imposed onto the +5 V DC supply voltage at VA+ and VD+ pins. The "+" and "-" input pins of both input channels are shorted to AGND. Then the CS5463 is commanded to continuous conversion acquisition mode, and digital output data is collected for the channel under test. The (zero-to-peak) value of the digital sinusoidal output signal is determined, and this value is converted into the (zero-to-peak) value of the sinusoidal voltage (measured in mV) that would need to be applied at the channel's inputs, in order to cause the same digital sinusoidal output. This voltage is then defined as Veq. PSRR is then (in dB):

$$PSRR = 20 \cdot \log\left[\frac{150}{V_{eq}}\right]$$

6. When voltage level on PFMON is sagging, and LSD bit = 0, the voltage at which LSD is set to 1.
7. If the LSD bit has been set to 1 (because PFMON voltage fell below PMLO), this is the voltage level on PFMON at which the LSD bit can be permanently reset back to 0.

VOLTAGE REFERENCE

Parameter		Symbol	Min	Typ	Max	Unit
Reference Output						
Output Voltage		VREFOUT	+2.4	+2.5	+2.6	V
Temperature Coefficient	(Note 8)	TC_{VREF}	-	25	60	ppm/°C
Load Regulation	(Note 9)	ΔV_R	-	6	10	mV
Reference Input						
Input Voltage Range		VREFIN	+2.4	+2.5	+2.6	V
Input Capacitance			-	4	-	pF
Input CVF Current			-	25	-	nA

Notes: 8. The voltage at VREFOUT is measured across the temperature range. From these measurements the following formula is used to calculate the VREFOUT Temperature Coefficient:.

$$TC_{VREF} = \left(\frac{(VREFOUT_{MAX} - VREFOUT_{MIN})}{VREFOUT_{AVG}}\right)\left(\frac{1}{T_{AMAX} - T_{AMIN}}\right)\left(1.0 \times 10^{6}\right)$$

9. Specified at maximum recommended output of 1 µA, source or sink.

DIGITAL CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all *Recommended Operating Conditions*.
- Typical characteristics and specifications are measured at nominal supply voltages and TA = 25 °C.
- VA+ = VD+ = 5V ±5%; AGND = DGND = 0 V. All voltages with respect to 0 V.
- MCLK = 4.096 MHz.

Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Characteristics						
Master Clock Frequency	Internal Gate Oscillator (Note 11)	MCLK	2.5	4.096	20	MHz
Master Clock Duty Cycle			40	-	60	%
CPUCLK Duty Cycle	(Note 12 and 13)		40	-	60	%
Filter Characteristics						
Phase Compensation Range	(Voltage Channel, 60 Hz)		-2.8	-	+2.8	°
Input Sampling Rate	DCLK = MCLK/K		-	DCLK/8	-	Hz
Digital Filter Output Word Rate	(Both Channels)	OWR	-	DCLK/1024	-	Hz
High-pass Filter Corner Frequency	-3 dB		-	0.5	-	Hz
Full-scale DC Calibration Range (Referred to Input)	(Note 14)	FSCR	25	-	100	%F.S.
Channel-to-channel Time-shift Error	(Note 15)			1.0		µs
Input/Output Characteristics						
High-level Input Voltage		V_{IH}				
	All Pins Except XIN and SCLK and $\overline{RESET}$		0.6 VD+	-	-	V
	XIN		(VD+) - 0.5	-	-	V
	SCLK and $\overline{RESET}$		0.8 VD+	-	-	V
Low-level Input Voltage (VD = 5 V)		V_{IL}				
	All Pins Except XIN and SCLK and $\overline{RESET}$		-	-	0.8	V
	XIN		-	-	1.5	V
	SCLK and $\overline{RESET}$		-	-	0.2 VD+	V

Parameter	Symbol	Min	Typ	Max	Unit
Low-level Input Voltage (VD = 3.3 V)	V_{IL}				
All Pins Except XIN and SCLK and $\overline{\text{RESET}}$		-	-	0.48	V
XIN		-	-	0.3	V
SCLK and $\overline{\text{RESET}}$		-	-	0.2 VD+	V
High-level Output Voltage I_{out} = +5 mA	V_{OH}	(VD+) - 1.0	-	-	V
Low-level Output Voltage I_{out} = -5 mA	V_{OL}	-	-	0.4	V
Input Leakage Current (Note 16)	I_{in}	-	±1	±10	µA
3-state Leakage Current	I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance	C_{out}	-	5	-	pF

Notes: 10. All measurements performed under static conditions.

11. If a crystal is used, then XIN frequency must remain between 2.5 MHz - 5.0 MHz. If an external oscillator is used, XIN frequency range is 2.5 MHz - 20 MHz, but K must be set so that MCLK is between 2.5 MHz - 5.0 MHz.
12. If external MCLK is used, then the duty cycle must be between 45% and 55% to maintain this specification.
13. The frequency of CPUCLK is equal to MCLK.
14. The minimum FSCR is limited by the maximum allowed gain register value. The maximum FSCR is limited by the full-scale signal applied to the channel input.
15. Configuration Register bits PC[6:0] are set to “0000000”.
16. The MODE pin is pulled low by an internal resistor.

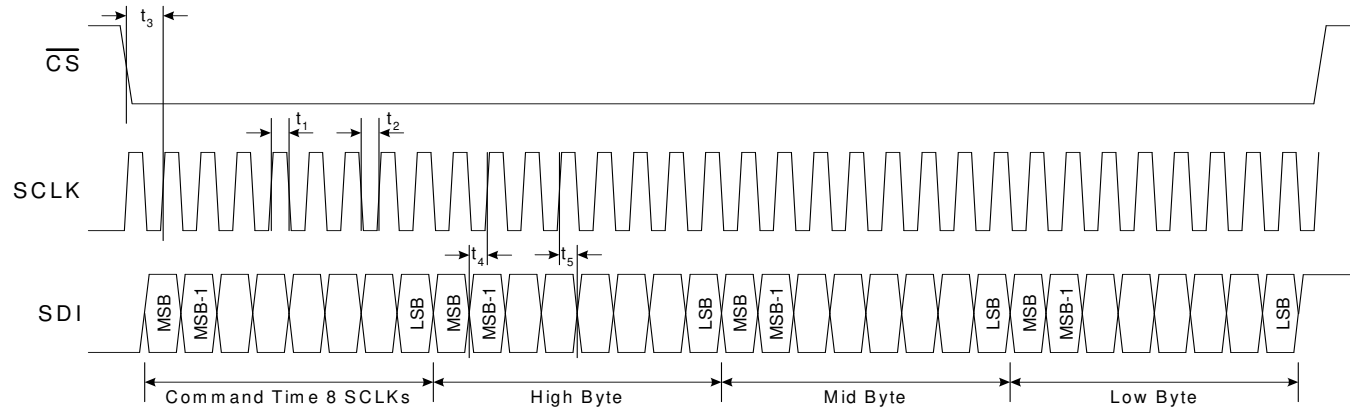
SWITCHING CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all *Recommended Operating Conditions*.
- Typical characteristics and specifications are measured at nominal supply voltages and TA = 25 °C.
- VA+ = 5 V ±5% VD+ = 3.3 V ±5% or 5 V ±5%; AGND = DGND = 0 V. All voltages with respect to 0 V.
- Logic Levels: Logic 0 = 0 V, Logic 1 = VD+.

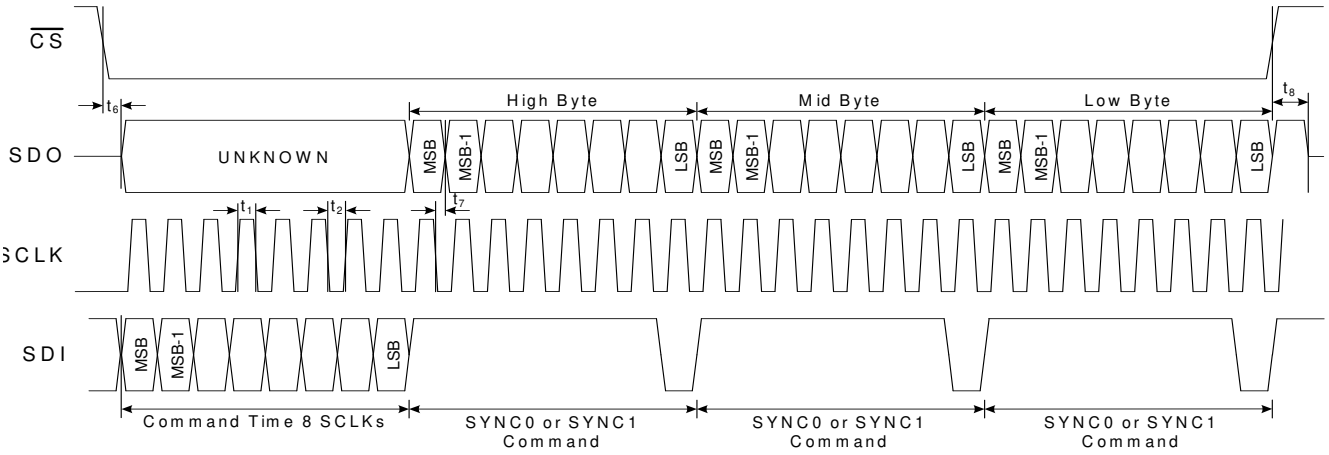
Parameter		Symbol	Min	Typ	Max	Unit
Rise Times	Any Digital Input Except SCLK	t_{rise}	-	-	1.0	µs
(Note 17)	SCLK		-	-	100	µs
	Any Digital Output		-	50	-	ns
Fall Times	Any Digital Input Except SCLK	t_{fall}	-	-	1.0	µs
(Note 17)	SCLK		-	-	100	µs
	Any Digital Output		-	50	-	ns
Start-up						
Oscillator Start-up Time	XTAL = 4.096 MHz (Note 18)	t_{ost}	-	60	-	ms
Serial Port Timing						
Serial Clock Frequency		SCLK	-	-	2	MHz
Serial Clock	Pulse Width High	t_1	200	-	-	ns
	Pulse Width Low	t_2	200	-	-	ns
SDI Timing						
$\overline{CS}$ Falling to SCLK Rising		t_3	50	-	-	ns
Data Set-up Time Prior to SCLK Rising		t_4	50	-	-	ns
Data Hold Time After SCLK Rising		t_5	100	-	-	ns
SDO Timing						
$\overline{CS}$ Falling to SDI Driving		t_6	-	20	50	ns
SCLK Falling to New Data Bit (hold time)		t_7	-	20	50	ns
$\overline{CS}$ Rising to SDO Hi-Z		t_8	-	20	50	ns
Auto-Boot Timing						
Serial Clock	Pulse Width Low	t_9		8		MCLK
	Pulse Width High	t_{10}		8		MCLK
MODE setup time to $\overline{RESET}$ Rising		t_{11}	50			ns
$\overline{RESET}$ rising to $\overline{CS}$ falling		t_{12}	48			MCLK
$\overline{CS}$ falling to SCLK rising		t_{13}	100	8		MCLK
SCLK falling to $\overline{CS}$ rising		t_{14}		16		MCLK
$\overline{CS}$ rising to driving MODE low (to end auto-boot sequence)		t_{15}	50			ns
SDO guaranteed setup time to SCLK rising		t_{16}	100			ns

Notes: 17. Specified using 10% and 90% points on waveform of interest. Output loaded with 50 pF.

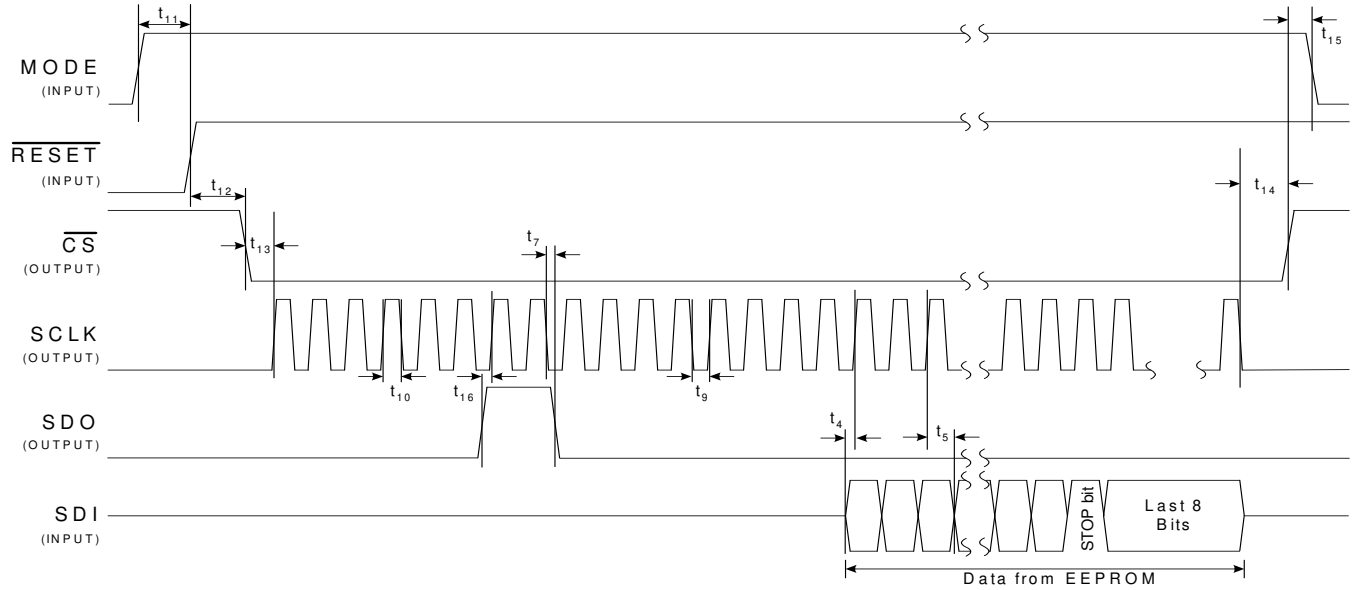
18. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.



SDI Write Timing (Not to Scale)



SDO Read Timing (Not to Scale)



Auto-boot Sequence Timing (Not to Scale)

Figure 1. CS5463 Read and Write Timing Diagrams

SWITCHING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{E1}$, $\overline{E2}$, and $\overline{E3}$ Timing (Note 19 and 20)					
Period	t_{period}	250	-	-	µs
Pulse Width	t_{pw}	244	-	-	µs
Rising Edge to Falling Edge	t_3	6	-	-	µs
$\overline{E2}$ Setup to $\overline{E1}$ and/or $\overline{E3}$ Falling Edge	t_4	1.5	-	-	µs
$\overline{E1}$ Falling Edge to $\overline{E3}$ Falling Edge	t_5	248	-	-	µs

Notes: 19. Pulse output timing is specified at MCLK = 4.096 MHz, E2MODE = 0, and E3MODE[1:0] = 0. Refer to Section 5.5 *Energy Pulse Output* on page 17 for more information on pulse output pins.

20. Timing is proportional to the frequency of MCLK.

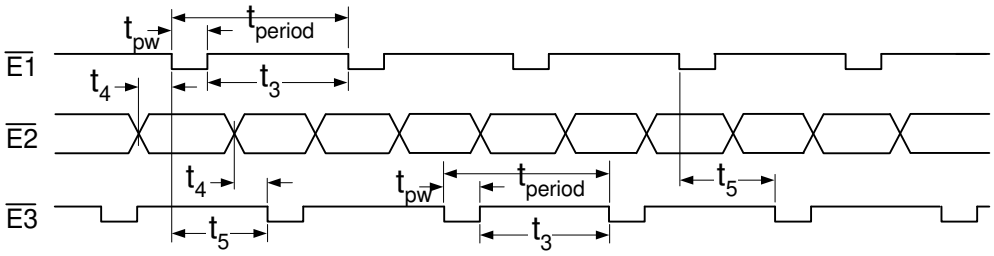


Figure 2. Timing Diagram for $\overline{E1}$, $\overline{E2}$, and $\overline{E3}$

ABSOLUTE MAXIMUM RATINGS

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	(Notes 21 and 22)					
	Positive Digital	VD+	-0.3	-	+6.0	V
	Positive Analog	VA+	-0.3	-	+6.0	V
Input Current, Any Pin Except Supplies	(Notes 23, 24, 25)	I_{IN}	-	-	±10	mA
Output Current, Any Pin Except VREFOUT		I_{OUT}	-	-	100	mA
Power Dissipation	(Note 26)	P_D	-	-	500	mW
Analog Input Voltage	All Analog Pins	V_{INA}	- 0.3	-	(VA+) + 0.3	V
Digital Input Voltage	All Digital Pins	V_{IND}	-0.3	-	(VD+) + 0.3	V
Ambient Operating Temperature		T_A	-40	-	85	°C
Storage Temperature		T_{stg}	-65	-	150	°C

Notes: 21. VA+ and AGND must satisfy [(VA+) - (AGND)] ≤ + 6.0 V.

22. VD+ and AGND must satisfy [(VD+) - (AGND)] ≤ + 6.0 V.

23. Applies to all pins including continuous over-voltage conditions at the analog input pins.

24. Transient current of up to 100 mA will not cause SCR latch-up.

25. Maximum DC input current for a power supply pin is ±50 mA.

26. Total power dissipation, including all input currents and output currents.

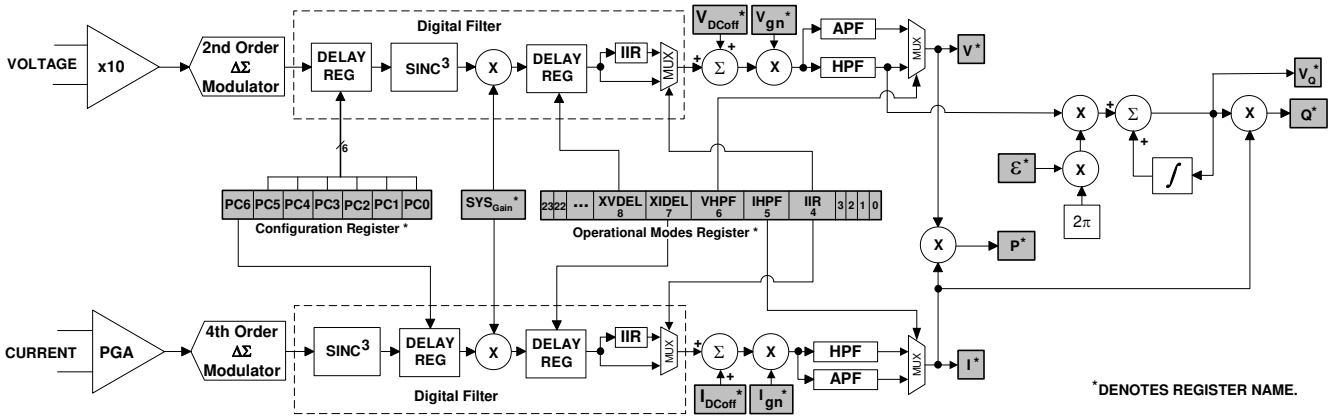


Figure 3. Data Measurement Flow Diagram.

4. THEORY OF OPERATION

The CS5463 is a dual-channel analog-to-digital converter (ADC) followed by a computation engine that performs power calculations and energy-to-pulse conversion. The data flow for the voltage and current channel measurement and the power calculation algorithms are depicted in Figure 3 and 4, respectively.

The analog inputs are structured with two dedicated channels, *Voltage* and *Current*, then optimized to simplify interfacing to various sensing elements.

The voltage-sensing element introduces a voltage waveform on the voltage channel input VIN± and is subject to a gain of 10x. A second-order delta-sigma modulator samples the amplified signal for digitization.

Simultaneously, the current-sensing element introduces a voltage waveform on the current channel input IIN± and is subject to two selectable gains of the programmable gain amplifier (PGA). The amplified signal is sampled by a fourth-order delta-sigma modulator for digitization. Both converters sample at a rate of MCLK/8, the over-sampling provides a wide dynamic range and simplified anti-alias filter design.

4.1 Digital Filters

The decimating digital filters on both channels are $Sinc^3$ filters followed by 4th-order IIR filters. The single-bit data is passed to the low-pass decimation filter and output at a fixed word rate. The output word is passed to an optional IIR filter to compensate for the magnitude roll off of the low-pass filtering operation.

An optional digital high-pass filter (*HPF* in Figure 3) removes any DC component from the selected signal path. By removing the DC component from the voltage and/or the current channel, any DC content will also be removed from the calculated active power as well. With both HPFs enabled the DC component will be removed from the calculated V_{RMS} and I_{RMS} as well as the apparent power.

When the optional HPF in either channel is disabled, an all-pass filter (APF) is implemented. The APF has an amplitude response that is flat within the channel bandwidth and is used for matching phase in systems where only one HPF is engaged.

4.2 Voltage and Current Measurements

The digital filter output word is then subject to a DC offset adjustment and a gain calibration (See Section 7. *System Calibration* on page 37). The calibrated measurement is available by reading the instantaneous voltage and current registers.

The Root Mean Square (*RMS* in Figure 4) calculations are performed on N instantaneous voltage and current samples, V_n and I_n, respectively (where N is the cycle count), using the formula:

$$I_{RMS} = \sqrt{\frac{\sum_{n=0}^{N-1} I_n}{N}}$$

and likewise for V_{RMS}, using V_n. I_{RMS} and V_{RMS} are accessible by register reads, which are updated once every cycle count (referred to as a computational cycle).

4.3 Power Measurements

The instantaneous voltage and current samples are multiplied to obtain the instantaneous power (see Figure 3). The product is then averaged over N conversions to compute active power and is used to drive energy pulse output $\overline{E1}$. Energy output $\overline{E2}$ is selectable, providing an energy sign or a pulse output that is proportional to the apparent power. Energy output $\overline{E3}$

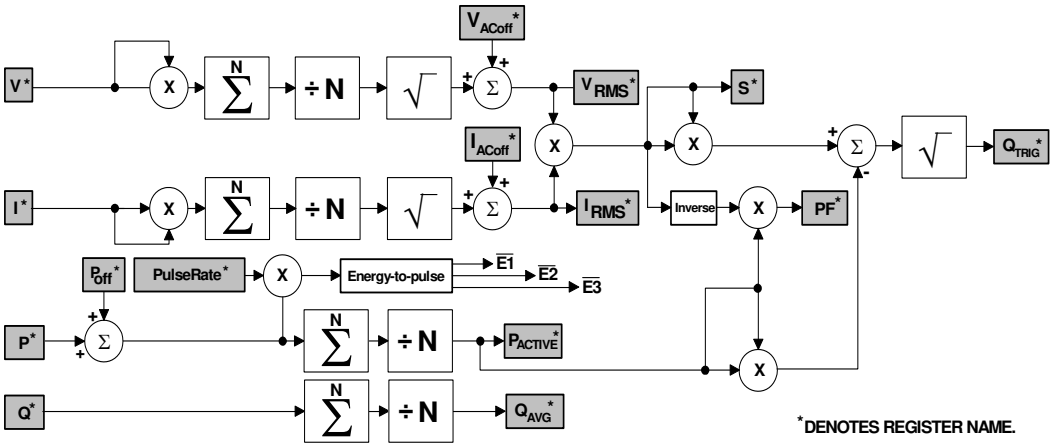


Figure 4. Power Calculation Flow.

provides a pulse output that is proportional to the reactive power or apparent power. Output $\overline{E3}$ can also be set to display the sign of the voltage applied to the voltage channel or the PFMON comparator output.

The apparent power (S) is the combination of the active power and reactive power, without reference to an impedance phase angle, and is calculated by the CS5463 using the following formula:

$$S = V_{RMS} \times I_{RMS}$$

Power Factor (PF) is the active power (P_{Active}) divided by the apparent power (S)

$$PF = \frac{P_{Active}}{S}$$

The sign of the power factor is determined by the active power.

The CS5463 calculates the reactive power, Q_{Trig} utilizing trigonometric identities, giving the formula

$$Q_{Trig} = \sqrt{S^2 - P_{Active}^2}$$

Average reactive power, Q_{Avg}, is generated by averaging the voltage multiplied by the current with a 90° phase shift difference between them. The 90° phase shift is realized by applying an IIR digital filter in the voltage channel to obtain quadrature voltage (see Figure 3). This filter will give exactly -90° phase shift across all frequencies, and utilizes epsilon (ε) to achieve unity gain at the line frequency.

The instantaneous quadrature voltage (V_Q) and current (I) samples are multiplied to obtain the instantaneous quadrature power (Q). The product is then averaged over N conversions, utilizing the formula

$$Q_{Avg} = \frac{\sum_{n=1}^{N} Q_n}{N}$$

Fundamental active (P_F) and reactive (Q_F) power is calculated by performing a discrete Fourier transform (DFT) at the relevant frequency on the instantaneous voltage (V) and current (I). Epsilon is used to set the frequency of the internal sine (imaginary component) and cosine (real component) waveform generator. The harmonic active power (P_H) is calculated by subtracting the fundamental active power (P_F) from the active power (P_{Active}).

The peak current (I_{peak}) and peak voltage (V_{peak}) are the instantaneous current and voltage, respectively, with the greatest magnitude detected during the last computation cycle. Active, apparent, reactive, and fundamental power are updated every computation cycle.

4.4 Linearity Performance

The linearity of the V_{RMS}, I_{RMS}, active, reactive, and power-factor power measurements (before calibration) will be within ±0.1% of reading over the ranges specified, with respect to the input voltage levels required to cause full-scale readings in the I_{RMS} and V_{RMS} registers. Refer to *Accuracy Specifications* on page 7.

Until the CS5463 is calibrated, the *accuracy* of the CS5463 (with respect to a reference line-voltage and line-current level on the power mains) is not guaranteed to within ±0.1%. (See Section 7. *System Calibration* on page 37.) The accuracy of the internal calculations can often be improved by selecting a value for the Cycle Count Register that will cause the time duration of one computation cycle to be equal to (or very close to) a whole number of power-line cycles (and N must be greater than or equal to 4000).

5. FUNCTIONAL DESCRIPTION

5.1 Analog Inputs

The CS5463 is equipped with two fully differential input channels. The inputs VIN± and IIN± are designated as the voltage and current channel inputs, respectively. The full-scale differential input voltage for the current and voltage channel is ±250 mV_P.

5.1.1 Voltage Channel

The output of the line voltage resistive divider or transformer is connected to the VIN+ and VIN- input pins of the CS5463. The voltage channel is equipped with a 10x fixed-gain amplifier. The full-scale signal level that can be applied to the voltage channel is ±250 mV. If the input signal is a sine wave the maximum RMS voltage at a gain 10x is:

$$\frac{250\,mV_P}{\sqrt{2}} \cong 176.78\,mV_{RMS}$$

which is approximately 70.7% of maximum peak voltage. The voltage channel is also equipped with a *Voltage Gain Register*, allowing for an additional programmable gain of up to 4x.

5.1.2 Current Channel

The output of the current-sense resistor or transformer is connected to the IIN+ and IIN- input pins of the CS5463. To accommodate different current sensing elements the current channel incorporates a programmable gain amplifier (PGA) with two programmable input gains. *Configuration Register* bit Igain (see Table 1) defines the two gain selections and corresponding maximum input-signal level.

Igain	Maximum Input Range	
0	±250 mV	10x
1	±50 mV	50x

Table 1. Current Channel PGA Setting

For example, if Igain=0, the current channel's PGA gain is set to 10x. If the input signals are pure sinusoids with zero phase shift, the maximum peak differential signal on the current or voltage channel is ±250 mV_P. The input signal levels are approximately 70.7% of maximum peak voltage producing a full-scale energy pulse registration equal to 50% of absolute maximum energy pulse registration. This will be discussed further in See Section 5.5 *Energy Pulse Output* on page 17.

The *Current Gain Register* also facilitates an additional programmable gain of up to 4x. If an additional gain is applied to the voltage and/or current channel, the maximum input range should be adjusted accordingly.

5.2 IIR Filters

The current and voltage channel are equipped with a 4th-order IIR filter, that is used to compensate for the magnitude roll off of the low-pass decimation filter. *Operational Mode Register* bit $\overline{IIR}$ engages the IIR filters in both the voltage and current channels.

5.3 High-pass Filters

By removing the offset from either channel, no error component will be generated at DC when computing the active power. By removing the offset from both channels, no error component will be generated at DC when computing V_{RMS}, I_{RMS}, and apparent power. *Operational Mode Register* bits VHPF and IHPF activate the HPF in the voltage and current channel respectively. When a high-pass filter is active in only one channel, an all-pass filter (APF) is applied to the other channel. The APF has an amplitude response that is flat within the channel bandwidth and is used for matching phase in systems where only one HPF is engaged.

5.4 Performing Measurements

The CS5463 performs measurements of instantaneous voltage (V_n) and current (I_n), and calculates instantaneous power (P_n) at an output word rate (OWR) of

$$OWR = \frac{(MCLK/K)}{1024}$$

where K is the clock divider selected in the *Configuration Register*.

The RMS voltage (V_{RMS}), RMS current (I_{RMS}), and active power (P_{active}) are computed using N instantaneous samples of V_n, I_n, and P_n respectively, where N is the value in the *Cycle Count Register* and is referred to as a "*computation cycle*". The apparent power (S) is the product of V_{RMS} and I_{RMS}. A computation cycle is derived from the master clock (MCLK), with frequency:

$$\text{Computation Cycle} = \frac{OWR}{N}$$

Under default conditions and with K = 1, N = 4000, and MCLK = 4.096 MHz – the OWR = 4000 Hz and the Computation Cycle = 1 Hz.

All measurements are available as a percentage of full scale. The format for *signed* registers is a two's complement, normalized value between -1 and +1. The format

for *unsigned* registers is a normalized value between 0 and 1. A register value of

$$\frac{(2^{23}-1)}{2^{23}} = 0.99999988$$

represents the maximum possible value.

At each instantaneous measurement, the CRDY bit will be set in the *Status Register*, and the $\overline{INT}$ pin will become active if the CRDY bit is unmasked in the *Mask Register*. At the end of each computation cycle, the DRDY bit will be set in the *Status Register*, and the $\overline{INT}$ pin will become active if the DRDY bit is unmasked in the *Mask Register*. When these bits are asserted, they must be cleared before they can be asserted again.

If the *Cycle Count Register* (N) is set to 1, all output calculations are instantaneous, and DRDY, like CRDY, will indicate when instantaneous measurements are finished. Some calculations are inhibited when the cycle count is less than 2.

Epsilon (ε) is the ratio of the input line frequency (f_i) to the sample frequency (f_s) of the ADC.

$$\varepsilon = f_i / f_s$$

where f_s = MCLK / (K*1024). With MCLK = 4.096 MHz and clock divider K = 1, f_s = 4000 Hz. For the two most-common line frequencies, 50 Hz and 60 Hz

$$\varepsilon = 50\ Hz / 4000\ Hz = 0.0125$$

and

$$\varepsilon = 60\ Hz / 4000\ Hz = 0.015$$

respectively. Epsilon is used to set the frequency of the internal sine/cosine reference for the fundamental active and reactive measurements, and the gain of the 90° phase shift (IIR) filter for the average reactive power.

5.5 Energy Pulse Output

The CS5463 provides three output pins for energy registration. By default, $\overline{E1}$ registers active energy, $\overline{E3}$ registers reactive energy, and $\overline{E2}$ indicates the sign of both active and reactive energy. (See Figure 2. *Timing Diagram for E1, E2, and E3* on page13.) The $\overline{E1}$ pulse output is designed to register the Active Energy. The $\overline{E2}$ pin can be set to register Apparent Energy. Table 2 defines the pulse output mode, which is controlled by bit E2MODE in the *Operational Mode Register*.

E2MODE	$\overline{E2}$ Output Mode
0	Sign of Energy
1	Apparent Energy

Table 2. $\overline{E2}$ Pin Configuration

The $\overline{E3}$ pin can be set to register Reactive Energy (default), PFMON, Voltage Channel Sign, or Apparent Energy. Table 3 defines the pulse output format, which is controlled by bits E3MODE[1:0] in the *Operational Mode Register.*

E3MODE1	E3MODE0	$\overline{E3}$ OutPut Mode
0	0	Reactive Energy
0	1	PFMON
1	0	Voltage Channel Sign
1	1	Apparent Energy

Table 3. $\overline{E3}$ Pin Configuration

The pulse output frequency of $\overline{E1}$, $\overline{E2}$, and $\overline{E3}$ is directly proportional to the power calculated from the input signals. The value contained in the *PulseRateE Register* is the ratio of the frequency of energy-output pulses to the number of samples, at full scale, which defines the average frequency for the output pulses. The pulse width, t_{pw} in Figure 2, is programmable through the PulseWidth register, and is approximately equal to:

$$t_{pw}(sec) \cong PulseWidth \bullet \frac{1}{(MCLK/K)/1024}$$

If MCLK = 4.096 MHz, K = 1, and PulseWidth = 1, then $t_{pw} \cong 0.25$ ms.

5.5.1 Active Energy

The $\overline{E1}$ pin produces active-low pulses with an output frequency proportional to the active power. The $\overline{E2}$ pin is the energy direction indicator. Positive energy is represented by $\overline{E1}$ pin falling while the $\overline{E2}$ is high. Negative energy is represented by the $\overline{E1}$ pin falling while the $\overline{E2}$ is low. The $\overline{E1}$ and $\overline{E2}$ switching characteristics are specified in Figure 2. *Timing Diagram for E1, E2, and E3* on page13.

Figure 5 illustrates the pulse output format with positive active energy and negative reactive energy.

Figure 5. Active and Reactive energy pulse outputs

The pulse output frequency of $\overline{E1}$ is directly proportional to the active power calculated from the input signals. To calculate the output frequency of $\overline{E1}$, the following transfer function can be utilized:

$$FREQ_P = \frac{VIN \times VGAIN \times IIN \times IGAIN \times PF \times PulseRate}{VREFIN^2}$$

$FREQ_P$ = Average frequency of active energy $\overline{E1}$ pulses [Hz]
VIN = rms voltage across VIN+ and VIN- [V]
VGAIN = Voltage channel gain
IIN = rms voltage across IIN+ and IIN- [V]
IGAIN = Current channel gain
PF = Power Factor
PulseRate = PulseRateE x (MCLK/K)/2048 [Hz]
VREFIN = Voltage at VREFIN pin [V]

With MCLK = 4.096 MHz, PF = 1, and default settings, the pulses will have an average frequency equal to the frequency specified by *PulseRate* when the input signals applied to the voltage and current channels cause full-scale readings in the instantaneous voltage and current registers. The maximum pulse frequency from the $\overline{E1}$ pin is (MCLK/K)/2048.

5.5.2 Apparent Energy Mode

Pin $\overline{E2}$ outputs apparent energy pulses when the *Operational Mode Register* bit E2MODE = 1. Pin $\overline{E3}$ outputs apparent energy pulses when the *Operational Mode Register* bits E3MODE[1:0] = 3 (11b). Figure 6 illustrates the pulse output format with apparent energy on $\overline{E2}$ (E2MODE = 1 and E3MODE[1:0] = 0)

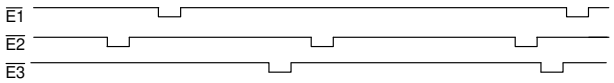


Figure 6. Apparent energy pulse outputs

The pulse output frequency of $\overline{E2}$ (and/or $\overline{E3}$) is directly proportional to the apparent power calculated from the input signals. Since apparent power is without reference to an impedance phase angle, the following transfer function can be utilized to calculate the output frequency on $\overline{E2}$ (and/or $\overline{E3}$).

$$FREQ_S = \frac{VIN \times VGAIN \times IIN \times IGAIN \times PulseRate}{VREFIN^2}$$

$FREQ_S$ = Average frequency of apparent energy $\overline{E2}$ and/or $\overline{E3}$ pulses [Hz]
VIN = rms voltage across VIN+ and VIN- [V]
VGAIN = Voltage channel gain
IIN = rms voltage across IIN+ and IIN- [V]
IGAIN = Current channel gain
PulseRate = PulseRateE x (MCLK/K)/2048 [Hz]
VREFIN = Voltage at VREFIN pin [V]

With MCLK = 4.096 MHz and default settings, the pulses will have an average frequency equal to the frequency specified by *PulseRate* when the input signals applied to the voltage and current channels cause full-scale readings in the instantaneous voltage and current registers. The maximum pulse frequency from the $\overline{E2}$ (and/or $\overline{E3}$) pin is (MCLK/K)/2048. The $\overline{E2}$ (and/or $\overline{E3}$) pin outputs apparent energy, but has no energy direction indicator.

5.5.3 Reactive Energy Mode

Reactive energy pulses are output on pin $\overline{E3}$ by setting bit E3MODE[1:0] = 0 (default) in the *Operational Mode Register*. Positive reactive energy is registered by $\overline{E3}$ falling when $\overline{E2}$ is high. Negative reactive energy is registered by $\overline{E3}$ falling when $\overline{E2}$ is low. Figure 5 on page 17 illustrates the pulse output format with negative reactive energy output on pin $\overline{E3}$ and the sign of the energy on $\overline{E2}$. The $\overline{E3}$ and $\overline{E2}$ pulse output switching characteristics are specified in Figure 2 on page 13.

The pulse output frequency of $\overline{E3}$ is directly proportional to the reactive power calculated from the input signals. To calculate the output frequency on $\overline{E3}$, the following transfer function can be utilized:

$$FREQ_Q = \frac{VIN \times VGAIN \times IIN \times IGAIN \times PQ \times PulseRate}{VREFIN^2}$$

$FREQ_Q$ = Average frequency of reactive energy $\overline{E3}$ pulses [Hz]
VIN = rms voltage across VIN+ and VIN- [V]
VGAIN = Voltage channel gain
IIN = rms voltage across IIN+ and IIN- [V]
IGAIN = Current channel gain
$PQ = \sqrt{1 - PF^2}$
PulseRate = PulseRateE x (MCLK/K)/2048 [Hz]
VREFIN = Voltage at VREFIN pin [V]

With MCLK = 4.096 MHz, PF = 0 and default settings, the pulses will have an average frequency equal to the frequency specified by *PulseRate* when the input signals applied to the voltage and current channels cause full-scale readings in the instantaneous voltage and current registers. The maximum pulse frequency from the $\overline{E1}$ pin is (MCLK/K)/2048.

5.5.4 Voltage Channel Sign Mode

Setting bits E3MODE[1:0] = 2 (10b) in the *Operational Mode Register* outputs the sign of the voltage channel on pin $\overline{E3}$. Figure 7 illustrates the output format with voltage channel sign on $\overline{E3}$

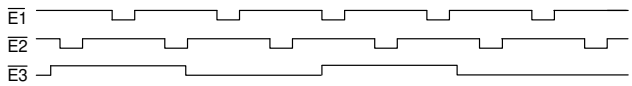


Figure 7. Voltage Channel Sign Pulse outputs

Output pin $\overline{E3}$ is high when the line voltage is positive and pin $\overline{E3}$ is low when the line voltage is negative.

5.5.5 PFMON Output Mode

Setting bit E3MODE[1:0] = 1 (01b) in the *Operational Mode Register* outputs the state of the PFMON comparator on pin $\overline{E3}$. Figure 8 illustrates the output format with PFMON on $\overline{E3}$

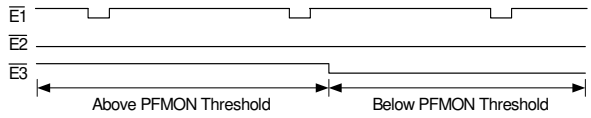


Figure 8. PFMON output to pin $\overline{E3}$

When PFMON is greater then the threshold, pin $\overline{E3}$ is high and when PFMON is less than the threshold pin $\overline{E3}$ is low.

5.5.6 Design Example

EXAMPLE #1:

The maximum rated levels for a power line meter are 250 V rms and 20 A rms. The required number of pulses-per-second on $\overline{E1}$ is 100 pulses per second (100 Hz), when the levels on the power line are 220 V rms and 15 A rms.

With a 10x gain on the voltage and current channel the maximum input signal is 250 mV_P. (See Section 5.1 *Analog Inputs* on page 16.) To prevent over-driving the channel inputs, the maximum rated rms input levels will register 0.6 in V_{RMS} and I_{RMS} by design. Therefore the voltage level at the channel inputs will be 150 mV rms when the maximum rated levels on the power lines are 250 V rms and 20 A rms.

Solving for *PulseRate* using the transfer function:

$$\text{PulseRate} = \frac{\text{FREQ}_P \times \text{VREFIN}^2}{\text{VIN} \times \text{VGAIN} \times \text{IIN} \times \text{IGAIN} \times \text{PF}}$$

Therefore with PF = 1 and:

$$\text{VIN} = 220\text{V} \times ((150\text{mV})/(250\text{V})) = 132\text{mV}$$

$$\text{IIN} = 15\text{A} \times ((150\text{mV})/(20\text{A})) = 112.5\text{mV}$$

the pulse rate is:

$$\text{PulseRate} = \frac{100 \times 2.5^2}{0.132 \times 10 \times 0.1125 \times 10} = 420.8754\text{Hz}$$

and the *PulseRateE Register* is set to:

$$\text{PulseRateE} = \frac{\text{PulseRate}}{(\text{MCLK}/\text{K})/2048} = 0.2104377$$

with MCLK = 4.096 MHz and K = 1.

5.6 Sag and Fault Detect Feature

Status bit VSAG and IFAULT in the *Status Register,* indicates a sag occurred in the power line voltage and current, respectively. For a sag condition to be identified, the absolute value of the instantaneous voltage or current must be less than the sag level for more than half of the sag duration (see Figure 9).

To activate voltage sag detection, a voltage sag level must be specified in the *Voltage Sag Level Register* ($VSAG_{Level}$), and a voltage sag duration must be specified in the *Voltage Sag Duration Register* ($VSAG_{Duration}$). To activate current fault detection, a current sag level must be specified in the *Current Fault Level Register* ($ISAG_{Level}$), and a current sag duration must be specified in the *Current Fault Duration Register* ($ISAG_{Duration}$). The voltage and current sag levels are specified as the average of the absolute instantaneous voltage and current, respectively. Voltage and current sag duration is specified in terms of ADC cycles.

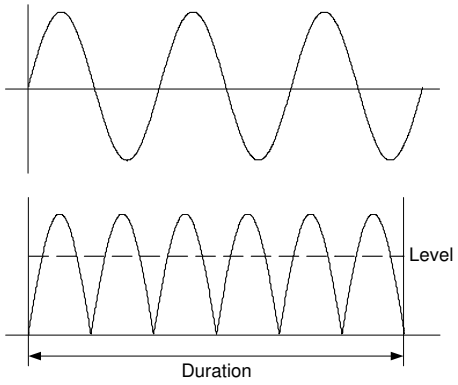


Figure 9. Sag and Fault Detect

5.7 No Load Threshold

The *No Load Threshold* register ($Load_{Min}$) is used to disable the active energy pulse output when the magnitude of the P_{Active} register is less than the value in the $Load_{Min}$ register.

5.8 On-chip Temperature Sensor

The on-chip temperature sensor is designed to assist in characterizing the measurement element over a desired temperature range. Once a temperature characterization is performed, the temperature sensor can then be utilized to assist in compensating for temperature drift.

Temperature measurements are performed during continuous conversions and stored in the *Temperature Register*. The *Temperature Register* (T) default is Celsius scale (°C). The *Temperature Gain Register* (T_{gain}) and *Temperature Offset Register* (T_{off}) are constant values allowing for temperature scale conversions.

The temperature update rate is a function of the number of ADC samples. With MCLK = 4.096 MHz and K = 1 the update rate is:

$$\frac{2240 \text{ samples}}{(MCLK/K)/1024} = 0.56 \text{ sec}$$

The *Cycle Count Register* (N) must be set to a value greater then one. Status bit TUP in the *Status Register,* indicates when the *Temperature Register* is updated.

The *Temperature Offset Register* sets the zero-degree measurement. To improve temperature measurement accuracy, the zero-degree offset may need to be adjusted after the CS5463 is initialized. Temperature-offset calibration is achieved by adjusting the *Temperature Offset Register* (T_{off}) by the differential temperature (ΔT) measured from a calibrated digital thermometer and the CS5463 temperature sensor. A one-degree adjustment to the *Temperature Register* (T) is achieved by adding 2.737649×10^{-4} to the *Temperature Offset Register* (T_{off}). Therefore,

$$T_{off} = T_{off} + (\Delta T \times 2.737649 \cdot 10^{-4})$$

if T_{off} = -0.0951126 and ΔT = -2.0 (°C), then

$$T_{off} = [-0.0951126 + (-2.0 \times 2.737649 \cdot 10^{-4})] = -0.09566$$

or 0xF3C168 (2's compliment notation) is stored in the *Temperature Offset Register* (T_{off}).

To convert the *Temperature Register* (T) from a Celsius scale (°C) to a Fahrenheit scale (°F) utilize the formula

$$^{o}F = \frac{9}{5}(^{o}C + 17.7778)$$

Applying the above relationship to the CS5461A temperature measurement algorithm

$$T\langle^{o}F\rangle = \left(\frac{9}{5} \times T_{gain}\right)\left[T\langle^{o}C\rangle + \left(T_{off} + (17.7778 \times 2.737649 \cdot 10^{-4})\right)\right]$$

If T_{off} = -0.09566 and T_{gain} = 23.507 for a Celsius scale, then the modified values are T_{off} = -0.09079 (0xF460E1) and T_{gain} = 42.3132 (0x54A05E) for a Fahrenheit scale.

5.9 Voltage Reference

The CS5463 is specified for operation with a +2.5 V reference between the VREFIN and AGND pins. To utilize the on-chip 2.5 V reference, connect the VREFOUT pin to the VREFIN pin of the device. The VREFIN can be used to connect external filtering and/or references.

5.10 System Initialization

Upon powering up, the digital circuitry is held in reset until the analog voltage reaches 4.0 V. At that time, an eight-XIN-clock-period delay is enabled to allow the oscillator to stabilize. The CS5463 will then initialize.

A hardware reset is initiated when the $\overline{\text{RESET}}$ pin is asserted with a minimum pulse width of 50 ns. The $\overline{\text{RESET}}$ signal is asynchronous, with a Schmitt-trigger input. Once the $\overline{\text{RESET}}$ pin is de-asserted, an eight-XIN-clock-period delay is enabled.

A software reset is initiated by writing the command 0x80. After a hardware or software reset, the internal registers (some of which drive output pins) will be reset to their default values. Status bit DRDY in the *Status Register,* indicates the CS5463 is in its *active* state and ready to receive commands.

5.11 Power-down States

The CS5463 has two power-down states, *Stand-by* and *Sleep*. In the stand-by state all circuitry except the voltage reference and crystal oscillator is turned off. To return the device to the active state, a power-up command is sent to the device.

In Sleep state, all circuitry except the instruction decoder is turned off. When the power-up command is sent to the device, a system initialization is performed (See Section 5.10 *System Initialization* on page 20).

5.12 Oscillator Characteristics

XIN and XOUT are the input and output of an inverting amplifier configured as an on-chip oscillator, as shown in Figure 10. The oscillator circuit is designed to work with a quartz crystal. To reduce circuit cost, two load capacitors C1 and C2 are integrated in the device, from XIN to DGND, and XOUT to DGND. PCB trace lengths should be minimized to reduce stray capacitance. To

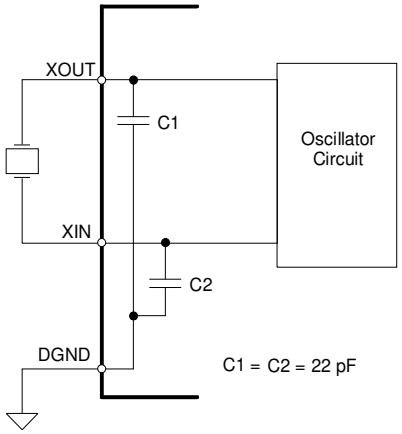


Figure 10. Oscillator Connection

drive the device from an external clock source, XOUT should be left unconnected while XIN is driven by the external circuitry. There is an amplifier between XIN and the digital section which provides CMOS level signals. This amplifier works with sinusoidal inputs so there are no problems with slow edge times.

The CS5463 can be driven by an external oscillator ranging from 2.5 to 20 MHz, but the K divider value must be set such that the internal MCLK will run somewhere between 2.5 MHz and 5 MHz. The K divider value is set with the K[3:0] bits in the *Configuration Register*. As an example, if XIN = MCLK = 15 MHz, and K is set to 5, DCLK will equal 3 MHz, which is a valid value for DCLK.

5.13 Event Handler

The $\overline{\text{INT}}$ pin is used to indicate that an internal error or event has taken place in the CS5463. Writing a logic 1 to any bit in the *Mask Register* allows the corresponding bit in the *Status Register* to activate the $\overline{\text{INT}}$ pin. The interrupt condition is cleared by writing a logic 1 to the bit that has been set in the *Status Register*.

The behavior of the $\overline{\text{INT}}$ pin is controlled by the IMODE and IINV bits of the *Configuration Register*.

IMODE	IINV	$\overline{\text{INT}}$ Pin	
0	0	Active-low Level	
0	1	Active-high Level	
1	0	Low Pulse	
1	1	High Pulse	

Table 4. Interrupt Configuration

If the interrupt output signal format is set for either falling or rising edge, the duration of the $\overline{\text{INT}}$ pulse will be at least one DCLK cycle (DCLK = MCLK/K).

5.13.1 Typical Interrupt Handler

The steps below show how interrupts can be handled.

INITIALIZATION:

1) All Status bits are cleared by writing 0xFFFFFF to the Status Register.
2) The condition bits which will be used to generate interrupts are then set to logic 1 in the Mask Register.
3) Enable interrupts.

INTERRUPT HANDLER ROUTINE:

4) Read the Status Register.
5) Disable all interrupts.
6) Branch to the proper interrupt service routine.
7) Clear the Status Register by writing back the read value in step 4.
8) Re-enable interrupt
9) Return from interrupt service routine.

This handshaking procedure ensures that any new interrupts activated between steps 4 and 7 are not lost (cleared) by step 7.

5.14 Serial Port Overview

The CS5463 incorporates a serial port transmit and receive buffer with a command decoder that interprets one-byte (8-bit) commands as they are received. There are four types of commands: instructions, synchronizing, register writes, and register reads (See Section 5.16 *Commands* on page 23).

Instructions are one byte in length and will interrupt any instruction currently executing. Instructions do not affect register reads currently being transmitted.

Synchronizing commands are one byte in length and only affect the serial interface. Synchronizing commands do not affect operations currently in progress.

Register writes must be followed by three bytes of data. Register reads can return up to four bytes of data.

Commands and data are transferred most-significant bit (MSB) first. Figure 1 on page 12, defines the serial port timing and required sequence necessary for writing to and reading from the serial port receive and transmit buffer, respectively. While reading data from the serial port, commands and data can be written simultaneously. Starting a new register read command while data is being read will terminate the current read in progress. This is acceptable if the remainder of the current read data is not needed. During data reads, the serial port requires input data. If a new command and data is not sent, SYNC0 or SYNC1 must be sent.

5.14.1 Serial Port Interface

The serial port interface is a “4-wire” synchronous serial communications interface. The interface is enabled to start excepting SCLKs when $\overline{\text{CS}}$ (Chip Select) is asserted (logic 0). SCLK (Serial bit-clock) is a Schmitt-trigger input that is used to strobe the data on SDI (Serial Data In) into the receive buffer and out of the transmit buffer onto SDO (Serial Data Out).

If the serial port interface becomes unsynchronized with respect to the SCLK input, any attempt to clock valid commands into the serial interface may result in unexpected operation. Therefor, the serial port interface must then be re-initialized by one of the following actions:

- Drive the $\overline{CS}$ pin high, then low.
- Hardware Reset (drive $\overline{RESET}$ pin low for at least 10 µs).
- Issue the *Serial Port Initialization Sequence*, which is 3 (or more) SYNC1 command bytes (0xFF) followed by one SYNC0 command byte (0xFE).

If a re-synchronization is necessary, it is best to re-initialize the part either by hardware or software reset (command 0x80), as the state of the part may be unknown.

5.15 Register Paging

Read/write commands access one of the 32 registers within a specified page. By default, Page = 0. To access registers in another page, the *Page Register* (address 0x1F) must be written with the desired page number.

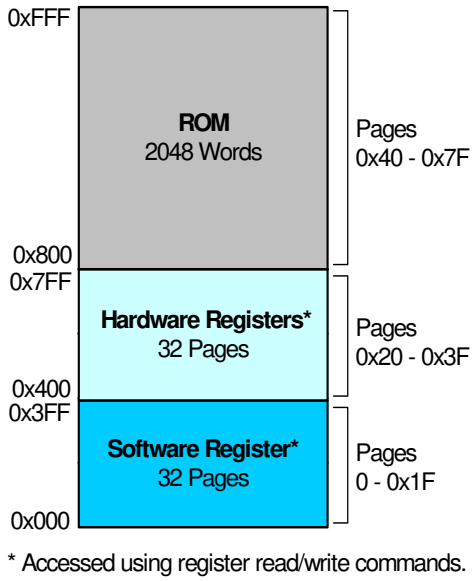


Figure 11. CS5463 Memory Map

Example:

Reading register 6 in page 3.

1. Write 3 to page register with command and data:

   0x7E 0x00 0x00 0x03

2. Read register 6 with command:

   0x0C 0xFF 0xFF 0xFF

5.16 Commands

All commands are 8 bits in length. Any command byte value that is not listed in this section is invalid. Commands that write to registers must be followed by 3 bytes of data. Commands that read data can be chained with other commands (e.g., while reading data, a new command can be sent which can execute during the original read). All commands except register reads, register writes, and SYNC0 & SYNC1 will abort any currently executing commands.

5.16.1 Start Conversions

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	0	C3	0	0	0

Initiates acquiring measurements and calculating results. The device has two modes of acquisition.

C3 — Modes of acquisition/measurement
0 = Perform a single computation cycle
1 = Perform continuous computation cycles

5.16.2 SYNC0 and SYNC1

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	1	1	1	1	SYNC

The serial port can be initialized by asserting $\overline{CS}$ or by sending three or more consecutive SYNC1 commands followed by a SYNC0 command. The SYNC0 or SYNC1 can also be sent while sending data out.

SYNC — 0 = Last byte of a serial port re-initialization sequence.
1 = Used during reads and serial port initialization.

5.16.3 Power-up/Halt

B7	B6	B5	B4	B3	B2	B1	B0
1	0	1	0	0	0	0	0

If the device is powered-down, Power-Up/Halt will initiate a power on reset. If the part is already powered-on, all computations will be halted.

5.16.4 Power-down and Software Reset

B7	B6	B5	B4	B3	B2	B1	B0
1	0	0	S1	S0	0	0	0

To conserve power the CS5463 has two power-down states. In stand-by state all circuitry, except the analog/digital clock generators, is turned off. In the sleep state all circuitry, except the command decoder, is turned off. Bringing the CS5463 out of sleep state requires more time than out of stand-by state, because of the extra time needed to re-start and re-stabilize the analog oscillator.

S[1:0] — Power-down state
00 = Software Reset
01 = Halt and enter stand-by power saving state. This state allows quick power-on
10 = Halt and enter sleep power saving state.
11 = Reserved

5.16.5 Register Read/Write

B7	B6	B5	B4	B3	B2	B1	B0
0	W/R	RA4	RA3	RA2	RA1	RA0	0

The Read/Write informs the command decoder that a register access is required. During a *read* operation, the addressed register is loaded into an output buffer and clocked out by SCLK. During a *write* operation, the data is clocked into an input buffer and transferred to the addressed register upon completion of the 24th SCLK.

W/$\overline{R}$ Write/Read control
0 = Read
1 = Write

RA[4:0] Register address bits (bits 5 through 1) of the read/write command.

Register Page 0

Address	RA[4:0]	Name	Description
0	00000	Config	Configuration
1	00001	I_{DCoff}	Current DC Offset
2	00010	I_{gn}	Current Gain
3	00011	V_{DCoff}	Voltage DC Offset
4	00100	V_{gn}	Voltage Gain
5	00101	Cycle Count	Number of A/D conversions used in one computation cycle (N)).
6	00110	PulseRateE	Sets the $\overline{E1}$, $\overline{E2}$ and $\overline{E3}$ energy-to-frequency output pulse rate.
7	00111	I	Instantaneous Current
8	01000	V	Instantaneous Voltage
9	01001	P	Instantaneous Power
10	01010	P_{Active}	Active (Real) Power
11	01011	I_{RMS}	RMS Current
12	01100	V_{RMS}	RMS Voltage
13	01101	ε (Epsilon)	Ratio of line frequency to output word rate (OWR)
14	01110	P_{off}	Power Offset
15	01111	Status	Status
16	10000	I_{ACoff}	Current AC (RMS) Offset
17	10001	V_{ACoff}	Voltage AC (RMS) Offset
18	10010	Mode	Operation Mode
19	10011	T	Temperature
20	10100	Q_{AVG}	Average Reactive Power
21	10101	Q	Instantaneous Reactive Power
22	10110	I_{Peak}	Peak Current
23	10111	V_{Peak}	Peak Voltage
24	11000	Q_{Trig}	Reactive Power calculated from Power Triangle
25	11001	PF	Power Factor
26	11010	Mask	Interrupt Mask
27	11011	S	Apparent Power
28	11100	Ctrl	Control
29	11101	P_H	Harmonic Active Power
30	11110	P_F	Fundamental Active Power
31	11111	Q_F	Fundamental Reactive Power / Page

Note: For proper operation, *do not* attempt to write to unspecified registers.

Register Page 1

Address	RA[4:0]	Name	Description
0	00000	PulseWidth	Energy Pulse Output Width
1	00001	$Load_{Min}$	No Load Threshold
2	00010	T_{Gain}	Temperature Sensor Gain
3	00011	T_{off}	Temperature Sensor Offset

Register Page 3

Address	RA[4:0]	Name	Description
6	00110	$VSAG_{Duration}$	Voltage sag sample interval
7	00111	$VSAG_{Level}$	Voltage sag level
10	01010	$ISAG_{Duration}$	Current fault sample interval
11	01011	$ISAG_{Level}$	Current fault level

Note: For proper operation, *do not* attempt to write to unspecified registers.

5.16.6 Calibration

B7	B6	B5	B4	B3	B2	B1	B0
1	1	0	CAL4	CAL3	CAL2	CAL1	CAL0

The CS5463 can perform system calibrations. Proper input signals must be applied to the current and voltage channel before performing a designated calibration.

CAL[4:0]* Designates calibration to be performed
- 01001 = Current channel DC offset
- 01010 = Current channel DC gain
- 01101 = Current channel AC offset
- 01110 = Current channel AC gain
- 10001 = Voltage channel DC offset
- 10010 = Voltage channel DC gain
- 10101 = Voltage channel AC offset
- 10110 = Voltage channel AC gain
- 11001 = Current and Voltage channel DC offset
- 11010 = Current and Voltage channel DC gain
- 11101 = Current and Voltage channel AC offset
- 11110 = Current and Voltage channel AC gain

*For proper operation, values for CAL[4:0] not specified should not be used.