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CS5464

Three-channel, Single-phase Power/Energy IC

Features

- Energy Linearity: ±0.1% of Reading over 1000:1 Dynamic Range
- On-chip Functions:
  - Voltage and Current Measurement
  - Active, Reactive, and Apparent Power/Energy
  - RMS Voltage and Current Calculations
  - Current Fault and Voltage Sag Detection
  - Calibration
  - Phase Compensation
  - Temperature Sensor
  - Energy Pulse Outputs
- Meets Accuracy Spec for IEC, ANSI, & JIS
- Low Power Consumption
- Tamper Detection and Correction
- Ground-referenced Inputs with Single Supply
- On-chip 2.5 V Reference (40 ppm / °C typ.)
- Power Supply Monitor Function
- Three-wire Serial Interface to Microcontroller or E^2PROM
- Power Supply Configurations
  GND: 0 V, VA+: +5 V, VD+: +3.3 V to +5 V

Description

The CS5464 is a watt-hour meter on a chip. It measures line voltage and current and calculates active, reactive, apparent power, energy, power factor, and RMS voltage and current.

There are two separate inputs to measure line, ground, and/or neutral current enabling the meter to detect tampering and to continue operating. An internal RMS voltage reference can be used if voltage measurement is disabled by tampering.

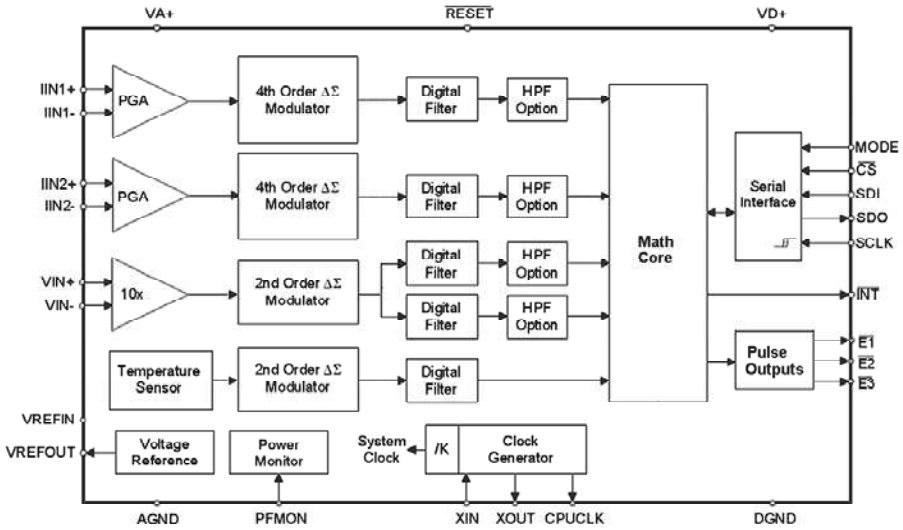
Four ΔΣ analog-to-digital converters are used to measure voltage, two currents, and temperature.

The CS5464 is designed to interface to a variety of voltage and current sensors.

Additional features include system-level calibration, voltage sag and current fault detection, peak detection, phase compensation, and energy pulse outputs.

ORDERING INFORMATION

See Page 44.



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1. OVERVIEW

The CS5464 is a CMOS power measurement integrated circuit utilizing four ΔΣ analog-to-digital converters to measure line voltage, temperature, and current from up to two sources. It calculates active, reactive, and apparent power as well as RMS and peak voltage and current. It handles other system-related functions, such as pulse output conversion, voltage sag, current fault, voltage zero crossing, line frequency, and tamper detection.

The CS5464 is optimized to interface to current transformers or shunt resistors for current measurement, and to a resistive divider or voltage transformer for voltage measurement. Two full-scale ranges are provided on the current inputs to accommodate both types of current sensors. The second current channel can be used for tamper detection or as a second current input. The CS5464's three differential inputs have a common-mode input range from analog ground (AGND) to the positive analog supply (VA+).

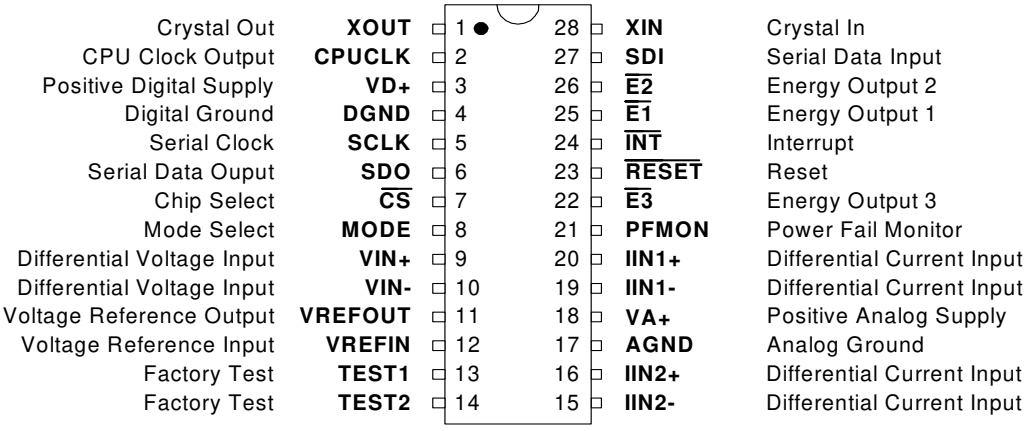
An additional analog input (PFMON) is provided to allow the application to determine when a power failure is in progress. By monitoring the unregulated power supply, the application can take any required action when a power loss occurs.

An on-chip voltage reference (nominally 2.5 volts) is generated and provided at analog output, VREFOUT. This reference can be supplied to the chip by connecting it to the reference voltage input, VREFIN. Alternatively, an external voltage reference can be supplied to the reference input.

Three digital outputs ($\overline{E1}$, $\overline{E2}$, $\overline{E3}$) provide a variety of output signals and, depending on the mode selected, provide energy pulses, power failure indication, or other choices.

The CS5464 includes a three-wire serial host interface to an external microcontroller or serial E^2PROM. Signals include serial data input (SDI), serial data output (SDO), serial clock (SCLK), and optionally, a chip select ($\overline{CS}$), which allows the CS5464 to share the SDO signal with other devices. A MODE input is used to control whether an E^2PROM will be used instead of a host microcontroller.

2. PIN DESCRIPTION



Clock Generator		
Crystal Out **Crystal In**	1,28	**XOUT, XIN** — Connect to an external quartz crystal. Alternatively, an external clock can be supplied to the XIN pin to provide the system clock for the device.
CPU Clock Output	2	**CPUCLK** - Logic-level output from crystal oscillator. Can be used to clock an external CPU.
Control Pins and Serial Data I/O		
Serial Clock	5	**SCLK** — Clocks serial data from the SDI pin and to the SDO pin when $\overline{CS}$ is low. SCLK is a Schmitt-trigger input when MODE is low and a driven output when MODE is high.
Serial Data Output	6	**SDO** — Serial data output. Data is clocked out by SCLK.
Chip Select	7	**$\overline{CS}$** — An input that enables the serial interface when MODE is low and a driven output when MODE is high.
Mode Select	8	**MODE** — High selects external E^2PROM, Low selects external microcontroller. MODE includes a weak internal pull-down and therefore selects microcontroller mode if not connected.
Energy Outputs	22, 25, 26	**$\overline{E3}$, $\overline{E1}$, $\overline{E2}$** — Primarily active-low energy pulse outputs. These can be programmed to output other conditions.
Reset	23	**$\overline{RESET}$** — An active-low Schmitt-trigger input used to reset the chip.
Interrupt	24	**$\overline{INT}$** — Active-low output, indicates that an enabled condition has occurred.
Serial Data Input	27	**SDI** — Serial data input. Data is clocked in by SCLK.
Analog Inputs/Outputs		
Differential Voltage Inputs	9,10	**VIN+, VIN-** — Differential analog inputs for the voltage channel.
Differential Current Inputs	20,19, 16,15	**IIN1+, IIN1-, IIN2+, IIN2-** — Differential analog inputs for the current channels.
Power Fail Monitor	21	**PFMON** — Used to monitor the unregulated power supply via a resistive divider. If the PFMON voltage drops below its low limit, the low-supply detect (LSD) bit is set in the *Status* register.
Voltage Reference Output	11	**VREFOUT** — The on-chip voltage reference output. Nominally 2.5 V, referenced to AGND.
Voltage Reference Input	12	**VREFIN** — The voltage reference input. Can be connected to VREFOUT or external 2.5 V reference.
Power Connections		
Positive Digital Supply	3	**VD+** — The positive digital supply.
Digital Ground	4	**DGND** — Digital ground.
Positive Analog Supply	18	**VA+** — The positive analog supply.
Analog Ground	17	**AGND** — Analog ground.
Other Pins		
Test1, Test2	13,14	**NC** — Factory use only. Connect to AGND.

3. CHARACTERISTICS & SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Positive Digital Power Supply	VD+	3.135	5.0	5.25	V
Positive Analog Power Supply	VA+	4.75	5.0	5.25	V
Voltage Reference	VREFIN	-	2.5	-	V
Specified Temperature Range	T_A	-40	-	+85	°C

ANALOG CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all Recommended Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and TA = 25 °C.
- VA+ = VD+ = 5 V ±5%; AGND = DGND = 0 V; VREFIN = +2.5 V. All voltages with respect to 0 V.
- DCLK = 4.096 MHz.

Parameter		Symbol	Min	Typ	Max	Unit
Accuracy						
Active Power (Note 1)	All Gain Ranges Input Range 0.1% - 100%	P_{Active}	-	±0.1	-	%
Reactive Power (Note 1 and 2)	All Gain Ranges Input Range 0.1% - 100%	Q_{Avg}	-	±0.2	-	%
Power Factor (Note 1 and 2)	All Gain Ranges Input Range 1.0% - 100% Input Range 0.1% - 1.0%	PF	- -	±0.2 ±0.27	- -	% %
Current RMS (Note 1)	All Gain Ranges Input Range 1.0% - 100% Input Range 0.1% - 1.0%	I_{RMS}	- -	±0.1 ±0.17	- -	% % %
Voltage RMS (Note 1)	All Gain Ranges Input Range 5% - 100%	V_{RMS}	-	±0.1	-	%
Analog Inputs (All Inputs)						
Common Mode Rejection	(DC, 50, 60 Hz)	CMRR	80	-	-	dB
Common Mode + Signal			-0.25	-	VA+	V
Analog Inputs (Current Inputs)						
Differential Input Range [(IIN+) – (IIN-)]	(Gain = 10) (Gain = 50)	IIN	- -	500 100	- -	mV_{P-P} mV_{P-P}
Total Harmonic Distortion	(Gain = 50)	THD	80	94	-	dB
Crosstalk from Voltage Input at Full Scale	(50, 60 Hz)		-	-115	-	dB
Input Capacitance		IC	-	27	-	pF
Effective Input Impedance		EII	30	-	-	kΩ
Noise (Referred to Input)	(Gain = 10) (Gain = 50)	N_I	- -	- -	22.5 4.5	μV_{rms} μV_{rms}
Offset Drift (Without the High-pass Filter)		OD	-	4.0	-	µV/°C
Gain Error	(Note 3)	GE	-	±0.4		%

Notes: 1. Applies when the HPF option is enabled.

2. Applies when the line frequency is equal to the product of the output word rate (OWR) and the value of *Epsilon*.

ANALOG CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
Analog Inputs (Voltage Inputs)					
Differential Input Range [(VIN+) – (VIN-)]	VIN	-	500	-	mV_{P-P}
Total Harmonic Distortion	THD	65	75	-	dB
Crosstalk from Current Inputs at Full Scale (50, 60 Hz)		-	-70	-	dB
Input Capacitance All Gain Ranges	IC	-	2.0	-	pF
Effective Input Impedance	EII	2	-	-	MΩ
Noise (Referred to Input)	N_V	-	-	140	μV_{rms}
Offset Drift (Without the High-pass Filter)	OD	-	16.0	-	µV/°C
Gain Error (Note 3)	GE	-	±3.0		%
Temperature					
Temperature Accuracy	T	-	±5	-	°C
Power Supplies					
Power Supply Currents (Active State) I_{A+}	PSCA	-	1.5	-	mA
I_{D+} (VA+ = VD+ = 5 V)	PSCD	-	3.5	-	mA
I_{D+} (VA+ = 5 V, VD+ = 3.3 V)	PSCD	-	2.3	-	mA
Power Consumption Active State (VA+ = VD+ = 5 V) (Note 4)	PC	-	25	33	mW
Active State (VA+ = 5 V, VD+ = 3.3 V)	PC	-	15	20	mW
Stand-by State	PC	-	7	-	mW
Sleep State	PC	-	10	-	uW
Power Supply Rejection Ratio (50, 60 Hz) (Note 5)					
Voltage	PSRR	48	55	-	dB
Current (Gain = 50x)	PSRR	68	75	-	dB
Current (Gain = 10x)	PSRR	60	65	-	dB
PFMON Low-voltage Trigger Threshold (Note 6)	PMLO	2.3	2.45	-	V
PFMON High-voltage Power-on Trip Point (Note 7)	PMHI	-	2.55	2.7	V

Notes:
3. Applies before system calibration.
4. All outputs unloaded. All inputs CMOS level.
5. Measurement method for PSRR: VREFIN tied to VREFOUT, VA+ = VD+ = 5 V, a 150 mV (zero-to-peak) (60 Hz) sinewave is imposed onto the +5 V DC supply voltage at VA+ and VD+ pins. The "+" and "-" input pins of both input channels are shorted to AGND. The CS5464 is then commanded to continuous conversion acquisition mode, and digital output data is collected for the channel under test. The (zero-to-peak) value of the digital sinusoidal output signal is determined, and this value is converted into the (zero-to-peak) value of the sinusoidal voltage (measured in mV) that would need to be applied at the channel's inputs, in order to cause the same digital sinusoidal output. This voltage is then defined as Veq. PSRR is (in dB):

$$PSRR = 20 \cdot \log\left[\frac{150}{V_{eq}}\right]$$

6. When voltage level on PFMON is sagging, and LSD bit = 0, the voltage at which LSD is set to 1.
7. If the LSD bit has been set to 1 (because PFMON voltage fell below PMLO), this is the voltage level on PFMON at which the LSD bit can be permanently reset back to 0.

VOLTAGE REFERENCE

Parameter		Symbol	Min	Typ	Max	Unit
Reference Output						
Output Voltage		VREFOUT	+2.4	+2.5	+2.6	V
Temperature Coefficient	(Note 8)	TC_{VREF}	-	40	-	ppm/°C
Load Regulation	(Note 9)	ΔV_R	-	6	10	mV
Reference Input						
Input Voltage Range		VREFIN	+2.4	+2.5	+2.6	V
Input Capacitance			-	4	-	pF
Input CVF Current			-	100	-	nA

Notes: 8. The voltage at VREFOUT is measured across the temperature range. From these measurements the following formula is used to calculate the VREFOUT temperature coefficient:.

$$TC_{VREF} = \left(\frac{(VREFOUT_{MAX} - VREFOUT_{MIN})}{VREFOUT_{AVG}}\right)\left(\frac{1}{T_{A}MAX - T_{A}MIN}\right)\left(1.0 \times 10^{6}\right)$$

9. Specified at maximum recommended output of 1 µA, source or sink.

DIGITAL CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all Recommended Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and TA = 25 °C.
- VA+ = VD+ = 5V ±5%; AGND = DGND = 0 V. All voltages with respect to 0 V.
- DCLK = 4.096 MHz.

Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Characteristics						
Master Clock Frequency	Internal Gate Oscillator (Note 11)	DCLK	2.5	4.096	20	MHz
Master Clock Duty Cycle			40	-	60	%
CPUCLK Duty Cycle	(Note 12 and 13)		40	-	60	%
Filter Characteristics						
Phase Compensation Range	(60 Hz, OWR = 4000 Hz)		-5.4	-	+5.4	°
Input Sampling Rate	DCLK = MCLK/K		-	DCLK/8	-	Hz
Digital Filter Output Word Rate	(Both channels)	OWR	-	DCLK/1024	-	Hz
High-pass Filter Corner Frequency	-3 dB		-	0.5	-	Hz
Full-scale DC Calibration Range (Referred to Input)	(Note 14)	FSCR	25	-	100	%FS
Channel-to-channel Time-shift Error	(Note 15)			1.0		µs
Input/Output Characteristics						
High-level Input Voltage						
	All Pins Except XIN and SCLK and $\overline{\text{RESET}}$	V_{IH}	0.6 VD+	-	-	V
	XIN		(VD+) – 0.5	-	-	V
	SCLK and $\overline{\text{RESET}}$		0.8 VD+	-	-	V
Low-level Input Voltage (VD = 5 V)						
	All Pins Except XIN and SCLK and $\overline{\text{RESET}}$	V_{IL}	-	-	0.8	V
	XIN		-	-	1.5	V
	SCLK and $\overline{\text{RESET}}$		-	-	0.2 VD+	V
Low-level Input Voltage (VD = 3.3 V)						
	All Pins Except XIN and SCLK and $\overline{\text{RESET}}$	V_{IL}	-	-	0.48	V
	XIN		-	-	0.3	V
	SCLK and $\overline{\text{RESET}}$		-	-	0.2 VD+	V
High-level Output Voltage	I_{out} = +5 mA	V_{OH}	(VD+) - 1.0	-	-	V
Low-level Output Voltage						
	I_{out} = -5 mA (VD = +5V)	V_{OL}	-	-	0.4	V
	I_{out} = -2.5 mA (VD = +3.3V)		-	-	0.4	V
Input Leakage Current	(Note 16)	I_{in}	-	±1	±10	µA
3-state Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	5	-	pF

Notes: 10. All measurements performed under static conditions.

11. If a crystal is used, XIN frequency must remain between 2.5 MHz - 5.0 MHz. If an external oscillator is used, XIN frequency range is 2.5 MHz - 20 MHz, but K must be set so that MCLK is between 2.5 MHz - 5.0 MHz.
12. If external MCLK is used, the duty cycle must be between 45% and 55% to maintain this specification.
13. The frequency of CPUCLK is equal to MCLK.
14. The minimum FSCR is limited by the maximum allowed gain register value. The maximum FSCR is limited by the full-scale signal applied to the input.
15. Configuration register (*Config*) bits PC[6:0] are set to “0000000”.
16. The MODE pin is pulled low by an internal resistor.

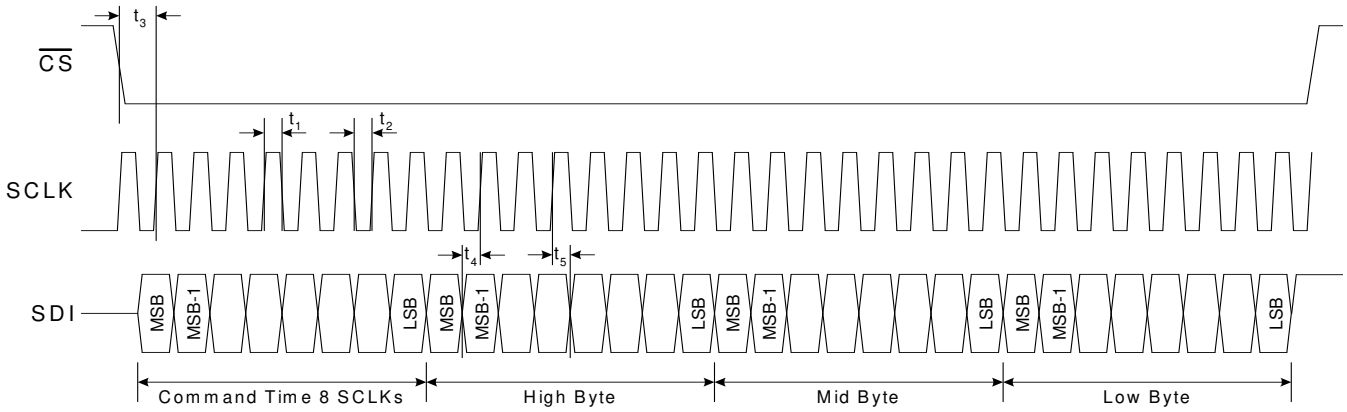
SWITCHING CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all Recommended Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and TA = 25 °C.
- VA+ = 5 V ±5% VD+ = 3.3 V ±5% or 5 V ±5%; AGND = DGND = 0 V. All voltages with respect to 0 V.
- Logic Levels: Logic 0 = 0 V, Logic 1 = VD+.

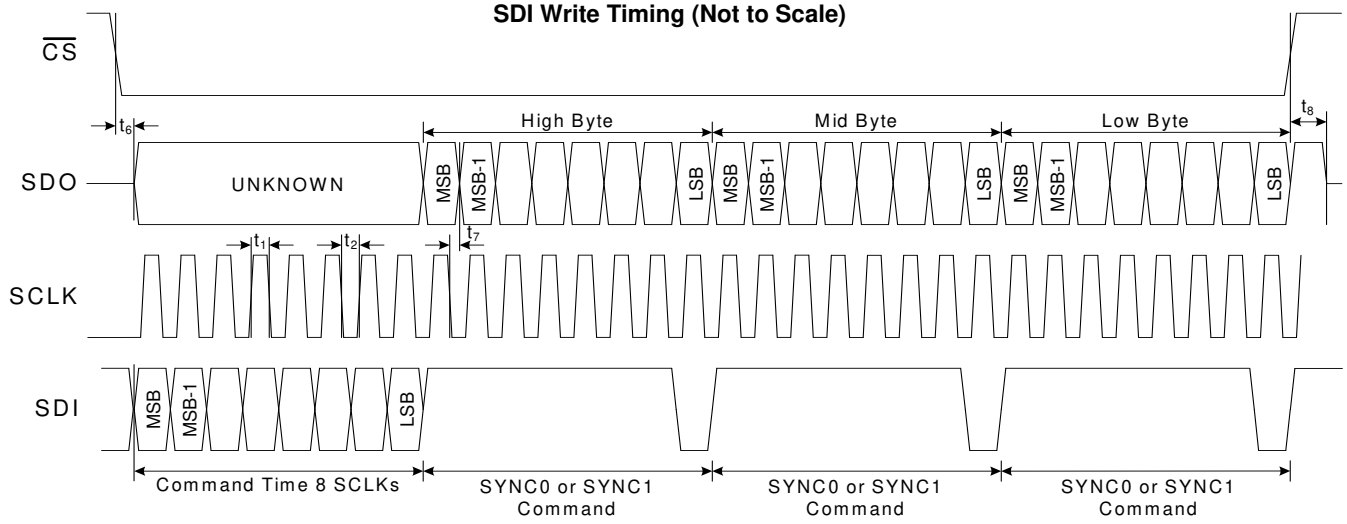
Parameter		Symbol	Min	Typ	Max	Unit
Rise Times (Note 17)	Any Digital Output	t_{rise}	- -	- 50	1.0 -	µs ns
Fall Times (Note 17)	Any Digital Output	t_{fall}	- -	- 50	1.0 -	µs ns
Start-up						
Oscillator Start-up Time	XTAL = 4.096 MHz (Note 11)	t_{ost}	-	60	-	ms
Serial Port Timing						
Serial Clock Frequency		SCLK	-	-	2	MHz
Serial Clock	Pulse Width High Pulse Width Low	t_1 t_2	200 200	- -	- -	ns ns
SDI Timing						
$\overline{CS}$ Falling to SCLK Rising		t_3	50	-	-	ns
Data Set-up Time Prior to SCLK Rising		t_4	50	-	-	ns
Data Hold Time After SCLK Rising		t_5	100	-	-	ns
SDO Timing						
$\overline{CS}$ Falling to SDO Driving		t_6	-	20	50	ns
SCLK Falling to New Data Bit (hold time)		t_7	-	20	50	ns
$\overline{CS}$ Rising to SDO Hi-Z		t_8	-	20	50	ns
E^2PROM mode Timing						
Serial Clock	Pulse Width Low Pulse Width High	t_9 t_{10}		8 8		DCLK DCLK
MODE setup time to $\overline{RESET}$ Rising		t_{11}	50			ns
$\overline{RESET}$ rising to $\overline{CS}$ falling		t_{12}	48			DCLK
$\overline{CS}$ falling to SCLK rising		t_{13}	100	8		DCLK
SCLK falling to $\overline{CS}$ rising		t_{14}		16		DCLK
$\overline{CS}$ rising to driving MODE low		t_{15}	50			ns
SDO setup time to SCLK rising		t_{16}	100			ns

Notes: 17. Specified using 10% and 90% points on waveform of interest. Output loaded with 50 pF.

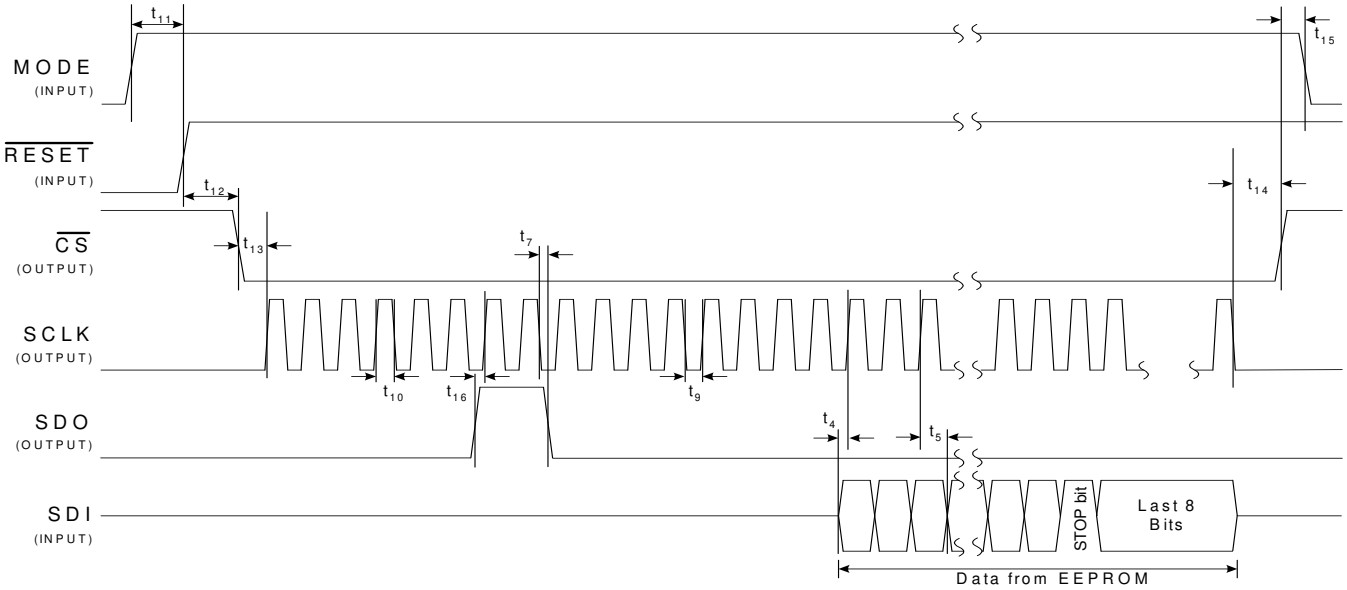
18. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.



SDI Write Timing (Not to Scale)



SDO Read Timing (Not to Scale)



E^{2}PROM mode Sequence Timing (Not to Scale)

Figure 1. CS5464 Read and Write Timing Diagrams

SWITCHING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{E1}$, $\overline{E2}$, and $\overline{E3}$ Timing (Note 19 and 20)					
Period	t_{period}	500	-	-	µs
Pulse Width	t_{pw}	244	-	-	µs
Rising Edge to Falling Edge	t_3	6	-	-	µs
$\overline{E2}$ Setup to $\overline{E1}$ and/or $\overline{E3}$ Falling Edge	t_4	1.5	-	-	µs
$\overline{E1}$ Falling Edge to $\overline{E3}$ Falling Edge	t_5	248	-	-	µs

Notes: 19. Pulse output timing is specified at DCLK = 4.096 MHz, E2MODE = 0, and E3MODE[1:0] = 0. Refer to 6.7 *Energy Pulse Outputs* on page 19 for more information on pulse output pins.

20. Timing is proportional to the frequency of DCLK.

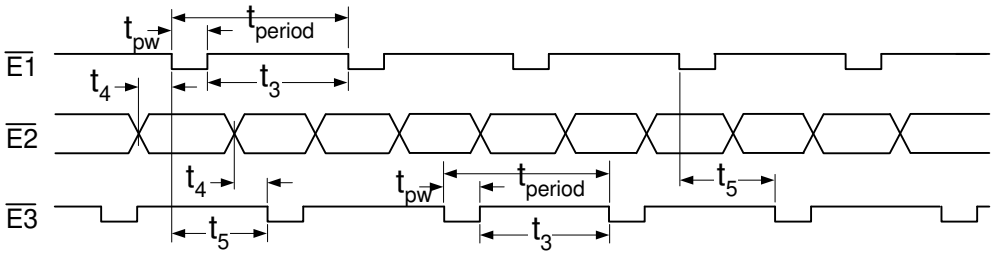


Figure 2. Timing Diagram for $\overline{E1}$, $\overline{E2}$, and $\overline{E3}$

ABSOLUTE MAXIMUM RATINGS

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	(Notes 21 and 22)					
	Positive Digital	VD+	-0.3	-	+6.0	V
	Positive Analog	VA+	-0.3	-	+6.0	V
Input Current, Any Pin Except Supplies	(Notes 23, 24, 25)	I_{IN}	-	-	±10	mA
Output Current, Any Pin Except VREFOUT		I_{OUT}	-	-	100	mA
Power Dissipation	(Note 26)	P_D	-	-	500	mW
Analog Input Voltage	All Analog Pins	V_{INA}	- 0.3	-	(VA+) + 0.3	V
Digital Input Voltage	All Digital Pins	V_{IND}	-0.3	-	(VD+) + 0.3	V
Ambient Operating Temperature		T_A	-40	-	85	°C
Storage Temperature		T_{stg}	-65	-	150	°C

Notes: 21. VA+ and AGND must satisfy [(VA+) - (AGND)] ≤ + 6.0 V.

22. VD+ and AGND must satisfy [(VD+) - (AGND)] ≤ + 6.0 V.

23. Applies to all pins including continuous over-voltage conditions at the analog input pins.

24. Transient current of up to 100 mA will not cause SCR latch-up.

25. Maximum DC input current for a power supply pin is ±50 mA.

26. Total power dissipation, including all input currents and output currents.

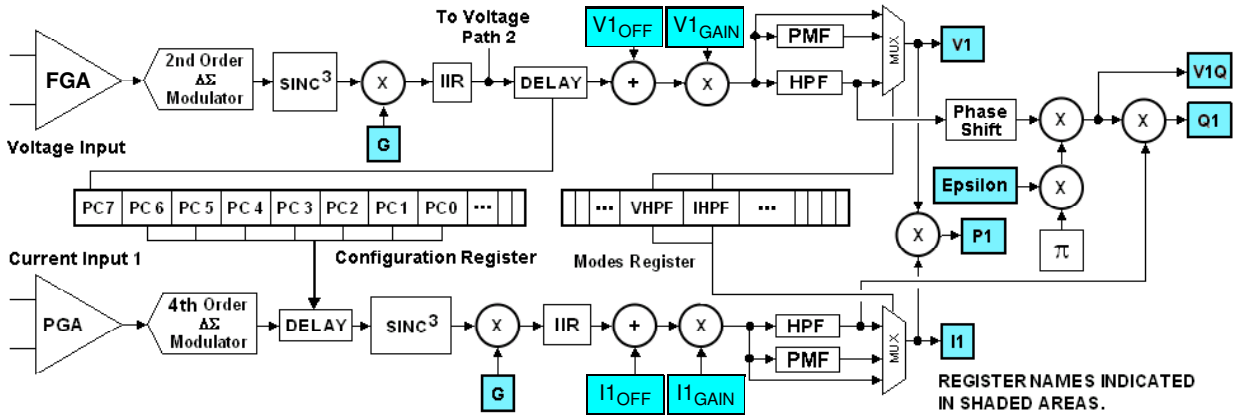


Figure 3. Signal Flow for V1, I1, P1, Q1 Measurements

4. SIGNAL PATH DESCRIPTION

The data flow for voltage and current measurement and the other calculations are shown in Figures 3, 4, and 5.

The data flow consists of two current paths and two voltage paths. Both voltage paths are derived from the same differential input pins. Each current path has its own differential input pins.

4.1 Analog-to-Digital Converters

The voltage and temperature channels use second-order delta-sigma modulators and the two current channels use fourth-order delta-sigma modulators to convert the analog inputs to single-bit digital data streams. The converters sample at a rate of DCLK/8. This high sampling provides a wide dynamic range and simplifies anti-alias filter design.

4.2 Decimation Filters

The single-bit modulator output data is widened to 24 bits and down-sampled to DCLK/1024 with low-pass decimation filters. These decimation filters are third-order Sinc. Their outputs are passed through third-order IIR "anti-sinc" filters, used to compensate for the amplitude roll-off of the decimation filters.

4.3 Phase Compensation

Phase compensation changes the phase of current relative to voltage by changing the sampling time in the decimation filters. The amount of phase shift is set by bits PC[7:0] in the Configuration register (*Config*) for channel 1 and bits PC[7:0] in the Control register (*Ctrl*) for channel 2.

Phase compensation, PC[7:0] is a signed two's complement binary value in the range of -1.0 to almost +1.0 output word rate (OWR) samples. For a sample rate of 4000 Hz, the delay range is ±250 µS, a phase shift of ±4.5° at 50 Hz and ±5.4° at 60 Hz. The step size would be 0.0352° at 50 Hz and 0.0422° at 60 Hz at this sample rate.

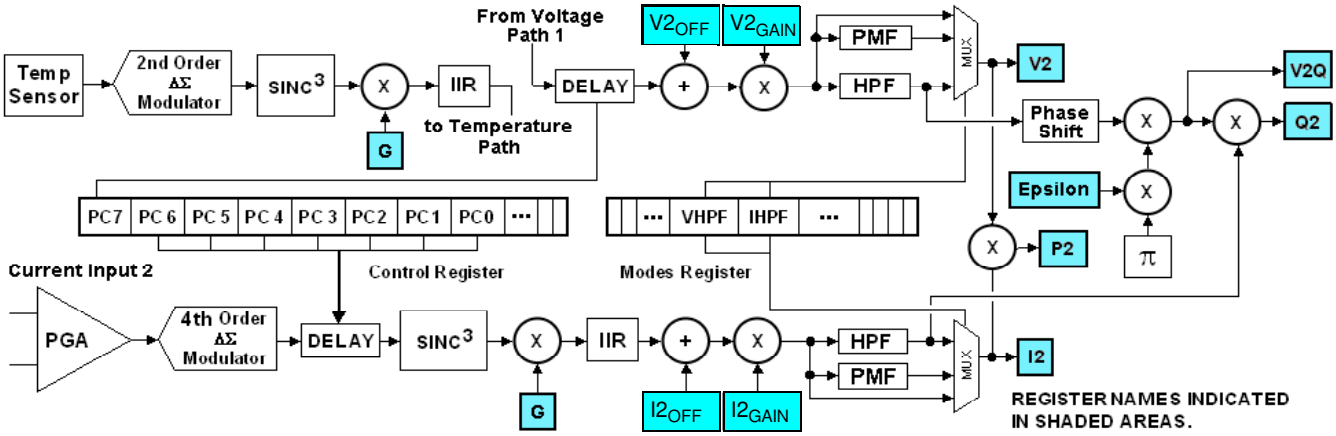


Figure 4. Signal Flow for V2, I2, P2, Q2 Measurements

4.4 DC Offset and Gain Correction

The system and chip inherently have gain and offset errors which can be removed using the gain and offset registers. (See Section 9. *System Calibration* on page 39). Each measurement channel has its own registers. For every channel, the output of the IIR filter is added to the offset register and multiplied by the gain register.

4.5 High-pass Filters

Optional high-pass filters (HPF in Figures 3 and 4) remove any DC from the selected signal paths. Subsequently, DC will also be removed from power, and all low-rate results. (see Figures 5).

Each energy channel has a current and voltage path. If an HPF is enabled in only one path, a phase-matching filter (PMF) is applied to the other path which matches the amplitude and phase delay of the HPF in the band of interest, but passes DC. For more information, see 6.5 *High-pass Filters* on page 19. The HPF filter multiplexers drive the *I1*, *V1*, *I2*, and *V2* result registers.

4.6 Low-Rate Calculations

Low-rate results are derived from sample-rate results integrated over *N* samples, where *N* is the value stored in the Cycle Count register. The low-rate interval is the sample interval multiplied by *N*.

4.7 RMS Results

The root mean square (*RMS* in Figure 5) calculations are performed on *N* instantaneous voltage and current samples, using the formula:

$$I_{RMS} = \sqrt{\frac{\sum_{n=0}^{N-1} I_n^2}{N}}$$

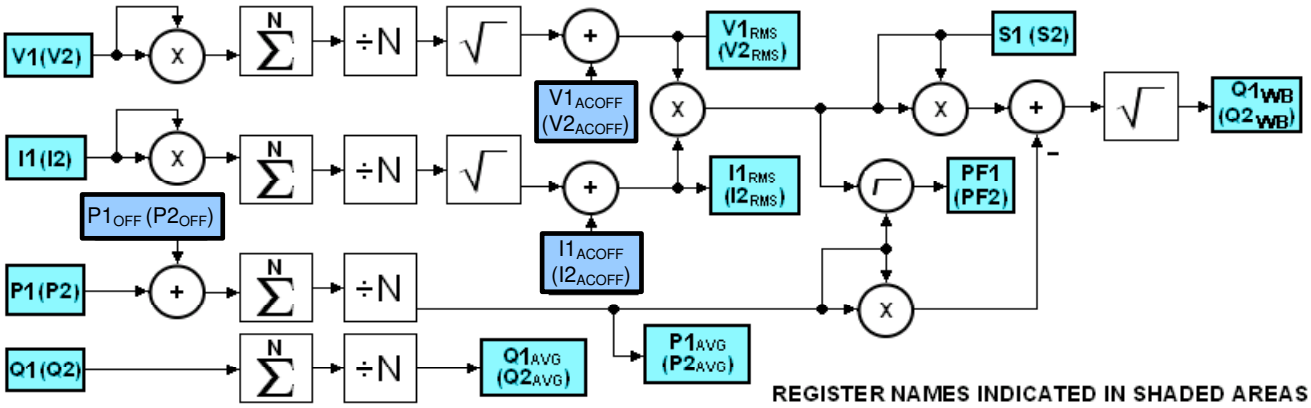


Figure 5. Low-rate Calculations

4.8 Power and Energy Results

The instantaneous voltage and current samples are multiplied to obtain the instantaneous power (*P1*, *P2*) (see Figure 3 and 4). The product is then averaged over *N* conversions to compute active power ($P1_{AVG}$, $P2_{AVG}$).

Apparent power (*S1*, *S2*) is the product of RMS voltage and current as shown:

$$S = V_{RMS} \times I_{RMS}$$

Power factor (*PF1*, *PF2*) is active power divided by apparent power as shown below. The sign of the power factor is determined by the active power.

$$PF = \frac{P_{ACTIVE}}{S}$$

Wideband reactive power ($Q1_{WB}$, $Q2_{WB}$) is calculated by doing a vector subtraction of active power from apparent power.

$$Q_{WB} = \sqrt{S^2 - P_{ACTIVE}^2}$$

Quadrature power (*Q1*, *Q2*) are sample rate results obtained by multiplying instantaneous current (*I1*, *I2*) by instantaneous quadrature voltage (*V1Q*, *V2Q*) which are created by phase shifting instantaneous voltage (*V1*, *V2*) 90 degrees using first-order integrators. (see Figure 3 and 4). The gain of these integrators is inversely related to line frequency, so their gain is corrected by the *Epsilon* register, which is based on line frequency.

Reactive power ($Q1_{AVG}$, $Q2_{AVG}$) is generated by integrating the instantaneous quadrature power over *N* samples.

4.9 Peak Voltage and Current

Peak current ($I1_{PEAK}$, $I2_{PEAK}$) and peak voltage ($V1_{PEAK}$, $V2_{PEAK}$) are the largest current and voltage samples detected in the previous low-rate interval.

4.10 Power Offset

The power offset registers, $P1_{OFF}$ ($P2_{OFF}$) can be used to offset erroneous power sources resident in the system not originating from the power line. Residual power offsets are usually caused by crosstalk into current paths from voltage paths or from ripple on the meter or chip's power supply, or from inductance from a nearby transformer.

These offsets can be either positive or negative, indicating crosstalk coupling either in phase or out of phase with the applied voltage input. The power offset registers can compensate for either condition.

To use this feature, measure the average power at no load using either Single or Continuous Conversion commands. Take the measured result (from the $P1_{AVG}$ ($P2_{AVG}$) register), invert (negate) the value and write it to the associated power offset register, $P1_{OFF}$ ($P2_{OFF}$).

5. PIN DESCRIPTIONS

5.1 Analog Pins

The CS5464 has three differential inputs: VIN±, IIN1±, and IIN2± are the voltage, current1, and current2 inputs, respectively. A single-ended power fail monitor input, voltage reference input, and voltage reference output are also available.

5.1.1 Voltage Inputs

The output of the line voltage resistive divider or transformer is connected to the VIN+ and VIN- input pins of the CS5464. The voltage channel is equipped with a 10x, fixed-gain amplifier. The full-scale signal level that can be applied to the voltage channel is ±250mV. If the input signal is a sine wave, the maximum RMS voltage is 250mVp / $\sqrt{2}$ ≈ 176.78mVRMS which is approximately 70.7% of maximum peak voltage.

5.1.2 Current1 and Current2 Inputs

The output of the current-sensing resistor or transformer is connected to the IIN1+ (IIN2+) and IIN1- (IIN2-) input pins of the CS5464. To accommodate different current-sensing elements, the current channel incorporates a programmable gain amplifier (PGA) with two selectable input gains. The full-scale signal level for the current channels is ±50mV or ±250mV. If the input signal is a sine wave, the maximum RMS voltage is 35.35mVRMS or 176.78mVRMS which is approximately 70.7% of maximum peak voltage.

5.1.3 Power Fail Monitor Input

An analog input (PFMON) is provided to determine when a power loss is imminent. By connecting a resistive divider from the unregulated meter power supply to the PFMON input, an interrupt can be generated, or the Low Supply Detected (LSD) *Status* register bit can be monitored to indicate low-supply conditions. The PFMON input has a comparator that trips around the level of the voltage reference input (VREFIN).

5.1.4 Voltage Reference Input

The CS5464 requires a stable voltage reference of 2.5 V applied to the VREFIN pin. This reference can be supplied from an external voltage reference or from the VREFOUT output. A bypass capacitor of at least 0.1 µF is recommended at the VREFIN pin.

5.1.5 Voltage Reference Output

The CS5464 generates a 2.5 V reference (VREFOUT). It is suitable for driving the VREFIN pin, but has very little fan-out and is not recommended for driving external circuits.

5.1.6 Crystal Oscillator

An external quartz crystal can be connected to the XIN and XOUT pins as shown in Figure 6. To reduce system cost, each pin is supplied with an on-chip, phase-shifting capacitor to ground.

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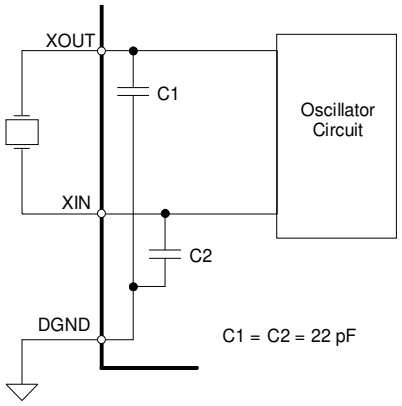

Figure 6. Oscillator Connections

Alternatively, an external clock source can be connected to the XIN pin.

5.2 Digital Pins

5.2.1 Reset Input

The active-low $\overline{\text{RESET}}$ pin, when asserted, will halt all CS5464 operations and reset internal hardware registers and states. When de-asserted, an initialization sequence begins, setting default register values.

5.2.2 CPU Clock Output

A logic-level clock output (CPUCLK) is provided at the crystal frequency to drive an external CPU or microcontroller clock. Two phase choices are available.

5.2.3 Interrupt Output

The $\overline{\text{INT}}$ pin indicates an enabled Internal Status register (*Status*) bit is set. *Status* register bits indicate conditions such as data ready, modulator oscillations, low supply, voltage sag, current faults, numerical overflows, and result updates.

5.2.4 Energy Pulse Outputs

The CS5464 provides three pins ($\overline{\text{E1}}$, $\overline{\text{E2}}$, $\overline{\text{E3}}$) for pulse energy outputs. These pins can also be used to output other conditions, such as voltage sign, power fail monitor, or energy channel in use.

5.2.5 Serial Interface

The CS5464 provides 5 pins, SCLK, SDI, SDO, $\overline{CS}$, and MODE for communication between a host microcontroller or serial E^2PROM and the CS5464.

MODE is an input that, when high, indicates to the CS5464 that a serial E^2PROM is being used instead of a host microcontroller. It has a weak pull-down allowing it to be left unconnected if microcontroller mode is used.

SCLK is used to shift and qualify serial data. Serial data changes as a result of the falling edge of SCLK and is valid during the rising edge. It is a Schmitt-trigger input for host microcontrollers, and a driven output for serial E^2PROMs.

SDI is the serial data input to the CS5464.

SDO is the serial data output from the CS5464. It's output drivers are disabled whenever $\overline{CS}$ is de-asserted, allowing other devices to drive the SDO line.

$\overline{CS}$ is the chip select input for the serial bus. A high logic level de-asserts it, tri-stating the SDO pin and clearing the serial interface. A low logic level enables the serial port. This pin may be tied low for systems not requiring multiple SDO drivers. $\overline{CS}$ is a driven output when interfacing to serial E^2PROMs.

6. SETTING UP THE CS5464

6.1 Clock Divider

The internal clock to the CS5464 needs to operate around 4 MHz. However, by using the internal clock divider, a higher crystal frequency can be used. This is important when driving an external microcontroller requiring a faster clock and using the CPUCLK output.

K is the divide ratio from the crystal input to the internal clock and is selected with Configuration register (*Config*) bits K[3:0]. It has a range of 1 to 16. A value of zero results in a setting of 16.

6.2 CPU Clock Inversion

By default, CPUCLK is inverted from XIN. Setting Configuration register bit iCPU removes this inversion. This can be useful when one phase adds more noise to the system than the other.

6.3 Interrupt Pin Behavior

The behavior of the $\overline{\text{INT}}$ pin is controlled by the IMODE and IINV bits in the Configuration register as shown.

IMODE	IINV	$\overline{\text{INT}}$ Pin	
0	0	Active-low Level	
0	1	Active-high Level	
1	0	Low Pulse	
1	1	High Pulse	

Table 1. Interrupt Configuration

If IMODE = 1, the duration of the $\overline{\text{INT}}$ pulse will be two DCLK cycles, where DCLK = MCLK/K.

6.4 Current Input Gain Ranges

Control register bits I1gain (I2gain) select the input range of the current inputs.

I1gain, I2gain	Maximum Input	Gain
0	±250 mV	10x
1	±50 mV	50x

Table 2. Current Input Gain Ranges

6.5 High-pass Filters

Mode Control (*Modes*) register bits VHPF and IHPF activate the HPF in the voltage and current paths, respectively. Each energy channel has separate VHPF and IHPF bits. When a high-pass filter is enabled in only one path within a channel, a phase matching filter (PMF) is applied to the other path within that channel. The PMF filter matches the amplitude and phase response of the HPF in the band of interest, but passes DC.

VHPF	IHPF	Filter Configuration
0	0	No filter on Voltage or Current
0	1	HPF on Current, PMF on Voltage
1	0	HPF on Voltage, PMF on Current
1	1	HPF on Current and Voltage

Table 3. High-pass Filter Configuration

6.6 Cycle Count

Low-rate calculations, such as average power and RMS voltage and current integrate over several (*N*) output word rate (OWR) samples. The duration of this averaging window is set by the Cycle Count (*N*) register. By default, Cycle Count is set to 4000 (1 second at output word rate [OWR] of 4000 Hz). The minimum value for Cycle Count is 10.

6.7 Energy Pulse Outputs

By default, $\overline{\text{E1}}$ outputs active energy, $\overline{\text{E3}}$, reactive energy, and $\overline{\text{E2}}$, the sign of both active and reactive energy. (See Figure 2. *Timing Diagram for E1, E2, and E3* on page 13.)

Three pairs of bits in the Mode Control (*Modes*) register control the operation of these outputs. These bits are named E1MODE[1:0], E2MODE[1:0], and E3MODE[1:0]. Some combinations of these bits override others, so read the following paragraphs carefully.

The $\overline{\text{E2}}$ pin can output energy sign, apparent energy, or energy channel in use (1 or 2). Table 4 lists the functions of $\overline{\text{E2}}$ as controlled by E2MODE[1:0] in the *Modes* register.

Note: E2MODE[1:0]=3 is a special mode.

E2MODE1	E2MODE0	$\overline{\text{E2}}$ output
0	0	Energy Sign
0	1	Apparent Energy
1	0	Channel in Use
1	1	Enable E1MODE

Table 4. $\overline{\text{E2}}$ Pin Configuration

The $\overline{\text{E3}}$ pin can output reactive energy, power fail monitor status, voltage sign, or apparent energy. Table 5

lists the functions of $\overline{E3}$ as controlled by E3MODE[1:0] in the *Modes* register when E1MODE is not enabled.

E3MODE1	E3MODE0	$\overline{E3}$ output
0	0	Reactive Energy
0	1	Power Fail Monitor
1	0	Voltage Sign
1	1	Apparent Energy

Table 5. $\overline{E3}$ Pin Configuration

When both E2MODE bits are high, the E1MODE bits are enabled, allowing active, apparent, reactive, or wideband reactive energy for ***both*** energy channels to be output on $\overline{E1}$ and $\overline{E2}$. Table 6 lists the functions of $\overline{E1}$ and $\overline{E2}$ with E1MODE enabled.

E1MODE1	E1MODE0	$\overline{E1}$ / $\overline{E2}$ outputs
0	0	Active Energy
0	1	Apparent Energy
1	0	Reactive Energy
1	1	Wideband Reactive

Table 6. $\overline{E1}$ / $\overline{E2}$ Modes

When E1MODE bits are enabled, the $\overline{E3}$ pin outputs either the power fail monitor status, or the sign of the $\overline{E1}$ and $\overline{E2}$ outputs. Table 7 list the functions of the $\overline{E3}$ pin using E3MODE[1:0] in the *Modes* register when E1MODE is enabled.

E3MODE1	E3MODE0	$\overline{E3}$ output
0	0	Power Fail Monitor
0	1	Energy Sign
1	0	not used
1	1	not used

Table 7. $\overline{E3}$ Pin with E1MODE enabled

6.8 No Load Threshold

The No Load Threshold register ($Load_{MIN}$) is used to zero out the contents of E_{PULSE} and Q_{PULSE} registers if their magnitude is less than the $Load_{MIN}$ register value.

6.9 Energy Pulse Width

Note: Energy Pulse Width (*PulseWidth*) only applies to $\overline{E1}$, $\overline{E2}$, or $\overline{E3}$ pins that are configured to output pulses. When any are configured to output steady-state signals, such as voltage sign, energy channel in use, power fail monitor, or energy sign, pulse widths and output rates do not apply.

The pulse width time (t_{pw}) in Figure 2, is set by the value in the *PulseWidth* register which is an integer multiple of the sample or output word rate (OWR). At OWR of 4000 Hz (a period of 250 uS) t_{pw} = *PulseWidth* x 250uS. By default, *PulseWidth* is set to 1.

6.10 Energy Pulse Rate

The full-scale pulse frequency of enabled $\overline{E1}$, $\overline{E2}$, $\overline{E3}$ pins is the *PulseRate* x output word rate (OWR)/2. The actual pulse frequency is the full-scale pulse frequency multiplied by the pulse register's (E_{PULSE}, S_{PULSE}, Q_{PULSE}) value.

Example:
If the output word rate (OWR) is 4000 Hz, and the *PulseRate* is set to 0.05, the full-rate pulse frequency is 0.05 x 4000 / 2 = 100 Hz. If the E_{PULSE} register, driving $\overline{E1}$, is 0.4567, the pulse output rate on $\overline{E1}$ will be 100 Hz x 0.4567 = 45.67 Hz.

6.11 Voltage Sag/Current Fault Detection

Voltage sag detection is used to determine when averaged voltage falls below a predetermined level for a specified interval of time. Current fault detection determines when averaged current falls below a predetermined level for a specified interval of time.

The specified interval of time (duration) is set by the value in the $V1Sag_{DUR}$ ($V2Sag_{DUR}$) and $I1Fault_{DUR}$ ($I2Fault_{DUR}$) registers. Setting any of these to zero (default) disables the detect feature for the given channel. The value is in output word rate (OWR) samples. The predetermined level is set by the values in the $V1Sag_{LEVEL}$ ($V2Sag_{LEVEL}$) and $I1Fault_{LEVEL}$ ($I2Fault_{LEVEL}$) registers.

Since the values of *V1* and *V2* come from the same input, only one voltage sag detector is necessary.

For each enabled input channel, the measured value is rectified and compared to the associated level register. Over the duration window, the number of samples above and below the level are counted. If the number of samples below the level exceeds the number of samples above, a *Status* register bit $V1_{SAG}$ ($V2_{SAG}$), $I1_{FAULT}$ ($I2_{FAULT}$) is set, indicating a sag or fault condition. (see Figure 7)..

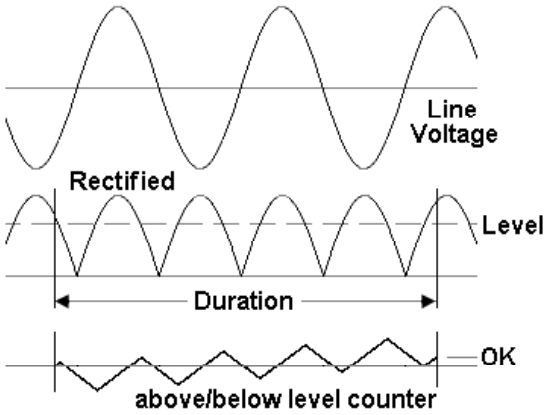

Figure 7. Sag and Fault Detect

6.12 Epsilon

The *Epsilon* register is used to set the gain of the 90° phase shift used in the quadrature power calculation.

The value in the *Epsilon* register is the ratio of the line frequency to the output word rate (OWR). It is, by default, 50/4000 (0.0125), for 50 Hz line and 4000 Hz sample (OWR) frequencies.

For 60 Hz line frequency, it is 60/4000 (0.015). Other output word rates (OWR) can be used.

Epsilon can also be calculated automatically by the CS5464 by setting the AFC bit in the Mode Control (*Modes*) register. The Frequency Update bit (FUP) in the *Status* register is set every time the *Epsilon* register has been automatically updated.

6.13 Temperature Measurement

The on-chip temperature sensor is designed to measure temperature and optionally compensate for temperature drift of the voltage reference. It uses the V_{BE} of a transistor to determine temperature.

Temperature measurements are stored in the Temperature register (*T*) which, by default, is configured to a range of ±128 degrees on the Celsius (°C) scale.

The application program can change both the scale and range of Temperature (*T*) by changing the Temperature Gain (T_{GAIN}) and Temperature Offset (T_{OFF}) registers.

Two values must be known — the transistor's ΔV_{BE} per degree, and the transistor's V_{BE} at 0 degrees. At the time of this publication, these values are:

ΔV_{BE} (per degree) = 0.2769523 mV/°C or °K

$V_{BE}0$ = 79.2604368 mV at 0°C

To determine the values to write to T_{GAIN} and T_{OFF}, use the following formulae:

$$T_{GAIN} = AD_{FS} / \Delta V_{BE} / T_{FS} \times 2^{17}$$
$$T_{OFF} = -V_{BE}0 / AD_{FS} \times 2^{23}$$

In the above equations, AD_{FS} is the full-scale input range of the temperature A/D converter or 833.333 mV and T_{FS} is the desired full-scale range of the Temperature register. The binary exponents are the bit positions of the binary point of these registers.

To use the Celsius scale (°C) and cover the chip's operating temperature range of -40°C to +85°C, the Temperature register range needs to be ±128 degrees. T_{FS} should be 128 degrees.

$$T_{GAIN} = 833.333 / 0.2769523 / 128 \times 131072$$
$$= 3081155 \text{ (0x2F03C3)}$$
$$T_{OFF} = -79.2604368 / 833.333 \times 8388608$$
$$= -797862 \text{ (0xF3D35A)}$$

These are the actual default values for these registers.

T_{GAIN} and T_{OFF} can also be used to calibrate the gain and/or offset of the temperature sensor or A/D converter. (See Section 9. *System Calibration* on page 39).

To use the Kelvin (°K) scale, simply add 273 times $\Delta V_{BE} / AD_{FS} \times 2^{23}$ to T_{OFF} since 0°C = 273°K,. You will also need more range. Since -40°C to +85°C is 233°K to 358°K, a T_{FS} of 512 degrees should be used in the T_{GAIN} calculation.

To use the Fahrenheit (°F) scale, multiply ΔV_{BE} by 5/9 and add 32 times the new $\Delta V_{BE} / AD_{FS} \times 2^{23}$ to T_{OFF} since 0°C = 32°F. You will also want to use a T_{FS} of 256 degrees to cover the -40°C to +85°C range.

The Temperature register (*T*) updates every 2240 output word rate (OWR) samples. The *Status* register bit TUP indicates when *T* is updated.

7. USING THE CS5464

7.1 Initialization

The CS5464 uses a power-on-reset circuit (POR) to provide an internal reset until the analog voltage reaches 4.0 V. The $\overline{\text{RESET}}$ input pin can also be used by the application circuit to reset the part.

After $\overline{\text{RESET}}$ is removed and the oscillator is stable, an initialization program is executed to set the default register values.

A Software Reset command is also provided to allow the application to run the initialization program without removing power or asserting $\overline{\text{RESET}}$.

The application should avoid sending commands during initialization. The DRDY bit in the *Status* register indicates when the initialization program has completed.

7.2 Power-down States

The CS5464 has two power-down states, stand-by and sleep. In the stand-by state, all circuitry except the voltage reference and crystal oscillator is powered off. In sleep state, all circuitry except the instruction decoder is powered off.

To return the device to the active state, send a Wake-Up/Halt command to the device. When returning from stand-by mode, registers will retain their contents prior to entering the stand-by state. When returning from sleep mode, a complete initialization occurs.

7.3 Tamper Detection and Correction

The CS5464 provides compensation for at least two forms of meter tampering. A second current input is provided in the event that the primary input is impaired by tampering. (See Figure 14 on page 42). An internal RMS voltage reference is also available in the event that the voltage input has been compromised by tampering.

Power and energy are calculated for BOTH current inputs (both energy channels). The CS5464 can automatically choose the channel with the greater magnitude. The register E_{MIN}, (also called $Irms_{MIN}$) sets a minimum level for automatic channel selection, and $Ichan_{LEVEL}$ sets a minimum difference that will allow a channel change. *Modes* register bit Ichan selects the energy channel, and is normally driven by the CS5464 program. This affects the pulse registers and pulse energy outputs. (See figure 8).

The application program can also choose the more appropriate energy channel. *Modes* register bit Ihold disables automatic selection and Ichan can be driven by the application. Shown below is the channel selector.

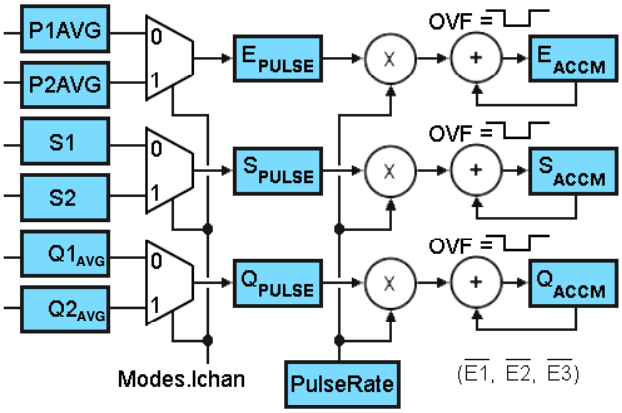

Figure 8. Energy Channel Selection

If the application detects that the voltage input has been impaired it may choose to use the fixed internal RMS voltage reference by setting the VFIX bit in the *Modes* register. The value of this reference (VF_{RMS}) is by default 0.707107 (full-scale RMS) but can be changed by the application program. (See figure 9)

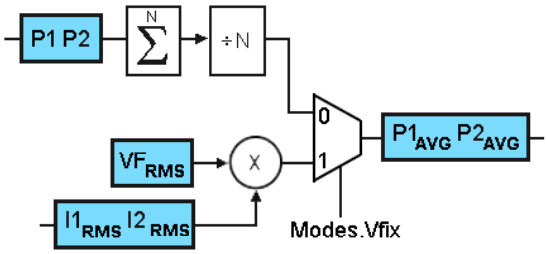

Figure 9. Fixed RMS Voltage Selection

7.4 Command Interface

Commands and data are transferred most-significant bit (MSB) first. Figure 1 on page 12, defines the serial port timing. Commands are clocked in on SDI using SCLK. They are a single byte (8 bits) long and fall into one of four basic types:

1. Register Read
2. Register Write
3. Synchronizing
4. Instructions

Register reads will cause up to four bytes of register data to be clocked out, MSB first on the SDO pin by SCLK. During this time, other commands can be clocked in on the SDI pin. Other commands will not interrupt read data, except another register read, which will cause the new read data to appear on SDO.

Synchronizing can be sent while read data is being clocked out if no other commands need to be sent.

Synchronizing commands are also used to synchronize the serial port to a byte boundary. The $\overline{CS}$ and $\overline{RESET}$ pins will also synchronize the serial port.

Register writes require three bytes of write data to follow, clocked in on the SDI pin, MSB first by SCLK.

Instructions are commands that will interrupt any instruction currently executing and begin the new instruction. These include conversions, calibrations, power control, and soft reset.

(See Section 7.6 *Commands* on page 24).

7.5 Register Paging

Read and Write commands access one of 32 registers within a specified page. The Resgister Page Select register's (*Page*) default value is 0. To access registers in another page, write the desired page number to the *Page* register. The *Page* register is always at address 31 and is accessible from within any page.

7.6 Commands

All commands are 1 byte (8 bits) long. Many command values are unused and should NOT be written by the application program. All commands except register reads, register writes, or synchronizing commands will abort any conversion, calibration, or any initialization sequence currently executing. This includes reset. No commands other than reads or synchronizing should be executed until the reset sequence completes.

7.6.1 Conversion

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	0	CC	0	0	0

Executes a conversion (measurement) program.

CC — Continuous/Single Conversion
0 = Perform a Single Conversion (0xE0)
1 = Perform Continuous Conversion (0xE8)

7.6.2 Synchronization (SYNC0 and SYNC1)

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	1	1	1	1	SYNC

The serial interface is bidirectional. While reading data on the SDO output, the SDI input must be receiving commands. If no command is needed during a read, SYNC0 or SYNC1 commands can be sent while read data is received on SDO.

The serial port is normally initialized by de-asserting $\overline{CS}$. An alternative method of initialization is to send 3 or more SYNC1 commands followed by a SYNC0. This is useful in systems where $\overline{CS}$ is not used and tied low.

7.6.3 Power Control (Stand-by, Sleep, Wake-up/Halt and Software Reset)

B7	B6	B5	B4	B3	B2	B1	B0
1	0	S1	S0	0	0	0	0

The CS5464 has two power-down states, stand-by and sleep. In stand-by, all circuitry except the voltage reference and clocks are turned off. In sleep, all circuitry except the command decoder is turned off. A Wake-up/Halt command restores full-power operation after stand-by and issues a hardware reset after sleep. The Software Reset command is a program that emulates a pin reset and is not a power control function.

S[1:0] — 00 = Software Reset
01 = Sleep
10 = Wake-up/Halt
11 = Stand-by

7.6.4 Calibration

B7	B6	B5	B4	B3	B2	B1	B0
1	0	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0

The CS5464 can perform gain and offset calibrations using either DC or AC signals. Proper input levels must be applied to the current inputs and voltage input before performing calibrations.

CAL[5:4]* 00 = DC Offset
01 = DC Gain
10 = AC Offset
11 = AC Gain

CAL[3:0] 0001 = Current for Channel 1
0010 = Voltage for Channel 1
0100 = Current for Channel 2
1000 = Voltage for Channel 2

Note: Anywhere from 1 to all 4 channels can be calibrated simultaneously. Voltage channels 1 and 2 use the same voltage input. Commands with CAL[5:0] = 0 are not calibrations.