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CS5480

Three Channel Energy Measurement IC

Features

- Superior Analog Performance with Ultra-low Noise Level & High SNR
- Energy Measurement Accuracy of 0.1% over 4000:1 Dynamic Range
- Current RMS Measurement Accuracy of 0.1% over 1000:1 Dynamic Range
- 3 Independent 24-bit, 4th-order, Delta-Sigma Modulators for Voltage and Current Measurements
- 3 Configurable Digital Outputs for Energy Pulses, Zero-crossing, or Energy Direction
- Supports Shunt Resistor, CT, & Rogowski Coil Current Sensors
- On-chip Measurements & Calculations:
  - Active, Reactive, and Apparent Power
  - RMS Voltage and Current
  - Power Factor and Line Frequency
  - Instantaneous Voltage, Current, and Power
- Overcurrent, Voltage Sag, and Voltage Swell Detection
- Ultra-fast On-chip Digital Calibration
- Internal Register Protection via Checksum and Write Protection
- UART/SPI™ Serial Interface
- On-chip Temperature Sensor
- On-chip Voltage Reference (25ppm / °C Typ.)
- Single 3.3V Power Supply
- Ultra-fine Phase Compensation
- Low Power Consumption: <13mW
- Power Supply Configurations
  GNDA = GNDD = 0V, VDDA = +3.3V
- 4mm x 4mm, 24-pin QFN Package

ORDERING INFORMATION

See Page 69.

Description

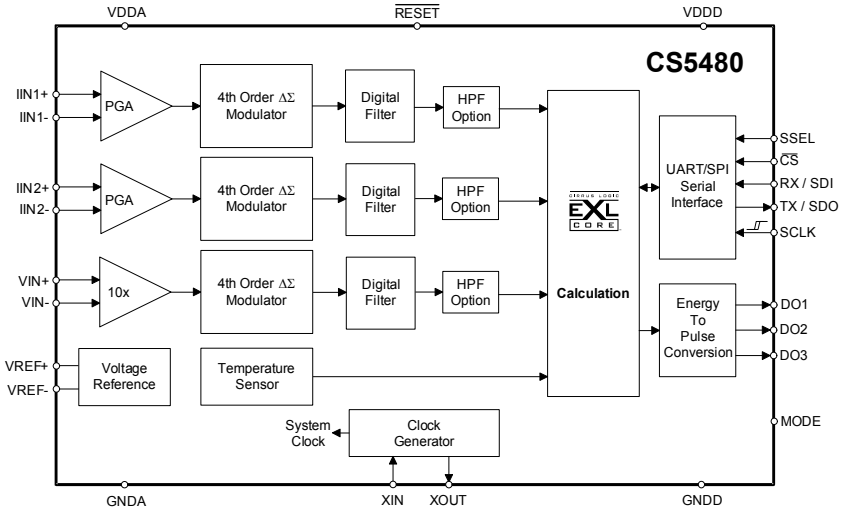
The CS5480 is a high-accuracy, three-channel, energy measurement analog front end.

The CS5480 incorporates independent, 4th order, Delta-Sigma analog-to-digital converters for every channel, reference circuitry, and the proven EXL signal processing core to provide active, reactive, and apparent energy measurement. In addition, RMS and power factor calculations are available. Calculations are output via configurable energy pulse, or direct UART/SPI™ serial access to on-chip registers.

Instantaneous current, voltage, and power measurements are also available over the serial port. Multiple serial options are offered to allow customer flexibility. The SPI provides higher speed, and the 2-wire UART minimizes the cost of isolation where required.

Three configurable digital outputs provide energy pulses, zero-crossing, energy direction, and interrupt functions. Interrupts can be generated for a variety of conditions including voltage sag or swell, overcurrent, and more. On-chip register integrity is assured via checksum and write protection. The CS5480 is designed to interface to a variety of voltage and current sensors including shunt resistors, current transformers, and Rogowski coils.

On-chip functionality makes digital calibration simple and ultra-fast, minimizing the time required at the end of the customer production line. Performance across temperature is ensured with an on-chip voltage reference with very low drift. A single 3.3V power supply is required, and power consumption is very low at <13mW. To minimize space requirements, the CS5480 is offered in a low-cost, 4mm x 4mm 24-pin QFN package.



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1. OVERVIEW

The CS5480 is a CMOS power measurement integrated circuit that uses three ΔΣ analog-to-digital converters to measure line voltage, two currents and temperature. It calculates active, reactive, and apparent power as well as RMS voltage and current and peak voltage and current. It handles other system-related functions, such as energy pulse generation, voltage sag and swell, overcurrent and zero-crossing detection, and line frequency measurement.

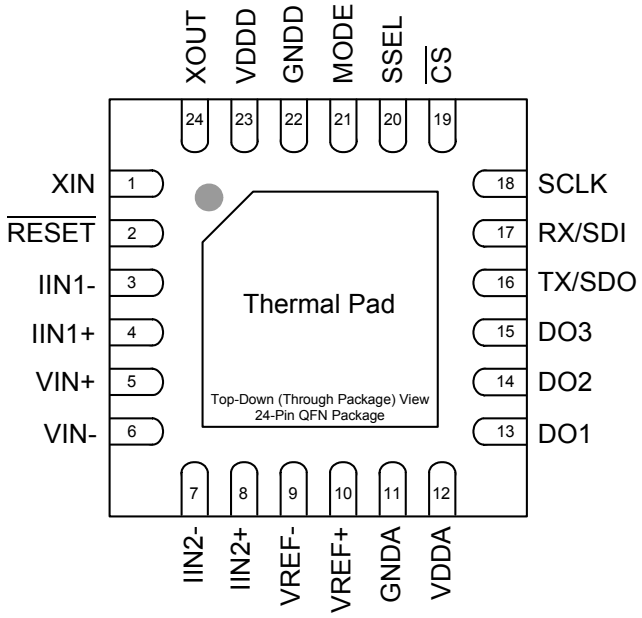
The CS5480 is optimized to interface to current transformers, shunt resistors, or Rogowski coils for current measurement and to resistive dividers or voltage transformers for voltage measurement. Two full-scale ranges are provided on the current inputs to accommodate different types of current sensors. The CS5480's three differential inputs have a common-mode input range from analog ground (GNDA) to the positive analog supply (VDDA).

An on-chip voltage reference (nominally 2.4 volts) is generated and provided at analog output, VREF±.

Three digital outputs (DO1, DO2, and DO3) provide a variety of output signals, and depending on the mode selected, energy pulses, zero-crossings, or other choices.

The CS5480 includes a UART/SPI™ serial host interface to an external microcontroller. The serial select (SSEL) pin is used to configure the serial port to be a SPI or UART. SPI signals include serial data input (SDI), serial data output (SDO), and serial clock (SCLK). UART signals include serial data input (RX) and serial data output (TX). A chip select ($\overline{CS}$) signal allows multiple CS5480s to share the same serial interface with the microcontroller.

2. PIN DESCRIPTION



Clock Generator		
Crystal In **Crystal Out**	1,24	**XIN, XOUT** — Connect to an external quartz crystal. Alternatively, an external clock can be supplied to the XIN pin to provide the system clock for the device.
Digital Pins and Serial Data I/O		
Digital Outputs	13,14,15	**DO1, DO2, DO3** — Configurable digital outputs for energy pulses, interrupt, tamper indication, energy direction, and zero-crossings.
Reset	2	**$\overline{\text{RESET}}$** — An active-low Schmitt-trigger input used to reset the chip.
Serial Data I/O	16,17	**TX/SDO, RX/SDI** — UART/SPI serial data output/input.
Serial Clock Input	18	**SCLK** — Serial clock for the SPI.
Serial Mode Select	20	**SSEL** — Selects the type of the serial interface, UART or SPI™. Logic level one - UART selected. Logic level zero - SPI selected.
Chip Select	19	**$\overline{\text{CS}}$** — Chip select for the UART/SPI.
Operating Mode Select	21	**MODE** — Connect to VDDA for proper operation.
Analog Inputs/Outputs		
Voltage Input	5,6	**VIN+, VIN-** — Differential analog input for the voltage channel.
Current Inputs	4,3,8,7	**IIN1+, IIN1-, IIN2+, IIN2-** — Differential analog inputs for the current channels.
Voltage Reference	10,9	**VREF+, VREF-** — The internal voltage reference. A 0.1 µF bypass capacitor is required between these two pins.
Power Supply Connections		
Internal Digital Supply	23	**VDDD** — Decoupling pin for the internal 1.8V digital supply. A 0.1µF bypass capacitor is required between this pin and GNDD.
Digital Ground	22	**GNDD** — Digital ground.
Positive Analog Supply	12	**VDDA** — The positive 3.3V analog supply.
Analog Ground	11	**GNDA** — Analog ground.
Thermal Pad	-	No Electrical Connection.

2.1 Analog Pins

The CS5480 has a differential input (VIN±) for voltage input and two differential inputs (IIN1±, IIN2±) for current1 and current2 inputs. The CS5480 also has two voltage reference pins (VREF±) between which a bypass capacitor should be placed.

2.1.1 Voltage Input

The output of the line voltage resistive divider or transformer is connected to the (VIN±) input of the CS5480. The voltage channel is equipped with a 10x, fixed-gain amplifier. The full-scale signal level that can be applied to the voltage channel is ±250 mV. If the input signal is a sine wave, the maximum RMS voltage is 250 mVp/$\sqrt{2}$ ≈ 176.78 mV_{RMS}, which is approximately 70.7% of maximum peak voltage.

2.1.2 Current1 and Current2 Inputs

The output of the current-sensing shunt resistor, transformer, or Rogowski coil is connected to the IIN1± or IIN2± input pins of the CS5480. To accommodate different current-sensing elements, the current channel incorporates a programmable gain amplifier (PGA) with two selectable input gains, as described in *Config0* register description section *6.6.1 Configuration 0 (Config0) – Page 0, Address 0* on page 37. There is a 10x gain setting and a 50x gain setting. The full-scale signal level for current channels is ±50 mV and ±250 mV for 50x and 10x gain settings, respectively. If the input signal is a sine wave, the maximum RMS voltage is 35.35 mV_{RMS} or 176.78 mV_{RMS}, which is approximately 70.7% of maximum peak voltage.

2.1.3 Voltage Reference

The CS5480 generates a stable voltage reference of 2.4 V between the VREF± pins. The reference system also requires a filter capacitor of at least 0.1 µF between the VREF± pins.

The reference system is capable of providing a reference for the CS5480 but has limited ability to drive external circuitry. It is strongly recommended that nothing other than the required filter capacitor be connected to the VREF± pins.

2.1.4 Crystal Oscillator

An external, 4.096 MHz quartz crystal can be connected to the XIN and XOUT pins, as shown in Figure 1. To reduce system cost, each pin is supplied with an on-chip load capacitor.

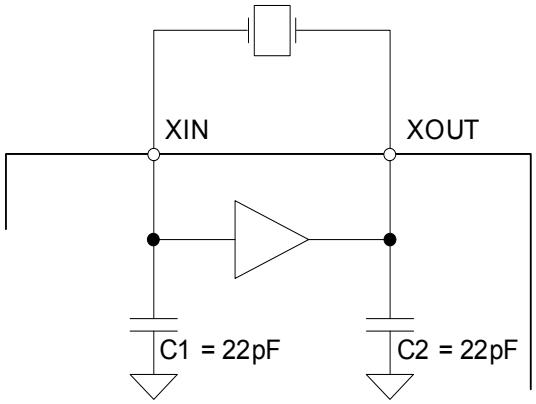


Figure 1. Oscillator Connections

Alternatively, an external clock source can be connected to the XIN pin.

2.2 Digital Pins

2.2.1 Reset Input

The active-low $\overline{\text{RESET}}$ pin, when asserted for longer than 120 µs, will halt all CS5480 operations and reset internal hardware registers and states. When de-asserted, an initialization sequence begins, setting default register values. To prevent erroneous noise-induced resets to the CS5480, an external pull-up resistor and a decoupling capacitor are necessary on the $\overline{\text{RESET}}$ pin.

2.2.2 Digital Outputs

The CS5480 provides three configurable digital outputs (DO1-DO3). They can be configured to output energy pulses, interrupt, zero-crossings, or energy directions. Refer to the description of the *Config1* register in section *6.6.2 Configuration 1 (Config1) – Page 0, Address 1* on page 38 for more details.

2.2.3 UART/SPI™ Serial Interface

The CS5480 provides five pins—SSEL, RX/SDI, TX/SDO, $\overline{\text{CS}}$, and SCLK—for communication between a host microcontroller and the CS5480.

SSEL is an input that, when low, indicates to the CS5480 to use the SPI port as the serial interface to communicate with the host microcontroller. The SSEL pin has an internal weak pull-up. When the SSEL pin is left unconnected or pulled high externally, the UART port is used as the serial interface.

2.2.3.1 SPI

The CS5480 provides a Serial Peripheral Interface (SPI) that operates as a slave device in 4-wire mode and supports multiple slaves on the SPI bus. The 4-wire SPI includes $\overline{CS}$, SCLK, SDI, and SDO signals.

$\overline{CS}$ is the chip select input for the CS5480 SPI port. A high logic level de-asserts it, tri-stating the SDO pin and clearing the SPI interface. A low logic level enables the SPI port. Although the $\overline{CS}$ pin may be tied low for systems that do not require multiple SDO drivers, using the $\overline{CS}$ signal is strongly recommended to achieve a more reliable SPI communication.

SCLK is the serial clock input for the CS5480 SPI port. Serial data changes as a result of the falling edge of SCLK and is valid at the rising edge. The SCLK pin is a Schmitt-trigger input.

SDI is the serial data input to the CS5480.

SDO is the serial data output from the CS5480.

The CS5480 SPI transmits and receives data MSB first. Refer to *Switching Characteristics* on page 14 and Figure 7 on page 15 for more detailed information of SPI timing.

2.2.3.2 UART

The CS5480 device contains an asynchronous, full-duplex UART. The UART may be used in either standard 2-wire communication mode (RX/TX) for connecting a single device or 3-wire communication mode (RX/TX/$\overline{CS}$) for connecting multiple devices. When connecting a single CS5480 device, $\overline{CS}$ should be held low to enable the UART. Multiple CS5480 devices can communicate to the same master UART in the 3-wire mode by pulling a slave $\overline{CS}$ pin low during data transmissions. Common RX and TX signals are provided to all the slave devices, and each slave device requires a separate $\overline{CS}$ signal for enabling communication to that slave. The multi-device UART mode connections are shown in Figure 2.

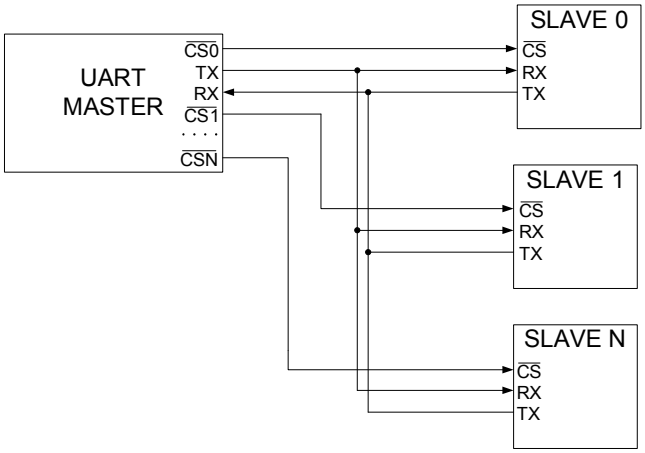


Figure 2. Multi-device UART Connections

The multi-device UART mode timing diagram provides the timing requirements for the $\overline{CS}$ control (see Figure 8. *Multi-device UART Timing* on page15).

The CS5480 UART operates in 8-bit mode, which transmits a total of 10 bits per byte. Data is transmitted and received LSB first, with one start bit, eight data bits, and one stop bit.

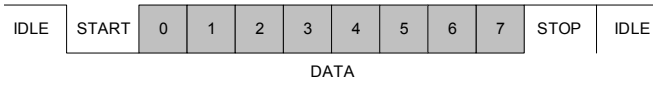


Figure 3. UART Serial Frame Format

The baud rate is defined in the *SerialCtrl* register. After chip reset, the default baud rate is 600, if MCLK is 4.096 MHz. The baud rate is based on the contents of bits BR[15:0] in the *SerialCtrl* register and is calculated as follows:

$$BR[15:0] = Baud\ Rate \times (524288 / MCLK)$$

or

$$Baud\ Rate = BR[15:0] / (524288 / MCLK)$$

The maximum baud rate is 512K if MCLK is 4.096 MHz.

2.2.4 MODE Pin

The MODE pin must be tied to VDDA for normal operation. The MODE pin is used primarily for factory test procedures.

3. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Positive Analog Power Supply	VDDA	3.0	3.3	3.6	V
Specified Temperature Range	T_A	-40	-	+85	°C

POWER MEASUREMENT CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Active Energy (Note 1 and 2)	All Gain Ranges Current Channel Input Signal Dynamic Range 4000:1	P_{Avg}	-	±0.1	-	%
Reactive Energy (Note 1 and 2)	All Gain Ranges Current Channel Input Signal Dynamic Range 4000:1	Q_{Avg}	-	±0.1	-	%
Apparent Power (Note 1 and 3)	All Gain Ranges Current Channel Input Signal Dynamic Range 1000:1	S	-	±0.1	-	%
Current RMS (Note 1, 3, and 4)	All Gain Ranges Current Channel Input Signal Dynamic Range 1000:1	I_{RMS}	-	±0.1	-	%
Voltage RMS (Note 1 and 3)	Voltage Channel Input Signal Dynamic Range 20:1	V_{RMS}	-	±0.1	-	%
Power Factor (Note 1 and 3)	All Gain Ranges Current Channel Input Signal Dynamic Range 1000:1	PF	-	±0.1	-	%

Notes:
1. Specifications guaranteed by design and characterization.
2. Active energy is tested with power factor (PF) = 1.0. Reactive energy is tested with Sin(φ) = 1.0. Energy error measured at system level using a single energy pulse. Where: 1) One energy pulse = 0.5Wh or 0.5Varh; 2) VDDA = +3.3V, T_A = 25°C, MCLK = 4.096MHz; 3) System is calibrated.
3. Calculated using register values; N≥4000.
4. I_{RMS} error calculated using register values. 1) VDDA = +3.3V; T_A = 25°C; MCLK = 4.096MHz; 2) AC offset calibration applied.

TYPICAL LOAD PERFORMANCE

- Energy error measured at system level using single energy pulse; where one energy pulse = 0.5Wh or 0.5Varh.
- I_{RMS} error calculated using register values.
- VDDA = +3.3V; T_A = 25°C; MCLK = 4.096MHz.

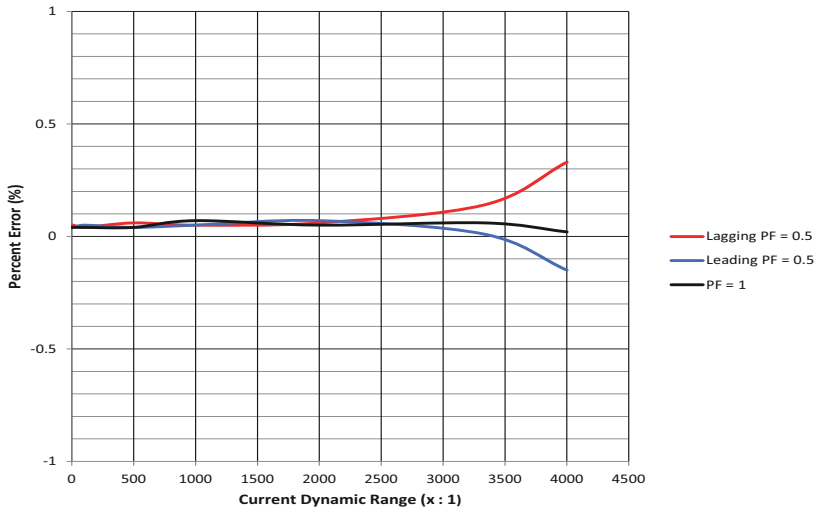


Figure 4. Active Energy Load Performance

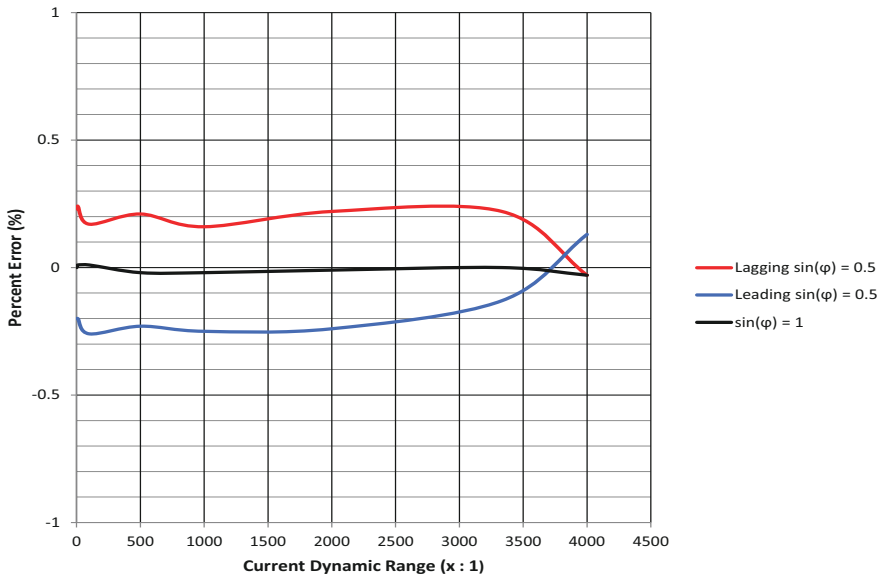


Figure 5. Reactive Energy Load Performance

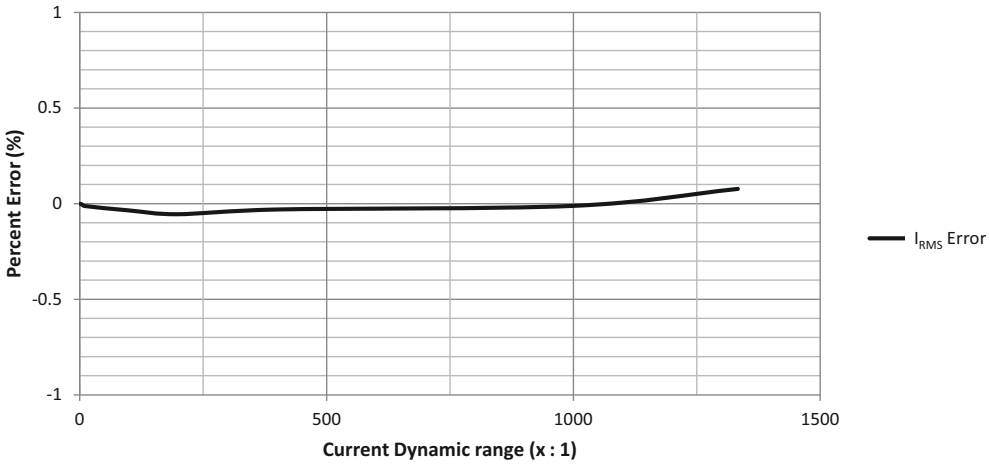


Figure 6. I_{RMS} Load Performance

ANALOG CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all Recommended Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and T_A = 25°C.
- VDDA = +3.3V ±10%; GNDA = GNDD = 0V. All voltages with respect to 0V.
- MCLK = 4.096MHz.

Parameter		Symbol	Min	Typ	Max	Unit
Analog Inputs (Current Channels)						
Common Mode Rejection	(DC, 50, 60Hz)	CMRR	80	-	-	dB
Common Mode+Signal			-0.25	-	VDDA	V
Differential Full-scale Input Range [(IIN+) – (IIN-)]	(Gain = 10) (Gain = 50)	IIN	- -	250 50	- -	mV_P mV_P
Total Harmonic Distortion	(Gain = 50)	THD	90	100	-	dB
Signal-to-Noise Ratio (SNR)	(Gain = 10) (Gain = 50)	SNR	- -	80 80	- -	dB dB
Crosstalk from Voltage Inputs at Full Scale	(50, 60Hz)		-	-115	-	dB
Crosstalk from Current Input at Full Scale	(50, 60Hz)		-	-115	-	dB
Input Capacitance		IC	-	27	-	pF
Effective Input Impedance		EII	30	-	-	kΩ
Offset Drift (Without the High-pass Filter)		OD	-	4.0	-	µV/°C
Noise (Referred to Input)	(Gain = 10) (Gain = 50)	N_I	- -	15 3.5	- -	μV_{RMS} μV_{RMS}
Power Supply Rejection Ratio (Note 7)	(60Hz) (Gain = 10) (Gain = 50)	PSRR	 60 68	 65 75	 - -	 dB dB
Analog Inputs (Voltage Channels)						
Common Mode Rejection	(DC, 50, 60Hz)	CMRR	80	-	-	dB
Common Mode+Signal			-0.25	-	VDDA	V
Differential Full-scale Input Range	[(VIN+) – (VIN-)]	VIN	-	250	-	mV_P
Total Harmonic Distortion		THD	80	88	-	dB
Signal-to-Noise Ratio (SNR)		SNR	-	73	-	dB
Crosstalk from Current Inputs at Full Scale	(50, 60Hz)		-	-115	-	dB
Input Capacitance		IC	-	2.0	-	pF
Effective Input Impedance		EII	2	-	-	MΩ
Noise (Referred to Input)		N_V	-	40	-	μV_{RMS}
Offset Drift (Without the High-pass Filter)		OD	-	16.0	-	µV/°C
Power Supply Rejection Ratio (Note 7)	(60Hz) (Gain = 10x)	PSRR	 60	 65	 -	 dB
Temperature						
Temperature Accuracy	(Note 6)	T	-	±5	-	°C

Parameter	Symbol	Min	Typ	Max	Unit
Power Supplies					
Power Supply Currents (Active State) I_{A+} (VDDA = +3.3V)	PSCA	-	3.9	-	mA
Power Consumption (Note 5) Active State (VDDA = +3.3V)	PC	-	12.9	-	mW
Stand-by State		-	4.5	-	mW

Notes:
5. All outputs unloaded. All inputs CMOS level.
6. Temperature accuracy measured after calibration is performed.
7. Measurement method for PSRR: VDDA = +3.3V, a 150mV (zero-to-peak) (60Hz) sine wave is imposed onto the +3.3V DC supply voltage at the VDDA pin. The "+" and "-" input pins of both input channels are shorted to GNDA. The CS5480 is then commanded to continuous conversion acquisition mode, and digital output data is collected for the channel under test. The (zero-to-peak) value of the digital sinusoidal output signal is determined, and this value is converted into the (zero-to-peak) value of the sinusoidal voltage (measured in mV) that would need to be applied at the channel's inputs in order to cause the same digital sinusoidal output. This voltage is then defined as V_{eq} PSRR is (in dB):

$$PSRR = 20 \cdot \log\left[\frac{150}{V_{eq}}\right]$$

VOLTAGE REFERENCE

Parameter	Symbol	Min	Typ	Max	Unit
Reference (Note 8)					
Output Voltage	VREF	+2.3	+2.4	+2.5	V
Temperature Coefficient (Note 9)	TC_{VREF}	-	25	-	ppm/°C
Load Regulation (Note 10)	ΔV_R	-	30	-	mV

Notes:
8. It is strongly recommended that no connection other than the required filter capacitor be made to VREF±.
9. The voltage at VREF± is measured across the temperature range. From these measurements the following formula is used to calculate the VREF temperature coefficient:

$$TC_{VREF} = \left(\frac{VREF_{MAX} - VREF_{MIN}}{VREF_{AVG}}\right)\left(\frac{1}{T_A MAX - T_A MIN}\right)(1.0 \times 10^6)$$

10. Specified at maximum recommended output of 1µA sourcing. VREF is a sensitive signal; the output of the VREF circuit has a high output impedance so that the 0.1µF reference capacitor provides attenuation even to low-frequency noise, such as 50Hz noise on the VREF output. Therefore VREF is intended for the CS5480 only and should not be connected to any external circuitry. The output impedance is sufficiently high that standard digital multimeters can significantly load this voltage. The accuracy of the metrology IC cannot be guaranteed when a multimeter or any component other than the 0.1µF capacitor is attached to VREF. If it is desired to measure VREF for any reason other than a very course indicator of VREF functionality, Cirrus recommends a very high input impedance multimeter such as the Keithley Model 2000 Digital Multimeter be used. Cirrus cannot guarantee the accuracy of the metrology with this meter connected to VREF.

DIGITAL CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all Recommended Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and T_A = 25°C.
- VDDA = +3.3V ±10%; GNDA = GNDD = 0V. All voltages with respect to 0V.
- MCLK = 4.096MHz.

Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Characteristics						
XIN Clock Frequency	Internal Gate Oscillator	MCLK	2.5	4.096	5	MHz
XIN Clock Duty Cycle			40	-	60	%
Filter Characteristics						
Phase Compensation Range	(60Hz, OWR = 4000Hz)		-10.79	-	+10.79	°
Input Sampling Rate			-	MCLK/8	-	Hz
Digital Filter Output Word Rate	(Both channels)	OWR	-	MCLK/1024	-	Hz
High-pass Filter Corner Frequency	-3dB		-	2.0	-	Hz
Input/Output Characteristics						
High-level Input Voltage (All Pins)		V_{IH}	0.6(VDDA)	-	-	V
Low-level Input Voltage (All Pins)		V_{IL}	-	-	0.6	V
High-level Output Voltage (Note 12)	DO1-DO3, I_{out} = +10mA All Other Outputs, I_{out} = +5mA	V_{OH}	VDDA-0.3 VDDA-0.3	- -	- -	V V
Low-level Output Voltage (Note 12)	DO1-DO3, I_{out} = -12mA All Other Outputs, I_{out} = -5mA	V_{OL}	- -	- -	0.5 0.5	V V
Input Leakage Current		I_{in}	-	±1	±10	µA
3-state Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	5	-	pF

Notes: 11. All measurements performed under static conditions.
12. XOUT pin used for crystal only. Typical drive current<1mA.

SWITCHING CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all Recommended Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and T_A = 25°C.
- VDDA = +3.3V ±10%; GNDA = GNDD = 0V. All voltages with respect to 0V.
- Logic Levels: Logic 0 = 0V, Logic 1 = VDDA.

Parameter		Symbol	Min	Typ	Max	Unit
Rise Times (Note 13)	DO1-DO3 Any Digital Output Except DO1-DO3	t_{rise}	- -	- 50	1.0 -	µs ns
Fall Times (Note 13)	DO1-DO3 Any Digital Output Except DO1-DO3	t_{fall}	- -	- 50	1.0 -	µs ns
Start-up						
Oscillator Start-up Time	XTAL = 4.096 MHz (Note 14)	t_{ost}	-	60	-	ms
SPI Timing						
Serial Clock Frequency	(Note 15)	SCLK	-	-	2	MHz
Serial Clock	Pulse Width High Pulse Width Low	t_1 t_2	200 200	- -	- -	ns ns
$\overline{CS}$ Enable to SCLK Falling		t_3	50	-	-	ns
Data Set-up Time prior to SCLK Rising		t_4	50	-	-	ns
Data Hold Time After SCLK Rising		t_5	100	-	-	ns
SCLK Rising Prior to $\overline{CS}$ Disable		t_6	1	-	-	µs
SCLK Falling to New Data Bit		t_7	-	-	150	ns
$\overline{CS}$ Rising to SDO Hi-Z		t_8	-	-	250	ns
UART Timing						
$\overline{CS}$ Enable to RX START bit		t_9	5	-	-	ns
STOP bit to $\overline{CS}$ Disable		t_{10}	1	-	-	µs
$\overline{CS}$ Disable to TX IDLE Hold Time		t_{11}	-	-	250	ns

Notes:
13. Specified using 10% and 90% points on waveform of interest. Output loaded with 50pF.
14. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.
15. The maximum SCLK is 2MHz during a byte transaction. The minimum 1µs idle time is required on the SCLK between two consecutive bytes.

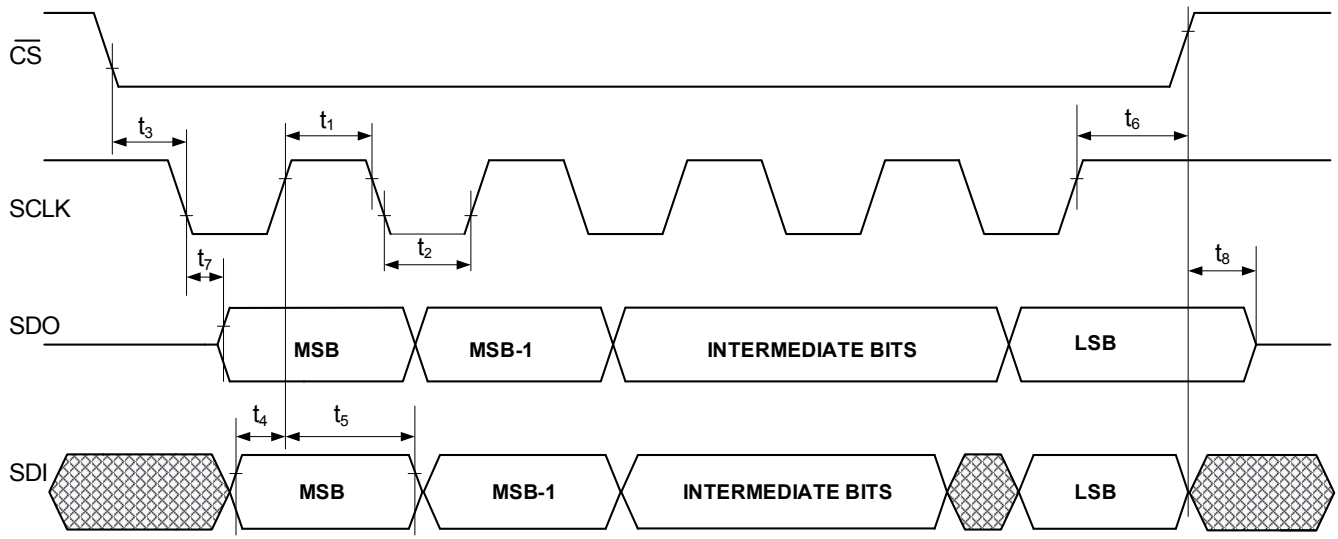


Figure 7. SPI Data and Clock Timing

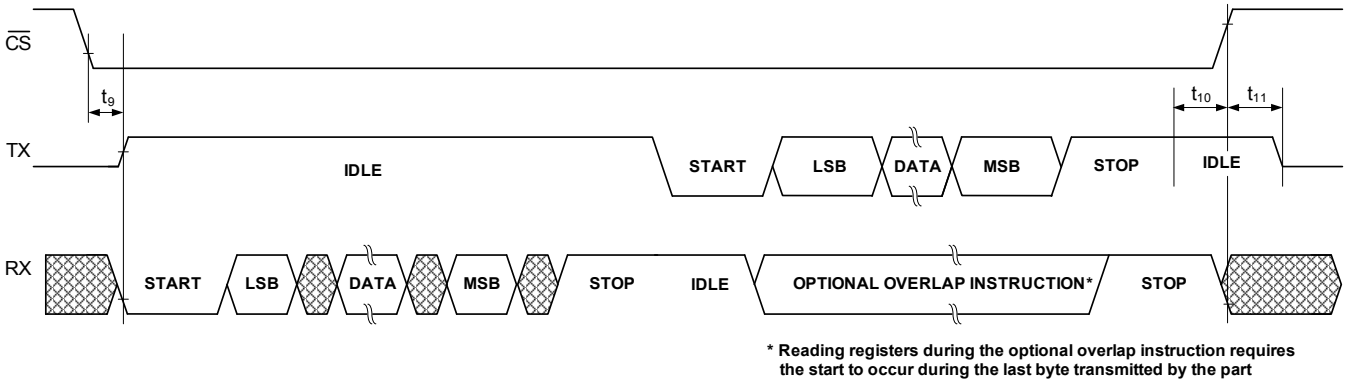


Figure 8. Multi-device UART Timing

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	(Note 16)	VDDA	-0.3	-	+4.0	V
Input Current	(Notes 17 and 18)	I_{IN}	-	-	±10	mA
Input Current for Power Supplies		-	-	-	±50	-
Output Current	(Note 19)	I_{OUT}	-	-	100	mA
Power Dissipation	(Note 20)	P_D	-	-	500	mW
Input Voltage	(Note 21)	V_{IN}	-0.3	-	(VDDA) + 0.3	V
Junction-to-Ambient Thermal Impedance	2 Layer Board 4 Layer Board	θ_{JA}	- -	55 46	- -	°C/W °C/W
Ambient Operating Temperature		T_A	-40	-	85	°C
Storage Temperature		T_{stg}	-65	-	150	°C

Notes:
16. VDDA and GNDA must satisfy [(VDDA) – (GNDA)] ≤ + 4.0V.
17. Applies to all pins, including continuous overvoltage conditions at the analog input pins.
18. Transient current of up to 100mA will not cause SCR latch-up.
19. Applies to all pins, except VREF±.
20. Total power dissipation, including all input currents and output currents.
21. Applies to all pins.

WARNING:

Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

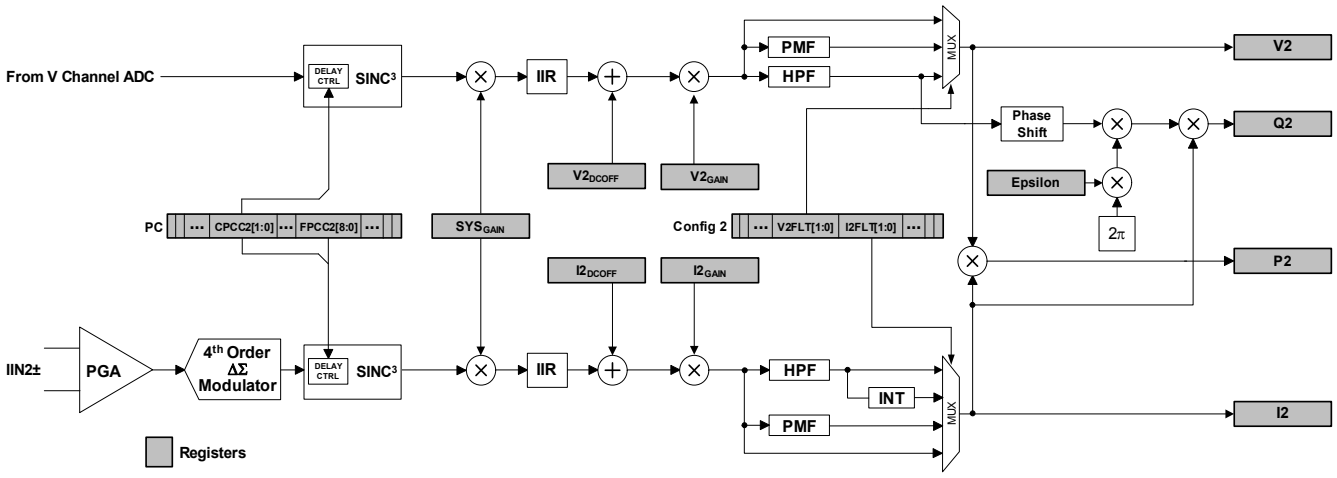


Figure 9. Signal Flow for V1, I1, P1, Q1 Measurements

4. SIGNAL FLOW DESCRIPTION

The signal flow for voltage measurement, current measurement, and the other calculations is shown in Figures 9, 10, and 11.

The signal flow consists of two current channels and a voltage channel. Even though the CS5480 has only one voltage channel or voltage analog signal input, there are two separate voltage digital signal paths (V1 and V2). Both V1 and V2 come from the same ADC output. Each current and voltage channel has its own differential input pin.

4.1 Analog-to-Digital Converters

All three input channels use fourth-order delta-sigma modulators to convert the analog inputs to single-bit digital data streams. The converters sample at a rate of MCLK/8. This high sampling provides a wide dynamic range and simplifies anti-alias filter design.

4.2 Decimation Filters

The single-bit modulator output data is widened to 24 bits and down sampled to MCLK/1024 with low-pass decimation filters. These decimation filters are third-order Sinc filters. The outputs of the filters are passed through an IIR "anti-sinc" filter.

4.3 IIR Filters

The IIR filters are used to compensate for the amplitude roll-off of the decimation filters. The droop-correction filter flattens the magnitude response of the channel out to the Nyquist frequency, thus allowing for accurate measurements of up to 2kHz (MCLK = 4.096MHz). By default, the IIR filters are enabled. The IIR filters can be bypassed by setting the IIR_OFF bit in the *Config2* register.

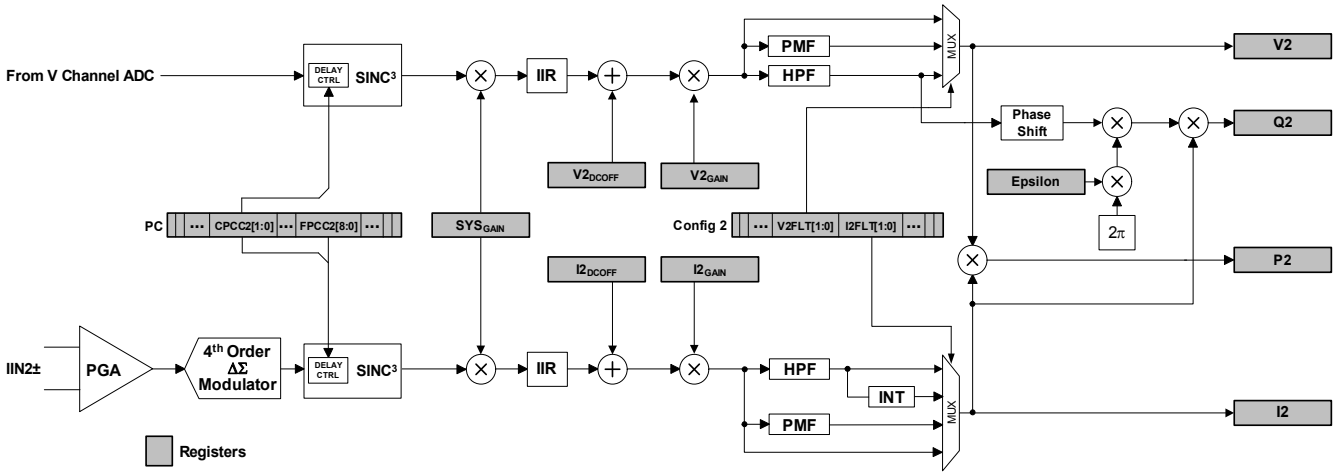


Figure 10. Signal Flow for V2, I2, P2, and Q2 Measurements

4.4 Phase Compensation

Phase compensation changes the phase of voltage relative to current by adding a delay in the decimation filters. The amount of phase shift is set by the PC register bits CPCCx[1:0] and FPCCx[8:0] for current channels. For voltage channels, only bits CPCCx[1:0] affect the delay.

Fine phase compensation control bits, FPCCx[8:0], provide up to 1/OWR delay in the current channels. Coarse phase compensation control bits, CPCCx[1:0], provide an additional 1/OWR delay in the current channel or up to 2/OWR delay in the voltage channel. Negative delay in voltage channel can be implemented by setting a longer delay in the current channel than the voltage channel. For a OWR of 4000 Hz, the delay range is ±500 µs, a phase shift of ±8.99° at 50 Hz and ±10.79° at 60 Hz. The step size is 0.008789° at 50 Hz and 0.010547° at 60 Hz.

4.5 DC Offset and Gain Correction

The system and CS5480 inherently have component tolerances and gain and offset errors, which can be removed using the gain and offset registers. Each measurement channel has its own set of gain and offset registers. For every instantaneous voltage and current sample, the offset and gain values are used to correct DC offset and gain errors in the channel (see section *7. System Calibration* on page 63 for more details).

4.6 High-pass and Phase Matching Filters

Optional high-pass filters (HPF in Figures 9 and 10) remove any DC component from the selected signal paths. Each power calculation contains a current and voltage channel. If an HPF is enabled in only one channel, a phase matching filter (PMF) should be applied to the other channel to match the phase response of the HPF. For AC power measurement, high-pass filters should be enabled on the voltage and current channels. For information about how to enable and disable the HPF or PMF on each channel, refer to section *6.6.3 Configuration 2 (Config2) – Page 16, Address 0* on page 40.

4.7 Digital Integrators

Optional digital integrators (INT in Figures 9 and 10) are implemented on both current channels (I1, I2) to compensate for the 90º phase shift and 20 dB/decade gain generated by the Rogowski coil current sensor. When a Rogowski coil is used as the current sensor, the integrator (INT) should be enabled on that current channel. For information about how to enable and disable the INT on each current channel, refer to section *6.6.3 Configuration 2 (Config2) – Page 16, Address 0* on page 40.

4.8 Low-rate Calculations

All the RMS and power results come from low-rate calculations by averaging the output word rate (OWR) instantaneous values over *N* samples where *N* is the value stored in the *SampleCount* register. The low-rate interval or averaging period is *N* divided by OWR (4000 Hz if MCLK = 4.096MHz). The CS5480 provides two averaging modes for low-rate calculations: Fixed Number of Samples Averaging mode and Line-cycle Synchronized Averaging mode. By default, the CS5480 averages with the Fixed Number of Samples Averaging mode. By setting the AVG_MODE bit in the *Config2* register, the CS5480 will use the Line-cycle Synchronized Averaging mode.

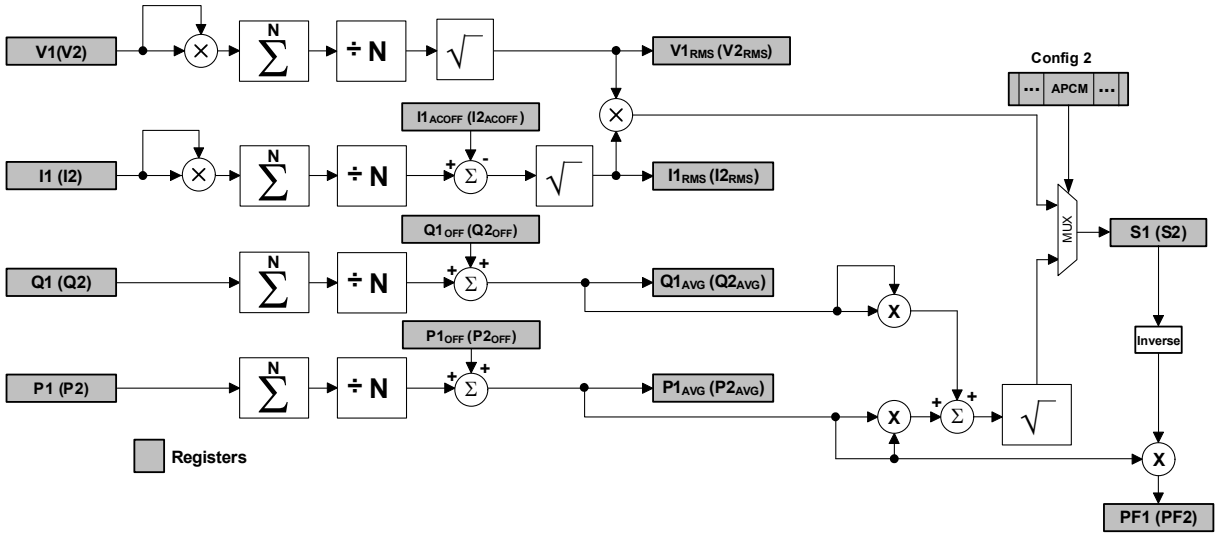


Figure 11. Low-rate Calculations

4.8.1 Fixed Number of Samples Averaging

N is the preset value in the *SampleCount* register and should not be set less than 100. By default, the *SampleCount* is 4000. With MCLK = 4.096MHz, the averaging period is fixed at N/4000 = 1 second, regardless of the line frequency.

4.8.2 Line-cycle Synchronized Averaging

When operating in Line-cycle Synchronized Averaging mode, and when line frequency measurement is enabled (see section *5.4 Line Frequency Measurement* on page 22), the CS5480 uses the voltage (V) channel zero crossings and measured line frequency to automatically adjust *N* such that the averaging period will be equal to the number of half line-cycles in the *CycleCount* register. For example, if the line frequency is 51Hz, and the *CycleCount* register is set to 100, *N* will be 4000×(100/2)/51 = 3921 during continuous conversion. *N* is self-adjusted according to the line frequency; therefore, the averaging period is always close to the whole number of half line-cycles, and the low-rate calculation results will minimize ripple and maximize resolution, especially when the line frequency varies. Before starting a low-rate conversion in Line-cycle Synchronized Averaging mode, the *SampleCount* register should not be changed from its default value of 4000, and bit AFC of the *Config2* register must be set. During continuous conversion, the host processor should not change the *SampleCount* register.

4.8.3 RMS Current and Voltage

The root mean square (RMS in Figure 11) calculations are performed on *N* instantaneous current and voltage samples using Equation 1:

$$I_{RMS} = \sqrt{\frac{\sum_{n=0}^{N-1} I_n^2}{N}} \quad V_{RMS} = \sqrt{\frac{\sum_{n=0}^{N-1} V_n^2}{N}} \qquad \text{[Eq. 1]}$$

4.8.4 Active Power

The instantaneous voltage and current samples are multiplied to obtain the instantaneous power (*P1, P2*) (see Figures 9 and 11). The product is then averaged over *N* samples to compute active power ($P1_{AVG}$, $P2_{AVG}$).

4.8.5 Reactive Power

Instantaneous reactive power (*Q1, Q2*) are sample rate results obtained by multiplying instantaneous current (*I1, I2*) by instantaneous quadrature voltage (*V1Q*, *V2Q*), which are created by phase shifting the instantaneous voltage (*V1, V2*) 90 degrees using first-order integrators (see Figures 9 and 11). The gain of these integrators is inversely related to line frequency, so their gain is corrected by the *Epsilon* register, which is based on line frequency. Reactive power ($Q1_{AVG}$, $Q2_{AVG}$) is generated by integrating the instantaneous quadrature power over *N* samples.

4.8.6 Apparent Power

By default, the CS5480 calculates the apparent power (*S1*, *S2*) as the product of RMS voltage and current as shown in Equation 2:

$$S = V_{RMS} \times I_{RMS} \qquad \text{[Eq. 2]}$$

The CS5480 also provides an alternate apparent power calculation method, which uses real power ($P1_{AVG}$, $P2_{AVG}$) and reactive power ($Q1_{AVG}$, $Q2_{AVG}$) to calculate apparent power, as shown in Equation 3:

$$S = \sqrt{Q_{AVG}^2 + P_{AVG}^2} \qquad \text{[Eq. 3]}$$

The APCM bit in the *Config2* register controls which method is used for apparent power calculation.

4.8.7 Peak Voltage and Current

Peak current ($I1_{PEAK}$, $I2_{PEAK}$) and peak voltage (V_{PEAK}) are calculated over *N* samples and recorded in the corresponding channel peak register documented in the register map. This peak value is updated every *N* samples.

4.8.8 Power Factor

Power factor (*PF1*, *PF2*) is active power divided by apparent power as shown in Equation 4. The sign of the power factor is determined by the active power.

$$PF = \frac{P_{ACTIVE}}{S} \qquad \text{[Eq. 4]}$$

4.9 Average Active Power Offset

The average active power offset registers, $P1_{OFF}$ ($P2_{OFF}$), can be used to offset erroneous power sources resident in the system not originating from the power line. Residual power offsets are usually caused by crosstalk into current channels from voltage channels, or from ripple on the meter's or chip's power supply, or from inductance from a nearby transformer.

These offsets can be either positive or negative, indicating crosstalk coupling either in phase or out of phase with the applied voltage input. The power offset registers can compensate for either condition.

To use this feature, measure the average power at no load. Take the measured result (from the $P1_{AVG}$ ($P2_{AVG}$) register), invert (negate) the value, and write it to the associated average active power offset register, $P1_{OFF}$ ($P2_{OFF}$).

4.10 Average Reactive Power Offset

The average reactive power offset registers, $Q1_{OFF}$ ($Q2_{OFF}$), can be used to offset erroneous power sources resident in the system not originating from the power line. Residual reactive power offsets are usually caused by crosstalk into current channels from voltage channels, or from ripple on the meter's or chip's power supply, or from inductance from a nearby transformer.

These offsets can be either positive or negative, depending on the phase angle between the crosstalk coupling and the applied voltage. The reactive power offset registers can compensate for either condition. To use this feature, measure the average reactive power at no load. Take the measured result from the $Q1_{AVG}$ ($Q2_{AVG}$) register, invert (negate) the value and write it to the associated reactive power offset register, $Q1_{OFF}$ ($Q2_{OFF}$).

5. FUNCTIONAL DESCRIPTION

5.1 Power-on Reset

The CS5480 has an internal power supply supervisor circuit that monitors the VDDA and VDDD power supplies and provides the master reset to the chip. If any of these voltages are in the reset range, the master reset is triggered.

The CS5480 has dedicated power-on reset (POR) circuits for the analog supply and digital supply. During power-up, both supplies have to be above the rising threshold for the master reset to be de-asserted.

Each POR is divided into two blocks: rough and fine. Rough POR triggers the fine POR. Rough POR depends only on the supply voltage. The trip point for the fine POR is dependent on bandgap voltage for precise control. The POR circuit also acts as a brownout detect. The fine POR detects supply drops and asserts the master reset. The rough and fine PORs have hysteresis in their rise and fall thresholds, which prevents the reset signal from chattering.

Figure 9 shows the POR outputs for each of the power supplies. The POR_Fine_VDDA and POR_Fine_VDDD signals are AND-ed to form the actual power-on reset signal to the digital circuity. The digital circuitry, in turn, holds the master reset signal for 130ms and then de-asserts the master reset.

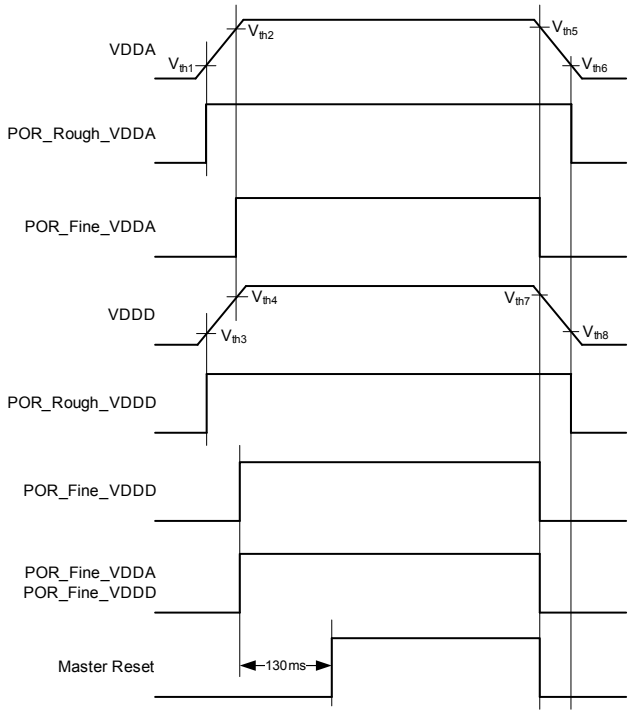


Figure 12. Power-on Reset Timing

Table 1. POR Thresholds

Typical POR Threshold		Rising	Falling
VDDA	Rough	V_{th1} = 2.34V	V_{th6} = 2.06V
	Fine	V_{th2} = 2.77V	V_{th5} = 2.59V
VDDD	Rough	V_{th3} = 1.20V	V_{th8} = 1.06V
	Fine	V_{th4} = 1.51V	V_{th7} = 1.42V

5.2 Power Saving Modes

Power Saving modes for the CS5480 are accessed through the Host Commands (see section *6.1 Host Commands* on page 29).

- Standby: Powers down all the ADCs, rough buffer, and the temperature sensor. Standby mode disables the system time calculations. Use the wake-up command to come out of standby mode.
- Wake-up: Clears the ADC power-down bits and starts the system time calculations.

After any of these commands are completed, the DRDY bit is set in the *Status0* register.

5.3 Zero-crossing Detection

Zero-crossing detection logic is implemented in the CS5480. One current and one voltage channel can be selected for zero-crossing detection. The IZX_CH control bit in the *Config0* register is used to select the zero-crossing channel. A low-pass filter can be enabled by setting ZX_LPF bit in register *Config2*. The low-pass filter has a cut-off frequency of 80Hz. It is used to eliminate any harmonics and help the zero-crossing detection on the 50Hz or 60Hz fundamental component. The zero-crossing level registers are used to set the minimum threshold over which the channel peak has to exceed in order for the zero-crossing detection logic to function. There are two separate zero-crossing level registers: VZX_{LEVEL} is the threshold for the voltage channels, and IZX_{LEVEL} is the threshold for the current channels.

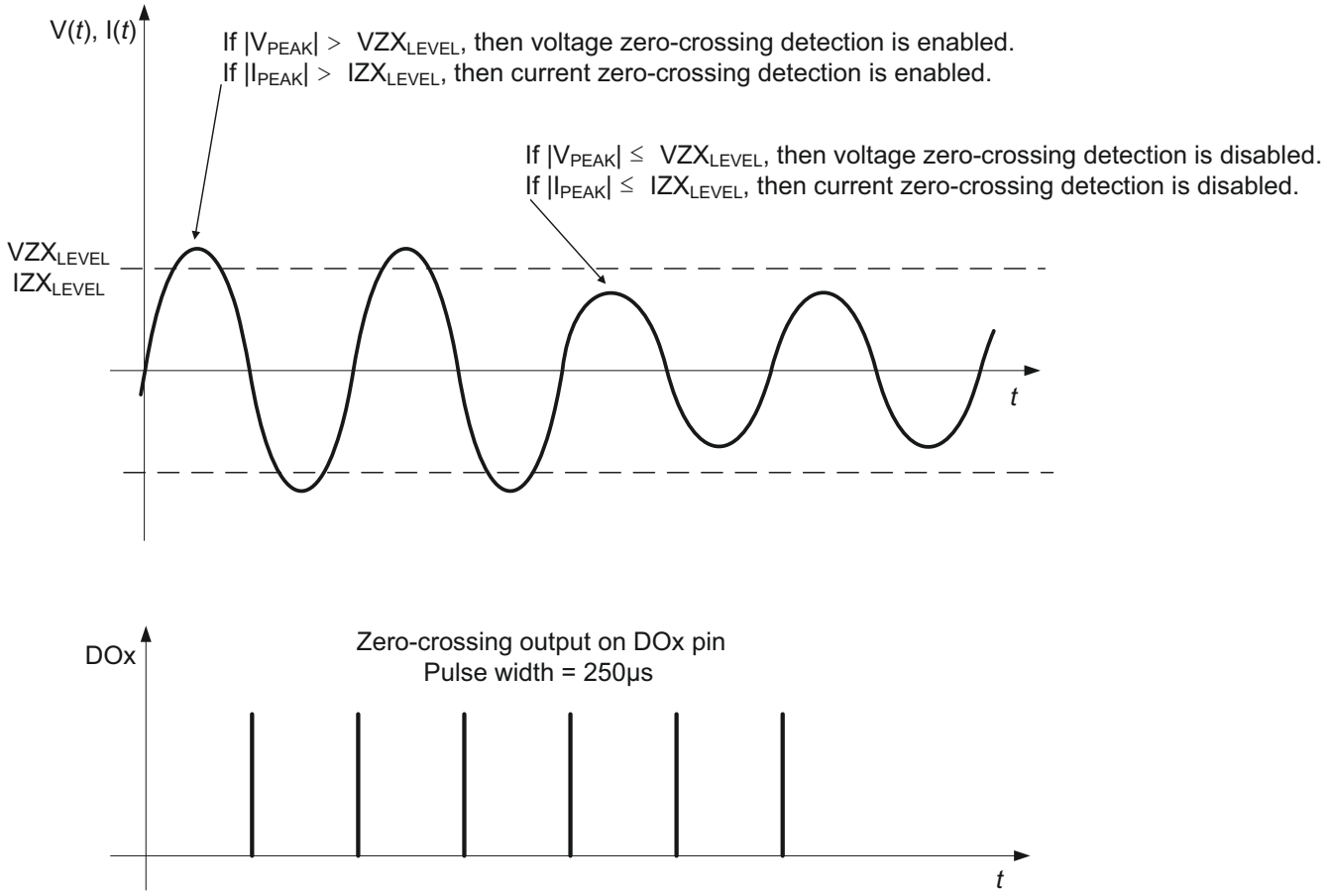


Figure 13. Zero-crossing Level and Zero-crossing Output on DOx

5.4 Line Frequency Measurement

If the Automatic Frequency Calculation (AFC) bit in the *Config2* register is set, the line frequency measurement on a voltage channel will be enabled. The line frequency measurement is based on a number of voltage channel zero crossings. This number is 100 by default and configurable through the ZX_{NUM} register (see section 6.6.7 on page 43). The *Epsilon* register will be updated automatically with the line frequency information. The Frequency Update (FUP) bit in the *Status0* interrupt status register is set when the frequency calculation is completed. When the line frequency is 50 Hz and the ZX_{NUM} register is 100, the *Epsilon* register is updated every one second with a resolution of less than 0.1%. A bigger zero-crossing number in the ZX_{NUM} register will increase both line frequency measurement resolution and period. Note that the CS5480 line frequency measurement function does not support the line frequency out of the range of 40 Hz to 75 Hz.

The *Epsilon* register is also used to set the gain of the 90° phase shift filter used in the quadrature power calculation. The value in the *Epsilon* register is the ratio of the line frequency to the output word rate (OWR). For 50 Hz line frequency and 4000 Hz OWR, *Epsilon* is 50/4000 (0.0125) (the default). For 60 Hz line frequency, it is 60/4000 (0.015).

5.5 *Meter Configuration Modes*

There are two distinct meter configuration modes in the CS5480 that affect how the total active, reactive, and apparent power calculations are performed. The CS5480 has power results for each current channel as well as total power registers (P_{SUM}, Q_{SUM}, and S_{SUM}). The total power registers are calculated from either one or both channels, depending on the meter configuration modes. See Table 2 for power calculations in each mode.

The Meter Configuration (MCFG) bits in the configuration (*Config2*) register set the meter configuration modes. For each meter mode, the current channels are interpreted differently. In the one voltage and two line currents (1V – 2I) mode, the CS5480 treats the two currents as individual contributors to the overall power. In the one voltage, one line current, and one neutral current (1V – 1I – 1N) mode, the currents are treated as duplicate copies of the same load current, and the total power is calculated from the highest current or the one the customer has specified. The MCFG multiplexers in Figure 14 show the data path for both modes.

Table 2. Meter Configuration Modes

Meter Mode	MCFG [1:0]	Total Power Calculations
1V-2I	01	$Psum = \frac{P1avg + P2avg}{2}$, $Qsum = \frac{Q1avg + Q2avg}{2}$, $Ssum = \frac{S1avg + S2avg}{2}$
1V-1I-1N ($I1_{RMS} > I2_{RMS}$) ($P1_{AVG} > P2_{AVG}$)	00 (Default)	$Psum = P1avg$, $Qsum = Q1avg$, $Ssum = S1avg$
1V-1I-1N ($I1_{RMS} < I2_{RMS}$) ($P1_{AVG} < P2_{AVG}$)	00 (Default)	$Psum = P2avg$, $Qsum = Q2avg$, $Ssum = S2avg$

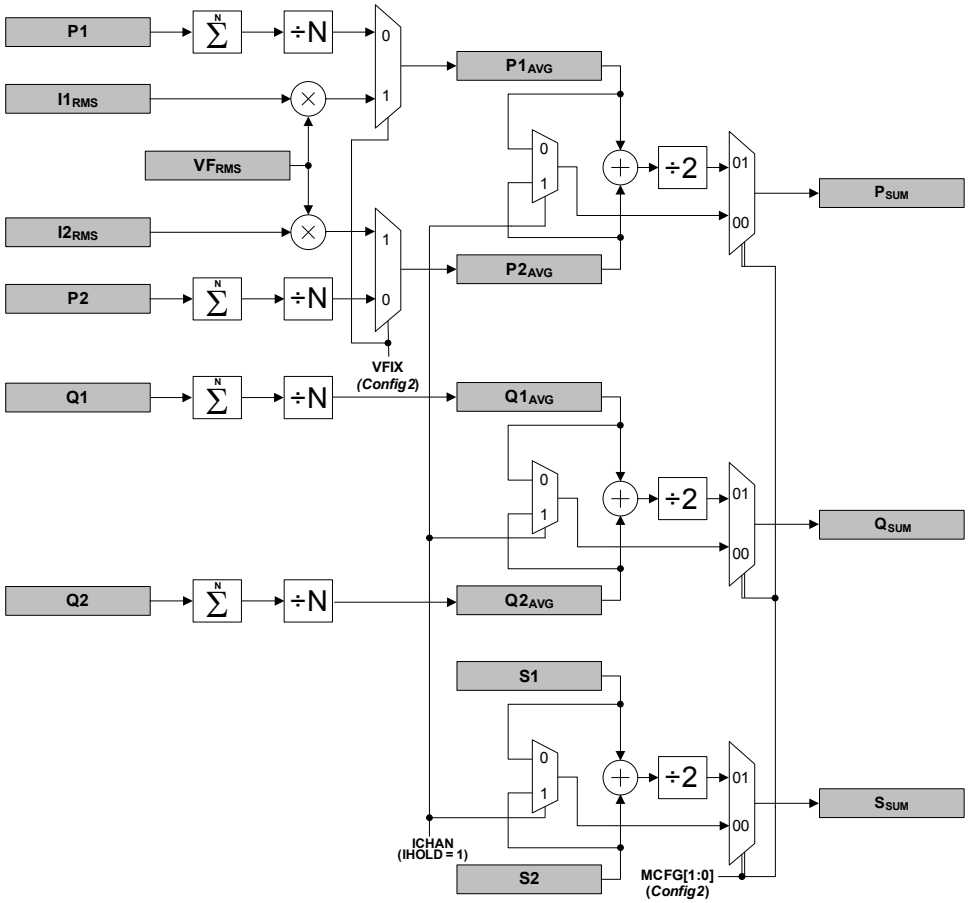


Figure 14. Channel Selection and Tamper Protection Flow

5.6 Tamper Detection and Correction

In the 1V-1I-1N meter configuration mode, the CS5480 provides flexibility for the user and application program to adjust the anti-tampering scheme automatically or manually. Automatic channel selection is enabled by default. For manual channel selection refer to section *5.6.1.2 Manual Channel Selection* on page 25.

The CS5480 provides compensation for at least two forms of meter tampering — current and voltage tampering.

5.6.1 Anti-tampering on Current

In the 1V-1I-1N mode, current tampering is deterred by an automatic or manual channel selection scheme. A dedicated second neutral current input is provided in the event that the primary current input is impaired by tampering.

5.6.1.1 Automatic Channel Selection

Automatic channel selection is standard in the CS5480. When tampering is detected, the CS5480 will automatically select the channel with the greater Px_{AVG} or Ix_{RMS} magnitude as the contributor to the total power registers. Using either Px_{AVG} or Ix_{RMS} magnitude depends on the setting of the IVSP bit in the *Config2* register.

To avoid repeated channel transitions at light load, the Channel Select Minimum Amplitude (P_{MIN} ($IRMS_{MIN}$)) register sets a minimum level for automatic channel selection. When either $P1_{AVG}$ ($I1_{RMS}$) or $P2_{AVG}$ ($I2_{RMS}$) is greater than P_{MIN} ($IRMS_{MIN}$), the CS5480 will enable automatic channel selection. Within the automatic selection region, the Channel Select Level ($Ichan_{LEVEL}$) register sets a minimum difference that will allow an automatic channel change. The channel select level provides hysteresis to prevent repeated channel transitions that would occur when the primary line current and neutral current are nearly equal.

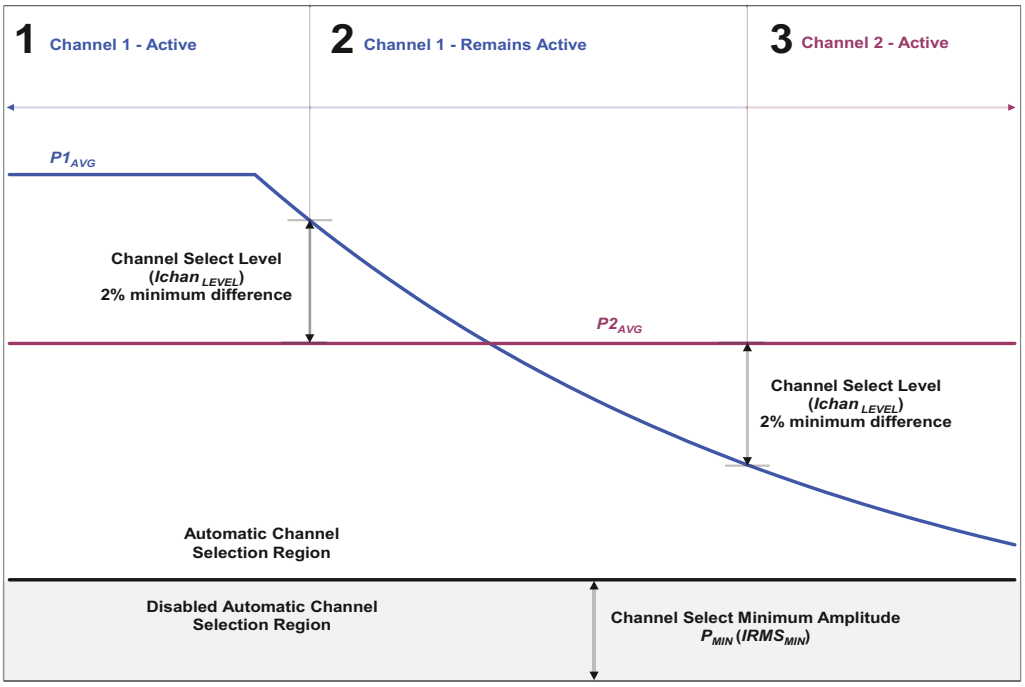


Figure 15. Automatic Channel Selection

Figure 15 shows how the automatic channel selection is performed. In this figure, the magnitudes of $P1_{AVG}$ and $P2_{AVG}$ are used for automatic channel selection (IVSP = 0) and $Ichan_{LEVEL}$ = 1.02.

- The $P1_{AVG}$ and $P2_{AVG}$ must meet the Channel Select Minimum Amplitude ($Ichan_{LEVEL}$). The highest channel is active, $P1_{AVG}$ in this example.
- Even when the active channel ($P1_{AVG}$) moves below the previously lower channel ($P2_{AVG}$), the channel selection does not change.
- The new channel selection is only made when the difference between $P1_{AVG}$ and $P2_{AVG}$ is greater than 2% x $P1_{AVG}$ or $P2_{AVG}$ > $P1_{AVG}$ x $Ichan_{LEVEL}$ (1.02).

5.6.1.2 Manual Channel Selection

In addition to automatic channel selection anti-tampering scheme, the CS5480 allows the user or application program to select the more appropriate energy channel manually. Configuration 2 (*Config2*) register bit IHOLD disable automatic channel selection, and ICHAN forces the selection of the contributor to the total power registers (see Figure 14).

5.6.2 Anti-tampering on Voltage

An internal RMS voltage reference is also available in the event that the voltage input has been compromised by tampering.

If the user application detects the voltage input has been impaired, it may choose to use the fixed internal RMS voltage reference in active power calculations by setting the VFIX bit in the Configuration 2 (*Config2*) register. The value of the Voltage Fixed RMS Reference (VF_{RMS}) register is by default 0.707107 (full-scale RMS) but can be changed by the application program. Figure 14 shows the entry point for the VF_{RMS} value. VF_{RMS} has no phase relationship to $I1_{RMS}$ or $I2_{RMS}$. Therefore, the VF_{RMS} only affects the active power calculation paths.

5.7 Energy Pulse Generation

The CS5480 provides three independent energy pulse generation blocks (EPG1, EPG2, and EPG3) in order to simultaneously output active, reactive, and apparent energy pulses on any of the three digital output pins (DO1, DO2, and DO3). The energy pulse frequency is proportional to the magnitude of the power. The energy pulse output is commonly used as the test output of a power meter. The host microcontroller can also use the energy pulses to accumulate the energy (see Figure 16).

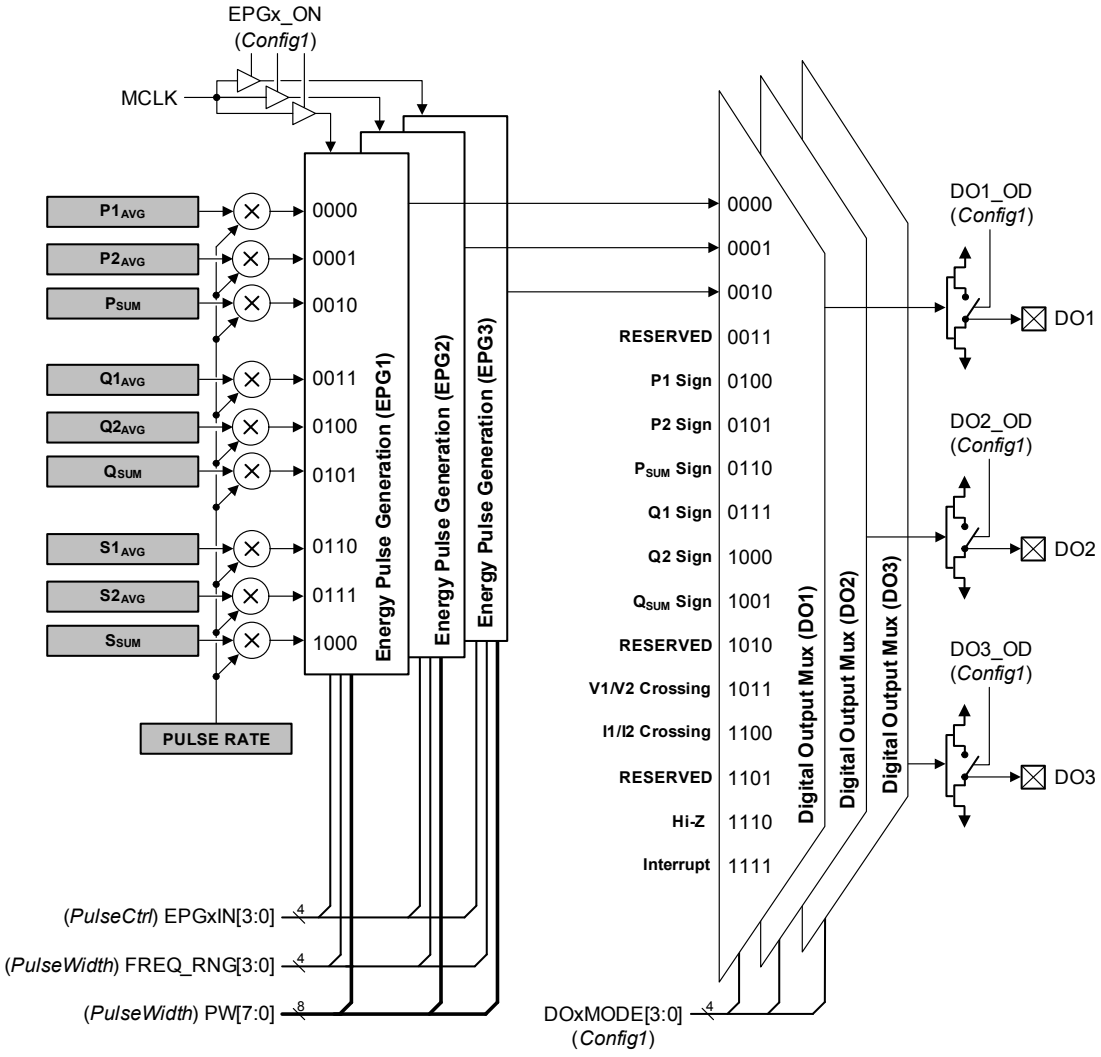


Figure 16. Energy Pulse Generation and Digital Output Control