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CS5484

Four Channel Energy Measurement IC

Features

- Superior Analog Performance with Ultra-low Noise Level and High SNR
- Energy Measurement Accuracy of 0.1% over 4000:1 Dynamic Range
- Current RMS Measurement Accuracy of 0.1% over 1000:1 Dynamic Range
- 4 Independent 24-bit, 4th-order, Delta-Sigma Modulators for Voltage and Current Measurements
- 4 Configurable Digital Outputs for Energy Pulses, Zero-crossing, or Energy Direction
- Supports Shunt Resistor, CT, and Rogowski Coil Current Sensors
- On-chip Measurements/Calculations:
  - Active, Reactive, and Apparent Power
  - RMS Voltage and Current
  - Power Factor and Line Frequency
  - Instantaneous Voltage, Current, and Power
- Overcurrent, Voltage Sag, and Voltage Swell Detection
- Ultra-fast On-chip Digital Calibration
- Internal Register Protection via Checksum and Write Protection
- UART/SPI™ Serial Interface
- On-chip Temperature Sensor
- On-chip Voltage Reference (25ppm/°C Typ.)
- Single 3.3V Power Supply
- Ultra-fine Phase Compensation
- Low Power Consumption: <13mW
- Power Supply Configurations
  - GNDA = GNDD = 0V, VDDA = +3.3V
- 5mm x 5mm 28-pin QFN Package

ORDERING INFORMATION

See Page 68.

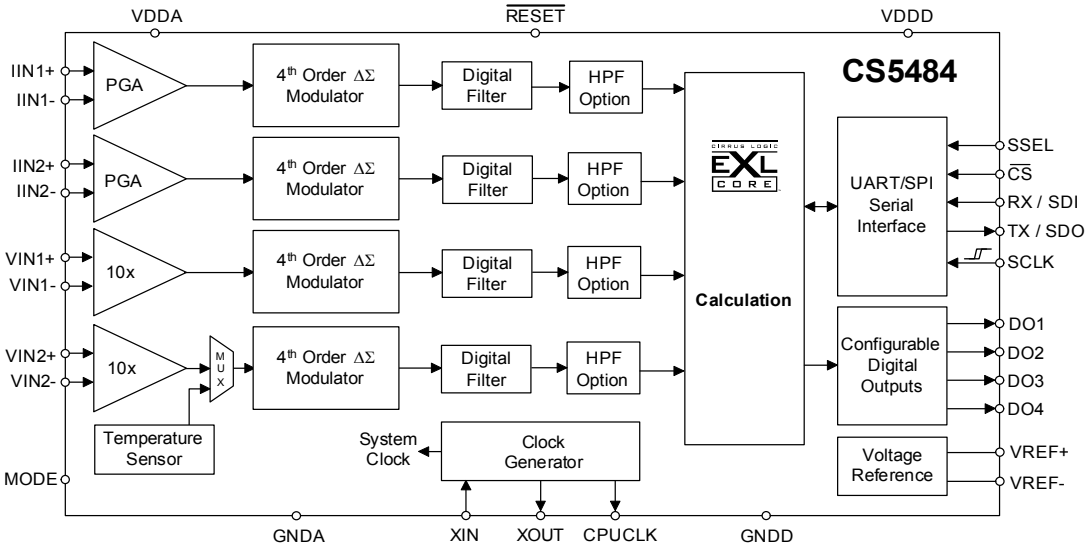
Description

The CS5484 is a high-accuracy, four-channel, energy measurement analog front end.

The CS5484 incorporates independent 4th order Delta-Sigma analog-to-digital converters for every channel, reference circuitry, and the proven EXL signal processing core to provide active, reactive, and apparent energy measurement. In addition, RMS and power factor calculations are available. Calculations are output through a configurable energy pulse, or direct UART/SPI™ serial access to on-chip registers. Instantaneous current, voltage, and power measurements are also available over the serial port. Multiple serial options are offered to allow customer flexibility. The SPI provides higher speed, and the 2-wire UART minimizes the cost of isolation where required.

Four configurable digital outputs provide energy pulses, zero-crossing, energy direction, and interrupt functions. Interrupts can be generated for a variety of conditions including voltage sag or swell, overcurrent, and more. On-chip register integrity is assured via checksum and write protection. The CS5484 is designed to interface to a variety of voltage and current sensors including shunt resistors, current transformers, and Rogowski coils.

On-chip functionality makes digital calibration simple and ultra-fast, minimizing the time required at the end of the customer production line. Performance across temperature is ensured with an on-chip voltage reference with low drift. A single 3.3V power supply is required, and power consumption is low at <13mW. To minimize space requirements, the CS5484 is offered in a low-cost, 5mm x 5mm 28-pin QFN package.



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1. OVERVIEW

The CS5484 is a CMOS power measurement integrated circuit using four ΔΣ analog-to-digital converters to measure two line voltages and two currents. Optionally, voltage2 channel can be used for temperature measurement. It calculates active, reactive, and apparent power as well as RMS voltage and current and peak voltage and current. It handles other system-related functions, such as energy pulse generation, voltage sag and swell, overcurrent and zero-crossing detection, and line frequency measurement.

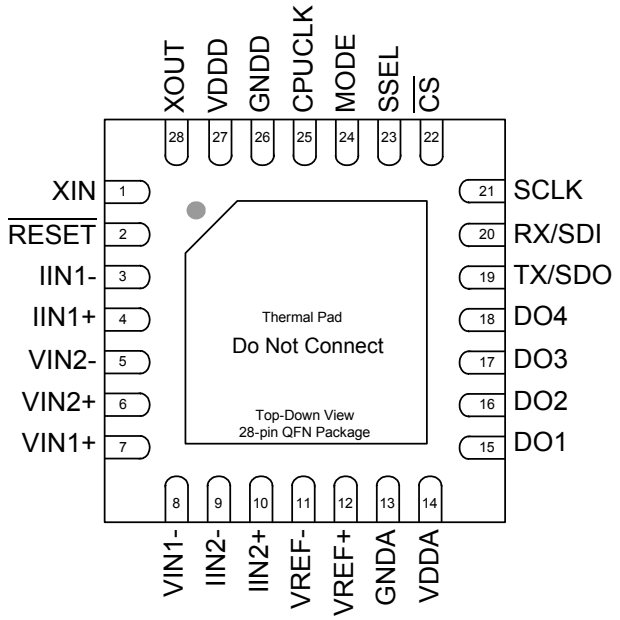
The CS5484 is optimized to interface to current transformers, shunt resistors, or Rogowski coils for current measurement and to resistive dividers or voltage transformers for voltage measurement. Two full-scale ranges are provided on the current inputs to accommodate different types of current sensors. The CS5484's four differential inputs have a common-mode input range from analog ground (GNDA) to the positive analog supply (VDDA).

An on-chip voltage reference (typically 2.4 volts) is generated and provided at analog output, VREF±.

Four digital outputs (DO1, DO2, DO3, and DO4) provide a variety of output signals, and depending on the mode selected, provide energy pulses, zero-crossings, or other choices.

The CS5484 includes a UART/SPI™ serial host interface to an external microcontroller. The serial select (SSEL) pin is used to configure the serial port to be a SPI or UART. SPI signals include serial data input (SDI), serial data output (SDO), and serial clock (SCLK). UART signals include serial data input (RX) and serial data output (TX). A chip select ($\overline{CS}$) signal allows multiple CS5484s to share the same serial interface with the microcontroller.

2. PIN DESCRIPTIONS



Digital Pins and Serial Data I/O		
Digital Outputs	15,16, 17,18	**DO1, DO2, DO3, DO4** — Configurable digital outputs for energy pulses, interrupt, energy direction, and zero-crossings.
Reset	2	**$\overline{\text{RESET}}$** — An active-low Schmitt-trigger input used to reset the chip.
Serial Data I/O	19,20	**TX/SDO, RX/SDI** — UART/SPI serial data output/input.
Serial Clock Input	21	**SCLK** — Serial clock for the SPI.
Chip Select	22	**$\overline{\text{CS}}$** — Chip select for the UART/SPI.
Serial Mode Select	23	**SSEL** — Selects the type of serial interface, UART or SPI™. Logic level one - UART selected. Logic level zero - SPI selected.
Operating Mode Select	24	**MODE** — Connect to VDDA for proper operation.
Analog Inputs/Outputs		
Voltage Inputs	7,8,6,5	**VIN1+, VIN1-, VIN2+, VIN2-** — Differential analog inputs for the voltage channels.
Current Inputs	4,3,10,9	**IIN1+, IIN1-, IIN2+, IIN2-** — Differential analog inputs for the current channels.
Voltage Reference Input	12,11	**VREF+, VREF-** — The internal voltage reference. A 0.1µF bypass capacitor is required between these two pins.
Power Supply Connections		
Internal Digital Supply	27	**VDDD** — Decoupling pin for the internal 1.8V digital supply. A 0.1µF bypass capacitor is required between this pin and GNDD.
Digital Ground	26	**GNDD** — Digital ground.
Positive Analog Supply	14	**VDDA** — The positive 3.3V analog supply.
Analog Ground	13	**GNDA** — Analog ground.
Clock Generator		
Crystal In Crystal Out	1,28	**XIN, XOUT** — Connect to an external quartz crystal. Alternatively, an external clock can be supplied to the XIN pin to provide the system clock for the device.
CPU Clock Output	25	**CPUCLK** — Output of on-chip oscillator which can drive one standard CMOS load.
Thermal Pad	-	No Electrical Connection.

2.1 Analog Pins

The CS5484 has two differential inputs (VIN1±, VIN2±) for voltage input and two differential inputs (IIN1±, IIN2±) for current1 and current2 inputs. The CS5484 also has two voltage reference pins (VREF±) between which a bypass capacitor should be placed.

2.1.1 Voltage Inputs

The output of the line voltage resistive divider or transformer is connected to the VIN1± or VIN2± input pins of the CS5484. The voltage channel is equipped with a 10x, fixed-gain amplifier. The full-scale signal level that can be applied to the voltage channel is ±250mV. If the input signal is a sine wave, the maximum RMS voltage is $250\text{mVp}/\sqrt{2} \approx 176.78\text{mV}_{RMS}$, which is approximately 70.7% of maximum peak voltage.

2.1.2 Current Inputs

The output of the current-sensing shunt resistor, transformer, or Rogowski coil is connected to the IIN1± or IIN2± input pins of the CS5484. To accommodate different current-sensing elements, the current channel incorporates a programmable gain amplifier (PGA) with two selectable input gains, as described in the *Config0* register description (see section *6.6.1 Configuration 0 (Config0) – Page 0, Address 0* on page 35.) There is a 10x gain setting and a 50x gain setting. The full-scale signal level for current channels is ±50mV and ±250mV for 50x and 10x gain settings, respectively. If the input signal is a sine wave, the maximum RMS voltage is 35.35mV_{RMS} or 176.78mV_{RMS}, which is approximately 70.7% of maximum peak voltage.

2.1.3 Voltage Reference

The CS5484 generates a stable voltage reference of 2.4V between the VREF± pins. The reference system also requires a filter capacitor of at least 0.1µF between the VREF± pins.

The reference system is capable of providing a reference for the CS5484 but has limited ability to drive external circuitry. It is strongly recommended that nothing other than the required filter capacitor be connected to the VREF± pins.

2.1.4 Crystal Oscillator

An external, 4.096MHz quartz crystal can be connected to the XIN and XOUT pins, as shown in Figure 1. To reduce system cost, each pin is supplied with an on-chip load capacitor.

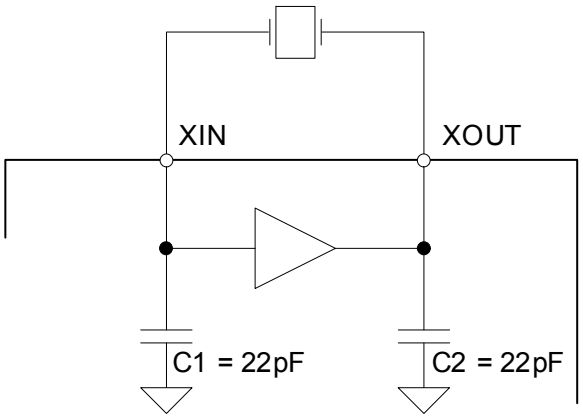


Figure 1. Oscillator Connections

Alternatively, an external clock source can be connected to the XIN pin.

2.2 Digital Pins

2.2.1 Reset Input

The active-low $\overline{\text{RESET}}$ pin, when asserted for longer than 120µs, will halt all CS5484 operations and reset internal hardware registers and states. When de-asserted, an initialization sequence begins, setting default register values. To prevent erroneous noise-induced resets to the CS5484, an external pull-up resistor and a decoupling capacitor are necessary on the $\overline{\text{RESET}}$ pin.

2.2.2 CPU Clock Output

A logic-level clock output (CPUCLK) is provided at the crystal frequency to drive another CS5484 IC or external microcontroller. Writing '1' to bit CPUCLK_ON of the *Config0* register enables the CPU clock output. After the CPU clock output is enabled, it can be disabled only by a power-on reset (POR) or by writing '0' to the CPUCLK_ON bit. A hardware reset through pin/RESET or a software reset instruction through the serial interface will not disable the CPU clock output. Two phase choices are available on the CPUCLK pin through bit iCPUCLK of the *Config0* register. Different from the CPUCLK_ON bit, the iCPUCLK bit can be cleared by a POR, a hardware reset, a software reset instruction, or a register write.

2.2.3 Digital Outputs

The CS5484 provides four configurable digital outputs (DO1-DO4). They can be configured to output energy pulses, interrupt, zero-crossings, or energy directions. Refer to section *6.6.2 Configuration 1 (Config1) – Page 0, Address 1* on page 36 for more details.

2.2.4 UART/SPI™ Serial Interface

The CS5484 provides five pins—SSEL, RX/SDI, TX/SDO, $\overline{CS}$, and SCLK—for communication between a host microcontroller and the CS5484.

SSEL is an input that, when low, indicates to the CS5484 to use the SPI port as the serial interface to communicate with the host microcontroller. The SSEL pin has an internal weak pull-up. When the SSEL pin is left unconnected or pulled high externally, the UART port is used as the serial interface.

2.2.5 SPI

The CS5484 provides a Serial Peripheral Interface (SPI) that operates as a slave device in 4-wire mode and supports multiple slaves on the SPI bus. The 4-wire SPI includes $\overline{CS}$, SCLK, SDI, and SDO signals.

$\overline{CS}$ is the chip select input for the CS5484 SPI port. A high logic level de-asserts it, tri-stating the SDO pin and clearing the SPI interface. A low logic level enables the SPI port. Although the $\overline{CS}$ pin may be tied low for systems that do not require multiple SDO drivers, using the $\overline{CS}$ signal is strongly recommended to achieve more reliable SPI communications.

SCLK is the serial clock input for the CS5484 SPI port. Serial data changes as a result of the falling edge of SCLK and is valid at the rising edge. The SCLK pin is a Schmitt-trigger input.

SDI is the serial data input to the CS5484.

SDO is the serial data output from the CS5484.

The CS5484 SPI transmits and receives data MSB first. Refer to *Switching Characteristics* on page 14 and Figure 7 on page 15 for more detailed information about SPI timing.

2.2.6 UART

The CS5484 device contains an asynchronous, full-duplex UART. The UART may be used in either standard 2-wire communication mode (RX/TX) for connecting a single device or 3-wire communication mode (RX/TX/$\overline{CS}$) for connecting multiple devices. When connecting a single CS5484 device, $\overline{CS}$ should be held low to enable the UART. Multiple CS5484 devices can communicate to the same master UART in the 3-wire mode by pulling a slave $\overline{CS}$ pin low during data transmissions. Common RX and TX signals are provided to all the slave devices, and each slave device requires a separate $\overline{CS}$ signal for enabling communication to that slave. The multi-device UART mode connections are shown in Figure 2.

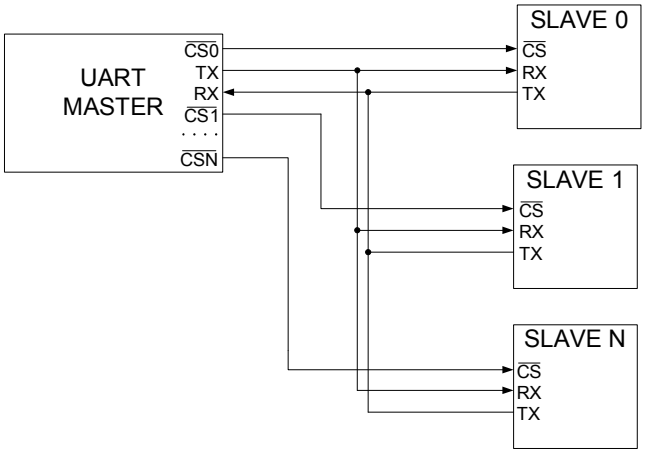


Figure 2. Multi-device UART Connections

The multi-device UART mode timing diagram provides the timing requirements for the $\overline{CS}$ control (see Figure 8. Multi-Device UART Timing on Page 15).

The CS5484 UART operates in 8-bit mode, which transmits a total of 10 bits per byte. Data is transmitted and received LSB first, with one start bit, eight data bits, and one stop bit.

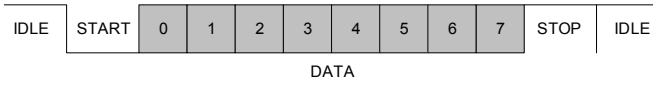


Figure 3. UART Serial Frame Format

The baud rate is defined in the *SerialCtrl* register. After chip reset, the default baud rate is 600, if MCLK is 4.096 MHz. The baud rate is based on the contents of bits BR[15:0] in the *SerialCtrl* register and is calculated as follows:

$$BR[15:0] = \text{Baud Rate} \times (524288 / MCLK)$$

or

$$\text{Baud Rate} = BR[15:0] / (524288 / MCLK)$$

The maximum baud rate is 512K if MCLK is 4.096 MHz.

2.2.7 MODE Pin

The MODE pin must be tied to VDDA for normal operation. The MODE pin is used primarily for factory test procedures.

3. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Positive Analog Power Supply	VDDA	3.0	3.3	3.6	V
Specified Temperature Range	T_A	-40	-	+85	°C

POWER MEASUREMENT CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Active Energy (Note 1 and 2)	All Gain Ranges Current Channel Input Signal Dynamic Range 4000:1	P_{Avg}	-	±0.1	-	%
Reactive Energy (Note 1 and 2)	All Gain Ranges Current Channel Input Signal Dynamic Range 4000:1	Q_{Avg}	-	±0.1	-	%
Apparent Power (Note 1 and 3)	All Gain Ranges Current Channel Input Signal Dynamic Range 1000:1	S	-	±0.1	-	%
Current RMS (Note 1, 3, and 4)	All Gain Ranges Current Channel Input Signal Dynamic Range 1000:1	I_{RMS}	-	±0.1	-	%
Voltage RMS (Note 1 and 3)	Voltage Channel Input Signal Dynamic Range 20:1	V_{RMS}	-	±0.1	-	%
Power Factor (Note 1 and 3)	All Gain Ranges Current Channel Input Signal Dynamic Range 1000:1	PF	-	±0.1	-	%

Notes:
1. Specifications guaranteed by design and characterization.
2. Active energy is tested with power factor (PF) = 1.0. Reactive energy is tested with Sin(φ) = 1.0. Energy error measured at system level using a single energy pulse. Where: 1) One energy pulse = 0.5Wh or 0.5Varh; 2) VDDA = +3.3V, T_A = 25°C, MCLK = 4.096MHz; 3) System is calibrated.
3. Calculated using register values; N≥4000.
4. I_{RMS} error calculated using register values. 1) VDDA = +3.3V; T_A = 25°C; MCLK = 4.096MHz; 2) AC offset calibration applied.

TYPICAL LOAD PERFORMANCE

- Energy error measured at system level using single energy pulse; where one energy pulse = 0.5Wh or 0.5Varh
- I_{RMS} error calculated using register values
- VDDA = +3.3V; T_A = 25°C; MCLK = 4.096MHz

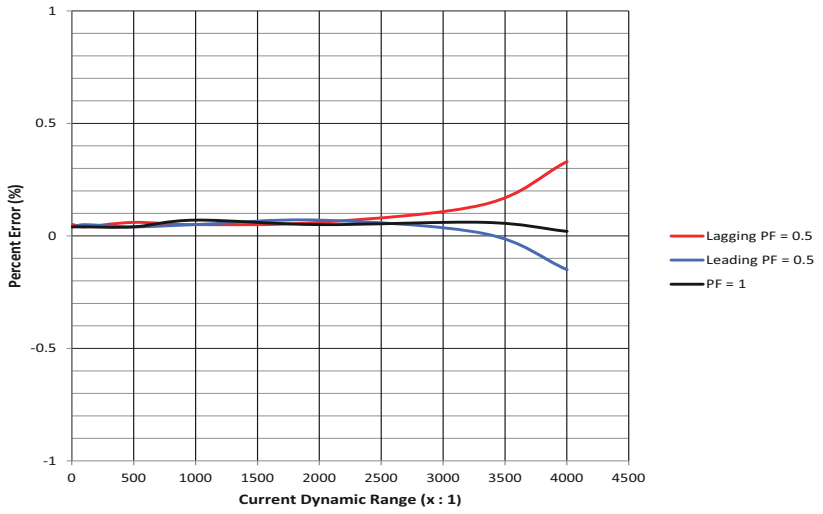


Figure 4. Active Energy Load Performance

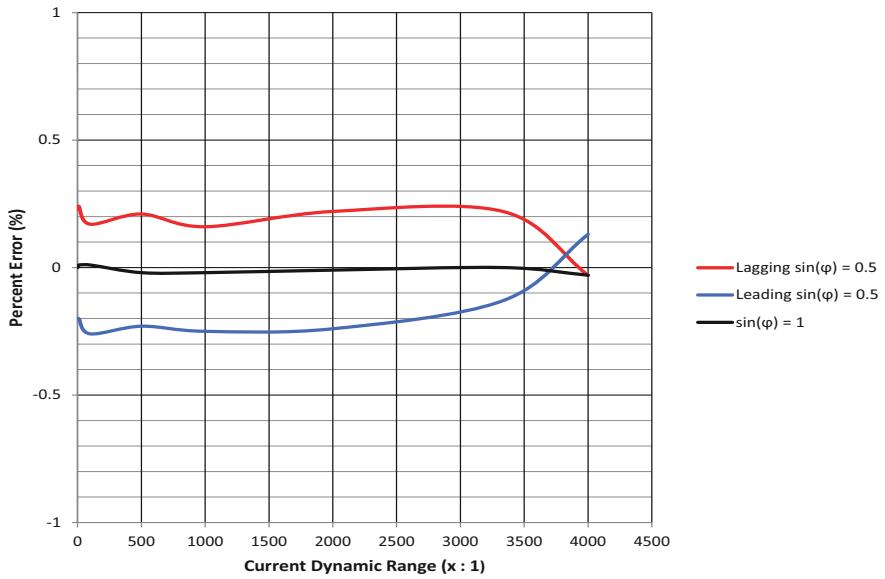


Figure 5. Reactive Energy Load Performance

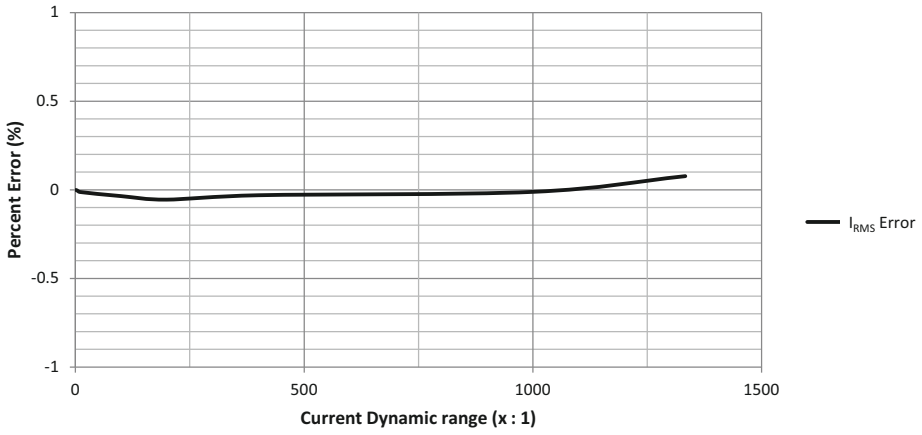


Figure 6. I_{RMS} Load Performance

ANALOG CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all Recommended Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and T_A = 25°C.
- VDDA = +3.3V ±10%; GNDA = GNDD = 0V. All voltages with respect to 0V.
- MCLK = 4.096MHz.

Parameter		Symbol	Min	Typ	Max	Unit
Analog Inputs (Current Channels)						
Common Mode Rejection	(DC, 50, 60Hz)	CMRR	80	-	-	dB
Common Mode+Signal			-0.25	-	VDDA	V
Differential Full-scale Input Range [(IIN+) – (IIN-)]	(Gain = 10) (Gain = 50)	IIN	- -	250 50	- -	mV_P mV_P
Total Harmonic Distortion	(Gain = 50)	THD	90	100	-	dB
Signal-to-Noise Ratio (SNR)	(Gain = 10) (Gain = 50)	SNR	- -	80 80	- -	dB dB
Crosstalk from Voltage Inputs at Full Scale	(50, 60Hz)		-	-115	-	dB
Crosstalk from Current Input at Full Scale	(50, 60Hz)		-	-115	-	dB
Input Capacitance		IC	-	27	-	pF
Effective Input Impedance		EII	30	-	-	kΩ
Offset Drift (Without the High-pass Filter)		OD	-	4.0	-	µV/°C
Noise (Referred to Input)	(Gain = 10) (Gain = 50)	N_I	- -	15 3.5	- -	$µV_{RMS}$ $µV_{RMS}$
Power Supply Rejection Ratio (Note 7)	(60Hz) (Gain = 10) (Gain = 50)	PSRR	 60 68	 65 75	 - -	 dB dB
Analog Inputs (Voltage Channels)						
Common Mode Rejection	(DC, 50, 60Hz)	CMRR	80	-	-	dB
Common Mode+Signal			-0.25	-	VDDA	V
Differential Full-scale Input Range	[(VIN+) – (VIN-)]	VIN	-	250	-	mV_P
Total Harmonic Distortion		THD	80	88	-	dB
Signal-to-Noise Ratio (SNR)		SNR	-	73	-	dB
Crosstalk from Current Inputs at Full Scale	(50, 60Hz)		-	-115	-	dB
Input Capacitance		IC	-	2.0	-	pF
Effective Input Impedance		EII	2	-	-	MΩ
Noise (Referred to Input)		N_V	-	40	-	$µV_{RMS}$
Offset Drift (Without the High-pass Filter)		OD	-	16.0	-	µV/°C
Power Supply Rejection Ratio (Note 7)	(60Hz) (Gain = 10)	PSRR	60	65	-	dB
Temperature						
Temperature Accuracy	(Note 6)	T	-	±5	-	°C

Parameter		Symbol	Min	Typ	Max	Unit
Power Supplies						
Power Supply Currents (Active State)	I_{A+} (VDDA = +3.3V)	PSCA	-	3.9	-	mA
Power Consumption (Note 5)	Active State (VDDA = +3.3V)	PC	-	12.9	-	mW
	Stand-by State		-	4.5	-	mW

Notes:
5. All outputs unloaded. All inputs CMOS level.
6. Temperature accuracy measured after calibration is performed.
7. Measurement method for PSRR: VDDA = +3.3V, a 150mV (zero-to-peak) (60Hz) sine wave is imposed onto the +3.3V DC supply voltage at the VDDA pin. The "+" and "-" input pins of both input channels are shorted to GNDA. The CS5484 is then commanded to continuous conversion acquisition mode, and digital output data is collected for the channel under test. The (zero-to-peak) value of the digital sinusoidal output signal is determined, and this value is converted into the (zero-to-peak) value of the sinusoidal voltage (measured in mV) that would need to be applied at the channel's inputs in order to cause the same digital sinusoidal output. This voltage is then defined as V_{eq} PSRR is (in dB):

$$PSRR = 20 \cdot \log\left[\frac{150}{V_{eq}}\right]$$

VOLTAGE REFERENCE

Parameter		Symbol	Min	Typ	Max	Unit
Reference	(Note 8)					
Output Voltage		VREF	+2.3	+2.4	+2.5	V
Temperature Coefficient	(Note 9)	TC_{VREF}	-	25	-	ppm/°C
Load Regulation	(Note 10)	ΔV_R	-	30	-	mV

Notes:
8. It is strongly recommended that no connection other than the required filter capacitor be made to VREF±.
9. The voltage at VREF± is measured across the temperature range. From these measurements the following formula is used to calculate the VREF temperature coefficient:

$$TC_{VREF} = \left(\frac{VREF_{MAX} - VREF_{MIN}}{VREF_{AVG}}\right)\left(\frac{1}{T_A MAX - T_A MIN}\right)(1.0 \times 10^6)$$

10. Specified at maximum recommended output of 1µA sourcing. VREF is a sensitive signal; the output of the VREF circuit has a high output impedance so that the 0.1µF reference capacitor provides attenuation even to low-frequency noise, such as 50Hz noise on the VREF output. Therefore VREF intended for the CS5484 only and should not be connected to any external circuitry. The output impedance is sufficiently high that standard digital multi-meters can significantly load this voltage. The accuracy of the metrology IC cannot be guaranteed when a multimeter or any component other than the 0.1µF capacitor is attached to VREF. If it is desired to measure VREF for any reason other than a very course indicator of VREF functionality, Cirrus recommends a very high input impedance multimeter such as the Keithley Model 2000 Digital Multimeter be used. Cirrus cannot guarantee the accuracy of the metrology with this meter connected to VREF.

DIGITAL CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all Recommended Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and T_A = 25°C.
- VDDA = +3.3V ±10%; GNDA = GNDD = 0V. All voltages with respect to 0V.
- MCLK = 4.096MHz.

Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Characteristics						
XIN Clock Frequency	Internal Gate Oscillator	MCLK	2.5	4.096	5	MHz
Filter Characteristics						
Phase Compensation Range	(60Hz, OWR = 4000Hz)		-10.79	-	+10.79	°
Input Sampling Rate			-	MCLK/8	-	Hz
Digital Filter Output Word Rate	(Both channels)	OWR	-	MCLK/1024	-	Hz
High-pass Filter Corner Frequency	-3dB		-	2.0	-	Hz
Input/Output Characteristics						
High-level Input Voltage (All Pins)		V_{IH}	0.6(VDDA)	-	-	V
Low-level Input Voltage (All Pins)		V_{IL}	-	-	0.6	V
High-level Output Voltage (Note 12)	DO1-DO4, I_{out} = +10mA All Other Outputs, I_{out} = +5mA	V_{OH}	VDDA-0.3 VDDA-0.3	- -	- -	V V
Low-level Output Voltage (Note 12)	DO1-DO4, I_{out} = -12mA All Other Outputs, I_{out} = -5mA	V_{OL}	- -	- -	0.5 0.5	V V
Input Leakage Current		I_{in}	-	±1	±10	µA
3-state Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	5	-	pF

Notes: 11. All measurements performed under static conditions.
12. XOUT pin used for crystal only. Typical drive current<1mA.

SWITCHING CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all Recommended Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and T_A = 25°C.
- VDDA = +3.3V ±10%; GNDA = GNDD = 0V. All voltages with respect to 0V.
- Logic Levels: Logic 0 = 0V, Logic 1 = VDDA.

Parameter		Symbol	Min	Typ	Max	Unit
Rise Times (Note 13)	DO1-DO4 Any Digital Output Except DO1-DO4	t_{rise}	- -	- 50	1.0 -	µs ns
Fall Times (Note 13)	DO1-DO4 Any Digital Output Except DO1-DO4	t_{fall}	- -	- 50	1.0 -	µs ns
Start-up						
Oscillator Start-up Time	XTAL = 4.096 MHz (Note 14)	t_{ost}	-	60	-	ms
SPI Timing						
Serial Clock Frequency	(Note 15)	SCLK	-	-	2	MHz
Serial Clock	Pulse Width High Pulse Width Low	t_1 t_2	200 200	- -	- -	ns ns
$\overline{CS}$ Enable to SCLK Falling		t_3	50	-	-	ns
Data Set-up Time prior to SCLK Rising		t_4	50	-	-	ns
Data Hold Time After SCLK Rising		t_5	100	-	-	ns
SCLK Rising Prior to $\overline{CS}$ Disable		t_6	1	-	-	µs
SCLK Falling to New Data Bit		t_7	-	-	150	ns
$\overline{CS}$ Rising to SDO Hi-Z		t_8	-	-	250	ns
UART Timing						
$\overline{CS}$ Enable to RX START bit		t_9	5	-	-	ns
STOP bit to $\overline{CS}$ Disable		t_{10}	1	-	-	µs
$\overline{CS}$ Disable to TX IDLE Hold Time		t_{11}	-	-	250	ns

Notes:
13. Specified using 10% and 90% points on waveform of interest. Output loaded with 50pF.
14. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.
15. The maximum SCLK is 2MHz during a byte transaction. The minimum 1µs idle time is required on the SCLK between two consecutive bytes.

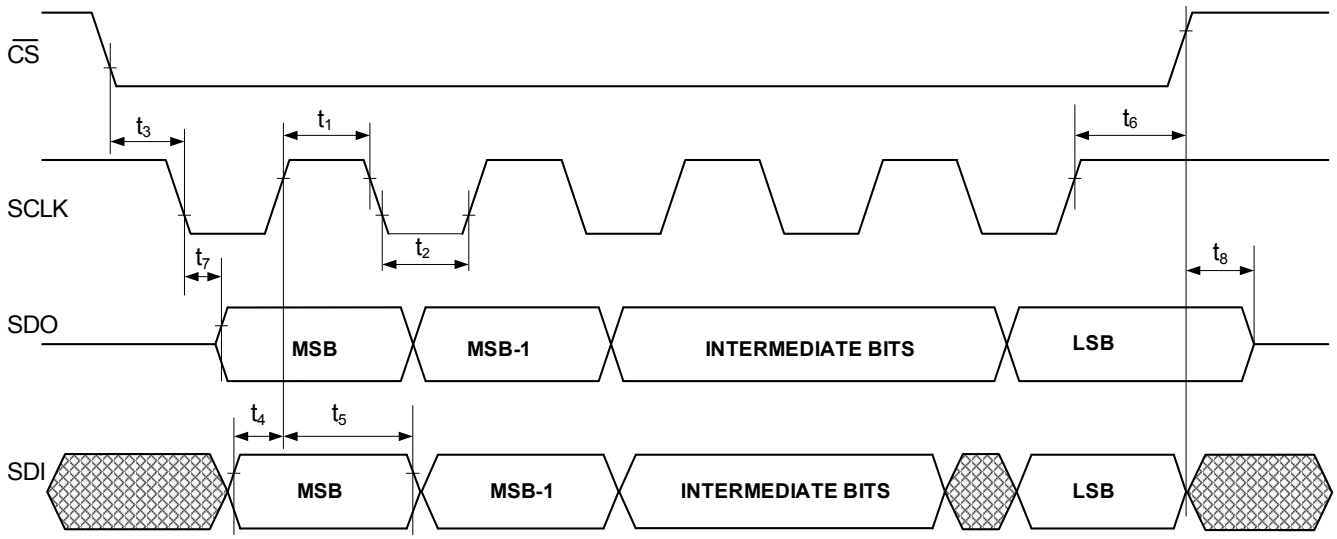


Figure 7. SPI Data and Clock Timing

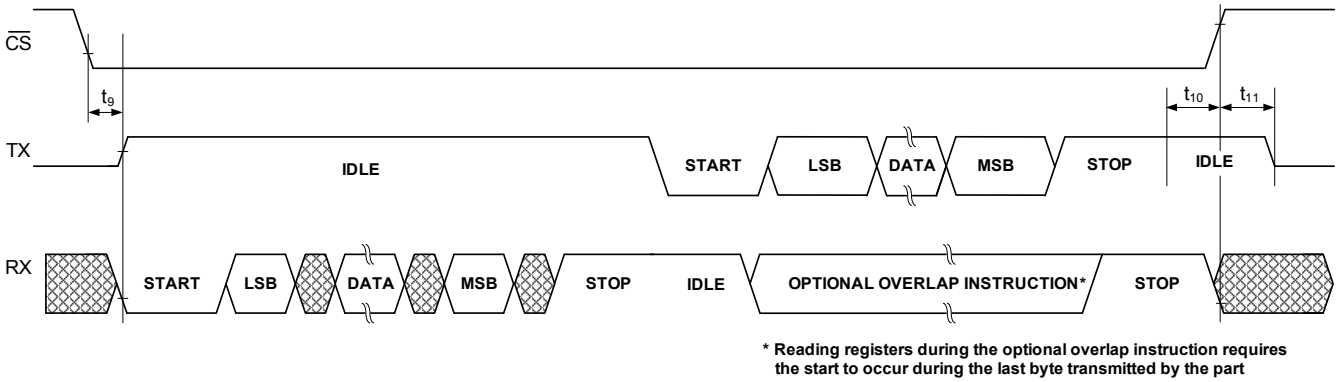


Figure 8. Multi-Device UART Timing

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	(Note 16)	VDDA	-0.3	-	+4.0	V
Input Current	(Notes 17 and 18)	I_{IN}	-	-	±10	mA
Input Current for Power Supplies		-	-	-	±50	-
Output Current	(Note 19)	I_{OUT}	-	-	100	mA
Power Dissipation	(Note 20)	P_D	-	-	500	mW
Input Voltage	(Note 21)	V_{IN}	-0.3	-	(VDDA) + 0.3	V
Junction-to-Ambient Thermal Impedance	2 Layer Board 4 Layer Board	θ_{JA}	- -	53 43	- -	°C/W °C/W
Ambient Operating Temperature		T_A	-40	-	85	°C
Storage Temperature		T_{stg}	-65	-	150	°C

Notes:
16. VDDA and GNDA must satisfy [(VDDA) – (GNDA)] ≤ + 4.0 V.
17. Applies to all pins, including continuous overvoltage conditions at the analog input pins.
18. Transient current of up to 100 mA will not cause SCR latch-up.
19. Applies to all pins, except VREF±.
20. Total power dissipation, including all input currents and output currents.
21. Applies to all pins.

WARNING:

Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

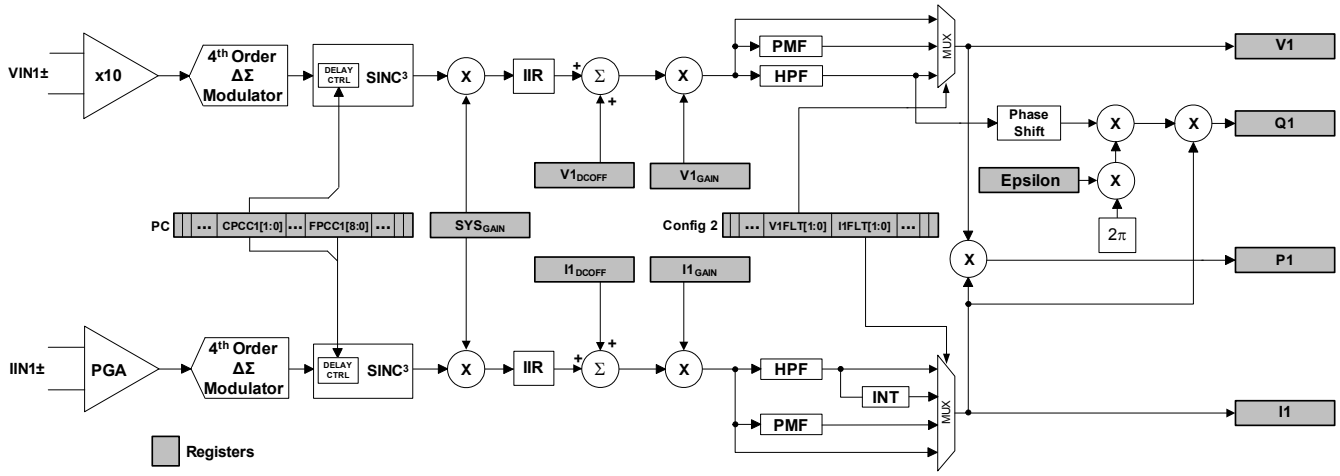


Figure 9. Signal Flow for V1, I1, P1, and Q1 Measurements

4. SIGNAL FLOW DESCRIPTION

The signal flow for voltage measurement, current measurement, and the other calculations is shown in Figures 9, 10, and 11.

The signal flow consists of two current channels and two voltage channels. The current and voltage channels have differential input pins.

4.1 Analog-to-Digital Converters

All four input channels use fourth-order delta-sigma modulators to convert the analog inputs to single-bit digital data streams. The converters sample at a rate of MCLK/8. This high sampling provides a wide dynamic range and simplifies anti-alias filter design.

4.2 Decimation Filters

The single-bit modulator output data is widened to 24 bits and down sampled to MCLK/1024 with low-pass decimation filters. These decimation filters are third-order Sinc filters. The filter outputs pass through an IIR "anti-sinc" filter.

4.3 IIR Filters

The IIR filters are used to compensate for the amplitude roll-off of the decimation filters. The droop-correction filter flattens the magnitude response of the channel out to the Nyquist frequency, thus allowing for accurate measurements of up to 2 kHz (MCLK = 4.096 MHz). By default, the IIR filters are enabled. The IIR filters can be bypassed by setting the IIR_OFF bit in the *Config2* register.

4.4 Phase Compensation

Phase compensation changes the phase of voltage relative to current by adding a delay in the decimation filters. The amount of phase shift is set by the PC register bits CPCCx[1:0] and FPCCx[8:0] for current channels. Bits CPCCx[1:0] set the delay for the voltage channels.

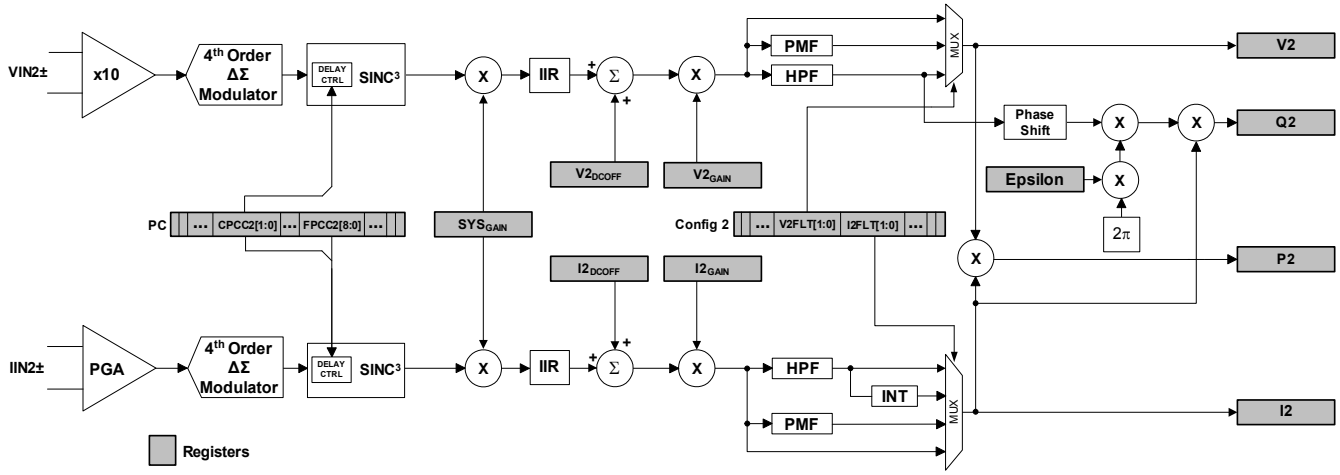


Figure 10. Signal Flow for V2, I2, P2, and Q2 Measurements

Fine phase compensation control bits, FPCCx[8:0], provide up to 1/OWR delay in the current channel. Coarse phase compensation control bits, CPCCx[1:0], provide an additional 1/OWR delay in the current channels or up to 2/OWR delay in the voltage channel. Negative delay in the voltage channel can be implemented by setting longer delay in the current channel than the voltage channel. For a OWR of 4000 Hz, the delay range is ±500 µs, a phase shift of ±8.99° at 50 Hz and ±10.79° at 60 Hz. The step size is 0.008789° at 50 Hz and 0.010547° at 60 Hz.

4.5 DC Offset and Gain Correction

The system and CS5484 inherently have component tolerances, gain, and offset errors, which can be removed using the gain and offset registers. Each measurement channel has its own set of gain and offset registers. For every instantaneous voltage and current sample, the offset and gain values are used to correct DC offset and gain errors in the channel (see section *7. System Calibration* on page 62 for more details).

4.6 High-pass and Phase Matching Filters

Optional high-pass filters (HPF in Figures 9 and 10) remove any DC component from the selected signal paths. Each power calculation contains a current and voltage channel. If an HPF is enabled in only one channel, a phase-matching filter (PMF) should be applied to the other channel to match the phase response of the HPF. For AC power measurement, high-pass filters should be enabled on the voltage and current channels. For information about how to enable and disable the HPF or PMF on each channel, refer to section *6.6.3 Configuration 2 (Config2) – Page 16, Address 0* on page 38.

4.7 Digital Integrators

Optional digital integrators (INT in Figures 9 and 10) are implemented on both current channels (I1, I2) to compensate for the 90º phase shift and 20 dB/decade gain generated by the Rogowski coil current sensor. When a Rogowski coil is used as the current sensor, the integrator (INT) should be enabled on that current channel. For information about how to enable and disable the INT on each current channel, refer to section *6.6.3 Configuration 2 (Config2) – Page 16, Address 0* on page 38.

4.8 Low-rate Calculations

All the RMS and power results come from low-rate calculations by averaging the output word rate (OWR) instantaneous values over *N* samples, where *N* is the value stored in the *SampleCount* register. The low-rate interval or averaging period is *N* divided by OWR (4000 Hz if MCLK = 4.096 MHz).

The CS5484 provides two averaging modes for low-rate calculations: Fixed Number of Samples Averaging mode and Line-cycle Synchronized Averaging mode. By default, the CS5484 averages with the Fixed Number of Samples Averaging mode. By setting the AVG_MODE bit in the *Config2* register, the CS5484 will use the Line-cycle Synchronized Averaging mode.

4.8.1 Fixed Number of Samples Averaging

N is the preset value in the *SampleCount* register and should not be set less than 100. By default, the *SampleCount* is 4000. With MCLK = 4.096 MHz, the averaging period is fixed at N/4000 = 1 second, regardless of the line frequency.

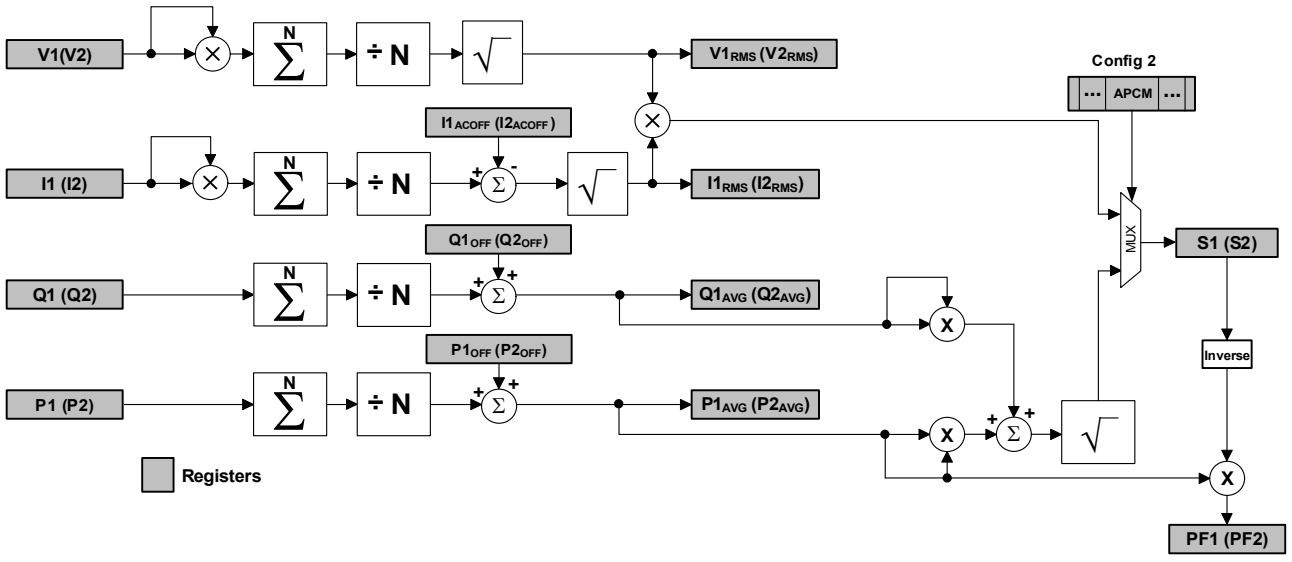


Figure 11. Low-rate Calculations

4.8.2 Line-cycle Synchronized Averaging

When operating in Line-cycle Synchronized Averaging mode, and when line frequency measurement is enabled (see section *5.4 Line Frequency Measurement* on page 22), the CS5484 uses the voltage (V) channel zero crossings and measured line frequency to automatically adjust *N* such that the averaging period will be equal to the number of half line-cycles in the *CycleCount* register. For example, if the line frequency is 51 Hz, and the *CycleCount* register is set to 100, *N* will be $4000 \times (100/2)/51 = 3921$ during continuous conversion. *N* is self-adjusted according to the line frequency, therefore the averaging period is always close to the whole number of half line-cycles, and the low-rate calculation results will minimize ripple and maximize resolution, especially when the line frequency varies. Before starting a low-rate conversion in the Line-cycle Synchronized Averaging mode, the *SampleCount* register should not be changed from its default value of 4000, and bit AFC of the *Config2* register must be set. During continuous conversion, the host processor should not change the *SampleCount* register.

4.8.3 RMS Current and Voltage

The root mean square (*RMS* in Figure 11) calculations are performed on *N* instantaneous current and voltage samples using Equation 1:

$$RMS = \sqrt{\frac{\sum_{n=0}^{N-1} I_n^2}{N}} \qquad V_{RMS} = \sqrt{\frac{\sum_{n=0}^{N-1} V_n^2}{N}} \qquad \text{[Eq: 1]}$$

4.8.4 Active Power

The instantaneous voltage and current samples are multiplied to obtain the instantaneous power (*P1, P2*) (see Figures 9 and 10). The product is then averaged over *N* samples to compute active power (*P1AVG, P2AVG*).

4.8.5 Reactive Power

Instantaneous reactive power (*Q1, Q2*) are sample rate results obtained by multiplying instantaneous current (*I1, I2*) by instantaneous quadrature voltage (*V1Q, V2Q*), which are created by phase shifting instantaneous voltage (*V1, V2*) 90 degrees using first-order integrators (see Figures 9 and 10). The gain of these integrators is inversely related to line frequency, so their gain is corrected by the *Epsilon* register, which is based on line frequency. Reactive power ($Q1_{AVG}$, $Q2_{AVG}$) is generated by integrating the instantaneous quadrature power over *N* samples.

4.8.6 Apparent Power

By default, the CS5484 calculates the apparent power (*S1*, *S2*) as the product of RMS voltage and current, as shown in Equation 2:

$$S = V_{RMS} \times I_{RMS} \qquad \text{[Eq: 2]}$$

The CS5484 also provides an alternate apparent power calculation method. The alternate apparent power method uses real power ($P1_{AVG}$, $P2_{AVG}$) and reactive power ($Q1_{AVG}$, $Q2_{AVG}$) to calculate apparent power. See Equation 3:

$$S = \sqrt{Q_{AVG}^2 + P_{AVG}^2} \qquad \text{[Eq: 3]}$$

The APCM bit in the *Config2* register controls which method is used for apparent power calculation.

4.8.7 Peak Voltage and Current

Peak current ($I1_{PEAK}$, $I2_{PEAK}$) and peak voltage ($V1_{PEAK}$, $V2_{PEAK}$) are calculated over *N* samples and recorded in the corresponding channel peak register documented in the register map. This peak value is updated every *N* samples.

4.8.8 Power Factor

Power factor (*PF1*, *PF2*) is active power divided by apparent power. The sign of the power factor is determined by the active power. See Equation 4:

$$PF = \frac{P_{ACTIVE}}{S} \qquad \text{[Eq: 4]}$$

4.9 Average Active Power Offset

The average active power offset registers, $P1_{OFF}$ ($P2_{OFF}$), can be used to offset erroneous power sources resident in the system not originating from the power line. Residual power offsets are usually caused by crosstalk into current channels from voltage channels, or from ripple on the meter's or chip's power supply, or from inductance from a nearby transformer.

These offsets can be either positive or negative, indicating crosstalk coupling either in phase or out of phase with the applied voltage input. The power offset registers can compensate for either condition.

To use this feature, measure the average power at no load. Take the measured result (from the $P1_{AVG}$ ($P2_{AVG}$) register), invert (negate) the value, and write it to the associated average active power offset register, $P1_{OFF}$ ($P2_{OFF}$).

4.10 Average Reactive Power Offset

The average reactive power offset registers, $Q1_{OFF}$ ($Q2_{OFF}$), can be used to offset erroneous power sources resident in the system not originating from the power line. Residual reactive power offsets are usually caused by crosstalk into current channels from voltage channels, or from ripple on the meter's or chip's power supply, or from inductance from a nearby transformer.

These offsets can be either positive or negative, depending on the phase angle between the crosstalk coupling and the applied voltage. The reactive power offset registers can compensate for either condition. To use this feature, measure the average reactive power at no load. Take the measured result from the $Q1_{AVG}$ ($Q2_{AVG}$) register, invert (negate) the value and write it to the associated reactive power offset register, $Q1_{OFF}$ ($Q2_{OFF}$).

5. FUNCTIONAL DESCRIPTION

5.1 Power-on Reset

The CS5484 has an internal power supply supervisor circuit that monitors the VDDA and VDDD power supplies and provides the master reset to the chip. If any of these voltages are in the reset range, the master reset is triggered.

The CS5484 has dedicated power-on reset (POR) circuits for the analog supply and digital supply. During power-up, both supplies have to be above the rising threshold for the master reset to be de-asserted.

Each POR is divided into two blocks: rough and fine. Rough POR triggers the fine POR. Rough POR depends only on the supply voltage. The trip point for the fine POR is dependent on bandgap voltage for precise control. The POR circuit also acts as a brownout detect. The fine POR detects supply drops and asserts the master reset. The rough and fine PORs have hysteresis in their rise and fall thresholds, which prevents the reset signal from chattering.

Figure 12 shows the POR outputs for each of the power supplies. The POR_Fine_VDDA and POR_Fine_VDDD signals are AND-ed to form the actual power-on reset signal to the digital circuity. The digital circuitry, in turn, holds the master reset signal for 130ms and then de-asserts the master reset.

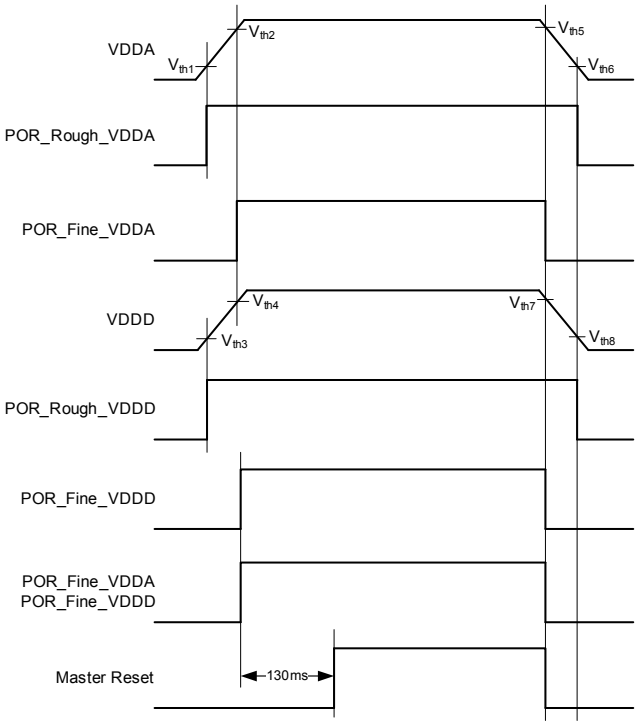


Figure 12. Power-on Reset Timing

Table 1. POR Thresholds

Typical POR Threshold		Rising	Falling
VDDA	Rough	V_{th1} = 2.34V	V_{th6} = 2.06V
	Fine	V_{th2} = 2.77V	V_{th5} = 2.59V
VDDD	Rough	V_{th3} = 1.20V	V_{th8} = 1.06V
	Fine	V_{th4} = 1.51V	V_{th7} = 1.42V

5.2 Power Saving Modes

Power Saving modes for the CS5484 are accessed through the Host Commands (see section *6.1 Host Commands* on page 27).

- Standby: Powers down all the ADCs, rough buffer, and the temperature sensor. Standby mode disables the system time calculations. Use the wake-up command to come out of standby mode.
- Wake-up: Clears the ADC power-down bits and starts the system time calculations.

After any of these commands are completed, the DRDY bit is set in the *Status0* register.

5.3 Zero-crossing Detection

Zero-crossing detection logic is implemented in the CS5484. One current and one voltage channel can be selected for zero-crossing detection. The IZX_CH and VZX_CH control bits in the *Config0* register are used to select the zero-crossing channel. A low-pass filter can be enabled by setting the ZX_LPF bit in register *Config2*. The low-pass filter has a cut-off frequency of 80Hz. It is used to eliminate any harmonics and help the zero-crossing detection on the 50Hz or 60Hz fundamental component. The zero-crossing level registers are used to set the minimum threshold over which the channel peak must exceed in order for the zero-crossing detection logic to function. There are two separate zero-crossing level registers: VZX_{LEVEL} is the threshold for the voltage channels, and IZX_{LEVEL} is the threshold for the current channels.

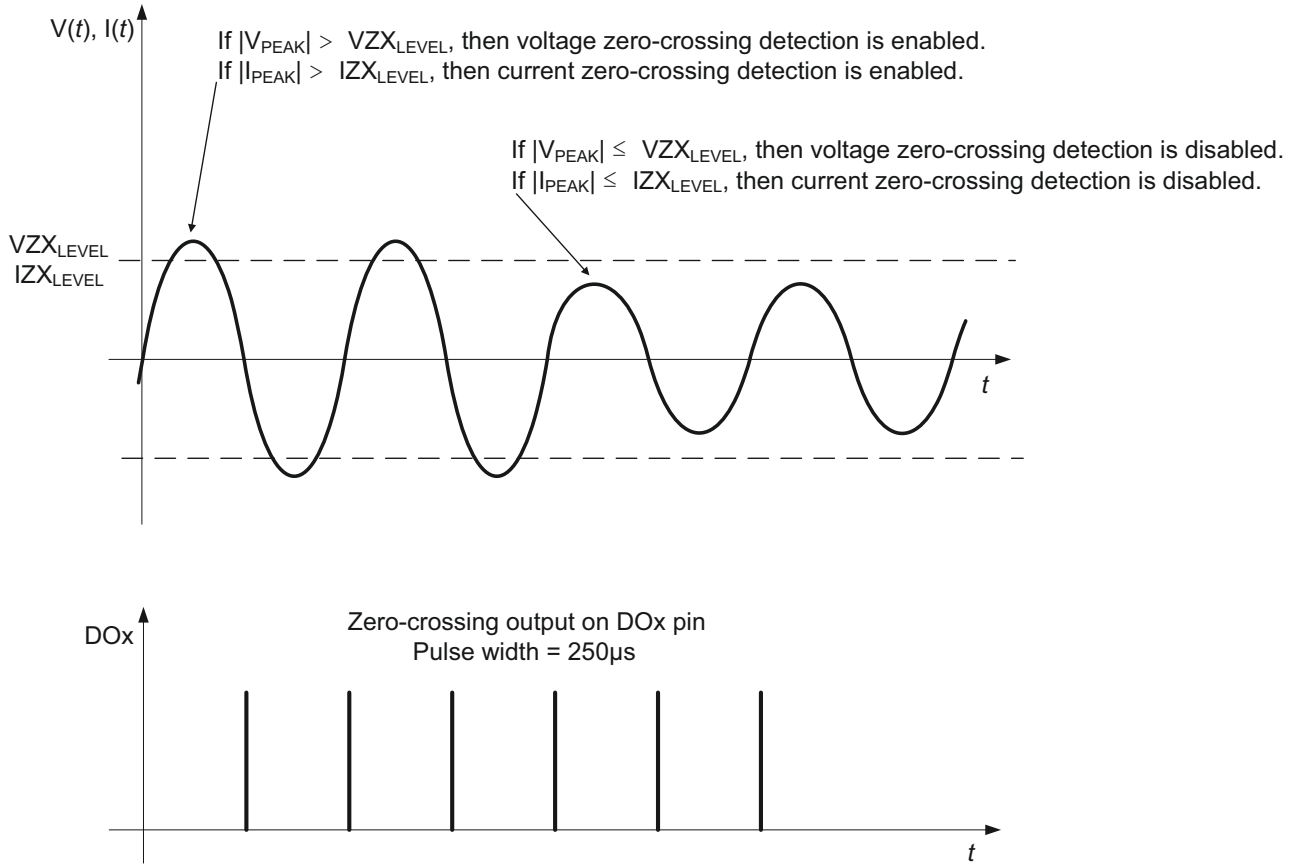


Figure 13. Zero-crossing Level and Zero-crossing Output on DOx

5.4 Line Frequency Measurement

If the Automatic Frequency Calculation (AFC) bit in the *Config2* register is set, the line frequency measurement on the voltage channel will be enabled. The line frequency measurement is based on a number of voltage channel zero crossings. This number is 100 by default and configurable through the ZX_{NUM} register (see section *6.6.76* on page 61). The *Epsilon* register will be updated automatically with the line frequency information. The Frequency Update (FUP) bit in the *Status0* interrupt status register is set when the frequency calculation is completed. When the line frequency is 50 Hz and the ZX_{NUM} register is 100, the *Epsilon* register is updated every one second with a resolution of less than 0.1%. A larger zero-crossing number in the ZX_{NUM} register will increase line frequency measurement resolution and the period. Note that the CS5484 line frequency measurement function does not support the line frequency out of the range of 40 Hz to 75 Hz.

The *Epsilon* register is also used to set the gain of the 90° phase shift filter used in the quadrature power calculation. The value in the *Epsilon* register is the ratio of the line frequency to the output word rate (OWR). For 50 Hz line frequency and 4000 Hz OWR, *Epsilon* is 50/4000 (0.0125) (the default). For 60 Hz line frequency, it is 60/4000 (0.015).

5.5 Energy Pulse Generation

The CS5484 provides four independent energy pulse generation blocks (EPG1, EPG2, EPG3, and EPG4) in order to simultaneously output active, reactive, and apparent energy pulses on any of the four digital output pins (DO1, DO2, DO3, and DO4). The energy pulse frequency is proportional to the magnitude of the power. The energy pulse output is commonly used as the test output of a power meter. The host microcontroller can also use the energy pulses to easily accumulate the energy. Refer to Figure 14.

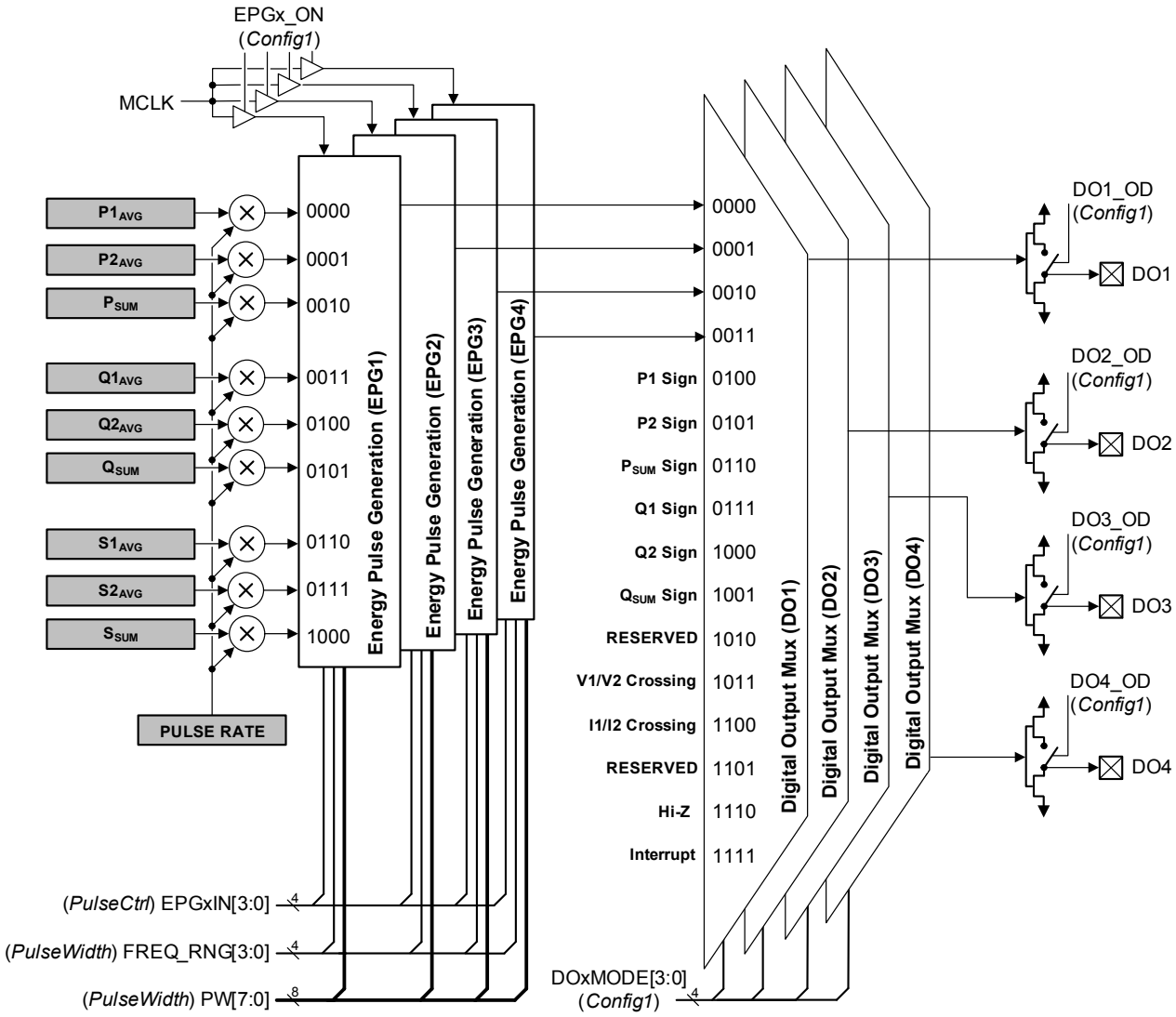


Figure 14. Energy Pulse Generation and Digital Output Control

After reset, all four energy pulse generation blocks are disabled (DOxMODE[3:0] = Hi-Z). To output a desired energy pulse to a DOx pin, it is necessary to follow the steps below:

1. Write to register *PulseWidth* (page 0, address 8) to select the energy pulse width and pulse frequency range.
2. Write to register *PulseRate* (page 18, address 28) to select the energy pulse rate.
3. Write to register *PulseCtrl* (page 0, address 9) to select the input to each energy pulse generation block.
4. Write '1' to bit EPGx_ON of register *Config1* (page 0, address 1) to enable the desired energy pulse generation blocks.
5. Wait at least 0.1 seconds.
6. Write bits DOxMODE[3:0] of register *Config1* to select DOx to output pulses from the appropriate energy pulse generation block.
7. Send DSP instruction (0xD5) to begin continuous conversion.

5.5.1 Pulse Rate

Before configuring the *PulseRate* register, the full-scale pulse rate needs to be calculated and the frequency range needs to be specified through FREQ_RNG[3:0] bits in the *PulseWidth* register. Refer to section *6.6.6 Pulse Output Width (PulseWidth) – Page 0, Address 8* on page 41. The FREQ_RNG[3:0] bits should be set to b[0110]. For example, if a meter has the meter constant of 1000imp/kWh, a maximum voltage (U_{MAX}) of 240V, and a maximum current (I_{MAX}) of 100A, the maximum pulse rate is:

$$[1000 \times (240 \times 100 / 1000)] / 3600 = 6.6667\,\text{Hz}.$$

Assume the meter is calibrated with U_{MAX} and I_{MAX}, and the *Scale* register contains the default value of 0.6. After gain calibration, the power register value will be 0.36, which represents 240x100 = 24kW or 6.6667Hz pulse output rate. The full-scale pulse rate is:

$$F_{out} = 6.6667 / 0.36 = 18.5185\,\text{Hz}.$$

The CS5484 pulse generation block behaves as follows:

- The pulse rate generated by full-scale (1.0decimal) power register is:

$$F_{OUT} = (PulseRate \times 2000) / 2^{FREQ\_RNG}$$

- The *PulseRate* register value is:

$$PulseRate = (F_{OUT} \times 2^{FREQ\_RNG}) / 2000$$
$$= (18.5186 \times 64) / 2000$$
$$= 0.5925952$$
$$= 0x4BDA29$$

5.5.2 Pulse Width

The *PulseWidth* register defines the Active-low time of each energy pulse:

$$\text{Active-low} = 250\,\mu s + (PulseWidth / 64000).$$

By default, the *PulseWidth* register value is 1, and the Active-low time of each energy pulse is 265.6µs. Note that the pulse width should never exceed the pulse period.

5.6 Voltage Sag, Voltage Swell, and Overcurrent Detection

Voltage sag detection is used to determine when the voltage falls below a predetermined level for a specified interval of time (duration). Voltage swell and overcurrent detection determine when the voltage or current rises above a predetermined level for the duration.

The duration is set by the value in the $V1Sag_{DUR}$ ($V2Sag_{DUR}$), $V1Swell_{DUR}$ ($V2Swell_{DUR}$), and $I1Over_{DUR}$ ($I2Over_{DUR}$) registers. Setting any of these to zero (default) disables the detect feature for the given channel. The value is in output word rate (OWR) samples. The predetermined level is set by the values in the $V1Sag_{LEVEL}$ ($V2Sag_{LEVEL}$), $V1Swell_{DUR}$ ($V2Swell_{DUR}$), and $I1Over_{LEVEL}$ ($I2Over_{LEVEL}$) registers.

For each enabled input channel, the measured value is rectified and compared to the associated level register. Over the duration window, the number of samples above and below the level are counted. If the number of samples below the level exceeds the number of samples above, a *Status0* register bit V1SAG (V2SAG) is set, indicating a sag condition. If the number of samples above the level exceeds the number of samples below, a *Status0* register bit V1SWELL (V2SWELL) or I1OVER (I2OVER) is set, indicating a swell or overcurrent condition (see Figure 15).

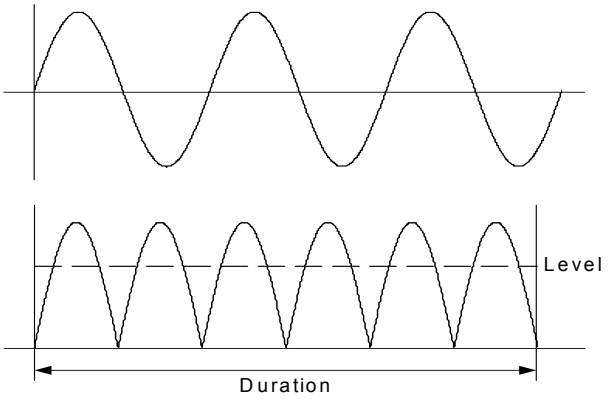


Figure 15. Sag, Swell, and Overcurrent Detect

5.7 Phase Sequence Detection

Polyphase meters using multiple CS5484 devices may be configured to sense the succession of voltage zero-crossings and determine which phase order is in service. The phase sequence detection within CS5484 involves counting the number of OWR samples from a starting point to the next voltage zero-crossing rising edge or falling for each phase. By comparing the count for each phase, the phase sequence can be easily determined: the smallest count is first, and the largest count is last.

The phase sequence detection and control (*PSDC*) register provides the count control, zero-crossing direction and count results. Writing '0' to bit DONE and '10110' to bits CODE[4:0] of the *PSDC* register followed by a falling edge on the RX pin will initiate the phase sequence detection circuit. The RX pin must be held low for a minimum of 500 ns. When the device is in UART mode, it is recommended that a 0xFF command be written to all parts to start the phase sequence detection. This command is ignored by the UART interface and a checksum is not needed. Multiple CS5484 devices in a polyphase meter must receive the register writing and the RX falling edge at the same time so that all CS5484 devices start to count simultaneously. Bit DIR of the *PSDC* register specifies the direction of the next zero-crossing at which the count stops. If bit DIR is '0', the count stops at the next negative-to-positive zero crossing. If bit DIR is '1', the count stops at the next positive-to-negative zero-crossing. When the count stops, the DONE bit will be set by the CS5484, and then the count result of each phase may be read from bits PSCNT[6:0] of the *PSDC* register.

If the PSCNT[6:0] bits are equal to 0x00, 0x7F or greater than 0x64 (for 50 Hz) or 0x50 (for 60 Hz), then a measurement error has occurred, and the measurement results should be disregarded. This could happen when the voltage input signal amplitude is lower than the amplitude specified in the VZX_{LEVEL} register.

To determine the phase order, the PSCNT[6:0] bit count from each CS5484 is sorted in ascending order. Figure 16 and Figure 17 illustrate how phase sequence detection is performed.

Phase sequences A, B, and C for the default rising edge transition are illustrated in Figure 16. The PSCNT[6:0] bits from the CS5484 on phase A will have the lowest count, followed by the PSCNT[6:0] bits from the CS5484 on phase B with the middle count, and the PSCNT[6:0] bits from the CS5484 on phase C with the highest count.

Phase sequences C, B, and A for rising edge transition are illustrated in Figure 17. The PSCNT[6:0] bits from the CS5484 on phase C will have the lowest count, followed by the PSCNT[6:0] bits from the CS5484 on phase B with the middle count, and the PSCNT[6:0] bits from the CS5484 on phase A with the highest count.

5.8 Temperature Measurement

The CS5484 has an internal temperature sensor, which is designed to measure temperature and optionally compensate for temperature drift of the voltage reference. Temperature measurements are stored in the Temperature register (*T*), which, by default, is configured to a range of ±128 degrees on the Celsius (°C) scale.

The application program can change both the scale and range of temperature by changing the Temperature Gain (T_{GAIN}) and Temperature Offset (T_{OFF}) registers.

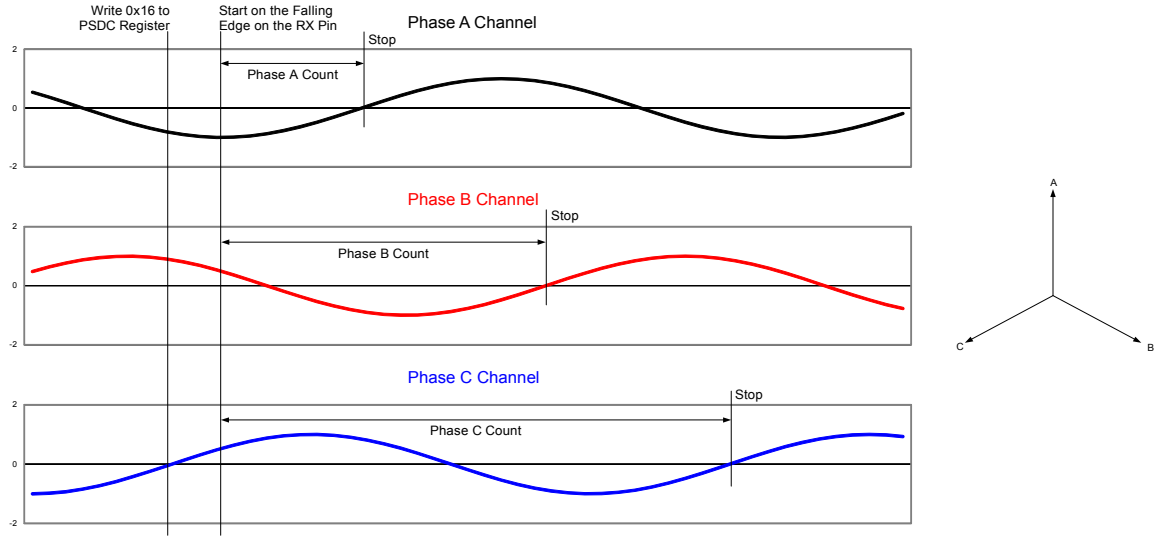


Figure 16. Phase Sequence A, B, C for Rising Edge Transition