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CS5490

Two Channel Energy Measurement IC

Features

- Superior Analog Performance with Ultra-low Noise Level & High SNR
- Energy Measurement Accuracy of 0.1% over a 4000:1 Dynamic Range
- Two Independent 24-bit, 4^{th}-order, Delta-Sigma Modulators for Voltage and Current Measurements
- Configurable Digital Output for Energy Pulses, Interrupt, zero-crossing, and Energy Direction
- Supports Shunt Resistor, CT, and Rogowski Coil Current Sensors
- On-chip Measurements/Calculations:
  - Active, Reactive, and Apparent Power
  - RMS Voltage and Current
  - Power Factor and Line Frequency
  - Instantaneous Voltage, Current, and Power
- Overcurrent, Voltage Sag, and Voltage Swell Detection
- Ultra-fast On-chip Digital Calibration
- Configurable No-load Threshold for Anti-creep
- Internal Register Protection via Checksum and Write Protection
- UART Serial Interface
- On-chip Temperature Sensor
- On-chip Voltage Reference (25ppm/°C Typ.)
- Single 3.3 V Power Supply
- Ultra-fine Phase Compensation
- Low Power Consumption: <13 mW
- Power Supply Configurations:
  - GNDA = 0 V, VDDA: +3.3 V
- Low-cost 16-pin SOIC Package

Description

The CS5490 is a high-accuracy, two-channel, energy measurement analog front end.

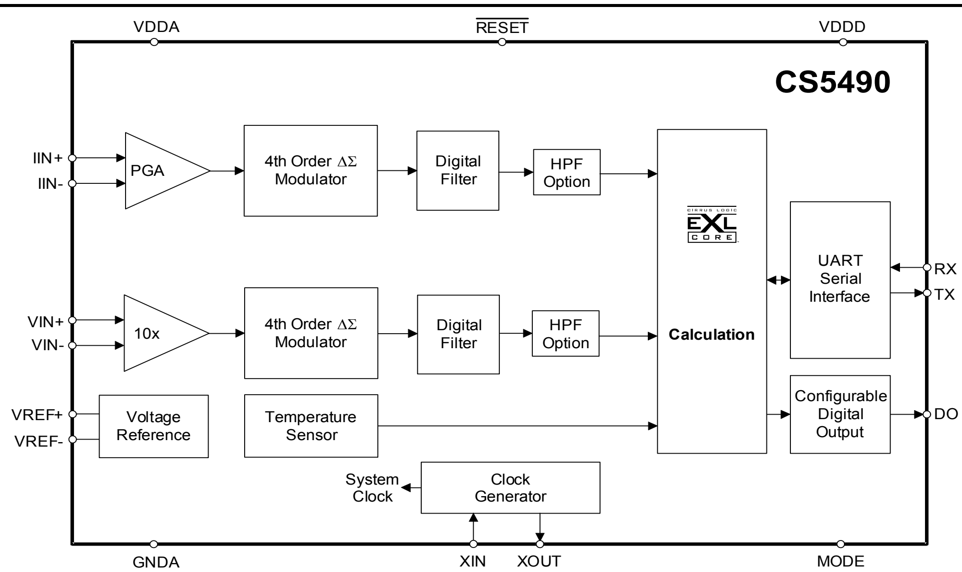
The CS5490 incorporates independent 4^{th} order Delta-Sigma analog-to-digital converters for both channels, reference circuitry, and the proven EXL signal processing core to provide active, reactive, and apparent energy measurement. In addition, RMS and power factor calculations are available. Calculations are output via a configurable energy pulse, or direct UART serial access to on-chip registers. Instantaneous current, voltage, and power measurements are also available over the serial port. The two-wire UART minimizes the cost of isolation where required.

A configurable digital output provides energy pulses, zero-crossing, energy direction, or interrupt functions. Interrupts can be generated for a variety of conditions including voltage sag or swell, overcurrent, and more. On-chip register integrity is assured via checksum and write protection. The CS5490 is designed to interface to a variety of voltage and current sensors, including shunt resistors, current transformers, and Rogowski coils.

On-chip functionality makes digital calibration simple and ultra fast to minimize the time required at the end of the customer production line. Performance across temperature is ensured with an on-chip voltage reference with low drift. A single 3.3V power supply is required, and power consumption is low at <13mW. To minimize space requirements, the CS5490 is offered in a low-cost 16-pin SOIC package.

ORDERING INFORMATION

See Page 57.



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1. OVERVIEW

The CS5490 is a CMOS power measurement integrated circuit that uses two ΔΣ analog-to-digital converters to measure line voltage and current. The CS5490 calculates active, reactive, and apparent power as well as RMS voltage and current and peak voltage and current. It handles other system-related functions, such as energy pulse generation, voltage sag and swell, overcurrent and zero-crossing detection, and line frequency measurement. A separate analog-to-digital converter is used for on-chip temperature measurement.

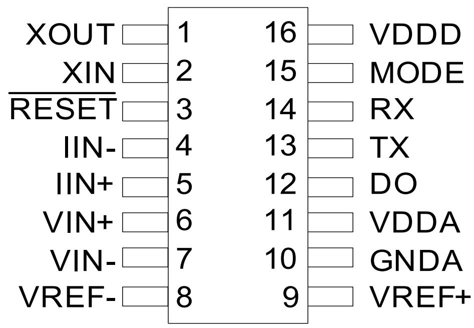
The CS5490 is optimized to interface to current transformers, shunt resistors, or Rogowski coils for current measurement, and to resistive dividers or voltage transformers for voltage measurement. Two full-scale ranges are provided on the current input to accommodate different types of current sensors. The CS5490's two differential inputs have a common-mode input range from analog ground (GNDA) to the positive analog supply (VDDA).

An on-chip voltage reference (typically 2.4 volts) is generated and provided at analog output, VREF±.

The digital output (DO) provides a variety of output signals and, depending on the mode selected, provides energy pulses, zero-crossings, or other choices.

The CS5490 includes a UART serial host interface to an external microcontroller. The UART signals include serial data input (RX) and serial data output (TX).

2. PIN DESCRIPTION



Clock Generator		
Crystal In **Crystal Out**	2,1	**XIN, XOUT** — Connect to an external quartz crystal. Alternatively, an external clock can be supplied to the XIN pin to provide the system clock for the device.
Control Pins and Serial Data I/O		
Digital Output	12	**DO** — Configurable digital output for energy pulses, interrupt, energy direction, and zero-crossings.
Reset	3	**$\overline{\text{RESET}}$** — An active-low Schmitt-trigger input used to reset the chip.
Serial Interface	13,14	**TX, RX** — UART serial data output/input.
Operating Mode Select	15	**MODE** — Connect to VDDA for proper operation.
Analog Inputs/Outputs		
Voltage Input	6,7	**VIN+, VIN-** — Differential analog input for the voltage channel.
Current Input	5,4	**IIN+, IIN-** — Differential analog input for the current channel.
Voltage Reference Input	9,8	**VREF+, VREF-** — The voltage reference output and return.
Power Supply Connections		
Internal Digital Supply	16	**VDDD** — Decoupling pin for the internal digital supply.
Positive Analog Supply	11	**VDDA** — The positive analog supply.
Analog Ground	10	**GNDA** — Analog ground.

2.1 Analog Pins

The CS5490 has two differential inputs, one for voltage (VIN±) and one for current (IIN±). The CS5490 also has two voltage reference pins (VREF±) between which a 0.1µ bypass capacitor must be placed.

2.1.1 Voltage Input

The output of the line voltage resistive divider or transformer is connected to the VIN± input of the CS5490. The voltage channel is equipped with a 10x, fixed-gain amplifier. The full-scale signal level that can be applied to the voltage channel is ±250 mV. If the input signal is a sine wave, the maximum RMS voltage is $250\,mVp / \sqrt{2} \approx 176.78\,mV_{RMS}$, which is approximately 70.7% of maximum peak voltage.

2.1.2 Current Input

The output of the current-sensing shunt resistor or transformer is connected to the IIN± input pins of the CS5490. To accommodate different current-sensing elements, the current channel incorporates a programmable gain amplifier (PGA) with two selectable input gains, as described in the *Config0* register description *6.6.1 Configuration 0 (Config0) – Page 0, Address 0* on page 32. There is a 10x gain setting and a 50x gain setting. The full-scale signal level for the current channel is ±50mV and ±250mV for 50x and 10x gain settings, respectively. If the input signal is a sine wave, the maximum RMS voltage is $35.35\,mV_{RMS}$ or $176.78\,mV_{RMS}$, which is approximately 70.7% of maximum peak voltage.

2.1.3 Voltage Reference

The CS5490 generates a stable voltage reference of 2.4V between the VREF± pins. The reference system also requires a filter capacitor of at least 0.1µF between the VREF± pins.

The reference system is capable of providing a reference for the CS5490 but has limited ability to drive external circuitry. It is strongly recommended that nothing other than the required filter capacitor is connected to the VREF± pins.

2.1.4 Crystal Oscillator

An external, 4.096MHz quartz crystal can be connected to the XIN and XOUT pins as shown in Figure 1. To reduce system cost, each pin is supplied with an on-chip load capacitor.

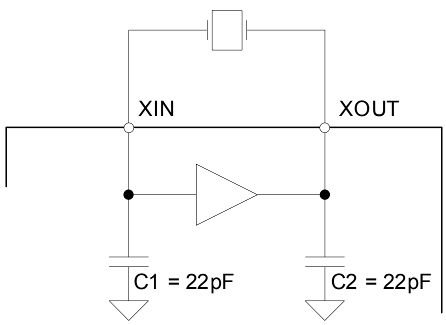


Figure 1. Oscillator Connections

Alternatively, an external clock source can be connected to the XIN pin.

2.2 Digital Pins

2.2.1 Reset Input

The active-low $\overline{\text{RESET}}$ pin, when asserted for longer than 120µs, will halt all CS5490 operations and reset internal hardware registers and states. When de-asserted, an initialization sequence begins, setting the default register values. To prevent erroneous, noise-induced resets to the part, an external pull-up resistor and a decoupling capacitor are necessary on the $\overline{\text{RESET}}$ pin.

2.2.2 Digital Output

The CS5490 provides a configurable digital output (DO). It can be configured to output energy pulses, interrupt, zero-crossings, or energy directions. Refer to the description of the *Config1* register in section *6.6 Register Descriptions* on page 32 for more details.

2.2.3 UART Serial Interface

The CS5490 provides two pins, RX and TX, for communication between a host microcontroller and the CS5490.

2.2.3.1 UART

The CS5490 provides a two-wire, asynchronous, full-duplex UART port. The CS5490 UART operates in 8-bit mode, which transmits a total of 10 bits per byte. Data is transmitted and received LSB first, with one start bit, eight data bits, and one stop bit.

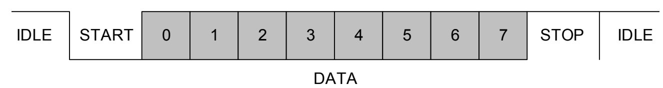


Figure 2. UART Serial Frame Format

The baud rate is defined in the *SerialCtrl* register. After chip reset, the default baud rate is 600, if MCLK is 4.096MHz. The baud rate is based on the contents of bits BR[15:0] in the *SerialCtrl* register and is calculated as follows:

$$BR[15:0] = \text{Baud Rate} \times (524288/\text{MCLK})$$
or
$$\text{Baud Rate} = BR[15:0]/(524288/\text{MCLK})$$

The maximum baud rate is 512K if MCLK is 4.096MHz.

The UART has two signals: TX and RX. TX is the serial data output from the CS5490; RX is the serial data input to the CS5490.

2.2.4 MODE Pin

The MODE pin must be tied to VDDA for normal operation. The MODE pin is used primarily for factory test procedures.

3. CHARACTERISTICS & SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Positive Analog Power Supply	VDDA	3.0	3.3	3.6	V
Specified Temperature Range	T_A	-40	-	+85	°C

POWER MEASUREMENT CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Active Energy (Note 1 & 2)	All Gain Ranges Current Channel Input Signal Dynamic Range 4000:1	P_{Avg}	-	±0.1	-	%
Reactive Energy (Note 1 & 2)	All Gain Ranges Current Channel Input Signal Dynamic Range 4000:1	Q_{Avg}	-	±0.1	-	%
Apparent Power (Note 1 & 3)	All Gain Ranges Current Channel Input Signal Dynamic Range 1000:1	S	-	±0.1	-	%
Current RMS (Note 1, 3, & 4)	All Gain Ranges Current Channel Input Signal Dynamic Range 1000:1	I_{RMS}	-	±0.1	-	%
Voltage RMS (Note 1 & 3)	Voltage Channel Input Signal Dynamic Range 20:1	V_{RMS}	-	±0.1	-	%
Power Factor (Note 1 & 3)	All Gain Ranges Current Channel Input Signal Dynamic Range 1000:1	PF	-	±0.1	-	%

Notes:
1. Specifications guaranteed by design and characterization.
2. Active energy is tested with power factor PF = 1.0. Reactive energy is tested with Sin(φ) = 1.0. Energy error measured at system level using single energy pulse. Where: 1) One energy pulse = 0.5Wh or 0.5Varh; 2) VDDA = +3.3V, T_A = 25°C, MCLK = 4.096MHz; 3) System is calibrated.
3. Calculated using register values; N≥4000.
4. I_{RMS} error calculated using register values. 1) VDDA = +3.3V; T_A = 25°C; MCLK = 4.096MHz; 2) AC offset calibration applied.

TYPICAL LOAD PERFORMANCE

- Energy error measured at system level using single energy pulse; where 1 energy pulse = 0.5Wh or 0.5Varh.
- I_{RMS} error calculated using register values
- VDDA = +3.3V; T_A = 25°C; MCLK = 4.096MHz

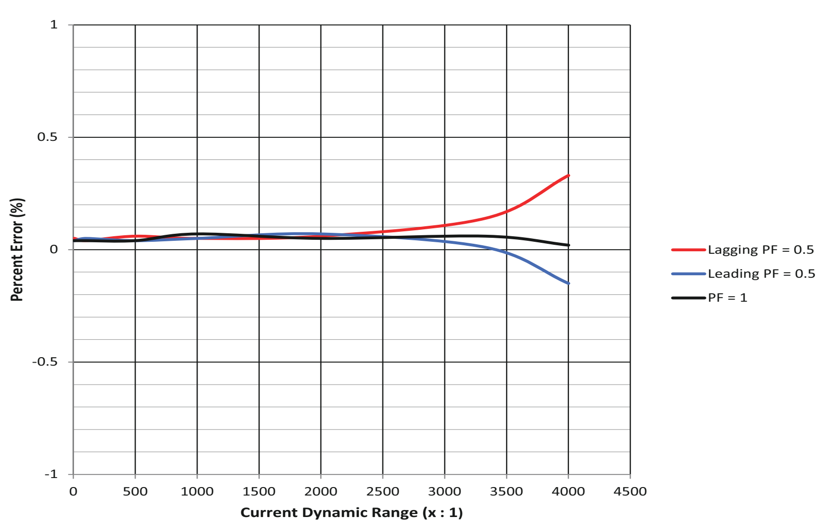


Figure 3. Active Energy Load Performance

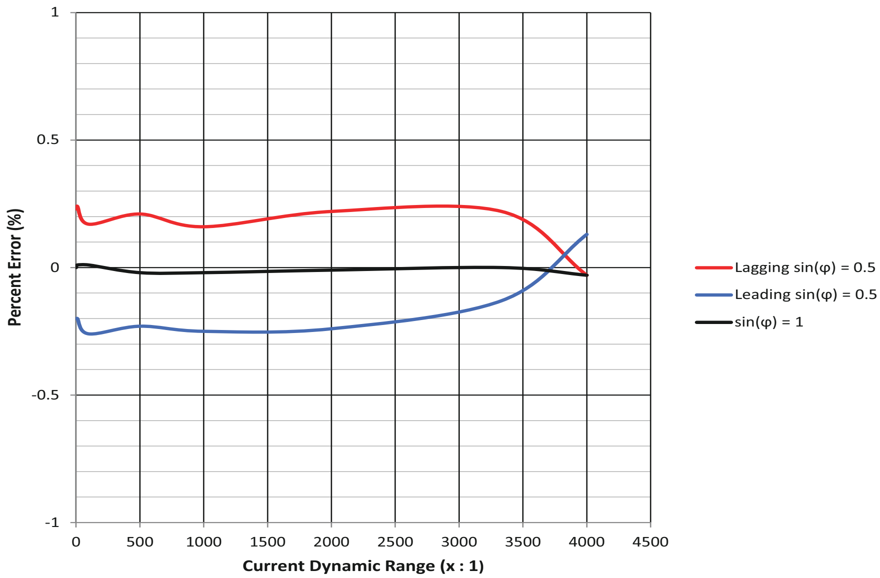


Figure 4. Reactive Energy Load Performance

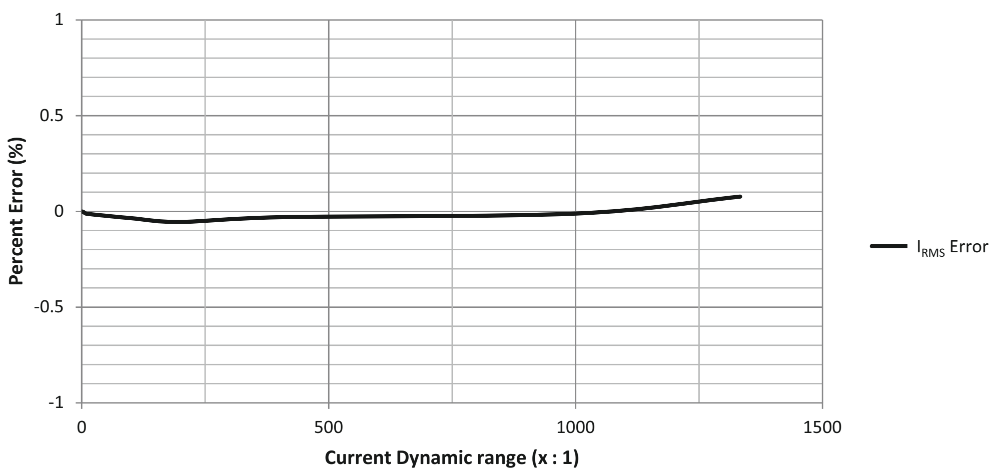


Figure 5. I_{RMS} Load Performance

ANALOG CHARACTERISTICS

- Min/Max characteristics and specifications are guaranteed over all Recommended Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and T_A = 25°C.
- VDDA = +3.3V ±10%; GNDA = 0V. All voltages with respect to 0V.
- MCLK = 4.096MHz.

Parameter		Symbol	Min	Typ	Max	Unit
Analog Inputs (Current Channels)						
Common Mode Rejection	(DC, 50, 60Hz)	CMRR	80	-	-	dB
Common Mode+Signal			-0.25	-	VDDA	V
Differential Full-scale Input Range [(IIN+) – (IIN-)]	(Gain = 10) (Gain = 50)	IIN	- -	250 50	- -	mV_P mV_P
Total Harmonic Distortion	(Gain = 50)	THD	90	100	-	dB
Signal-to-Noise Ratio (SNR)	(Gain = 10) (Gain = 50)	SNR	- -	80 80	- -	dB dB
Crosstalk from Voltage Inputs at Full Scale	(50, 60Hz)		-	-115	-	dB
Crosstalk from Current Input at Full Scale	(50, 60Hz)		-	-115	-	dB
Input Capacitance		IC	-	27	-	pF
Effective Input Impedance		EII	30	-	-	kΩ
Offset Drift (Without the High-pass Filter)		OD	-	4.0	-	μV/°C
Noise (Referred to Input)	(Gain = 10) (Gain = 50)	N_I	- -	9 2.2	- -	μV_{RMS} μV_{RMS}
Power Supply Rejection Ratio (Note 7)	(60Hz) (Gain = 10) (Gain = 50)	PSRR	60 68	65 75	- -	dB dB
Analog Inputs (Voltage Channels)						
Common Mode Rejection	(DC, 50, 60Hz)	CMRR	80	-	-	dB
Common Mode+Signal			-0.25	-	VDDA	V
Differential Full-scale Input Range	[(VIN+) – (VIN-)]	VIN	-	250	-	mV_P
Total Harmonic Distortion		THD	80	88	-	dB
Signal-to-Noise Ratio (SNR)		SNR	-	73	-	dB
Crosstalk from Current Inputs at Full Scale	(50, 60Hz)		-	-115	-	dB
Input Capacitance		IC	-	2.0	-	pF
Effective Input Impedance		EII	2	-	-	MΩ
Noise (Referred to Input)		N_V	-	40	-	μV_{RMS}
Offset Drift (Without the High-pass Filter)		OD	-	16.0	-	μV/°C
Power Supply Rejection Ratio (Note 7)	(60Hz) (Gain = 10)	PSRR	60	65	-	dB
Temperature						
Temperature Accuracy	(Note 6)	T	-	±5	-	°C

Parameter	Symbol	Min	Typ	Max	Unit
Power Supplies					
Power Supply Currents (Active State) I_{A+} (VDDA = +3.3V)	PSCA	-	3.9	-	mA
Power Consumption (Note 5) Active State (VDDA = +3.3V) Stand-by State	PC	- -	12.9 4.5	- -	mW mW

Notes: 5. All outputs unloaded. All inputs CMOS level.

6. Temperature accuracy measured after calibration is performed.

7. Measurement method for PSRR: VDDA = +3.3V, a 150mV (zero-to-peak) (60Hz) sinewave is imposed onto the +3.3V DC supply voltage at the VDDA pin. The "+" and "-" input pins of both input channels are shorted to GNDA. The CS5490 is then commanded to continuous conversion acquisition mode, and digital output data is collected for the channel under test. The (zero-to-peak) value of the digital sinusoidal output signal is determined, and this value is converted into the (zero-to-peak) value of the sinusoidal voltage (measured in mV) that would need to be applied at the channel's inputs, in order to cause the same digital sinusoidal output. This voltage is then defined as V_{eq} PSRR is (in dB):

$$PSRR = 20 \cdot \log\left[\frac{150}{V_{eq}}\right]$$

VOLTAGE REFERENCE

Parameter	Symbol	Min	Typ	Max	Unit
Reference (Note 8)					
Output Voltage	VREF	+2.3	+2.4	+2.5	V
Temperature Coefficient (Note 9)	TC_{VREF}	-	25	-	ppm/°C
Load Regulation (Note 10)	ΔV_R	-	30	-	mV

Notes: 8. It is strongly recommended that no connection other than the required filter capacitor be made to VREF±.

9. The voltage at VREF± is measured across the temperature range. From these measurements the following formula is used to calculate the VREF temperature coefficient:

$$TC_{VREF} = \left(\frac{VREF_{MAX} - VREF_{MIN}}{VREF_{AVG}}\right)\left(\frac{1}{T_AMAX - T_AMIN}\right)(1.0 \times 10^6)$$

10. Specified at maximum recommended output of 1µA sourcing. VREF is a very sensitive signal, the output of the VREF circuit has a very high output impedance so that the 0.1µF reference capacitor provides attenuation even to low frequency noise, such as 50Hz noise on the VREF output. As such VREF intended for the CS5490 only and should not be connected to any external circuitry. The output impedance is sufficiently high that standard digital multi-meters can significantly load this voltage. The accuracy of the metrology IC can not be guaranteed when a multimeter or any component other than the 0.1µF capacitor is attached to VREF. If it is desired to measure VREF for any reason other than a very course indicator of VREF functionality, Cirrus recommends a very high input impedance multimeter such as the Keithley Model 2000 Digital Multimeter be used, but still cannot guarantee the accuracy of the metrology with this meter connected to VREF.

DIGITAL CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all Recommended Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and T_A = 25°C.
- VDDA = +3.3V ±10%; GNDA = 0V. All voltages with respect to 0V.
- MCLK = 4.096MHz.

Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Characteristics						
XIN Clock Frequency	Internal Gate Oscillator	MCLK	2.5	4.096	5	MHz
XIN Clock Duty Cycle			40	-	60	%
Filter Characteristics						
Phase Compensation Range	(60Hz, OWR = 4000Hz)		-10.79	-	+10.79	°
Input Sampling Rate			-	MCLK/8	-	Hz
Digital Filter Output Word Rate	(Both channels)	OWR	-	MCLK/1024	-	Hz
High-pass Filter Corner Frequency	-3dB		-	2.0	-	Hz
Input/Output Characteristics						
High-level Input Voltage (All Pins)		V_{IH}	0.6(VDDA)	-	-	V
Low-level Input Voltage (All Pins)		V_{IL}	-	-	0.6	V
High-level Output Voltage (Note 12)	DO, I_{out} = +10mA I_{out} = +5mA	V_{OH}	VDDA-0.3 VDDA-0.3	- -	- -	V V
Low-level Output Voltage (Note 12)	DO, I_{out} = -12mA All Other Outputs, I_{out} = -5mA	V_{OL}	- -	- -	0.5 0.5	V V
Input Leakage Current		I_{in}	-	±1	±10	µA
3-state Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	5	-	pF

Notes: 11. All measurements performed under static conditions.

12. XOUT pin used for crystal only. Typical drive current<1mA.

SWITCHING CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all Recommended Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and T_A = 25°C.
- VDDA = +3.3V ±10%; GNDA = 0V. All voltages with respect to 0V.
- Logic Levels: Logic 0 = 0V, Logic 1 = VDDA.

Parameter		Symbol	Min	Typ	Max	Unit
Rise Times (Note 13)	DO Any Digital Output Except DO	t_{rise}	- -	- 50	1.0 -	µs ns
Fall Times (Note 13)	DO Any Digital Output Except DO	t_{fall}	- -	- 50	1.0 -	µs ns
Start-up						
Oscillator Start-up Time	XTAL = 4.096 MHz (Note 14)	t_{ost}	-	60	-	ms

Notes: 13. Specified using 10% and 90% points on waveform of interest. Output loaded with 50pF.

14. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	(Note 15)	VDDA	-0.3	-	+4.0	V
Input Current	(Notes 16 and 17)	I_{IN}	-	-	±10	mA
Input Current for Power Supplies		-	-	-	±50	-
Output Current	(Note 18)	I_{OUT}	-	-	100	mA
Power Dissipation	(Note 19)	P_D	-	-	500	mW
Input Voltage	(Note 20)	V_{IN}	-0.3	-	(VDDA) + 0.3	V
Junction-to-Ambient Thermal Impedance	2 Layer Board 4 Layer Board	θ_{JA}	- -	140 70	- -	°C/W °C/W
Ambient Operating Temperature		T_A	-40	-	85	°C
Storage Temperature		T_{stg}	-65	-	150	°C

Notes:
15. VDDA and GNDA must satisfy [(VDDA) – (GNDA)] ≤ + 4.0V.
16. Applies to all pins, including continuous overvoltage conditions at the analog input pins.
17. Transient current of up to 100mA will not cause SCR latch-up.
18. Applies to all pins, except VREF±.
19. Total power dissipation, including all input currents and output currents.
20. Applies to all pins.

WARNING:
Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

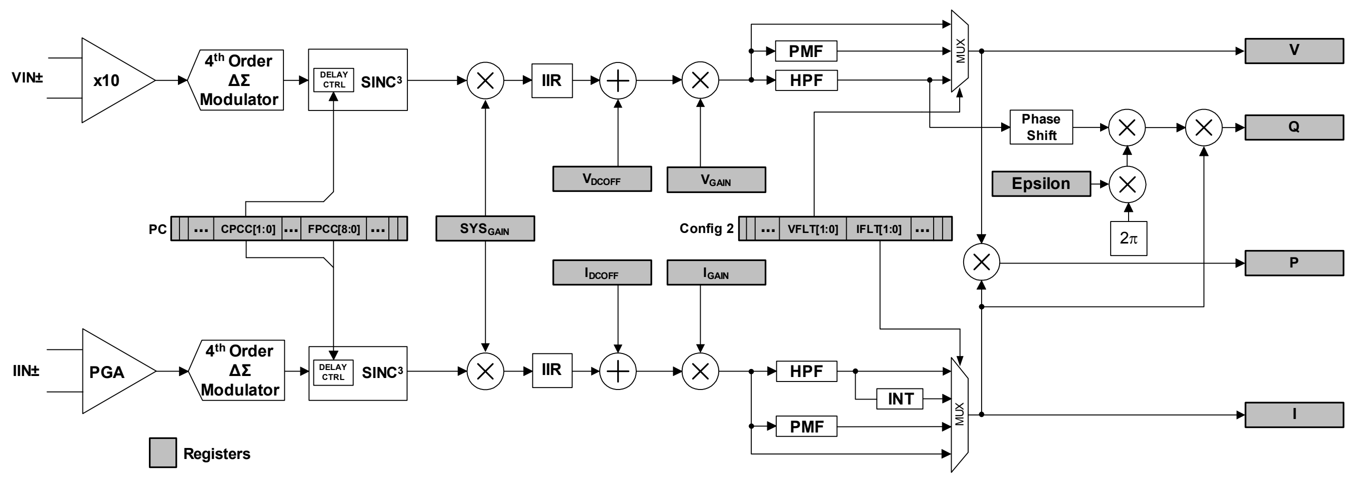


Figure 6. Signal Flow for V, I, P, and Q Measurements

4. SIGNAL FLOW DESCRIPTION

The signal flow for voltage, current measurement, and the other calculations is shown in Figure 6.

The signal flow consists of a current and a voltage channel. The current and voltage channels have differential input pins.

4.1 Analog-to-Digital Converters

Both input channels use fourth-order delta-sigma modulators to convert the analog inputs to single-bit digital data streams. The converters sample at a rate of MCLK/8. This high sampling provides a wide dynamic range and simplifies anti-alias filter design.

4.2 Decimation Filters

The single-bit modulator output data is widened to 24 bits and down sampled to MCLK/1024 with low-pass decimation filters. These decimation filters are third-order Sinc filters. The filter outputs pass through an IIR "anti-sinc" filter.

4.3 IIR Filter

The IIR filter is used to compensate for the amplitude roll-off of the decimation filters. The droop-correction filter flattens the magnitude response of the channel out to the Nyquist frequency, thus allowing for accurate measurements of up to 2kHz (MCLK = 4.096MHz). By default, the IIR filters are enabled. The IIR filters can be bypassed by setting the IIR_OFF bit in the *Config2* register.

4.4 Phase Compensation

Phase compensation changes the phase of voltage relative to current by adding a delay in the decimation filters. The amount of phase shift is set by the PC register bits CPCC[1:0] and FPCC[8:0] for the current channel. For the voltage channel, only bits CPCC[1:0] affect the delay.

Fine phase compensation control bits, FPCC[8:0], provide up to 1/OWR delay in the current channel. Coarse phase compensation control bits, CPCC[1:0], provide an additional 1/OWR delay in the current channel or up to 2/OWR delay in the voltage channel. Negative delay in the voltage channel can be implemented by setting longer delay in the current channel than the voltage channel. For a OWR of 4000Hz, the delay range is ±500μs, a phase shift of ±8.99° at 50Hz and ±10.79° at 60Hz. The step size is 0.008789° at 50Hz and 0.010547° at 60Hz. For more information about phase compensation, see section *7.2 Phase Compensation* on page 53.

4.5 DC Offset & Gain Correction

The system and CS5490 inherently have component tolerances, gain, and offset errors, which can be removed using the gain and offset registers. Each measurement channel has its own set of gain and offset registers. For every instantaneous voltage and current sample, the offset and gain values are used to correct DC offset and gain errors in the channel (see section *7. System Calibration* on page 52 for more details).

4.6 High-pass & Phase Matching Filters

Optional high-pass filters (HPF in Figure 6) remove any DC component from the selected signal paths. Each power calculation contains a current and voltage channel. If an HPF is enabled in only one channel, a phase-matching filter (PMF) should be applied to the other channel to match the phase response of the HPF. For AC power measurement, high-pass filters should be enabled on the voltage and current channels. For information about how to enable and disable the HPF or PMF on each channel, refer to *Config2* register descriptions in section *6.6 Register Descriptions* on page 32.

4.7 Digital Integrators

Optional digital integrators (INT in Figure 6) are implemented on the current channel to compensate for the 90° phase shift and 20dB/decade gain generated by the Rogowski coil current sensor. When a Rogowski coil is used as the current sensor, the integrator (INT) should be enabled on that current channel. For information about how to enable and disable the INT on the current channel, refer to *Config2* register descriptions in section *6.6 Register Descriptions* on page 32.

4.8 Low-rate Calculations

All the RMS and power results come from low-rate calculations by averaging the output word rate (OWR) instantaneous values over *N* samples, where *N* is the value stored in the *SampleCount* register. The low-rate interval or averaging period is *N* divided by OWR (4000Hz if MCLK = 4.096MHz). The CS5490 provides two averaging modes for low-rate calculations: Fixed Number of Sample Averaging mode and Line-cycle Synchronized Averaging mode. By default, the CS5490 averages with the Fixed Number of Samples Averaging mode. By setting the AVG_MODE bit in the *Config2* register, the CS5490 will use the Line-cycle Synchronized Averaging mode.

4.8.1 Fixed Number of Samples Averaging

N is the preset value in the *SampleCount* register and should not be set less than 100. By default, the *SampleCount* register is 4000. With MCLK = 4.096 MHz, the averaging period is fixed at N/4000 = 1 second, regardless of the line frequency.

4.8.2 Line-cycle Synchronized Averaging

When operating in Line-cycle Synchronized Averaging mode, and when line frequency measurement is enabled (see section *5.4 Line Frequency Measurement* on page 19), the CS5490 uses the voltage (V) channel zero crossings and measured line frequency to automatically adjust *N* such that the averaging period will be equal to the number of half line-cycles in the *CycleCount* register. For example, if the line frequency is 51Hz, and the *CycleCount* register is set to 100, *N* will be $4000 \times (100/2)/51 = 3921$ during continuous conversion. *N* is self-adjusted according to the line frequency, therefore the averaging period is always close to the whole number of half line-cycles, and the low-rate calculation results will minimize ripple and maximize resolution, especially when the line frequency varies. Before starting a low-rate conversion in the Line-cycle Synchronized Averaging mode, the

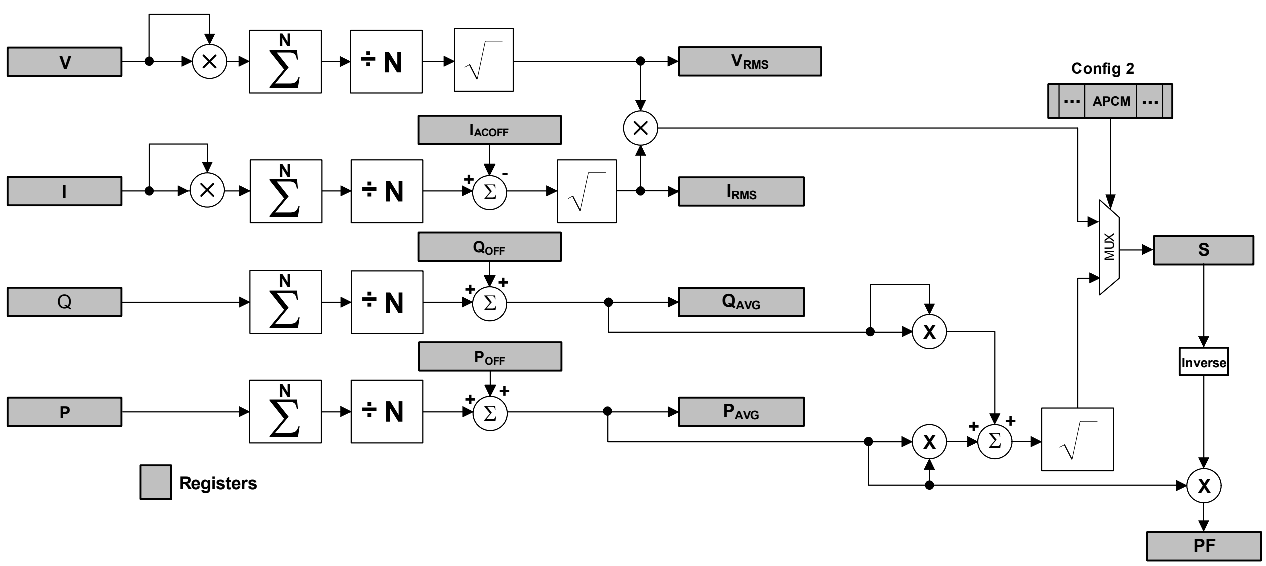


Figure 7. Low-rate Calculations

SampleCount register should not be changed from its default value of 4000, and bit AFC of the *Config2* register must be set. During continuous conversion, the host processor should not change the *SampleCount* register.

4.8.3 RMS Current & Voltage

The root mean square (*RMS* in Figure 7) calculations are performed on *N* instantaneous voltage and current samples using Equation 1:

$$I_{RMS} = \sqrt{\frac{\sum_{n=0}^{N-1} I_n^2}{N}} \qquad V_{RMS} = \sqrt{\frac{\sum_{n=0}^{N-1} V_n^2}{N}} \qquad \text{[Eq.1]}$$

4.8.4 Active Power

The instantaneous voltage and current samples are multiplied to obtain the instantaneous power (*P*) (see Figure 6). The product is then averaged over *N* samples to compute active power (P_{AVG}).

4.8.5 Reactive Power

Instantaneous reactive power (*Q*) is the sample rate result obtained by multiplying instantaneous current (*I*) by instantaneous quadrature voltage (*Q*). These values are created by phase shifting instantaneous voltage (*V*) 90° using first-order integrators (see Figure 6). The gain of these integrators is inversely related to line frequency, so their gain is corrected by the *Epsilon* register, which is based on line frequency. Reactive power (Q_{AVG}) is generated by integrating the instantaneous quadrature power over *N* samples.

4.8.6 Apparent Power

By default, the CS5490 calculates the apparent power (*S*) as the product of RMS voltage and current. See Equation 2:

$$S = V_{RMS} \times I_{RMS} \qquad \text{[Eq.2]}$$

The CS5490 also provides an alternate apparent power calculation method. The alternate apparent power method uses real power (P_{AVG}) and reactive power (Q_{AVG}) to calculate apparent power. See Equation 3.

$$S = \sqrt{{Q_{AVG}}^2 + {P_{AVG}}^2} \qquad \text{[Eq.3]}$$

The APCM bit in the *Config2* register controls which method is used for apparent power calculation.

4.8.7 Peak Voltage & Current

Peak current (I_{PEAK}) and peak voltage (V_{PEAK}) are calculated over *N* samples and recorded in the corresponding channel peak register documented in the register map. This peak value is updated every *N* samples.

4.8.8 Power Factor

Power factor (*PF*) is active power divided by apparent power, as shown below. The sign of the power factor is determined by the active power. See Equation 4.

$$PF = \frac{P_{ACTIVE}}{S} \qquad \text{[Eq.4]}$$

4.9 Average Active Power Offset

The average active power offset register, P_{OFF}, can be used to offset erroneous power sources resident in the system not originating from the power line. Residual power offsets are usually caused by crosstalk into the current channel from the voltage channel, or from ripple on the meter's or chip's power supply, or from inductance from a nearby transformer.

These offsets can be either positive or negative, indicating crosstalk coupling either in phase or out of phase with the applied voltage input. The power offset register can compensate for either condition.

To use this feature, measure the average power at no load and take the measured result (from the P_{AVG} register), invert (negate) the value, and write it to the associated power offset register, P_{OFF}.

4.10 Average Reactive Power Offset

The average reactive power offset register, Q_{OFF}, can be used to offset erroneous power sources resident in the system not originating from the power line. Residual reactive power offsets are usually caused by crosstalk into the current channel from the voltage channel, or from ripple on the meter's or chip's power supply, or from inductance from a nearby transformer.

These offsets can be either positive or negative, depending on the phase angle between the crosstalk coupling and the applied voltage. The reactive power offset register can compensate for either condition. To use this feature, measure the average reactive power at no load. Take the measured result from the Q_{AVG} register, invert (negate) the value and write it to the reactive power offset register, Q_{OFF}.

5. FUNCTIONAL DESCRIPTION

5.1 Power-on Reset (POR)

The CS5490 has an internal power supply supervisor circuit that monitors the VDDA and VDDD power supplies and provides the master reset to the chip. If any of these voltages are in the reset range, the master reset is triggered.

Both the analog and the digital supply have their own POR circuit. During power-up, both supplies have to be above the rising threshold for the master reset to be de-asserted.

Each POR is divided into 2 blocks: rough and fine. Rough POR triggers the fine POR. Rough POR depends only on the supply voltage. The trip point for the fine POR is dependent on bandgap voltage for precise control.

The POR circuit also acts as a brownout detect. The fine POR detects supply drops and asserts the master reset.

The rough and fine PORs have hysteresis in their rise and fall thresholds which prevents the reset signal from chattering.

The following plot shows the POR outputs for each of the power supplies. The POR_Fine_VDDA and POR_Fine_VDDD signals are AND-ed to form the actual power-on reset signal to the digital circuitry. The digital circuitry, in turn, holds the master reset signal for 130ms and then de-asserts the master reset.

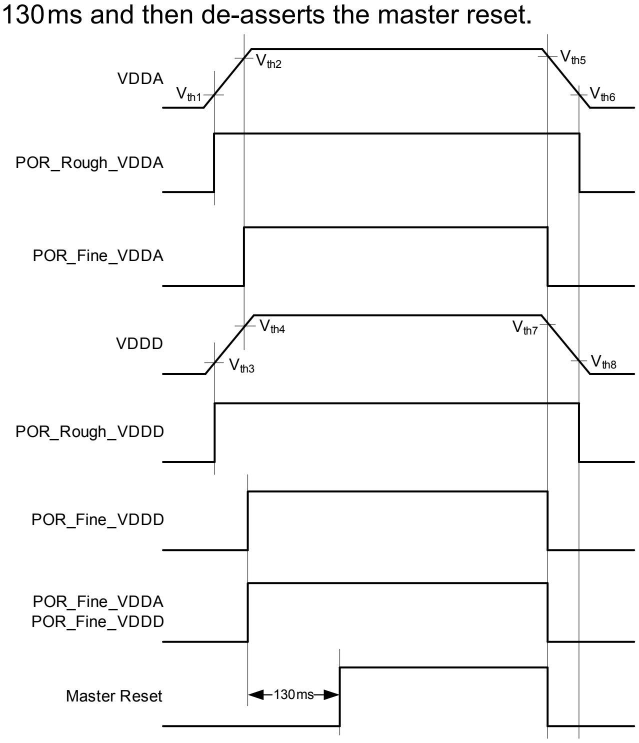


Figure 8. Power-on Reset Timing

Table 1. POR Thresholds

Typical POR Threshold		Rising	Falling
VDDA	Rough	V_{th1} = 2.34V	V_{th6} = 2.06V
	Fine	V_{th2} = 2.77V	V_{th5} = 2.59V
VDDD	Rough	V_{th3} = 1.20V	V_{th8} = 1.06V
	Fine	V_{th4} = 1.51V	V_{th7} = 1.42V

5.2 Power Saving Modes

Power Saving modes for CS5490 are accessed through the Host Instruction Commands (see *6.1 Host Commands* on page 24).

- Standby: Powers down all the ADCs, rough buffer, and the temperature sensor. Standby mode disables the system time calculations. Use the wake-up command to come out of standby mode.
- Wake-up: Clears the ADC power-down bits and starts the system time calculations.

After any of these commands are completed, the DRDY bit is set in the *Status0* register.

5.3 Zero-crossing Detection

Zero-crossing detection logic is implemented in CS5490. A low-pass filter can be enabled by setting ZX_LPF bit in register *Config2*. The low-pass filter has a cut-off frequency of 80Hz. It is used to eliminate any harmonics and to help the zero-crossing detection on the 50Hz or 60Hz fundamental component. The zero-crossing level registers are used to set the minimum threshold over which the channel peak has to exceed in order for the zero-crossing detection logic to function. There are two separate zero-crossing level registers: VZX_{LEVEL} is the threshold for the voltage channels, and IZX_{LEVEL} is the threshold for the current channels.

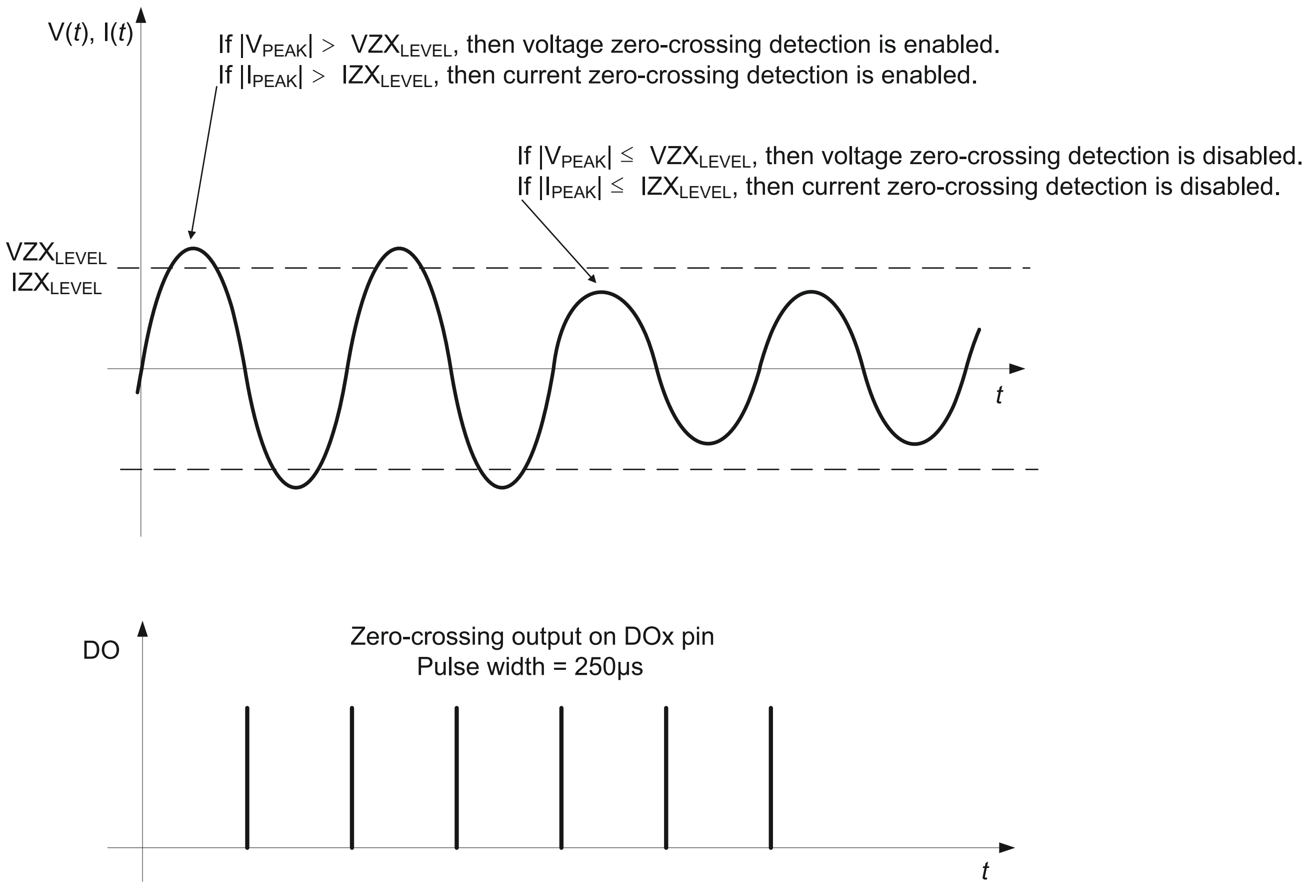


Figure 9. Zero-crossing Level and Zero-crossing Output on DO

5.4 Line Frequency Measurement

If the Automatic Frequency Calculation (AFC) bit in the *Config2* register is set, the line frequency measurement on the voltage channel will be enabled. The line frequency measurement is based on a number of voltage channel zero crossings. This number is 100 by default and configurable through the ZX_{NUM} register (see section 6.6.56 on page 51). The *Epsilon* register will be updated automatically with the line frequency information. The Frequency Update (FUP) bit in the *Status0* interrupt status register is set when the frequency calculation is completed. When the line frequency is 50Hz and the ZX_{NUM} register is 100, the *Epsilon* register is updated every one second with a resolution of less than 0.1%. A larger zero-crossing number in the ZX_{NUM} register will increase line frequency measurement resolution and period. Note that the CS5490 line frequency measurement function does not support the line frequency out of the range of 40Hz to 75Hz.

The *Epsilon* register is also used to set the gain of the 90° phase shift filter used in the quadrature power calculation. The value in the *Epsilon* register is the ratio of the line frequency to the output word rate (OWR). For 50Hz line frequency and 4000Hz OWR, *Epsilon* is 50/4000 (0.0125) (the default). For 60Hz line frequency, it is 60/4000 (0.015).

5.5 Energy Pulse Generation

The CS5490 provides an independent energy pulse generation (EPG) block in order to output active, reactive, and apparent energy pulses on the digital output pin (DO). The energy pulse frequency is proportional to the magnitude of the power. The energy pulse output is commonly used as the test output of a power meter. The host microcontroller can also use the energy pulses to easily accumulate the energy. Refer to Figure 10.

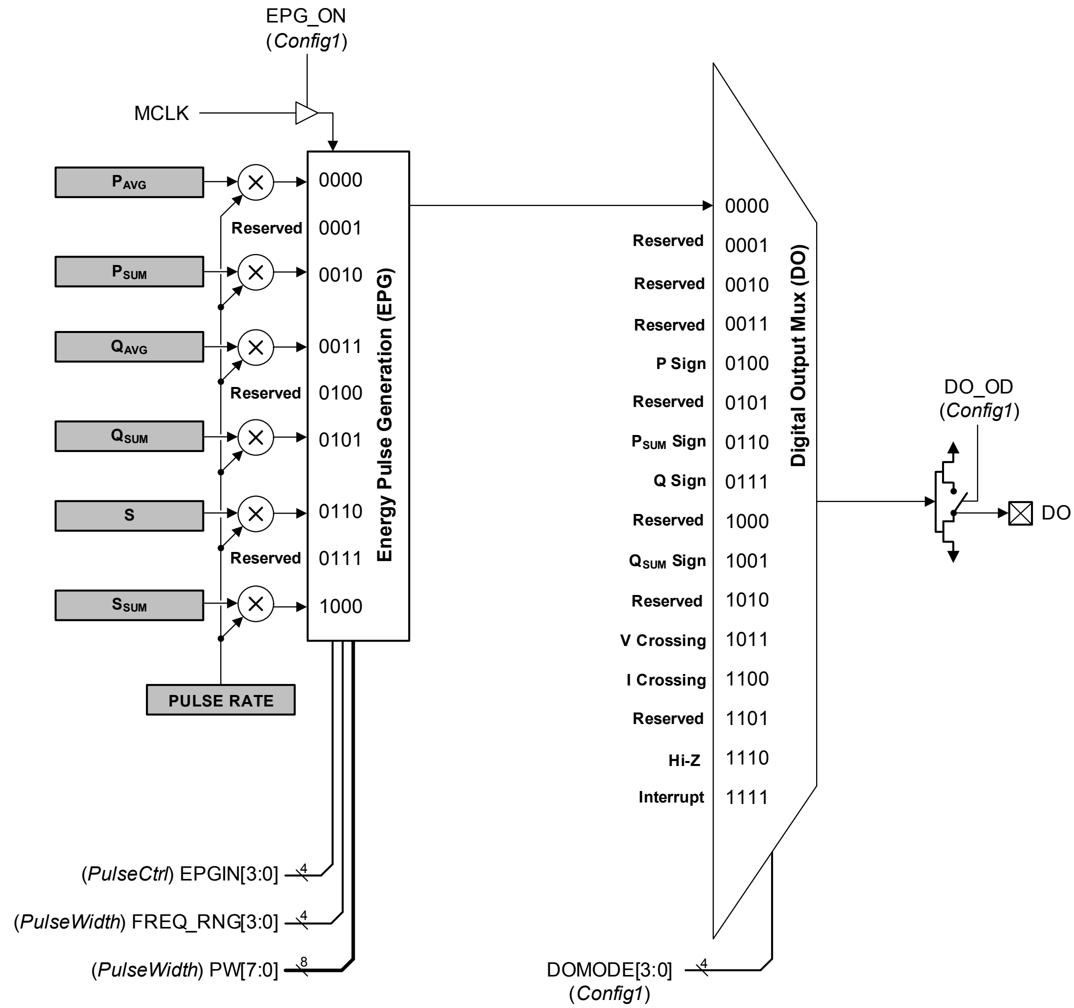


Figure 10. Energy Pulse Generation and Digital Output Control

After reset, the energy pulse generation block is disabled (DOMODE[3:0] = Hi-Z). To output a desired energy pulse to a DO pin, it is necessary to follow the steps below:

1. Write to register *PulseWidth* (page 0, address 8) to select the energy pulse width and pulse frequency range.
2. Write to register *PulseRate* (page 18, address 28) to select the energy pulse rate.
3. Write to register *PulseCtrl* (page 0, address 9) to select the input to the energy pulse generation block.
4. Write '1' to bit EPG_ON of register *Config1* (page 0, address 1) to enable the energy pulse generation block.
5. Wait at least 0.1s.
6. Write bits DOMODE[3:0] of register *Config1* to select DO to output pulses from the energy pulse generation block.
7. Send DSP instruction (0xD5) to begin continuous conversion.

5.5.1 Pulse Rate

Before configuring the *PulseRate* register, the full-scale pulse rate needs to be calculated, and the frequency range needs to be specified through FREQ_RNG[3:0] bits in the *PulseWidth* register. For example, if a meter has the meter constant of 1000imp/kWh, a maximum voltage (U_{MAX}) of 240V, and a maximum current (I_{MAX}) of 100A, the maximum pulse rate is:

$$[1000 \times (240 \times 100/1000)]/3600 = 6.6667\,Hz.$$

Assume the meter is calibrated with U_{MAX} and I_{MAX}, and the *Scale* register contains the default value of 0.6. After gain calibration, the power register value will be 0.36, which represents 240 x 100 = 24kW or 6.6667Hz pulse output rate. The full-scale pulse rate is:

$$F_{out} = 6.6667/0.36 = 18.5185\,Hz.$$

Refer to section *6.6.6 Pulse Output Width (PulseWidth) – Page 0, Address 8* on page 36. The FREQ_RNG[3:0] bits should be set to b[0110].

The CS5490 pulse generation block behaves as follows:

- The pulse rate generated by full-scale (1.0 decimal) power register is

  F_{OUT} = (*PulseRate* x 2000)/2^{FREQ_RNG}

- The *PulseRate* register value is

  PulseRate = (F_{OUT} x 2^{FREQ_RNG})/2000

  = (18.5186 x 64)/2000

  = 0.5925952

  = 0x4BDA29

5.5.2 Pulse Width

The *PulseWidth* register defines the Active-low time of each energy pulse:

Active-low = 250 µs + (*PulseWidth*/64000).

By default, the *PulseWidth* register value is 1, and the Active-low time of each energy pulse is 265.6 µs. Note that the pulse width should never exceed the pulse period.

5.6 Voltage Sag, Voltage Swell, and Overcurrent Detection

Voltage sag detection is used to determine when the voltage falls below a predetermined level for a specified interval of time (duration). Voltage swell and overcurrent detection determine when the voltage or current rises above a predetermined level for the duration.

The duration is set by the value in the $VSag_{DUR}$, $VSwell_{DUR}$, and $IOver_{DUR}$ registers. Setting any of these to zero (default) disables the detect feature for the given channel. The value is in output word rate (OWR) samples. The predetermined level is set by the values in the $VSag_{LEVEL}$, $VSwell_{LEVEL}$, and $IOver_{LEVEL}$ registers.

For each enabled input channel, the measured value is rectified and compared to the associated level register. Over the duration window, the number of samples above and below the level are counted. If the number of samples below the level exceeds the number of samples above, a *Status0* register bit VSAG is set, indicating a sag condition. If the number of samples above the level exceeds the number of samples below, a *Status0* register bit VSWELL or IOVER is set, indicating a swell or overcurrent condition (see Figure 11).

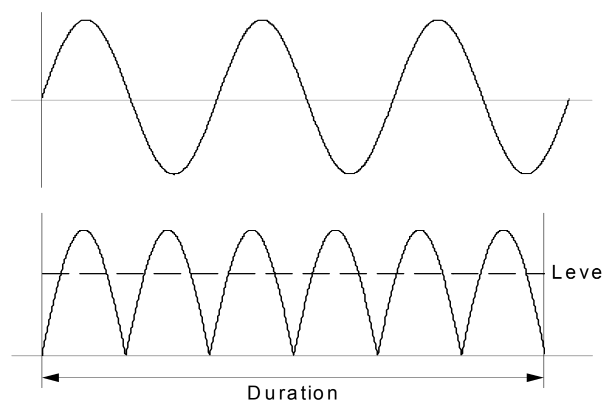


Figure 11. Sag, Swell, & Overcurrent Detect

5.7 Phase Sequence Detection

Polyphase meters using multiple CS5490 devices may be configured to sense the succession of voltage zero-crossings and determine which phase order is in service. The phase sequence detection within CS5490 involves counting the number of OWR samples from a starting point to the next voltage zero-crossing rising edge or falling for each phase. By comparing the count for each phase, the phase sequence can be easily determined: the smallest count is first, and the largest count is last.

The phase sequence detection and control (*PSDC*) register provides the count control, zero-crossing direction and count results. Writing '0' to bit DONE and '10110' to bits CODE[4:0] of the *PSDC* register followed by a falling edge on the RX pin will initiate the phase sequence detection circuit. The RX pin must be held low for a minimum of 500ns. When the device is in UART mode, it is recommended that a 0xFF command be written to all parts to start the phase sequence detection. Multiple CS5490 devices in a polyphase meter must receive the register writing and the RX falling edge at the same time so that all CS5490 devices starts to count simultaneously. Bit DIR of *PSDC* register specifies the direction of the next zero crossing at which the count stops. If bit DIR is '0', the count stops at the next negative-to-positive zero crossing. If bit DIR is '1', the count stops at the next positive-to-negative zero crossing. When the count stops, the DONE bit will be set by the CS5490, and then the count result of each phase may be read from bits PSCNT[6:0] of the PSDC register.

If the PSCNT[6:0] bits are equal to 0x00, 0x7F or greater than 0x64 (for 50Hz) or 0x50 (for 60Hz), then a measurement error has occurred, and the measurement results should be disregarded. This could happen when the voltage input signal amplitude is lower than the amplitude specified in the VZX_{LEVEL} register.

To determine the phase order, the PSCNT[6:0] bit counts from each CS5490 are sorted in ascending order. Figure 12 and Figure 13 illustrate how phase sequence detection is performed.

Phase sequences A, B, and C for the default rising edge transition are illustrated in Figure 12. The PSCNT[6:0] bits from the CS5490 on phase A will have the lowest count, followed by the PSCNT[6:0] bits from the CS5490 on phase B with the middle count, and the PSCNT[6:0] bits from the CS5490 on phase C with the highest count.

Phase sequences C, B, and A for rising edge transition are illustrated in Figure 13. The PSCNT[6:0] bits from the CS5490 on phase C will have the lowest count, followed by the PSCNT[6:0] bits from the CS5490 on phase B with the middle count, and the PSCNT[6:0] bits from the CS5490 on phase A with the highest count.

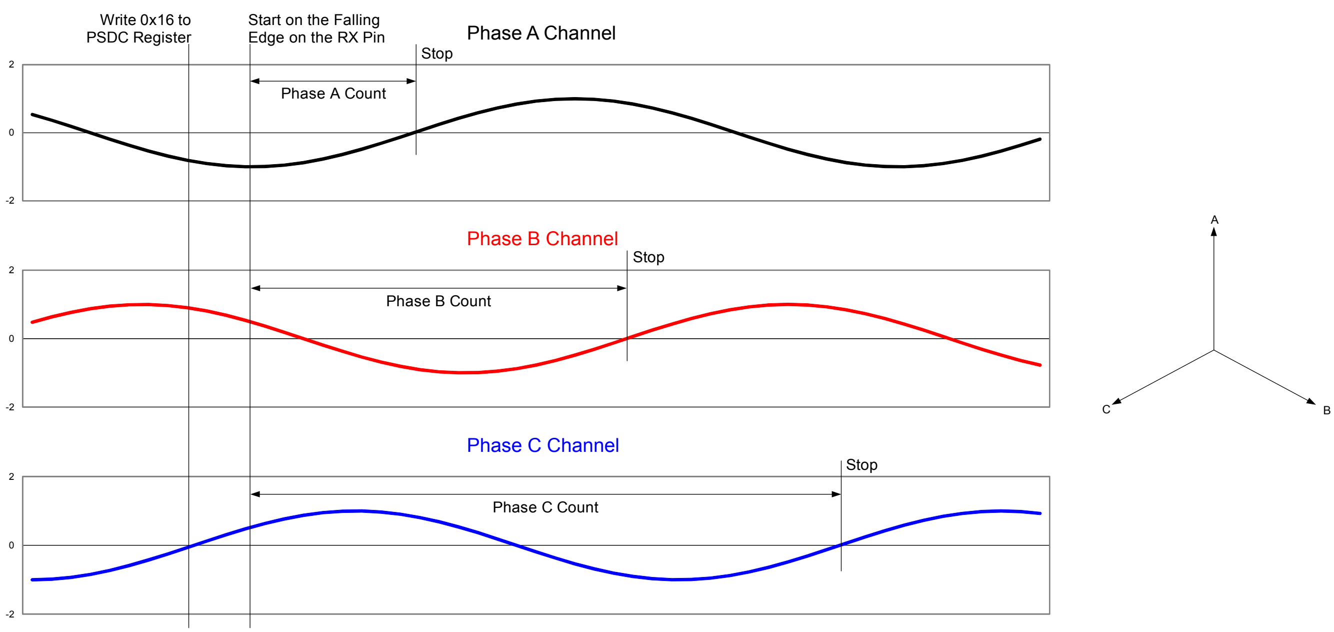


Figure 12. Phase Sequence A, B, C for Rising Edge Transition

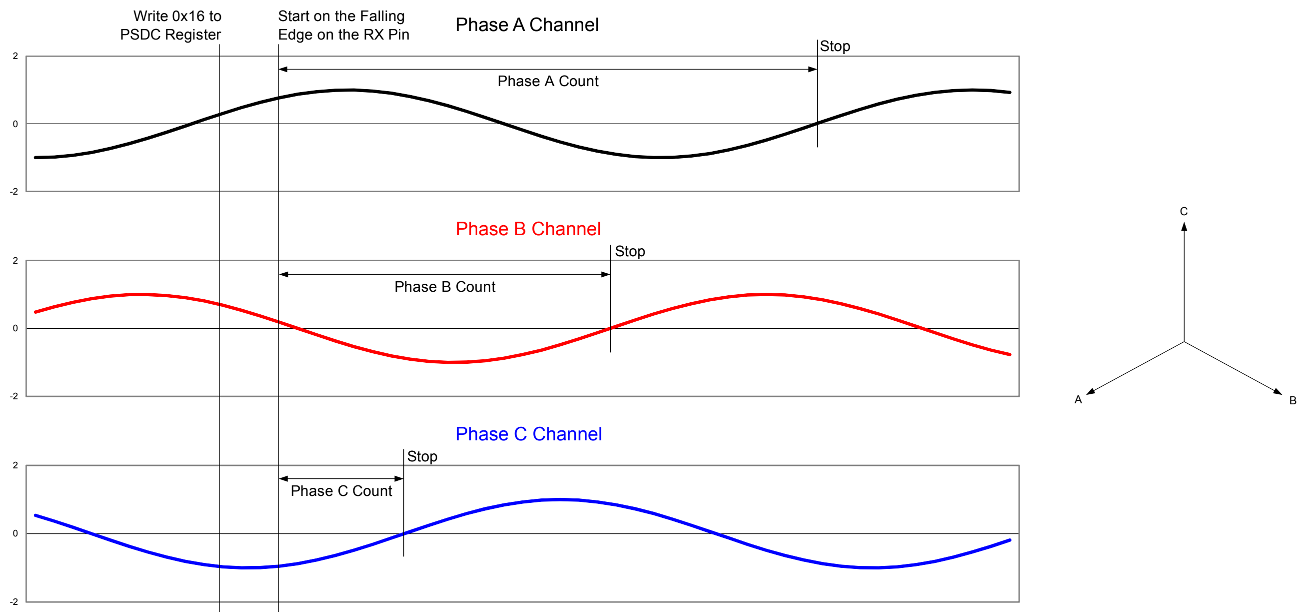


Figure 13. Phase Sequence C, B, A for Rising Edge Transition

5.8 Temperature Measurement

The CS5490 has an internal temperature sensor, which is designed to measure temperature and optionally compensate for temperature drift of the voltage reference. Temperature measurements are stored in the temperature register (*T*), which, by default, is configured to a range of ±128°C.

The application program can change the scale and range of the temperature (*T*) register by changing the temperature gain (T_{GAIN}) register and temperature offset (T_{OFF}) register.

The temperature (*T*) register updates every 2240 output word rate (OWR) samples. The *Status0* register bit TUP indicates when *T* is updated.

5.9 Anti-creep

The anti-creep (no-load threshold) is used to determine if a no-load condition is detected. The $|P_{Sum}|$ and $|Q_{Sum}|$ are compared to the value in the no-load threshold ($Load_{Min}$) register. If both $|P_{Sum}|$ and $|Q_{Sum}|$ are less than this threshold, then P_{Sum} and Q_{Sum} are forced to zero. If S_{Sum} is less than the value in $Load_{Min}$ register, then S_{Sum} is forced to zero.

5.10 Register Protection

To prevent the critical configuration and calibration registers from unintended changes, the CS5490 provides two enhanced register protection mechanisms: write protection and automatic checksum calculation.

5.10.1 Write Protection

Setting the DSP_LCK[4:0] bits in the *RegLock* register to 0x16 enables the CS5490 DSP lockable registers to be write-protected from the calculation engine. Setting the DSP_LCK[4:0] bits to 0x09 disables the write-protection mode.

Setting the HOST_LCK[4:0] bits in the *RegLock* register to 0x16 enables the CS5490 HOST lockable registers to be write-protected from the serial interface. Setting the HOST_LCK[4:0] bits to 0x09 disables the write-protection mode.

For registers that are DSP lockable, HOST lockable, or both, refer to sections *6.2 Hardware Registers Summary (Page 0)* on page 26, *6.3 Software Registers Summary (Page 16)* on page 28, and *6.4 Software Registers Summary (Page 17)* on page 30.

5.10.2 Register Checksum

All the configuration and calibration registers are protected by checksum, if enabled. Refer to sections *6.2 Hardware Registers Summary (Page 0)* on page 26, *6.3 Software Registers Summary (Page 16)* on page 28, and *6.4 Software Registers Summary (Page 17)* on page 30. The checksum for all registers marked with an asterisk symbol (*) is computed at the rate of OWR. The checksum result is stored in the *RegChk* register. After the CS5490 has been fully configured and loaded with the calibrations, the host microcontroller should keep a copy of the checksum (*RegChk_Copy*) in its memory. In normal operation, the host microcontroller can read the *RegChk* register and compare it with the saved copy of the *RegChk* register. If the two values mismatch, a reload of configurations and calibrations into the CS5490 is necessary.

The automatic checksum computation can be disabled by setting the REG_CSUM_OFF bit in the *Config2* register.

6. HOST COMMANDS AND REGISTERS

6.1 Host Commands

The first byte sent to the CS5490 RX pin contains the host command. Four types of host commands are required to read and write registers and instruct the calculation engine. The two most significant bits (MSBs) of the host command defines the function to be performed. The following table depicts the types of commands.

Table 2. Command Format

Function	Binary Value	Note
Register Read	0 0 A_5 A_4 A_3 A_2 A_1 A_0	$A_{[5:0]}$ specifies the register address.
Register Write	0 1 A_5 A_4 A_3 A_2 A_1 A_0	
Page Select	1 0 P_5 P_4 P_3 P_2 P_1 P_0	$P_{[5:0]}$ specifies the page.
Instruction	1 1 C_5 C_4 C_3 C_2 C_1 C_0	$C_{[5:0]}$ specifies the instruction.

6.1.1 Memory Access Commands

The CS5490 memory has 12-bit addresses and is organized as P_5 P_4 P_3 P_2 P_1 P_0 A_5 A_4 A_3 A_2 A_1 A_0 in 64 pages of 64 addresses each. The higher 6 bits specify the page number. The lower 6 bits specify the address within the selected page.

6.1.1.1 Page Select

A page select command is designated by setting the two MSBs of the command to binary ‘10’. The page select command provides the CS5490 with the page number of the register to access. Register read and write commands access 1 of 64 registers within a specified page. Subsequent register reads and writes can be performed once the page has been selected.

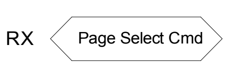


Figure 14. Byte Sequence for Page Select

6.1.1.2 Register Read

A register read is designated by setting the two MSBs of the command to binary ‘00’. The lower 6 bits of the read register command are the lower 6 bits of the 12-bit register address. After the register read command has been received, the CS5490 will send 3 bytes of register data onto the TX pin.

Figure 15. Byte Sequence for Register Read

6.1.1.3 Register Write

A register write command is designated by setting the two MSBs of the command to binary ‘01’. The lower 6 bits of the register write command are the lower 6 bits of the 12-bit register address. A register write command must be followed by 3 bytes of data.

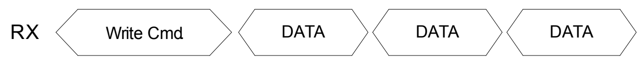


Figure 16. Byte Sequence for Register Write

6.1.2 Instructions

An instruction command is designated by setting the two MSBs of the command to binary '11'. An instruction command will interrupt any process currently running and initiate a new process in the CS5490.

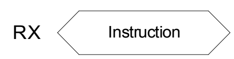


Figure 17. Byte Sequence for Instructions

These new processes include calibration, power control, and soft reset. The following table depicts the types of instructions. Note that when the CS5490 is in continuous conversion mode, an unexpected or invalid instruction command could cause the device to stop continuous conversion and enter an unexpected operation mode. The host processor should keep monitoring the CS5490 operation status and react accordingly.

Table 3. Instruction Format

Function	Binary Value	Note
Controls	0 **C_4 C_3 C_2 C_1 C_0** **0** 00001 - Software Reset **0** 00010 - Standby **0** 00011 - Wakeup **0** 10100 - Single Conv. **0** 10101 - Continuous Conv. **0** 11000 - Halt Conv.	$C_{[5]}$ specifies the instruction type: 0 = Controls 1 = Calibrations
Calibration	1 **C_4 C_3** C_2 C_1 C_0 **1** 00 $C_2C_1C_0$ DC Offset **1** 10 $C_2C_1C_0$ AC Offset* **1** 11 $C_2C_1C_0$ Gain ***AC offset calibration valid only for current channel.**	For calibration, $C_{[4:3]}$ specifies the type of calibration.
	1 C_4 C_3 **C_2 C_1 C_0** **1** C_4C_3 0 0 1 I **1** C_4C_3 0 1 0 V **1** C_4C_3 1 1 0 I & V	For calibration, $C_{[2:0]}$ specifies the channel(s).

6.1.3 Checksum

To improve the communication reliability on the serial interface, the CS5490 provides a checksum mechanism on transmitted and received signals. Checksum is disabled by default but can be enabled by setting the appropriate bit in the *SerialCtrl* register. When enabled, both host and CS5490 are expected to send one additional checksum byte after the normal command byte and applicable 3-byte register data have been transmitted.

The checksum is calculated by subtracting each transmit byte from 0xFF. Any overflow is truncated and the result wraps. The CS5490 executes the command only if the checksum transmitted by the host matches the checksum calculated locally. Otherwise, it sets a status bit (RX_CSUM_ERR in *Status0* register), ignores the command, and clears the serial interface in preparation for the next transmission.

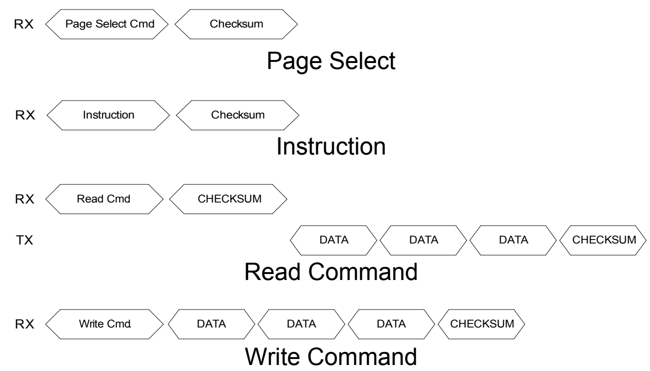


Figure 18. Byte Sequence for Checksum

6.1.4 Serial Time Out

In case a transaction from the host is not completed (for example, a data byte is missing in a register write), a time out circuit will reset the interface after 128 ms. This will require that each byte be sent from the host within 128 ms of the previous byte.