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CS5509

Single-supply, 16-bit A/D Converter

Features

- Delta-sigma A/D Converter
  - 16-bit, No Missing Codes
  - Linearity Error: ±0.0015%FS
- Differential Input
  - Pin-selectable Unipolar/Bipolar Ranges
  - Common Mode Rejection
    105 dB @ dc
    120 dB @ 50, 60 Hz
- Either 5V or 3.3V Digital Interface
- On-chip Self-calibration Circuitry
- Output Update Rates up to 200/second
- Ultra Low Power: 1.7 mW

Description

The CS5509 is a single-supply, 16-bit, serial-output CMOS A/D converter. The CS5509 uses charge-balanced (delta-sigma) techniques to provide low-cost, high-resolution measurements at output word rates up to 200 samples per second.

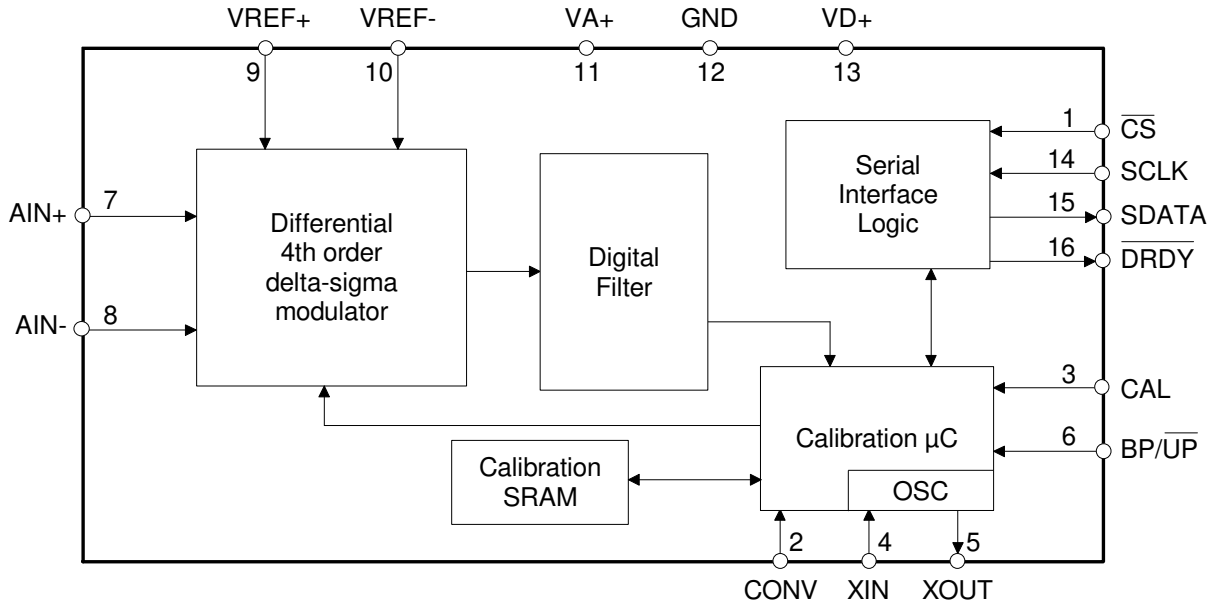
The on-chip digital filter offers superior line rejection at 50Hz and 60Hz when the device is operated from a 32.768 kHz clock (output word rate = 20 Sps).

The CS5509 has on-chip self-calibration circuitry which can be initiated at any time or temperature to ensure minimum offset and full-scale errors.

Low power, high resolution, and small package size make the CS5509 an ideal solution for loop-powered transmitters, panel meters, weigh scales, and battery powered instruments.

ORDERING INFORMATION

CS5509-ASZ	-40 °C to +85 °C	16-pin SOIC	Lead Free



ANALOG CHARACTERISTICS

(T_A = 25 °C; VA+ = 5V ±5%; VD+ = 3.3V ±5%; VREF+ = 2.5V, VREF- = 0V; f_{CLK} = 32.768 kHz; Bipolar Mode; R_{source} = 40 Ω with a 10 nF to GND at AIN; AIN- = 2.5V; unless otherwise specified.) (Notes 1 and 2)

Parameter*			Min	Typ	Max	Unit
Accuracy						
Linearity Error	f_{CLK} = 32.768 kHz f_{CLK} = 165 kHz f_{CLK} = 247.5 kHz f_{CLK} = 330 kHz		- - - -	0.0015 0.0015 0.0015 0.005	0.003 0.003 0.003 0.0125	± %FS ± %FS ± %FS ± %FS
Differential Nonlinearity			-	±0.25	±0.5	LSB
Full-scale Error		(Note 3)	-	±0.25	±2	LSB
Full-scale Drift		(Note 4)	-	±0.5	-	LSB
Unipolar Offset		(Note 3)	-	±0.5	±2	LSB
Unipolar Offset Drift		(Note 4)	-	±0.5	-	LSB
Bipolar Offset		(Note 3)	-	±0.25	±1	LSB
Bipolar Offset Drift		(Note 4)	-	±0.25	-	LSB
Noise (Referred to Output)			-	0.16	-	LSB_{rms}
Analog Input						
Analog Input Range	Unipolar Bipolar	 (Notes 5 and 6)	- -	0 to +2.5 ±2.5	- -	V V
Common Mode Rejection f_{CLK} = 32.768 kHz	dc 50, 60 Hz	 (Note 2)	- 120	105 -	- -	dB dB
Input Capacitance			-	15	-	pF
DC Bias Current		(Note 1)	-	5	-	nA
Power Supplies						
DC Power Supply Currents		I_{Total} I_{Analog} $I_{Digital}$	- - -	350 300 60	450 - -	µA µA µA
Power Dissipation		(Note 7)	-	1.7	2.25	mW
Power Supply Rejection			-	80	-	dB

Notes:
1. Both source resistance and shunt capacitance are critical in determining the CS5509's source impedance requirements. Refer to the text section Analog Input Impedance Considerations.
2. Specifications guaranteed by design, characterization and/or test.
3. Applies after calibration at the temperature of interest.
4. Total drift over the specified temperature range since calibration at power-up at 25 °C.
5. The input is differential. Therefore, GND ≤ Signal + Common Mode Voltage ≤ VA+.
6. The CS5509 can accept input voltages up to the VA+ analog supply. In unipolar mode the CS5509 will output all 1's if the dc input magnitude ((AIN+) - (AIN-)) exceeds ((VREF+) - (VREF-)) and will output all 0's if the input becomes more negative than 0 Volts. In bipolar mode the CS5509 will output all 1's if the dc input magnitude ((AIN+) - (AIN-)) exceeds ((VREF+) - (VREF-)) and will output all 0's if the input becomes more negative in magnitude than -((VREF+) - (VREF-)).
7. All outputs unloaded. All inputs CMOS levels.

* Refer to the Specification Definitions immediately following the Pin Description Section.

DYNAMIC CHARACTERISTICS

Parameter	Symbol	Ratio	Unit
Modulator Sampling Frequency	f_s	$f_{clk}/2$	Hz
Output Update Rate (CONV = 1)	f_{out}	$f_{clk}/1622$	Hz
Filter Corner Frequency	f_{-3dB}	$f_{clk}/1928$	Hz
Settling Time to 1/2 LSB (FS Step)	t_s	$1/f_{out}$	s

5V DIGITAL CHARACTERISTICS (T_A = 25 °C; VA+, VD+ = 5V ±5%; GND = 0) (Notes 2 and 8)

Parameter		Symbol	Min	Typ	Max	Unit
High-level Input Voltage	XIN	V_{IH}	3.5	-	-	V
	All Pins Except XIN		2.0	-	-	V
Low-level Input Voltage	XIN	V_{IL}	-	-	1.5	V
	All Pins Except XIN		-	-	0.8	V
High-level Output Voltage	(Note 9)	V_{OH}	(VD+) -1.0	-	-	V
Low-level Output Voiltage	I_{out} = 1.6 mA	V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	±1	±10	µA
3-State Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

Notes: 8. All measurements are performed under static conditions.

9. I_{out} = -100 µA. This guarantees the ability to drive one TTL load. (V_{OH} = 2.4 V at I_{out} = -40 µA).

3.3V DIGITAL CHARACTERISTICS (T_A = 25 °C; VA+ = 5V ±5%; VD+ = 3.3V ±5%; GND = 0) (Notes 2 and 8)

Parameter		Symbol	Min	Typ	Max	Unit
High-level Input Voltage	XIN	V_{IH}	0.7 VD+	-	-	V
	All Pins Except XIN		0.6 VD+	-	-	V
Low-level Input Voltage	XIN	V_{IL}	-	-	0.3 VD+	V
	All Pins Except XIN		-	-	0.16 VD+	V
High-level Output Voltage	(Note 9)	V_{OH}	(VD+) -0.3	-	-	V
Low-level Output Voltage	I_{out} = 1.6 mA	V_{OL}	-	-	0.3	V
Input Leakage Current		I_{in}	-	±1	±10	µA
3-state Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

Specifications are subject to change without notice

5V SWITCHING CHARACTERISTICS (T_A = 25 °C; VA+, VD+ = 5V ±5%;
Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF) (Note 2)

Parameter			Symbol	Min	Typ	Max	Unit
Master Clock Frequency	Internal Oscillator External Clock		XIN f_{clk}	30.0 30	32.768 -	53.0 330	kHz kHz
Master Clock Duty Cycle				40	-	60	%
Rise Times	Any Digital Input Any Digital Output	(Note 10)	 t_{rise}	- -	- 50	1.0 -	µs ns
Fall Time	Any Digital Input Any Digital Output	(Note 10)	 t_{fall}	- -	- 20	1.0 -	µs ns
Start-Up							
Power-On Reset Period		(Note 11)	t_{res}	-	10	-	ms
Oscillator Start-up Time	XTAL = 32.768 kHz	(Note 12)	t_{osu}	-	500	-	ms
Wake-up Period		(Note 13)	t_{wup}	-	$1800/f_{clk}$	-	s
Calibration							
CONV Pulse Width (CAL = 1)		(Note 14)	t_{ccw}	100	-	-	ns
CONV and CAL High to Start of Calibration			t_{scl}	-	-	$2/f_{clk}+200$	ns
Start of Calibration to End of Calibration			t_{cal}	-	$3246/f_{clk}$	-	s
Conversion							
CONV Pulse Width			t_{cpw}	100	-	-	ns
CONV High to Start of Conversion			t_{scn}	-	-	$2/f_{clk}+200$	ns
Set Up Time	BP/$\overline{UP}$ stable prior to $\overline{DRDY}$ falling		t_{bus}	$82/f_{clk}$	-	-	s
Hold Time	BP/$\overline{UP}$ stable after $\overline{DRDY}$ falls		t_{buh}	0	-	-	ns
Start of Conversion to End of Conversion		(Note 15)	t_{con}	-	$1624/f_{clk}$	-	s

Notes: 10. Specified using 10% and 90% points on waveform of interest.

11. An internal power-on-reset is activated whenever power is applied to the device.

12. Oscillator start-up time varies with the crystal parameters. This specification does not apply when using an external clock source.

13. The wake-up period begins once the oscillator starts; or when using an external f_{clk}, after the power-on reset time elapses.

14. Calibration can also be initiated by pulsing CAL high while CONV=1.

15. Conversion time will be $1622/f_{clk}$ if CONV remains high continuously.

3.3V SWITCHING CHARACTERISTICS (T_A = 25 °C; VA+ = 5V ±5%; VD+ = 3.3V ±5%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF) (Note 2)

Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Frequency	Internal Oscillator External Clock	XIN f_{clk}	30.0 30	32.768 -	53.0 330	kHz kHz
Master Clock Duty Cycle			40	-	60	%
Rise Times	Any Digital Input (Note 10) Any Digital Output	 t_{rise}	- -	- 50	1.0 -	µs ns
Fall Time	Any Digital Input (Note 10) Any Digital Output	 t_{fall}	- -	- 20	1.0 -	µs ns
Start-Up						
Power-On Reset Period	(Note 11)	t_{res}	-	10	-	ms
Oscillator Start-up Time	XTAL = 32.768 kHz (Note 12)	t_{osu}	-	500	-	ms
Wake-up Period	(Note 13)	t_{wup}	-	$1800/f_{clk}$	-	s
Calibration						
CONV Pulse Width (CAL = 1)	(Note 14)	t_{ccw}	100	-	-	ns
CONV and CAL High to Start of Calibration		t_{scl}	-	-	$2/f_{clk}+200$	ns
Start of Calibration to End of Calibration		t_{cal}	-	$3246/f_{clk}$	-	s
Conversion						
CONV Pulse Width		t_{cpw}	100	-	-	ns
CONV High to Start of Conversion		t_{scn}	-	-	$2/f_{clk}+200$	ns
Set Up Time	BP/$\overline{UP}$ stable prior to $\overline{DRDY}$ falling	t_{bus}	$82/f_{clk}$	-	-	s
Hold Time	BP/$\overline{UP}$ stable after $\overline{DRDY}$ falls	t_{buh}	0	-	-	ns
Start of Conversion to End of Conversion	(Note 15)	t_{con}	-	$1624/f_{clk}$	-	s

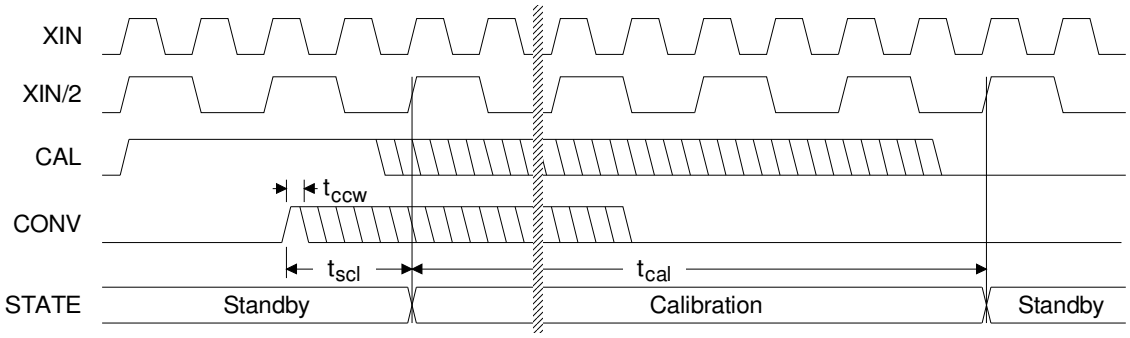


Figure 1. Calibration Timing (Not to Scale)

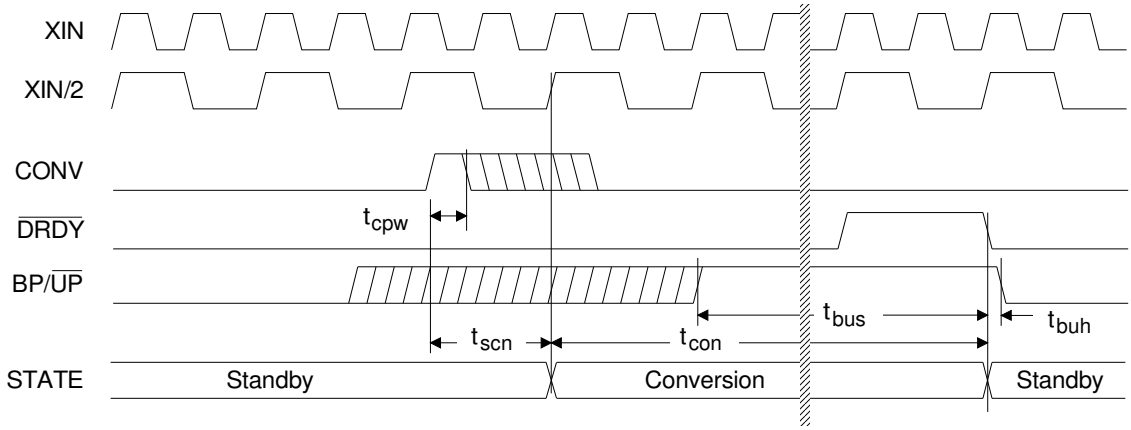


Figure 2. Conversion Timing (Not to Scale)

5V SWITCHING CHARACTERISTICS (T_A = 25 °C; VA+, VD+ = 5V ±5%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF) (Note 2)

Parameter		Symbol	Min	Typ	Max	Unit
Serial Clock		f_{sclk}	0	-	2.5	MHz
Serial Clock	Pulse Width High	t_{ph}	200	-	-	ns
	Pulse Width Low	t_{pl}	200	-	-	ns
Access Time	$\overline{CS}$ Low to data valid (Note 16)	t_{csd}	-	60	200	ns
Maximum Delay Time SCLK falling to new SDATA bit	(Note 17)	t_{dd}	-	150	310	ns
Output Float Delay	$\overline{CS}$ High to output Hi-Z (Note 18)	t_{fd1}	-	60	150	ns
	SCLK falling to Hi-Z	t_{fd2}	-	160	300	ns

Notes: 16. If $\overline{CS}$ is activated asynchronously to $\overline{DRDY}$, $\overline{CS}$ will not be recognized if it occurs when $\overline{DRDY}$ is high for 2 clock cycles. The propagation delay time may be as great as 2 f_{clk} cycles plus 200 ns. To guarantee proper clocking of SDATA when using asynchronous $\overline{CS}$, SCLK(i) should not be taken high sooner than 2 f_{clk} + 200 ns after $\overline{CS}$ goes low.

17. SDATA transitions on the falling edge of SCLK. Note that a rising SCLK must occur to enable the serial port shifting mechanism before falling edges can be recognized.

18. If $\overline{CS}$ is returned high before all data bits are output, the SDATA output will complete the current data bit and then go to high impedance.

3.3V SWITCHING CHARACTERISTICS (T_A = 25 °C; VA+ = 5V ±5%; VD+ = 3.3V ±5%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF) (Note 2)

Parameter		Symbol	Min	Typ	Max	Unit
Serial Clock		f_{sclk}	0	-	1.25	MHz
Serial Clock	Pulse Width High	t_{ph}	200	-	-	ns
	Pulse Width Low	t_{pl}	200	-	-	ns
Access Time	$\overline{CS}$ Low to data valid (Note 16)	t_{csd}	-	100	200	ns
Maximum Delay Time SCLK falling to new SDATA bit	(Note 17)	t_{dd}	-	400	600	ns
Output Float Delay	$\overline{CS}$ High to output Hi-Z (Note 18)	t_{fd1}	-	70	150	ns
	SCLK falling to Hi-Z	t_{fd2}	-	320	500	ns

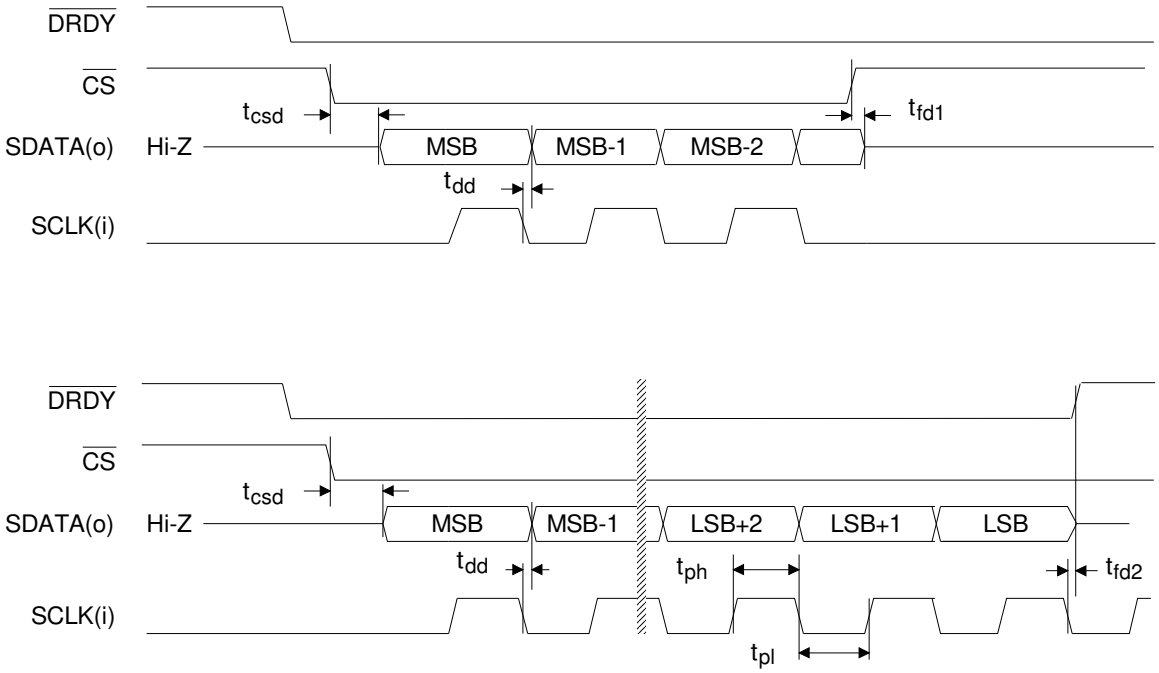


Figure 3. Timing Relationships (Not to Scale)

RECOMMENDED OPERATING CONDITIONS (DGND = 0V) (Note 19)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	Positive Digital	VD+	3.15	5.0	5.5	V
	Positive Analog	VA+	4.75	5.0	5.5	V
Analog Reference Voltage	(Note 20)	(VREF+) - (VREF-)	1.0	2.5	3.6	V
Analog Input Voltage	(Note 6)					
	Unipolar	VAIN	0	-	(VREF+) - (VREF-)	V
	Bipolar	VAIN	-((VREF+) - (VREF-))	-	(VREF+) - (VREF-)	V

Notes: 19. All voltages with respect to ground.

20. The CS5509 can be operated with a reference voltage as low as 100 mV; but with a corresponding reduction in noise-free resolution. The common mode voltage of the voltage reference may be any value as long as +VREF and -VREF remain inside the supply values of VA+ and GND.

ABSOLUTE MAXIMUM RATINGS*

Parameter			Symbol	Min	Typ	Max	Unit
DC Power Supplies	Ground	(Note 21)	GND	-0.3	-	(VD+)-0.3	V
	Positive Digital	(Note 22)	VD+	-0.3	-	6.0	V
	Positive Analog		VA+	-0.3	-	6.0	V
Input Current, Any Pin Except Supplies		(Notes 23 and 24)	I_{in}	-	-	±10	mA
Output Current			I_{out}	-	-	±25	mA
Power Dissipation (Total)		(Note 25)		-	-	500	mW
Analog Input Voltage		AIN and VREF pins	V_{INA}	-0.3	-	(VA+)+0.3	V
Digital Input Voltage			V_{IND}	-0.3	-	(VD+)+0.3	V
Ambient Operating Temperature			T_A	-40	-	85	°C
Storage Temperature			T_{stg}	-65	-	150	°C

Notes: 21. No pin should go more positive than (VA+) + 0.3 V.

22. VD+ must always be less than (VA+) + 0.3 V, and can never exceed +6.0 V.

23. Applies to all pins including continuous overvoltage conditions at the analog input (AIN) pin.

24. Transient currents of up to 100 mA will not cause SCR latch-up. Maximum input current for a power supply pin is ± 50 mA.

25. Total power dissipation, including all input currents and output currents.

*WARNING:Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

GENERAL DESCRIPTION

The CS5509 is a low power, 16-bit, monolithic CMOS A/D converter designed specifically for measurement of dc signals. The CS5509 includes a delta-sigma charge-balance converter, a voltage reference, a calibration microcontroller with SRAM, a digital filter and a serial interface.

The CS5509 is optimized to operate from a 32.768 kHz crystal but can be driven by an external clock whose frequency is between 30kHz and 330kHz. When the digital filter is operated with a 32.768 kHz clock, the filter has zeros precisely at 50 and 60 Hz line frequencies and multiples thereof.

The CS5509 uses a "start convert" command to start a convolution cycle on the digital filter. Once the filter cycle is completed, the output port is updated.When operated with a 32.768kHz clock the ADC converts and updates its output port at 20 samples/sec.The output port operates in a synchronous externally-clocked interface format.

THEORY OF OPERATION

Basic Converter Operation

The CS5509 A/D converter has three operating states. These are stand-by, calibration, and conversion. When power is first applied, an internal power-on reset delay of about 10 ms resets all of the logic in the device. The oscillator must then begin oscillating before the device can be considered functional. After the power-on reset is applied, the device enters the wake-up period for 1800 clock cycles after clock is present. This allows the delta-sigma modulator and other circuitry (which are operating with very low currents) to reach a stable bias condition prior to entering into either the calibration or conversion states. During the 1800 cycle wake-up period, the device can accept an input command. Execution of this command will not occur until the complete wake-up period elapses. If no command is given, the device enters the standby state.

Calibration

After the initial application of power, the CS5509 must enter the calibration state prior to performing accurate conversions. During calibration, the chip executes a two-step process. The device first performs an offset calibration and then follows this with a gain calibration. The two calibration steps determine the zero reference point and the full scale reference point of the converter's transfer function. From these points it calibrates the zero point and a gain slope to be used to properly scale the output digital codes when doing conversions.

The calibration state is entered whenever the CAL and CONV pins are high at the same time. The state of the CAL and CONV pins at power-on are recognized as commands, but will not be executed until the end of the 1800 clock cycle wake-up period.

If CAL and CONV become active (high) during the 1800 clock cycle wake-up time, the converter will wait until the wake-up period elapses before executing the calibration. If the wake-up time has elapsed, the converter will be in the standby mode waiting for instruction and will enter the calibration cycle immediately if CAL and CONV become active. The calibration lasts for 3246 clock cycles. Calibration coefficients are then retained in the SRAM (static RAM) for use during conversion.

The state of BP/$\overline{\text{UP}}$ is ignored during calibration but should remain stable throughout the calibration period to minimize noise.

When conversions are performed in unipolar mode or in bipolar mode, the converter uses the same calibration factors to compute the digital output code. The only difference is that in bipolar mode the on-chip microcontroller offsets the computed output word by a code value of 8000H. This means that the bipolar measurement range is not calibrated from full scale positive to full scale negative. Instead it is calibrated from the bipolar zero scale point to full scale positive. The slope factor is then extended below bipolar zero to accommodate the negative in-

put signals. The converter can be used to convert both unipolar and bipolar signals by changing the BP/$\overline{UP}$ pin. Recalibration is not required when switching between unipolar and bipolar modes.

At the end of the calibration cycle, the on-chip microcontroller checks the logic state of the CONV signal. If the CONV input is low the device will enter the standby mode where it waits for further instruction. If the CONV signal is high at the end of the calibration cycle, the converter will enter the conversion state and perform a conversion on the input channel. The CAL signal can be returned low any time after calibration is initiated. CONV can also be returned low, but it should never be taken low and then taken back high until the calibration period has ended and the converter is in the standby state. If CONV is taken low and then high again with CAL high while the converter is calibrating, the device will interrupt the current calibration cycle and start a new one. If CAL is taken low and CONV is taken low and then high during calibration, the calibration cycle will continue as the conversion command is disregarded. The state of BP/$\overline{UP}$ is not important during calibrations.

If an "end of calibration" signal is desired, pulse the CAL signal high while leaving the CONV signal high continuously. Once the calibration is completed, a conversion will be performed. At the end of the conversion, $\overline{DRDY}$ will fall to indicate the first valid conversion after the calibration has been completed.

Conversion

The conversion state can be entered at the end of the calibration cycle, or whenever the converter is idle in the standby mode. If CONV is taken high to initiate a calibration cycle (CAL also high), and remains high until the calibration cycle is completed (CAL is taken low after CONV transitions high), the converter will begin a conversion upon completion of the calibration period.

The BP/$\overline{UP}$ pin is not a latched input. The BP/$\overline{UP}$ pin controls how the output word from the digital filter is processed. In bipolar mode the output word computed by the digital filter is offset by 8000H (see Understanding Converter Calibration). BP/$\overline{UP}$ can be changed after a conversion is started as long as it is stable for 82 clock cycles of the conversion period prior to $\overline{DRDY}$ falling. If one wishes to intermix measurement of bipolar and unipolar signals on various input signals, it is best to switch the BP/$\overline{UP}$ pin immediately after $\overline{DRDY}$ falls and leave BP/$\overline{UP}$ stable until $\overline{DRDY}$ falls again.

The digital filter in the CS5509 has a Finite Impulse Response and is designed to settle to full accuracy in one conversion time.

If CONV is left high, the CS5509 will perform continuous conversions. The conversion time will be 1622 clock cycles. If conversion is initiated from the standby state, there may be up to two XIN clock cycles of uncertainty as to when conversion actually begins. This is because the internal logic operates at one half the external clock rate and the exact phase of the internal clock may be 180° out of phase relative to the XIN clock. When a new conversion is initiated from the standby state, it will take up to two XIN clock cycles to begin. Actual conversion will use 1624 clock cycles before $\overline{DRDY}$ goes low to indicate that the serial port has been updated. See the Serial Interface Logic section of the data sheet for information on reading data from the serial port.

In the event the A/D conversion command (CONV going positive) is issued during the conversion state, the current conversion will be terminated and a new conversion will be initiated.

Voltage Reference

The CS5509 uses a differential voltage reference input. The positive input is VREF+ and the negative input is VREF-. The voltage between VREF+ and VREF- can range from 1 volt minimum to 3.6 volts maximum. The gain slope will track changes

in the reference without recalibration, accommodating ratiometric applications.

Analog Input Range

The analog input range is set by the magnitude of the voltage between the VREF+ and VREF- pins. In unipolar mode the input range will equal the magnitude of the voltage reference. In bipolar mode the input voltage range will equate to plus and minus the magnitude of the voltage reference. While the voltage reference can be as great as 3.6 volts, its common mode voltage can be any value as long as the reference inputs VREF+ and VREF- stay within the supply voltages VA+ and GND. The differential input voltage can also have any common mode value as long as the maximum signal magnitude stays within the supply voltages.

The A/D converter is intended to measure dc or low frequency inputs. It is designed to yield accurate conversions even with noise exceeding the input voltage range as long as the spectral components of this noise will be filtered out by the digital filter. For example, with a 3.0 volt reference in unipolar mode, the converter will accurately convert an input dc signal up to 3.0volts with up to 15% overrange for 60Hz noise. A 3.0volt dc signal could have a 60Hz component which is 0.5volts above the maximum input of 3.0 (3.5 volts peak; 3.0 volts dc plus 0.5 volts peak noise) and still accurately convert the input signal (XIN = 32.768 kHz). This assumes that the signal plus noise amplitude stays within the supply voltages.

The CS5509 converters output data in binary format when converting unipolar signals and in offset binary format when converting bipolar signals. Table 1 outlines the output coding for both unipolar and bipolar measurement modes.

Converter Performance

The CS5509 A/D converter has excellent linearity performance. Calibration minimizes the errors in offset and gain. The CS5509 device has no missing code performance to 16-bits. Figure4 illustrates the DNL of the CS5509. The converter achieves Common Mode Rejection (CMR) at dc of 105dB typical, and CMR at 50 and 60Hz of 120dB typical.

Unipolar Input Voltage	Output Codes	Bipolar Input Voltage
> (VREF - 1.5 LSB)	FFFF	> (VREF - 1.5 LSB)
VREF - 1.5 LSB	FFFF FFFE	VREF - 1.5 LSB
VREF/2 - 0.5 LSB	8000 7FFF	-0.5 LSB
+0.5 LSB	0001 0000	-VREF + 0.5 LSB
< (+0.5 LSB)	0000	< (-VREF + 0.5 LSB)
Note: Table excludes common mode voltage on the signal and reference inputs.		

Table 1. Output Coding

The CS5509 can experience some drift as temperature changes. The CS5509 uses chopper-stabilized techniques to minimize drift. Measurement errors due to offset or gain drift can be eliminated at any time by recalibrating the converter.

Analog Input Impedance Considerations

The analog input of the CS5509 can be modeled as illustrated in Figure 5. Capacitors (15 pF each) are used to dynamically sample each of the inputs (AIN+ and AIN-). Every half XIN cycle the switch alternately connects the capacitor to the output of the buffer and then directly to the AIN pin. Whenever the sample capacitor is switched from the output of the buffer to the AIN pin, a small packet of charge (a dynamic demand of current) is required from the input source to settle the voltage of the sample capacitor to its final value. The voltage on the output of the buffer may differ up to 100 mV from the actual input voltage due to the offset voltage of the buffer. Timing allows one half of a XIN clock cycle for the voltage on the sample capacitor to settle to its final value.

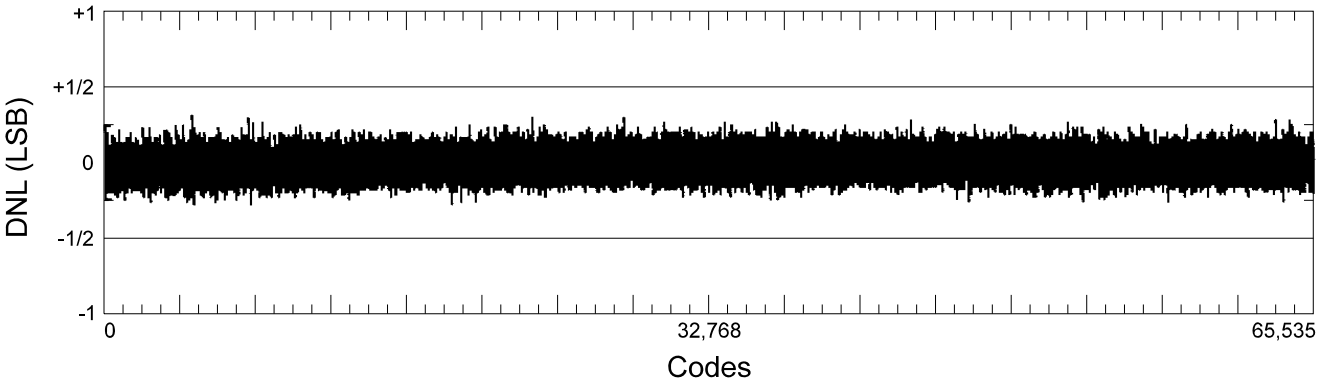


Figure 4. CS5509 Differential Nonlinearity Plot

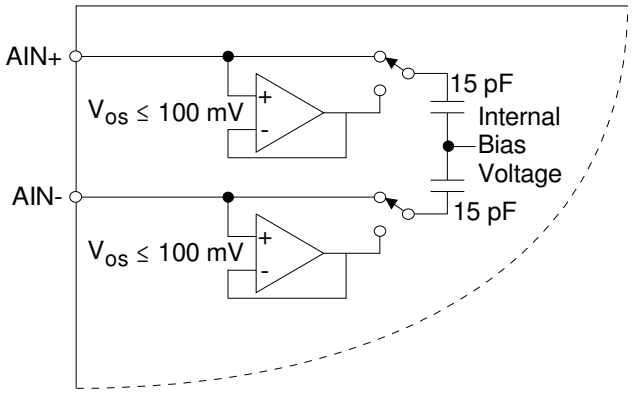


Figure 5. Analog Input Model

An equation for the maximum acceptable source resistance is derived.

$$Rs_{max} = \frac{-1}{2XIN(15pF + C_{EXT})\ln\left[\frac{V_e}{V_e + \frac{15pF(100mV)}{15pF + C_{EXT}}}\right]}$$

This equation assumes that the offset voltage of the buffer is 100 mV, which is the worst case. The value of Ve is the maximum error voltage which is acceptable. C_{EXT} is the combination of any external or stray capacitance.

For a maximum error voltage (Ve) of 10 µV in the CS5509 (1/4LSB at 16-bits), the above equation indicates that when operating from a 32.768 kHz XIN, source resistances up to 110 kΩ are acceptable in the absence of external capacitance (C_{EXT}=0).

The VREF+ and VREF- inputs have nearly the same structure as the AIN+ and AIN- inputs. Therefore, the discussion on analog input impedance applies to the voltage reference inputs as well.

Digital Filter Characteristics

The digital filter in the CS5509 is the combination of a comb filter and a low pass filter. The comb filter has zeros in its transfer function which are optimally placed to reject line interference frequencies (50 and 60 Hz and their multiples) when the CS5509 is clocked at 32.768 kHz. Figures 6, 7 and 8 illustrate the magnitude and phase characteristics of the filter. Figure 6 illustrates the filter attenuation from dc to 260 Hz. At exactly 50, 60, 100, and 120 Hz the filter provides over 120 dB of rejection. Table 2 indicates the filter attenuation for each of the potential line interference frequencies when the converter is operating with a 32.768 kHz clock. The converter yields excellent attenuation of these interference frequencies even if the fundamental line frequency should vary ± 1% from its specified frequency. The -3 dB corner frequency of the filter when operating from a 32.768 kHz clock is 17 Hz. Figure 8 illustrates that the phase characteristics of the filter are precisely linear phase.

If the CS5509 is operated at a clock rate other than 32.768kHz, the filter characteristics, including the comb filter zeros, will scale with the operating clock frequency. Therefore, optimum rejection of

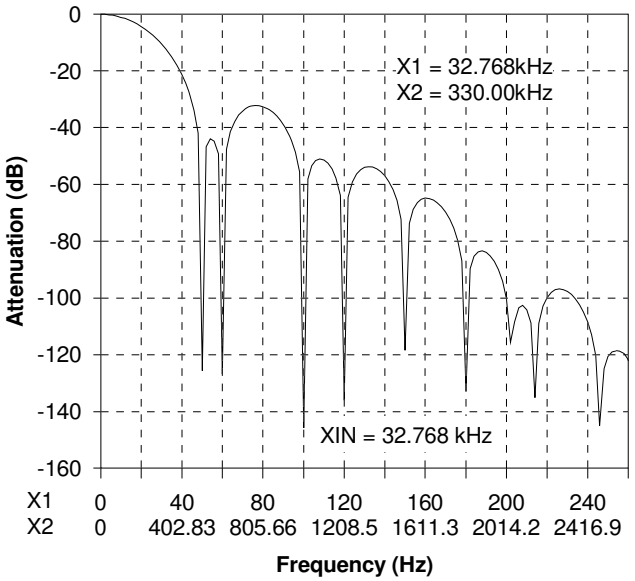


Figure 6. Filter Magnitude Plot to 260 Hz

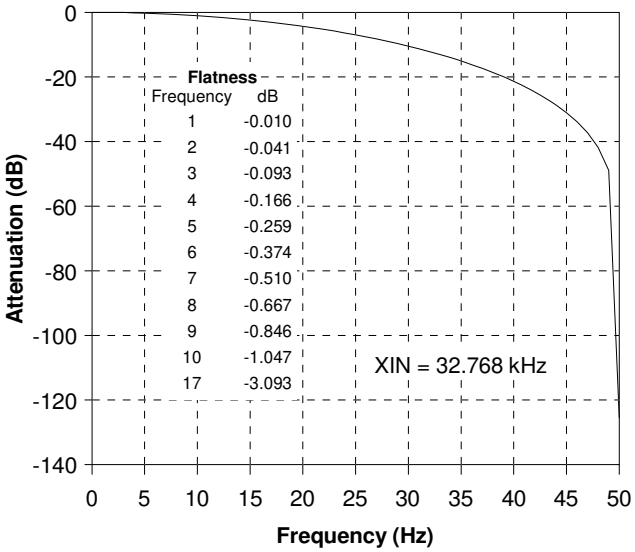


Figure 7. Filter Magnitude Plot to 50 Hz

line frequency interference will occur with the CS5509 running at 32.768kHz.

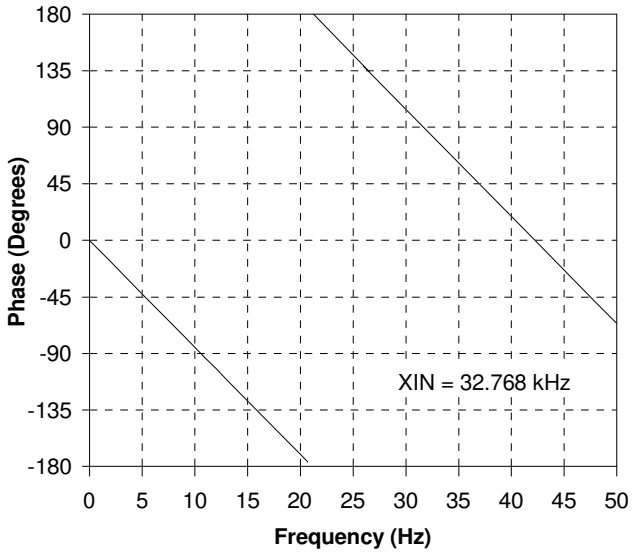


Figure 8. Filter Phase Plot to 50 Hz

Frequency (Hz)	Notch Depth (dB)	Frequency (Hz)	Minimum Attenuation (dB)
50	125.6	50 ±1%	55.5
60	126.7	60 ±1%	58.4
100	145.7	100 ±1%	62.2
120	136.0	120 ±1%	68.4
150	118.4	150 ±1%	74.9
180	132.9	180 ±1%	87.9
200	102.5	200 ±1%	94.0
240	108.4	240 ±1%	104.4

Table 2. Filter Notch Attenuation (XIN = 32.768 kHz)

Anti-Alias Considerations for Spectral Measurement Applications

Input frequencies greater than one half the output word rate (CONV = 1) may be aliased by the converter. To prevent this, input signals should be limited in frequency to no greater than one half the output word rate of the converter (when CONV =1). Frequencies close to the modulator sample rate (XIN/2) and multiples thereof may also be aliased. If the signal source includes spectral components above one half the output word rate (when CONV = 1) these components should be removed by means of low-pass filtering prior to the A/D input

to prevent aliasing. Spectral components greater than one half the output word rate on the VREF inputs (VREF+ and VREF-) may also be aliased. Filtering of the reference voltage to remove these spectral components from the reference voltage is desirable.

Crystal Oscillator

The CS5509 is designed to be operated using a 32.768kHz "tuning fork" type crystal. One end of the crystal should be connected to the XIN input. The other end should be attached to XOUT. Short lead lengths should be used to minimize stray capacitance.

Over the industrial temperature range (-40 to +85 °C) the on-chip gate oscillator will oscillate with other crystals in the range of 30kHz to 53 kHz. The chip will operate with external clock frequencies from 30kHz to 330kHz over the industrial temperature range. The 32.768 kHz crystal is normally specified as a time-keeping crystal with tight specifications for both initial frequency and for drift over temperature. To maintain excellent frequency stability, these crystals are specified only over limited operating temperature ranges (i.e. -10 °C to +60 °C) by the manufacturers. Applications of these crystals with the CS5509 does not require tight initial tolerance or low tempco drift. Therefore, a lower cost crystal with looser initial tolerance and tempco will generally be adequate for use with the CS5509. Also check with the manufacturer about wide temperature range application of their standard crystals. Generally, even those crystals specified for limited temperature range will operate over much larger ranges if frequency stability over temperature is not a requirement. The frequency stability can be as bad as ±3000 ppm over the operating temperature range and still be typically better than the line frequency (50 Hz or 60Hz) stability over cycle-to-cycle during the course of a day.

Serial Interface Logic

The digital filter in the CS5509 takes 1624 clock cycles to compute an output word once a conversion begins. At the end of the conversion cycle, the filter will attempt to update the serial port. Two clock cycles prior to the update $\overline{\text{DRDY}}$ will go high. When $\overline{\text{DRDY}}$ goes high just prior to a port update it checks to see if the port is either empty or unselected ($\overline{\text{CS}}$ = 1). If the port is empty or unselected, the digital filter will update the port with a new output word. When new data is put into the port $\overline{\text{DRDY}}$ will go low.

Reading Serial Data

SDATA is the output pin for the serial data. When $\overline{\text{CS}}$ goes low after new data becomes available ($\overline{\text{DRDY}}$ goes low), the SDATA pin comes out of Hi-Z with the MSB data bit present. SCLK is the input pin for the serial clock. If the MSB data bit is on the SDATA pin, the first rising edge of SCLK enables the shifting mechanism. This allows the falling edges of SCLK to shift subsequent data bits out of the port. Note that if the MSB data bit is output and the SCLK signal is high, the first falling edge of SCLK will be ignored because the shifting mechanism has not become activated. After the first rising edge of SCLK, each subsequent falling edge will shift out the serial data. Once the LSB is present, the falling edge of SCLK will cause the SDATA output to go to Hi-Z and $\overline{\text{DRDY}}$ to return high. The serial port register will be updated with a new data word upon the completion of another conversion if the serial port has been emptied, or if the $\overline{\text{CS}}$ is inactive (high).

$\overline{\text{CS}}$ can be operated asynchronously to the $\overline{\text{DRDY}}$ signal. The $\overline{\text{DRDY}}$ signal need not be monitored as long as the $\overline{\text{CS}}$ signal is taken low for at least two XIN clock cycles plus 200ns prior to SCLK being toggled. This ensures that $\overline{\text{CS}}$ has gained control over the serial port.

Power Supplies and Grounding

The analog and digital supply pins to the CS5509 are brought out on separate pins to minimize noise coupling between the analog and digital sections of the chip. In the digital section of the chip the supply current flows into the VD+ pin and out of the GND pin. As a CMOS device, the CS5509 requires that the supply voltage on the VA+ pin always be more positive than the voltage on any other pin of the device. If this requirement is not met, the device can latch-up or be damaged. In all circumstances the VA+ voltage must remain more positive than the VD+ or GND pins; VD+ must remain more positive than the GND pin.

Figure 9a illustrates the System Connection Diagram for the CS5509. Note that all supply pins are bypassed with 0.1 µF capacitors and that the VD+ digital supply is derived from the VA+ supply. Figure 9b illustrates the CS5509 operating from a +5V analog supply and +3.3V digital supply.

When using separate supplies for VA+ and VD+, VA+ must be established first. VD+ should never become more positive than VA+ under any operating condition. Remember to investigate transient power-up conditions, when one power supply may have a faster rise time.

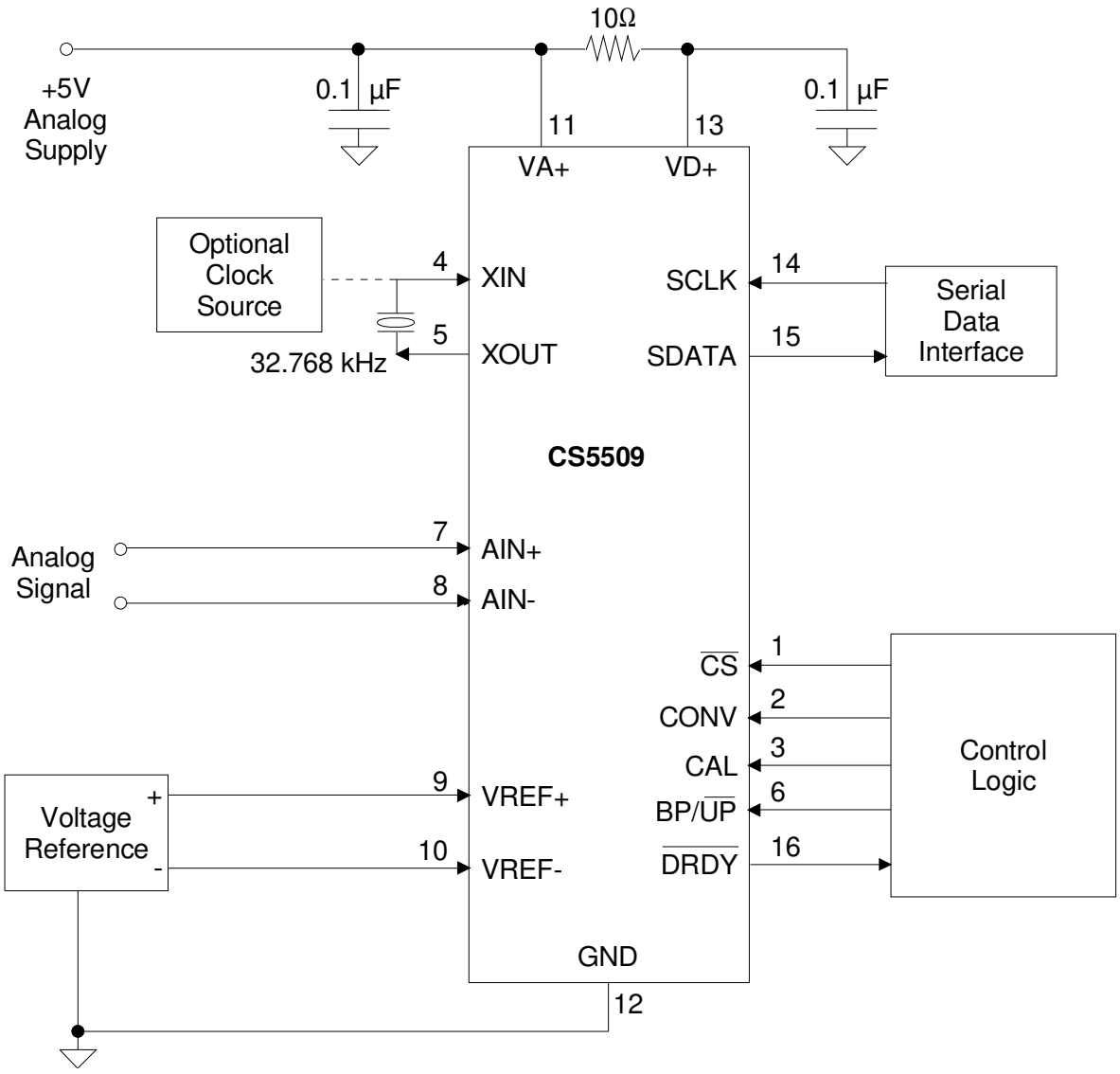


Figure 9a. System Connection Diagram Using a Single Supply

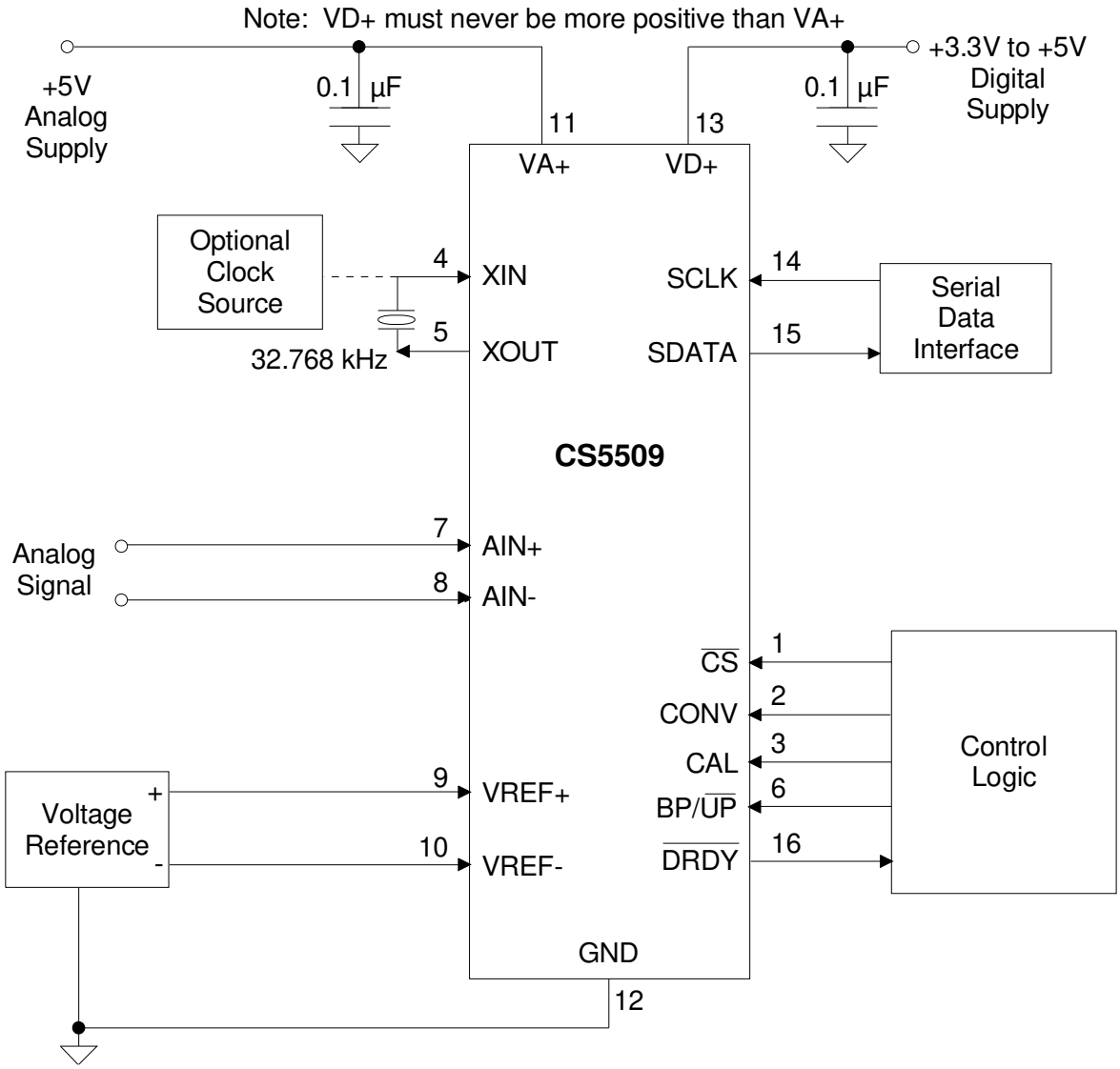
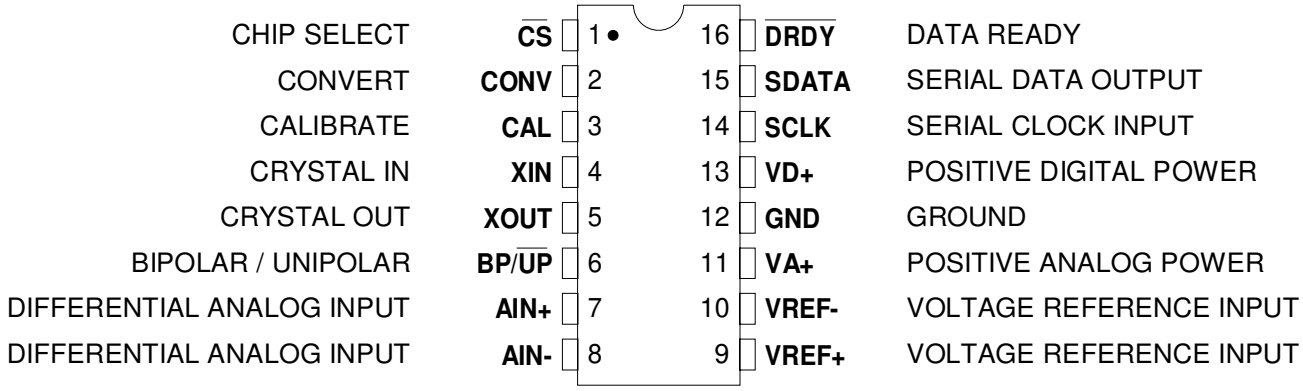


Figure 9b. System Connection Diagram Using Split Supplies

PIN DESCRIPTIONS*



* Pinout applies to both PDIP and SOIC

Clock Generator

XIN; XOUT - Crystal In; Crystal Out, Pins 4, 5.

A gate inside the chip is connected to these pins and can be used with a crystal to provide the master clock for the device. Alternatively, an external (CMOS compatible) clock can be supplied into the XIN pin to provide the master clock for the device. Loss of clock will put the device into a lower powered state (approximately 70% power reduction).

Serial Output I/O

$\overline{CS}$ - Chip Select, Pin 1.

This input allows an external device to access the serial port.

$\overline{DRDY}$ - Data Ready, Pin 16.

Data Ready goes low at the end of a digital filter convolution cycle to indicate that a new output word has been placed into the serial port. $\overline{DRDY}$ will return high after all data bits are shifted out of the serial port or two master clock cycles before new data becomes available if the $\overline{CS}$ pin is inactive (high).

SDATA - Serial Data Output, Pin 15.

SDATA is the output pin of the serial output port. Data from this pin will be output at a rate determined by SCLK. Data is output MSB first and advances to the next data bit on the falling edges of SCLK. SDATA will be in a high impedance state when not transmitting data.

SCLK - Serial Clock Input, Pin 14.

A clock signal on this pin determines the output rate of the data from the SDATA pin. This pin must not be allowed to float.

Control Input Pins

CAL - Calibrate, Pin 3.

When taken high the same time that the CONV pin is taken high the converter will perform a self-calibration which includes calibration of the offset and gain scale factors in the converter.

CONV - Convert, Pin 2.

The CONV pin initiates a calibration cycle if it is taken from low to high while the CAL pin is high, or it initiates a conversion if it is taken from low to high with the CAL pin low. If CONV is held high (CAL low) the converter will do continuous conversions.

BP/$\overline{\text{UP}}$ - Bipolar/Unipolar, Pin 6.

The BP/$\overline{\text{UP}}$ pin selects the conversion mode of the converter. When high the converter will convert bipolar input signals; when low it will convert unipolar input signals.

Measurement and Reference Inputs

AIN+, AIN- - Differential Analog Inputs, Pins 7, 8.

Analog differential inputs to the delta-sigma modulator.

VREF+, VREF- - Differential Voltage Reference Inputs, Pins 9, 10.

A differential voltage reference on these pins operates as the voltage reference for the converter. The voltage between these pins can be any voltage between 1.0 and 3.6 volts.

Power Supply Connections

VA+ - Positive Analog Power, Pin 11.

Positive analog supply voltage. Nominally +5 volts.

VD+ - Positive Digital Power, Pin 13.

Positive digital supply voltage. Nominally +5 volts or +3.3 volts.

GND - Ground, Pin 12.

Ground.

SPECIFICATION DEFINITIONS

Linearity Error

The deviation of a code from a straight line which connects the two endpoints of the A/D Converter transfer function. One endpoint is located 1/2 LSB below the first code transition and the other endpoint is located 1/2 LSB beyond the code transition to all ones. Units in percent of full-scale.

Differential Nonlinearity

The deviation of a code's width from the ideal width. Units in LSBs.

Full Scale Error

The deviation of the last code transition from the ideal [{(VREF+) - (VREF-)} - LSB]. Units are in LSBs.

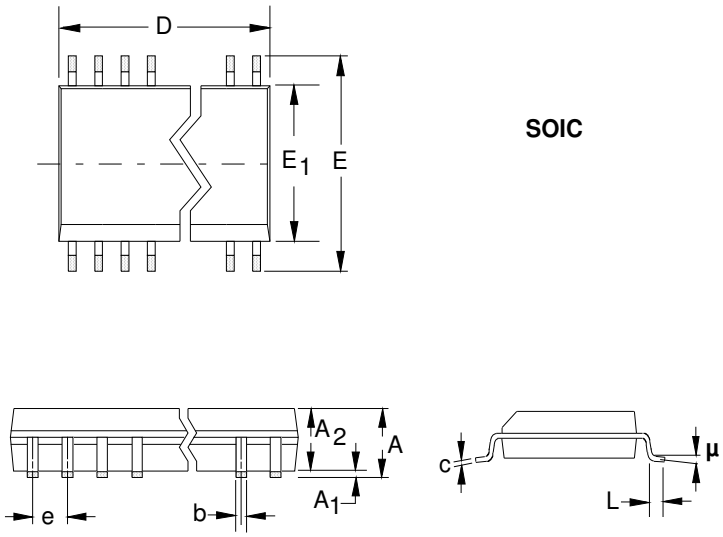
Unipolar Offset

The deviation of the first code transition from the ideal (LSB above the voltage on the AIN- pin.) when in unipolar mode (BP/$\overline{UP}$ low). Units are in LSBs.

Bipolar Offset

The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (LSB below the voltage on the AIN- pin.) when in bipolar mode (BP/$\overline{UP}$ high). Units are in LSBs

PACKAGE DIMENSIONS



SOIC

pins	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
16	9.91	10.16	10.41	0.390	0.400	0.410
20	12.45	12.70	12.95	0.490	0.500	0.510
24	14.99	15.24	15.50	0.590	0.600	0.610
28	17.53	17.78	18.03	0.690	0.700	0.710

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.41	2.54	2.67	0.095	0.100	0.105
A_1	0.127	-	0.300	0.005	-	0.012
A_2	2.29	2.41	2.54	0.090	0.095	0.100
b	0.33	0.46	0.51	0.013	0.018	0.020
c	0.203	0.280	0.381	0.008	0.011	0.015
D	see table above					
E	10.11	10.41	10.67	0.398	0.410	0.420
E_1	7.42	7.49	7.57	0.292	0.295	0.298
e	1.14	1.27	1.40	0.040	0.050	0.055
L	0.41	-	0.89	0.016	-	0.035
μ	0°	-	8°	0°	-	8°

ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model	Peak Relfow Temp	MSL Rating*	Maximum Floor Life
CS5509-ASZ (lead free)	260 °C	3	7 Days

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

REVISION HISTORY

Revision	Date	Changes
F1	Aug '97	First "final" release.
F2	Aug '05	Added lead-free device ordering info. Added legal notice. Added MSL data.
F3	Jul '09	Removed PDIP and leaded (Pb) devices from ordering information.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find the one nearest to you go to www.cirrus.com