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16-bit or 24-bit, 2/4/8-channel ADCs with PGIA

Features

- Low Input Current (100 pA), Chopper-stabilized Instrumentation Amplifier
- Scalable Input Span (Bipolar/Unipolar)
  - 2.5V VREF: 25 mV, 55 mV, 100 mV, 1 V, 2.5 V, 5 V
  - External: 10 V, 100 V
- Wide V_{REF} Input Range (+1 to +5 V)
- Fourth Order Delta-Sigma A/D Converter
- Easy to Use Three-wire Serial Interface Port
  - Programmable/Auto Channel Sequencer with Conversion Data FIFO
  - Accessible Calibration Registers per Channel
  - Compatible with SPI™ and Microwire™
- System and Self Calibration
- Eight Selectable Word Rates
  - Up to 617 Sps (XIN = 200 kHz)
  - Single Conversion Settling
  - 50/60 Hz ±3 Hz Simultaneous Rejection
- Single +5 V Power Supply Operation
  - Charge Pump Drive for Negative Supply
  - +3 to +5 V Digital Supply Operation
- Low Power Consumption: 6.0 mW

General Description

The CS5521/22/23/24/28 are highly integrated ΔΣ analog-to-digital converters (ADCs) which use charge-balance techniques to achieve 16-bit (CS5521/23) and 24-bit (CS5522/24/28) performance. The ADCs come as either two-channel (CS5521/22), four-channel (CS5523/24), or eight-channel (CS5528) devices and include a low-input-current, chopper-stabilized instrumentation amplifier. To permit selectable input spans of 25 mV, 55 mV, 100 mV, 1 V, 2.5 V, and 5 V, the ADCs include a PGA (programmable gain amplifier). To accommodate ground-based thermocouple applications, the devices include a charge pump drive which provides a negative bias voltage to the on-chip amplifiers.

These devices also include a fourth-order ΔΣ modulator followed by a digital filter which provides eight selectable output word rates. The digital filters are designed to settle to full accuracy within one conversion cycle and when operated at word rates below 30 Sps, they reject both 50 Hz and 60 Hz interference.

These single-supply products are ideal solutions for measuring isolated and non-isolated, low-level signals in process control applications.

ORDERING INFORMATION

See page 53.

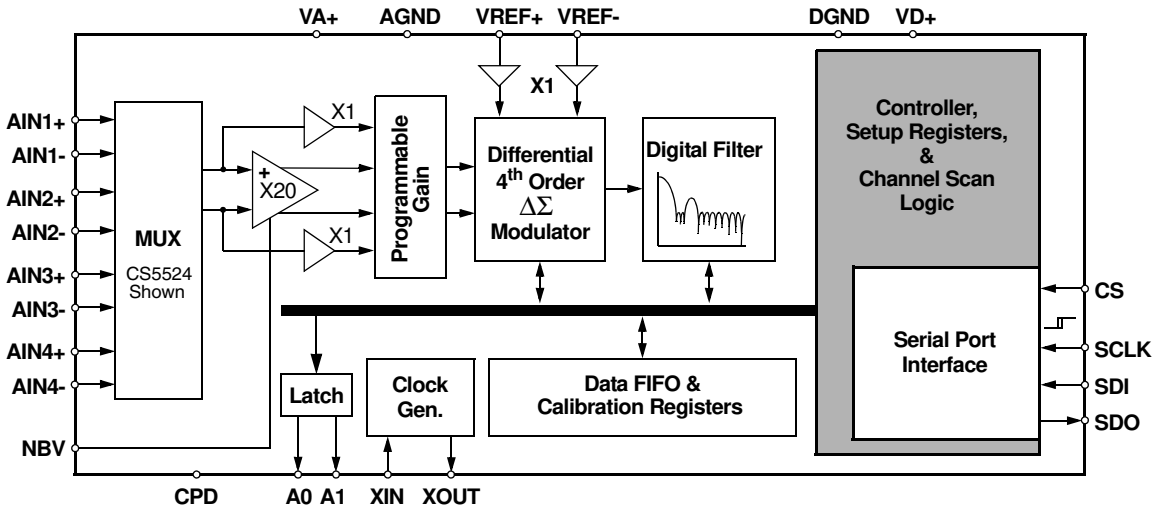

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARACTERISTICS (T_A = 25° C; VA+, VD+ = 5 V ±5%; VREF+ = 2.5 V, VREF- = AGND, NBV = -2.1 V, XIN = 32.768 kHz, CFS1-CFS0 = '00', OWR (Output Word Rate) = 15 Sps, Bipolar Mode, Input Range = ±100 mV; See Notes 1 and 2.)

Parameter	CS5521/23			CS5522/24/28			Unit
	Min	Typ	Max	Min	Typ	Max	
Accuracy							
Resolution	-	-	16	-	-	24	Bits
Linearity Error	-	±0.0015	±0.003	-	±0.0007	±0.0015	%FS
Bipolar Offset (Note 3)	-	±1	±2	-	±16	±32	LSB_N
Unipolar Offset (Note 3)	-	±2	±4	-	±32	±64	LSB_N
Offset Drift (Notes 3 and 4)	-	20	-	-	20	-	nV/°C
Bipolar Gain Error	-	±8	±31	-	±8	±31	ppm
Unipolar Gain Error	-	±16	±62	-	±16	±62	ppm
Gain Drift (Note 4)	-	1	3	-	1	3	ppm/°C
Power Supplies							
Power Supply Currents (Normal Mode)							
I_{A+}	-	1.2	1.6	-	1.5	2.1	mA
(Note 5) I_{D+}	-	110	150	-	110	150	µA
I_{NBV}	-	400	570	-	525	700	µA
Power Consumption (Note 6)							
Normal Mode	-	7.0	10	-	10.1	14.8	mW
Low Power Mode	N/A	N/A	N/A	-	5.5	7.5	mW
Sleep	-	500	-	-	500	-	µW
Power Supply Rejection							
Positive Supplies	-	120	-	-	120	-	dB
dc NBV	-	110	-	-	110	-	dB

Notes:
1. Applies after system calibration at any temperature within -40° C ~ +85° C.
2. Specifications guaranteed by design, characterization, and/or test.
3. Specification applies to the device only and does not include any effects by external parasitic thermocouples. LSB_N: N is 16 for the CS5521/23 and N is 24 for the CS5522/24/28
4. Drift over specified temperature range after calibration at power-up at 25° C.
5. Measured with Charge Pump Drive off.
6. All outputs unloaded. All input CMOS levels and the CS5521/23 do not have a low power mode.

ANALOG CHARACTERISTICS (Continued)

Parameter			Min	Typ	Max	Unit
Analog Input						
Common Mode + Signal on AIN+ or AIN-		Bipolar/Unipolar Mode				
NBV = -1.8 to -2.5 V		Range = 25 mV, 55 mV, or 100 mV	-0.150	-	0.950	V
		Range = 1 V, 2.5 V, or 5 V	NBV	-	VA+	V
NBV = AGND		Range = 25 mV, 55 mV, or 100 mV (Note 7)	1.85	-	2.65	V
		Range = 1 V, 2.5 V, or 5 V	0.0	-	VA+	V
CVF Current on AIN+ or AIN-		(Note 8)				
		Range = 25 mV, 55 mV, or 100 mV	-	100	300	pA
		Range = 1 V, 2.5 V, or 5 V	-	10	-	nA
Input Current Drift		(Note 8)				
		Range = 25 mV, 55 mV, or 100 mV	-	1	-	pA/°C
Input Leakage for Multiplexer when Off			-	10	-	pA
Common Mode Rejection	dc		-	120	-	dB
	50, 60 Hz		-	120	-	dB
Input Capacitance			-	10	-	pF
Voltage Reference Input						
Range	(VREF+) - (VREF-)		1	2.5	VA+	V
VREF+			(VREF-)+1	-	VA+	V
VREF-			NBV	-	(VREF+)-1	V
CVF Current		(Note 8)	-	5.0	-	nA
Common Mode Rejection	dc		-	110	-	dB
	50, 60 Hz		-	130	-	dB
Input Capacitance			-	16	-	pF
System Calibration Specifications						
Full Scale Calibration Range (VREF = 2.5V)		Bipolar/Unipolar Mode				
	25 mV		10	-	32.5	mV
	55 mV		25	-	71.5	mV
	100 mV		40	-	105	mV
	1 V		0.40	-	1.30	V
	2.5 V		1.0	-	3.25	V
	5 V		2.0	-	VA+	V
Offset Calibration Range		Bipolar/Unipolar Mode				
	25 mV		-	-	±12.5	mV
	55 mV		-	-	±27.5	mV
	100 mV	(Note 9)	-	-	±50	mV
	1 V		-	-	±0.5	V
	2.5 V		-	-	±1.25	V
	5 V		-	-	±2.50	V

Notes: 7. For the CS5528, the 25 mV, 55 mV and 100 mV ranges cannot be used unless NBV is powered at -1.8 to -2.5 V

8. See the section of the data sheet which discusses input models. Chop clock is 256 Hz (XIN/128) for PGIA (programmable gain instrumentation amplifier). XIN = 32.768 kHz.

9. The maximum full scale signal can be limited by saturation of circuitry within the internal signal path.

TYPICAL RMS NOISE, CS5521/23 (Notes 10 and 11)

Output Rate (Sps)	-3 dB Filter Frequency	Input Range, (Bipolar/Unipolar Mode)					
		25 mV	55 mV	100 mV	1 V	2.5 V	5 V
1.88	1.64	90 nV	148 nV	220 nV	1.8 µV	3.9 µV	7.8 µV
3.76	3.27	122 nV	182 nV	310 nV	2.6 µV	5.7 µV	11.3 µV
7.51	6.55	180 nV	267 nV	435 nV	3.7 µV	8.5 µV	18.1 µV
15.0	12.7	280 nV	440 nV	810 nV	5.7 µV	14 µV	28 µV
30.0	25.4	580 nV	1.1 µV	2.1 µV	18.2 µV	48 µV	96 µV
61.6 (Note 12)	50.4	2.6 µV	4.9 µV	8.5 µV	92 µV	238 µV	390 µV
84.5 (Note 12)	70.7	11 µV	27 µV	43 µV	458 µV	1.1 mV	2.4 mV
101.1 (Note 12)	84.6	41 µV	72 µV	130 µV	1.2 mV	3.4 mV	6.7 mV

Notes: 10. Wideband noise aliased into the baseband. Referred to the input. Typical values shown for 25° C.

11. To estimate Peak-to-Peak Noise, multiply RMS noise by 6.6 for all ranges and output rates.

12. For input ranges <100 mV and output rates ≥60 Sps, 16.384 kHz chopping frequency is used.

TYPICAL NOISE FREE RESOLUTION (BITS), CS5521/23 (Note 13)

Output Rate (Sps)	-3 dB Filter Frequency	Input Range, (Bipolar Mode)					
		25 mV	55 mV	100 mV	1 V	2.5 V	5 V
1.88	1.64	16	16	16	16	16	16
3.76	3.27	16	16	16	16	16	16
7.51	6.55	15	16	16	16	16	16
15.0	12.7	15	15	15	16	16	16
30.0	25.4	14	14	14	14	14	14
61.6 (Note 12)	50.4	12	12	12	12	12	12
84.5 (Note 12)	70.7	9	9	9	9	9	9
101.1 (Note 12)	84.6	8	8	8	8	8	8

Notes: 13. For bipolar mode, the number of bits of Noise Free Resolution is LOG((2XInput Range)/(6.6xRMS Noise))/LOG(2) rounded to the nearest bit. For unipolar mode, the number of bits of Noise Free Resolution is LOG((Input Range)/(6.6xRMS Noise))/LOG(2) rounded to the nearest bit. Also, the CS5521/23's output conversions are 16 bits. Noise free Resolution numbers are based upon VREF = 2.5 V and XIN = 32.768 kHz. The values will be affected directly by changes in VREF, but the effects due to changes in the XIN frequency will be minor.

TYPICAL RMS NOISE, CS5522/24/28 (Notes 14 and 15)

Output Rate (Sps)	-3 dB Filter Frequency	Input Range, (Bipolar/Unipolar Mode)					
		25 mV	55 mV	100 mV	1 V	2.5 V	5 V
1.88	1.64	90 nV	95 nV	140 nV	1.5 µV	3 µV	6 µV
3.76	3.27	110 nV	130 nV	190 nV	2 µV	4 µV	8 µV
7.51	6.55	170 nV	200 nV	275 nV	2.5 µV	6 µV	11.5 µV
15.0	12.7	250 nV	330 nV	580 nV	4.5 µV	10 µV	20 µV
30.0	25.4	500 nV	1 µV	1.5 µV	16 µV	45 µV	85 µV
61.6 (Note 16)	50.4	2 µV	4 µV	8 µV	72 µV	195 µV	350 µV
84.5 (Note 16)	70.7	10 µV	20 µV	35 µV	340 µV	900 µV	2 mV
101.1 (Note 16)	84.6	30 µV	60 µV	105 µV	1.1 mV	3 mV	5.3 mV

Notes: 14. Wideband noise aliased into the baseband. Referred to the input. Typical values shown for 25° C.

15. To estimate Peak-to-Peak Noise, multiply RMS noise by 6.6 for all ranges and output rates.

16. For input ranges <100 mV and output rates ≥60 Sps, 16.384 kHz chopping frequency is used.

TYPICAL NOISE FREE RESOLUTION (BITS), CS5522/24/28 (Note 17)

Output Rate (Sps)	-3 dB Filter Frequency	Input Range, (Bipolar Mode)					
		25 mV	55 mV	100 mV	1 V	2.5 V	5 V
1.88	1.64	16	17	18	18	18	18
3.76	3.27	16	17	17	17	18	18
7.51	6.55	15	16	17	17	17	17
15.0	12.7	15	16	16	16	16	16
30.0	25.4	14	14	14	14	14	14
61.6 (Note 16)	50.4	12	12	12	12	12	12
84.5 (Note 16)	70.7	10	10	10	10	10	10
101.1 (Note 16)	84.6	8	8	8	8	8	8

Notes: 17. For bipolar mode, the number of bits of Noise Free Resolution is LOG((2XInput Range)/(6.6xRMS Noise))/LOG(2) rounded to the nearest bit. For unipolar mode, the number of bits of Noise Free Resolution is LOG((Input Range)/(6.6xRMS Noise))/LOG(2) rounded to the nearest bit. Also, the CS5522/24/28's output conversions are 24 bits. Noise free Resolution numbers are based upon VREF = 2.5 V and XIN = 32.768 kHz. The values will be affected directly by changes in VREF, but the effects due to changes in the XIN frequency will be minor.

5 V DIGITAL CHARACTERISTICS (T_A = 25° C; VA+, VD+ = 5 V ±5%; GND = 0; See Notes 2 and 18.))

Parameter		Symbol	Min	Typ	Max	Unit
High-level Input Voltage	All Pins Except XIN and SCLK	V_{IH}	0.6 VD+	-	-	V
	XIN		(VD+)-0.5	-	-	V
	SCLK		(VD+) - 0.45	-	-	V
Low-level Input Voltage	All Pins Except XIN and SCLK	V_{IL}	-	-	0.8	V
	XIN		-	-	1.5	V
	SCLK		-	-	0.6	V
High-level Output Voltage		V_{OH}				
	All Pins Except CPD and SDO (Note 19)		(VA+) - 1.0	-	-	V
	CPD, I_{out} = -4.0 mA		(VD+) - 1.0	-	-	V
	SDO, I_{out} = -5.0 mA		(VD+) - 1.0	-	-	V
Low-level Output Voltage		V_{OL}				
	All Pins Except CPD and SDO, I_{out} = 1.6 mA		-	-	0.4	V
	CPD, I_{out} = 2 mA		-	-	0.4	V
	SDO, I_{out} = 5.0 mA		-	-	0.4	V
Input Leakage Current		I_{in}	-	±1	±10	µA
3-state Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

Notes: 18. All measurements performed under static conditions.

19. I_{out} = -100 µA unless stated otherwise. (V_{OH} = 2.4 V @ I_{out} = -40 µA.)

3 V DIGITAL CHARACTERISTICS (T_A = 25° C; VA+ = 5 V ±5%; VD+ = 3.0 V ±10%; GND = 0; See Notes 2 and 18.)

Parameter		Symbol	Min	Typ	Max	Unit
High-level Input Voltage	All Pins Except XIN and SCLK	V_{IH}	0.6 VD+	-	-	V
	XIN		(VD+)-0.5	-	-	V
	SCLK		(VD+) - 0.45	-	-	V
Low-level Input Voltage	All Pins Except XIN and SCLK	V_{IL}	-	-	0.16 VD+	V
	XIN		-	-	0.3	V
	SCLK		-	-	0.6	V
High-level Output Voltage		V_{OH}				
	All Pins Except CPD and SDO, I_{out} = -400 µA		(VA+) - 0.3	-	-	V
	CPD, I_{out} = -4.0 mA		(VD+) - 1.0	-	-	V
	SDO, I_{out} = -5.0 mA		(VD+) - 1.0	-	-	V
Low-level Output Voltage		V_{OL}				
	All Pins Except CPD and SDO, I_{out} = 400 µA		-	-	0.3	V
	CPD, I_{out} = 2 mA		-	-	0.4	V
	SDO, I_{out} = 5.0 mA		-	-	0.4	V
Input Leakage Current		I_{in}	-	±1	±10	µA
3-state Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

DYNAMIC CHARACTERISTICS

Parameter	Symbol	Ratio	Unit
Modulator Sampling Frequency	f_s	XIN/4	Hz
Filter Settling Time to 1/2 LSB (Full-scale Step)	t_s	$1/f_{out}$	s

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0 V; See Note 20.)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	Positive Digital	VD+	2.7	5.0	5.25	V
	Positive Analog	VA+	4.75	5.0	5.25	V
Analog Reference Voltage	(VREF+) - (VREF-)	$VRef_{diff}$	1.0	2.5	VA+	V
Negative Bias Voltage		NBV	-1.8	-2.1	-2.5	V

Notes: 20. All voltages with respect to ground.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0 V; See Note 20.)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	(Note 21)					
	Positive Digital	VD+	-0.3	-	+6.0	V
	Positive Analog	VA+	-0.3	-	+6.0	V
Negative Bias Voltage	Negative Potential	NBV	+0.3	-2.1	-3.0	V
Input Current, Any Pin Except Supplies	(Note 22 and 23)	I_{IN}	-	-	±10	mA
Output Current		I_{OUT}	-	-	±25	mA
Power Dissipation	(Note 24)	PDN	-	-	500	mW
Analog Input Voltage	VREF pins	V_{INR}	NBV -0.3	-	(VA+) + 0.3	V
	AIN Pins	V_{INA}	NBV -0.3	-	(VA+) + 0.3	V
Digital Input Voltage		V_{IND}	-0.3	-	(VD+) + 0.3	V
Ambient Operating Temperature		T_A	-40	-	85	°C
Storage Temperature		T_{stg}	-65	-	150	°C

Notes: 21. No pin should go more negative than NBV - 0.3 V.

22. Applies to all pins including continuous overvoltage conditions at the analog input (AIN) pins.

23. Transient current of up to 100 mA will not cause SCR latch-up. Maximum input current for a power supply pin is ±50 mA.

24. Total power dissipation, including all input currents and output currents.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS (T_A = 25° C; VA+ = 5 V ±5%; VD+ = 3.0 V ±10% or 5 V ±5%; Levels: Logic 0 = 0 V, Logic 1 = VD+; C_L = 50 pF.))

Parameter	Symbol	Min	Typ	Max	Unit
Master Clock Frequency (Note 25)	XIN				
External Clock or Internal Oscillator (CS5522/24/28)		30	32.768	200	kHz
(CS5521/23)		30	32.768	130	kHz
Master Clock Duty Cycle		40	-	60	%
Rise Times (Note 26)	t_{rise}				
Any Digital Input Except SCLK		-	-	1.0	µs
SCLK		-	-	100	µs
Any Digital Output		-	50	-	ns
Fall Times (Note 26)	t_{fall}				
Any Digital Input Except SCLK		-	-	1.0	µs
SCLK		-	-	100	µs
Any Digital Output		-	50	-	ns
Start-up					
Oscillator Start-up Time XTAL = 32.768 kHz (Note 27)	t_{ost}	-	500	-	ms
Serial Port Timing					
Serial Clock Frequency	SCLK	0	-	2	MHz
SCLK Falling to $\overline{CS}$ Falling for continuous running SCLK (Note 28)	t_0	100	-	-	ns
Serial Clock Pulse Width High	t_1	250	-	-	ns
Pulse Width Low	t_2	250	-	-	ns
SDI Write Timing					
$\overline{CS}$ Enable to Valid Latch Clock	t_3	50	-	-	ns
Data Set-up Time prior to SCLK rising	t_4	50	-	-	ns
Data Hold Time After SCLK Rising	t_5	100	-	-	ns
SCLK Falling Prior to $\overline{CS}$ Disable	t_6	100	-	-	ns
SDO Read Timing					
$\overline{CS}$ to Data Valid	t_7	-	-	150	ns
SCLK Falling to New Data Bit	t_8	-	-	150	ns
$\overline{CS}$ Rising to SDO Hi-Z	t_9	-	-	150	ns

Notes: 25. Device parameters are specified with a 32.768 kHz clock; however, clocks up to 200 kHz (CS5522/24/28) or 130 kHz (CS5521/23) can be used for increased throughput.

26. Specified using 10% and 90% points on waveform of interest. Output loaded with 50 pF.

27. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.

28. Applicable when SCLK is continuously running.

Specifications are subject to change without notice.

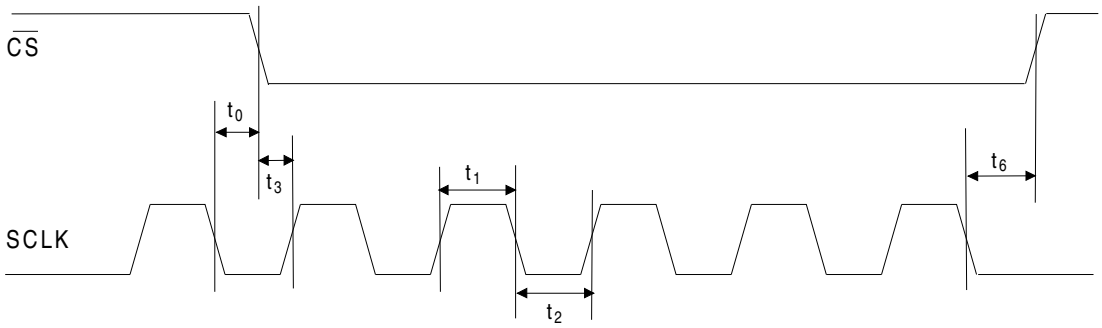

Figure 1. Continuous Running SCLK Timing (Not to Scale)

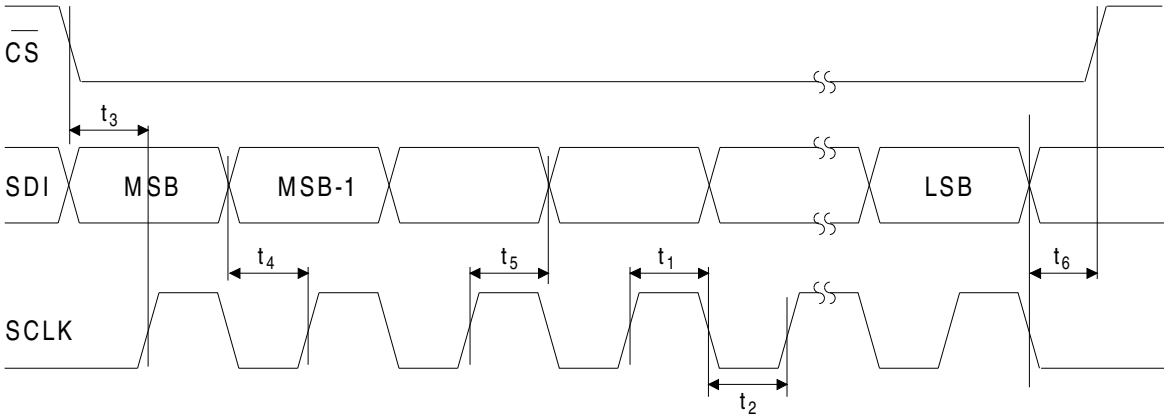

Figure 2. SDI Write Timing (Not to Scale)

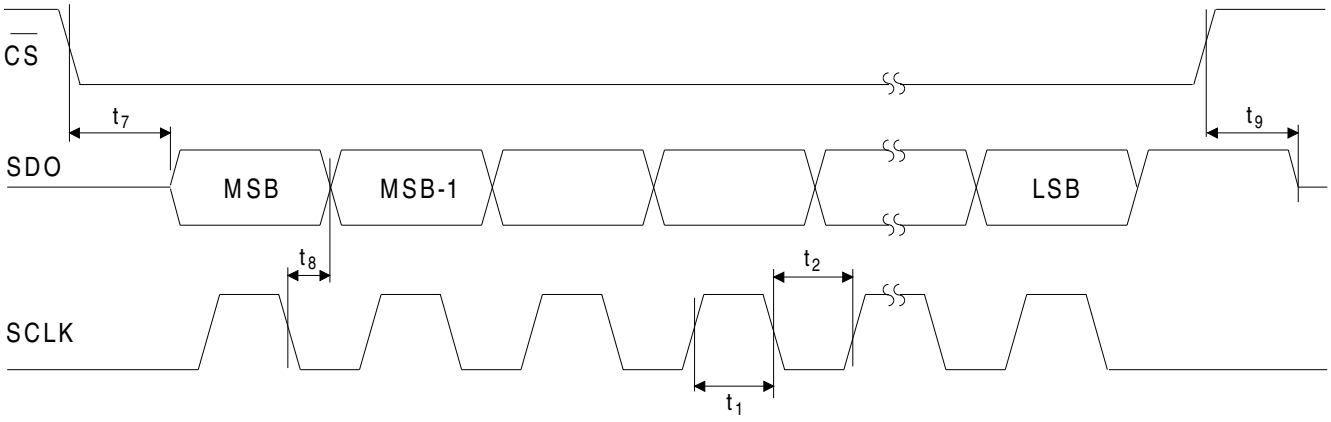

Figure 3. SDO Read Timing (Not to Scale)

1. GENERAL DESCRIPTION

The CS5521/22/23/24/28 are highly integrated ΔΣ Analog-to-Digital Converters (ADCs) which use charge-balance techniques to achieve 16-bit (CS5521/23) and 24-bit (CS5522/24/28) performance. The ADCs come as either two-channel (CS5521/22), four-channel (CS5523/24), or eight-channel (CS5528) devices, and include a low input current, chopper-stabilized instrumentation amplifier. To permit selectable input spans of 25 mV, 55 mV, 100 mV, 1 V, 2.5 V, and 5 V, the ADCs include a PGA (programmable gain amplifier). To accommodate ground-based thermocouple applications, the devices include a CPD (Charge Pump Drive) which provides a negative bias voltage to the on-chip amplifiers.

These devices also include a fourth order DS modulator followed by a digital filter which provides eight selectable output word rates of 1.88 Sps, 3.76 Sps, 7.51 Sps, 15 Sps, 30 Sps, 61.6 Sps, 84.5 Sps, and 101.1 Sps (XIN = 32.768 kHz). The devices are capable of producing output update rates up to 617 Sps when a 200 kHz clock is used (CS5522/24/28) or up to 401 Sps using a 130 kHz clock (CS5521/23). Further note that the digital filters are designed to settle to full accuracy within one conversion cycle and simultaneously reject both 50 Hz and 60 Hz interference when operated at word rates below 30 Sps (assuming a XIN clock frequency of 32.768 kHz).

To ease communication between the ADCs and a micro-controller, the converters include an easy to use three-wire serial interface which is SPI™ and Microwire™ compatible.

1.1 Analog Input

Figure 4 illustrates a block diagram of the analog input signal path inside the CS5521/22/23/24/28. The front end consists of a multiplexer (break before make configuration), a chopper-stabilized instrumentation amplifier with fixed gain of 20X, coarse/fine charge buffers, and a programmable gain section. For the 25 mV, 55 mV, and 100 mV input ranges, the input signals are amplified by the 20X instrumentation amplifier. For the 1 V, 2.5 V, and 5 V input ranges, the instrumentation amplifier is bypassed and the input signals are connected to the Programmable Gain block via coarse/fine charge buffers.

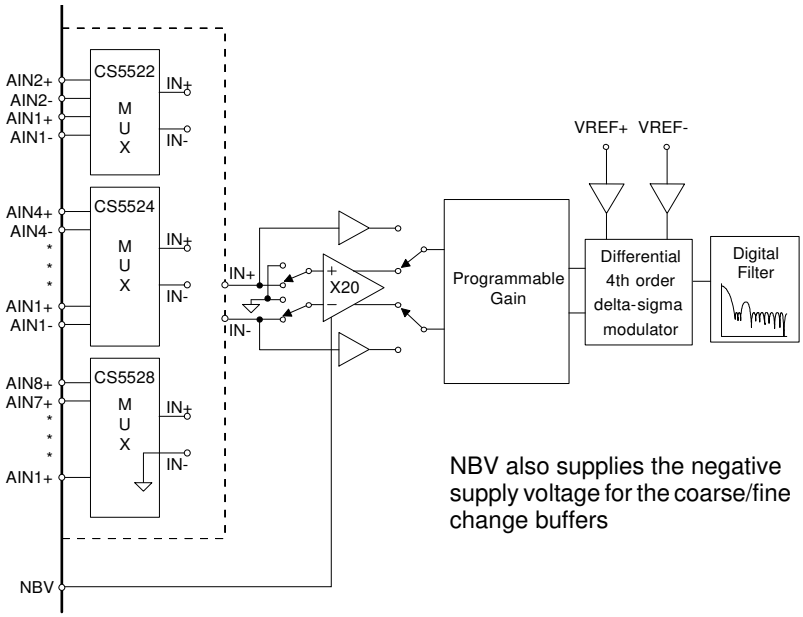

Figure 4. Multiplexer Configurations

1.1.1 Instrumentation Amplifier

The instrumentation amplifier is chopper stabilized and is activated any time conversions are performed with the low-level input ranges, ≤100 mV. The amplifier is powered from VA+ and from the NBV (Negative Bias Voltage) pin allowing the CS5521/22/23/24/28 to be operated in either of two analog input configurations. The NBV pin can be biased to a negative voltage between -1.8 V and -2.5 V, or tied to AGND (for the CS5528, NBV has to be between -1.8 V and -2.5 V for the ranges below 100 mV when the amplifier is engaged). The common-mode-plus-signal range of the instrumentation amplifier is 1.85 V to 2.65 V with NBV grounded. The common-mode-plus-signal range of the instrumentation amplifier is -0.150 V to 0.950 V with NBV between -1.8 V to -2.5 V. Whether NBV is tied between -1.8 V and -2.5 V or tied to AGND, the (Common Mode + Signal) input on AIN+ and AIN- must stay between NBV and VA+.

Figure 5 illustrates an analog input model for the ADCs when the instrumentation amplifier is engaged. The CVF (sampling) input current for each of the analog input pins depends on the CFS1 and CFS0 (Chop Frequency Select) bits in the configuration register (see *Configuration Register* for details). Note that the CVF current is lowest with the CFS bits in their default states (cleared to logic 0s). Further note that the CVF current into the instrumentation amplifier is less than 300 pA over -40°C to +85°C. Note that Figure 5 is for input current modeling only. For physical input capacitance see 'Input Capacitance' specification under *ANALOG CHARACTERISTICS*. Also refer to Applications Note AN30 - *"Switched-Capacitor A/D Converter Input Structures"* for more details on input models and input sampling currents.

Note: *Residual noise appears in the converter's baseband for output word rates greater than 61.6 Sps if the CFS bits are logic 0 (chop clock = 256 Hz). For word rates of 30 Sps and lower, 256 Sps chopping is recommended, and for 61.6 Sps, 84.5 Sps and 101.1 Sps word rate settings, 4096 Hz chopping is recommended.*

1.1.2 Coarse/Fine Charge Buffers

The unity gain buffers are activated any time conversions are performed with the high-level inputs ranges, 1 V, 2.5 V, and 5 V. The unity gain buffers are designed to accommodate rail-to-rail input signals. The common-mode-plus-signal range for the unity gain buffer amplifier is NBV to VA+.

Typical CVF (sampling) current for the unity gain buffer amplifiers is about 10 nA (XIN = 32.768 kHz, see Figure 6).

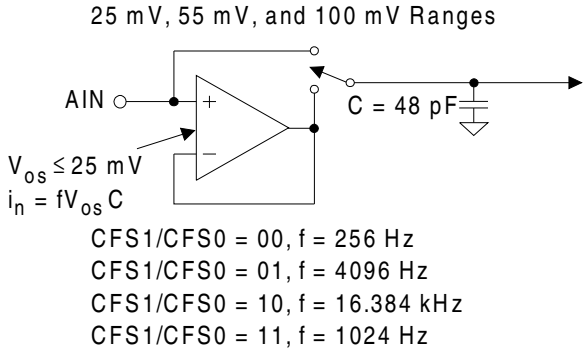

Figure 5. Input Models for AIN+ and AIN- pins, ≤100 mV Input Ranges

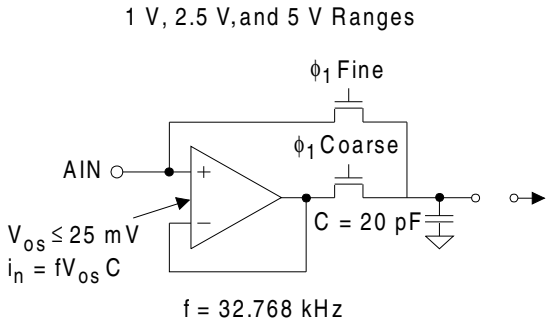

Figure 6. Input Models for AIN+ and AIN- pins, >100 mV input ranges

1.1.3 Analog Input Span Considerations

The CS5521/22/23/24/28 is designed to measure full-scale ranges of 25 mV, 55 mV, 100 mV, 1 V, 2.5 V, and 5 V. Other full scale values can be accommodated by performing a system calibration within the limits specified. See the *Calibration* section for more details. Another way to change the full scale range is to increase or to decrease the voltage reference to a voltage other than 2.5 . See the *Voltage Reference* section for more details.

Three factors set the operating limits for the input span. They include: instrumentation amplifier saturation, modulator 1's density, and a lower reference voltage. When the 25 mV, 55 mV, or 100 mV range is selected, the input signal (including the common-mode voltage and the amplifier offset voltage) must not cause the 20X amplifier to saturate in either its input stage or output stage. To prevent saturation, the absolute voltages on AIN+ and AIN- must stay within the limits specified (refer to the *Analog Input* section). Additionally, the differential output voltage of the amplifier must not exceed 2.8 V. The equation

$$ABS(VIN + VOS) \times 20 = 2.8\ V$$

defines the differential output limit, where

$$VIN = (AIN+) - (AIN-)$$

is the differential input voltage and VOS is the absolute maximum offset voltage for the instrumentation amplifier (VOS will not exceed 40 mV). If the differential output voltage from the amplifier exceeds 2.8 V, the amplifier may saturate, which will cause a measurement error.

The input voltage into the modulator must not cause the modulator to exceed a low of 20 percent or a high of 80 percent 1's density. The nominal full-scale input span of the modulator (from 30 percent to 70 percent 1's density) is determined by the VREF voltage divided by the Gain Factor. See Table 1 to determine if the CS5521/22/23/24/28 is being used properly. For example, in the 55 mV range, to determine the nominal input voltage to the modulator, divide VREF (2.5 V) by the Gain Factor (2.2727).

When a smaller voltage reference is used, the resulting code widths are smaller causing the converter output codes to exhibit more changing codes for a fixed amount of noise. Table 1 is based upon a VREF = 2.5 V. For other values of VREF, the values in Table 1 must be scaled accordingly.

1.1.4 Measuring Voltages Higher than 5 V

Some systems require the measurement of voltages greater than 5 V. The input current of the instru-

Input Range(1)	Max. Differential Output 20X Amplifier	VREF	Gain Factor	Δ-Σ Nominal(1) Differential Input	Δ-Σ(1) Max. Input
± 25 mV	2.8 V (2)	2.5V	5	± 0.5 V	± 0.75 V
± 55 mV	2.8 V (2)	2.5V	2.272727...	± 1.1 V	± 1.65 V
± 100 mV	2.8 V (2)	2.5V	1.25	± 2.0 V	± 3.0 V
± 1.0 V	-	2.5V	2.5	± 1.0 V	± 1.5 V
± 2.5 V	-	2.5V	1.0	± 2.5 V	± 5.0 V
± 5.0 V	-	2.5V	0.5	± 5.0 V	0V, VA+

Table 1. Relationship between Full Scale Input, Gain Factors, and Internal Analog Signal Limitations

Note: 1. The converter's actual input range, the delta-sigma's nominal full-scale input, and the delta-sigma's maximum full-scale input all scale directly with the value of the voltage reference. The values in the table assume a 2.5 V VREF voltage.
2. The 2.8 V limit at the output of the 20X amplifier is the differential output voltage.

mentation amplifier with a gain range setting of 100 mV or less, is typically 100 pA. This is low enough to permit large external resistors to divide down a large external signal without significant loading. Figure 7 illustrates an example circuit. Refer to Application Note 158 for more details on high-voltage (>5 V) measurement.

1.1.5 Voltage Reference

The CS5521/22/23/24/28 devices are specified for operation with a 2.5 V reference voltage between the VREF+ and VREF- pins of the device. For a single-ended reference voltage, such as the LT1019-2.5, the reference voltage is input into the VREF+ pin of the converter and the VREF- pin is grounded.

The differential voltage between the VREF+ and VREF- can be any voltage from 1.0 V up to VA+, however, the VREF+ cannot go above VA+ and the VREF- pin can not go below NBV.

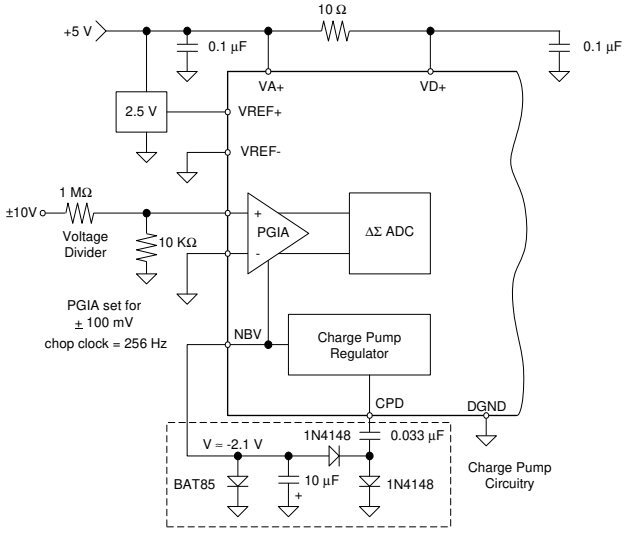

Figure 7. Input Ranges Greater than 5 V

Figure 8 illustrates the input models for the VREF pins. The dynamic input current for each of the pins can be determined from the models shown.

1.2 Overview of ADC Register Structure and Operating Modes

The CS5521/22/23/24/28 ADCs have an on-chip controller, which includes a number of user-accessible registers. The registers are used to hold offset and gain calibration results, configure the chip's operating modes, hold conversion instructions, and to store conversion data words. Figure 9 depicts a block diagram of the on-chip controller's internal registers for the CS5523/24.

Each of the converters has 24-bit registers to function as offset and gain calibration registers for each channel. The converters with two channels have two offset and two gain calibration registers, the converters with four channels have four offset and four gain calibration registers, and the eight channel converter has eight offset and eight gain calibration registers. These registers hold calibration results. The contents of these registers can be read or written by the user. This allows calibration data to be off-loaded into an external EEPROM. The user can also manipulate the contents of these registers to modify the offset or the gain slope of the converter.

The converters include a 24-bit configuration register of which 17 of the bits are used for setting options such as the conversion mode, operating power options, setting the chop clock rate of the instru-

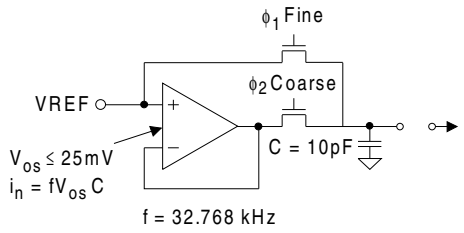

Figure 8. Input Model for VREF+ and VREF- Pins

mentation amplifier, and providing a number of flags which indicate converter operation.

A group of registers, called Channel Set-up Registers, are also included in the converters. These registers are used to hold pre-loaded conversion instructions. Each channel set-up register is 24 bits wide and holds two 12-bit conversion instructions (Setups). Upon power-up, these registers can be initialized by the user's microcontroller with conversion instructions. The user can then use bits in the configuration register to choose a conversion mode.

Several conversion modes are possible. Using the single conversion mode, an 8-bit command word can be written into the serial port. The command includes pointer bits which 'point' to a 12-bit command in one of the Channel Setup Registers which is to be executed. The 12-bit commands can be setup to perform a conversion on any of the input channels of the converter. More than one of the 12-bit Setups can be used for the same analog input channel. This allows the user to convert on the same signal with either a different conversion speed, a different gain range, or any of the other options available in the Setup Register. The user can set up the registers to perform conversions using different conversion options on each of the input channels.

The ADCs also include multiple-channel conversion capability. User bits in the configuration register of the ADCs can be configured to sequence through the 12-bit command Setups, performing a conversion according to the content of each 12-bit Setup. This channel scanning capability can be configured to run continuously, or to scan through a specified number of Setup Registers and stop until commanded to continue. In the multiple-channel scanning modes, the conversion data words are loaded into an on-chip data FIFO. The converter issues a flag on the SDO pin when a scan cycle is completed so the user can read the FIFO. More details are given in the following pages.

Instructions are provided on how to initialize the converter, perform offset and gain calibrations, and to configure the converter for the various conversion modes. Each of the bits of the configuration register and of the Channel Setup Registers is described. A list of examples follows the description section. Table 2 can be used to decode all valid commands (the first 8 bits into the serial port).

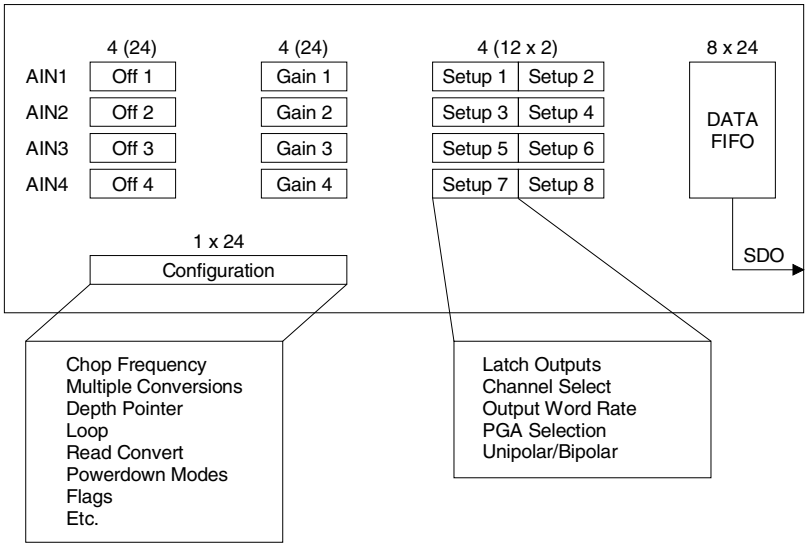

Figure 9. CS5523/24 Register Diagram

1.2.1 System Initialization

After power is first applied to the CS5521/22/2324/28 devices, the user should wait for the oscillator to start before attempting to communicate with the converter. If a 32.768 kHz crystal is used, this may be 500 milliseconds.

The initialization sequence should be as follows: Initialize the serial port by sending the port initialization sequence of 15 bytes of all 1's followed by one byte with the following bit contents '1111 110'. This sequence places the chip in the command mode where it waits for a valid command to be written. The first command should be to perform a system reset. This is accomplished by writing a logic 1 to the RS (Reset System) bit in the configuration register. After a reset the RV bit is set until the configuration register is read. The user must then write a logic 0 to the RS bit to take the part out of reset mode. Any other bits written to the configuration register at this time will be lost. The configuration register must be written again once RS= 0 to set any other bits to their desired settings.

After a reset, the on-chip registers are initialized to the following states:

configuration register:	000040(H)
offset registers:	000000(H)
gain registers:	400000(H)
channel setup registers:	000000(H)

1.2.2 Command Register Quick Reference

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
CB	CS2	CS1	CS0	R/$\overline{W}$	RSB2	RSB1	RSB0

BIT	NAME	VALUE	FUNCTION
D7	Command Bit, CB	0 1	Must be logic 0 for these commands. See table below.
D6-D4	Channel Select Bits, CSB2-CSB0	000 . . 111	CS2-CS0 provide the address of one of the eight physical channels. These bits are used to access the calibration registers associated with respective channels. Note: These bits are ignored when reading the data register.
D3	Read/$\overline{Write}$, R/$\overline{W}$	0 1	Write to selected register. Read from selected register.
D2-D0	Register Select Bit, RSB2-RSB0	000 001 010 011 101 110 111	Reserved Offset Register Gain Register Configuration Register Channel Set-up Registers - register is 48-bits long for CS5521/22 - register is 96-bits long for CS5523/24 - register is 192-bits long for CS5528 Reserved Reserved

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
CB	CSRP3	CSRP2	CSRP1	CSRP0	CC2	CC1	CC0

BIT	NAME	VALUE	FUNCTION
D7	Command Bit, CB	0 1	See table above. Must be logic 1 for these commands.
D6-D3	Channel Pointer Bits, CSRP3-CSRP0	0000 . . . 1111	These bits are used as pointers to the Setups. Note: The MC bit, must be logic 0 for these bits to take effect. When MC = 1, these bits are ignored. The LP, MC, and RC bits in the configuration register are ignored during calibration.
D2-D0	Conversion/Calibration Bits, CC2-CC0	000 001 010 011 100 101 110 111	Normal Conversion Self-Offset Calibration Self-Gain Calibration Reserved Reserved System-Offset Calibration System-Gain Calibration Reserved

Table 2. Command Register Quick Reference

1.2.3 Command Register Descriptions

READ/$\overline{\text{WRITE}}$ INDIVIDUAL OFFSET CALIBRATION REGISTER

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	CS2	CS1	CS0	R/$\overline{\text{W}}$	0	0	1

Function: *These commands are used to access each offset register separately. CS1 - CS0 decode the registers accessed.*

R/$\overline{\text{W}}$ (Read/$\overline{\text{Write}}$)

0 Write to selected register.

1 Read from selected register.

CS[2:0] (Channel Select Bits)

000 Offset Register 1(All devices)

001 Offset Register 2 (All devices)

010 Offset Register 3 (CS5523/24/28 only)

011 Offset Register 4 (CS5523/24/28 only)

100 Offset Register 5 (CS5528 only)

101 Offset Register 6 (CS5528 only)

110 Offset Register 7 (CS5528 only)

111 Offset Register 8 (CS5528 only)

READ/$\overline{\text{WRITE}}$ INDIVIDUAL GAIN REGISTER

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	CS2	CS1	CS0	R/$\overline{\text{W}}$	0	1	0

Function: *These commands are used to access each gain register separately. CS1 - CS0 decode the registers accessed.*

R/$\overline{\text{W}}$ (Read/$\overline{\text{Write}}$)

0 Write to selected register.

1 Read from selected register.

CS[2:0] (Channel Select Bits)

000 Gain Register 1(All devices)

001 Gain Register 2 (All devices)

010 Gain Register 3 (CS5523/24/28 only)

011 Gain Register 4 (CS5523/24/28 only)

100 Gain Register 5 (CS5528 only)

101 Gain Register 6 (CS5528 only)

110 Gain Register 7 (CS5528 only)

111 Gain Register 8 (CS5528 only)

READ/$\overline{\text{WRITE}}$ CONFIGURATION REGISTER

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	R/$\overline{\text{W}}$	0	1	1

Function: *These commands are used to read from or write to the configuration register.*

R/$\overline{\text{W}}$ (Read/$\overline{\text{Write}}$)

0 Write to selected register.

1 Read from selected register.

READ/$\overline{\text{WRITE}}$ CHANNEL-SETUP REGISTER(S)

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	R/$\overline{\text{W}}$	1	0	1

Function: *These commands are used to access the channel-setup registers (CSRs). The number of CSRs accessed is determined by the device being used and the number of CSRs that are being accessed (i.e. the depth bits in the configuration register determine the number of levels accessed). This register is 48-bits long (4 Setups) for the CS5521/22, 96-bits long (8 Setups) for the CS5523/24, and 192-bits (16 Setups) long for the CS5528.*

R/$\overline{\text{W}}$ (Read/$\overline{\text{Write}}$)

0 Write to selected register.

1 Read from selected register.

PERFORM CONVERSION

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	CSRP3	CSRP2	CSRP1	CSRP0	0	0	0

Function: *These commands instruct the ADC to perform conversions on the physical input channel pointed to by the pointer bits (CSRP2 - CSRP0) in the channel-setup registers. The particular type of conversion performed is determined by the states of the conversion control bits (the multiple conversion bit, the loop bit, read convert bit, and the depth pointer bits) in the configuration register.*

CSRP [3:0] (Channel Setup Register Pointer Bits)

0000	Setup 1 (All devices)
0001	Setup 2 (All devices)
0010	Setup 3 (All devices)
0011	Setup 4 (All devices)
0100	Setup 5 (CS5523/24/28)
0101	Setup 6 (CS5523/24/28)
0110	Setup 7 (CS5523/24/28)
0111	Setup 8 (CS5523/24/28)
1000	Setup 9 (CS5528 only)
1001	Setup 10 (CS5528 only)
1010	Setup 11 (CS5528 only)
1011	Setup 12 (CS5528 only)
1100	Setup 13 (CS5528 only)
1101	Setup 14 (CS5528 only)
1110	Setup 15 (CS5528 only)
1111	Setup 16 (CS5528 only)

PERFORM CALIBRATION

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	CSRP3	CSRP2	CSRP1	CSRP0	CC2	CC1	CC0

Function: *These commands instruct the ADC to perform a calibration on the physical input channel referenced which is chosen by the command byte pointer bits (CSRP3 - CRSP0).*

CSRP [3:0] (Channel Setup Register Pointer Bits)

0000 Setup 1 (All devices)
0001 Setup 2 (All devices)
0010 Setup 3 (All devices)
0011 Setup 4 (All devices)
0100 Setup 5 (CS5523/24/28 only)
0101 Setup 6 (CS5523/24/28 only)
0110 Setup 7 (CS5523/24/28 only)
0111 Setup 8 (CS5523/24/28 only)
1000 Setup 9 (CS5528 only)
1001 Setup 10 (CS5528 only)
1010 Setup 11 (CS5528 only)
1011 Setup 12 (CS5528 only)
1100 Setup 13 (CS5528 only)
1101 Setup 14 (CS5528 only)
1110 Setup 15 (CS5528 only)
1111 Setup 16 (CS5528 only)

CC [2:0] (Calibration Control Bits)

000 Reserved
001 Self-Offset Calibration
010 Self-Gain Calibration
011 Reserved
100 Reserved
101 System-Offset Calibration
110 System-Gain Calibration
111 Reserved

SYNC1

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Function: *Part of the serial port re-initialization sequence.*

SYNC0

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	0

Function: *End of the serial port re-initialization sequence.*

NULL

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

Function: *This command is used to clear a port flag and keep the converter in the continuous conversion mode.*

1.2.4 Serial Port Interface

The CS5521/22/23/24/28's serial interface consists of four control lines: $\overline{CS}$, SCLK, SDI, SDO. Figure 10 illustrates the serial sequence necessary to write to, or read from the serial port's registers.

$\overline{CS}$ (Chip Select) is the control line which enables access to the serial port. If the $\overline{CS}$ pin is tied low, the port can function as a three-wire interface.

SDI (Serial Data In) is the data signal used to transfer data to the converters.

SDO (Serial Data Out) is the data signal used to transfer output data from the converters. The SDO output will be held at high impedance any time $\overline{CS}$ is at logic 1.

SCLK (Serial Clock) is the serial bit clock which controls the shifting of data to or from the ADC's serial port. The $\overline{CS}$ pin must be held low (logic 0) before SCLK transitions can be recognized by the port logic. To accommodate opto-isolators SCLK is designed with a Schmitt-trigger input to allow an opto-isolator with slower rise and fall times to directly drive the pin. Additionally, SDO is capable of sinking or sourcing up to 5 mA to directly drive an opto-isolator LED. SDO will have less than a 400 mV loss in the drive voltage when sinking or sourcing 5 mA.

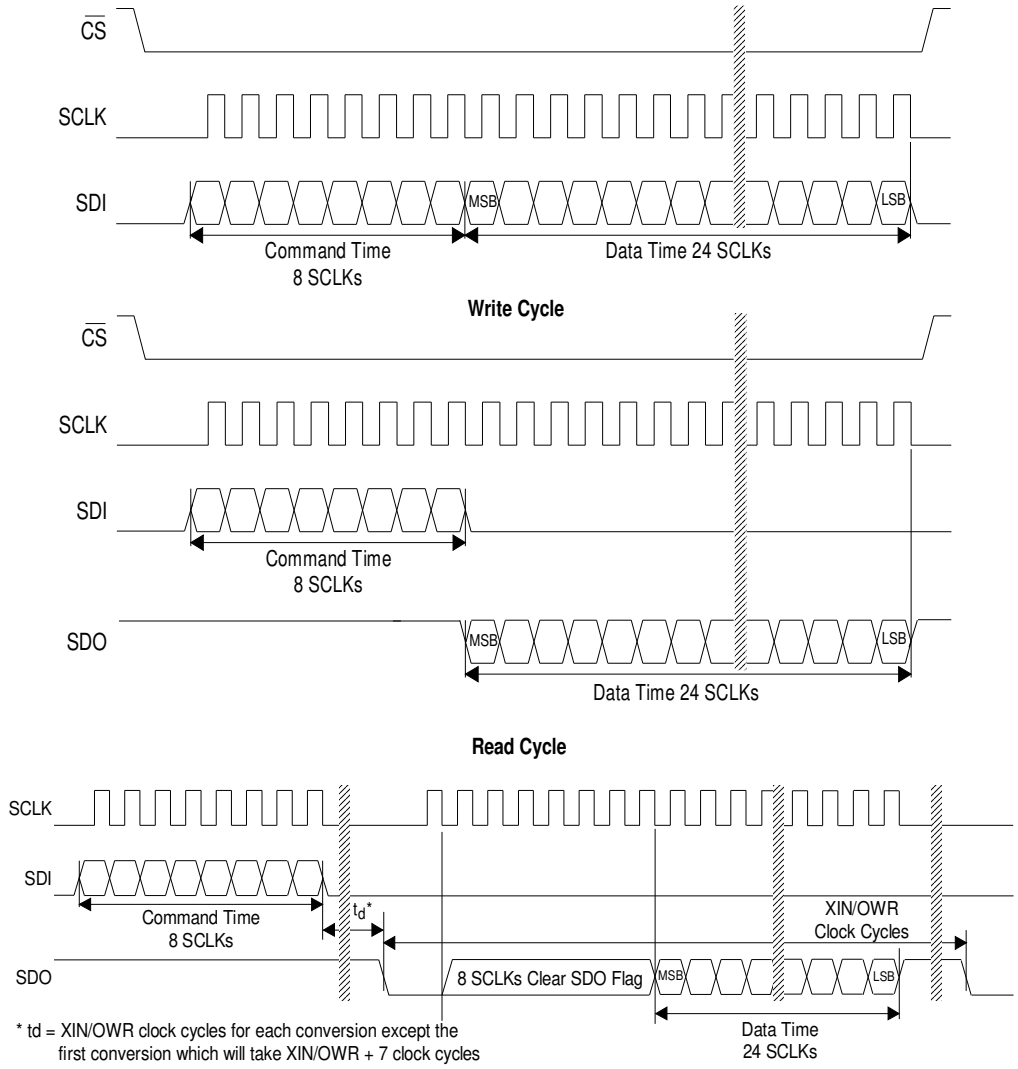

Figure 10. Command and Data Word Timing