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CS5532/34-BS

24-bit ΔΣ ADCs with Ultra-low-noise PGIA

Features

- Chopper-stabilized PGIA (Programmable Gain Instrumentation Amplifier, 1x to 64x)
  - 6 nV/√Hz @ 0.1 Hz (No 1/f noise) at 64x
  - 1200 pA Input Current with Gains >1
- Delta-sigma Analog-to-digital Converter
  - Linearity Error: 0.0007% FS
  - Noise-free Resolution: Up to 23 bits
- Two- or Four-channel Differential MUX
- Scalable Input Span via Calibration
  - ±5 mV to differential ±2.5V
- Scalable V_{REF} Input: Up to Analog Supply
- Simple Three-wire Serial Interface
  - SPI™ and Microwire™ Compatible
  - Schmitt Trigger on Serial Clock (SCLK)
- R/W Calibration Registers Per Channel
- Selectable Word Rates: 6.25 to 3,840 Sps
- Selectable 50 or 60 Hz Rejection
- Power Supply Configurations
  - VA+ = +5 V; VA- = 0 V; VD+ = +3 V to +5 V
  - VA+ = +2.5 V; VA- = -2.5 V; VD+ = +3 V to +5 V
  - VA+ = +3 V; VA- = -3 V; VD+ = +3 V

General Description

The CS5532/34 are highly integrated ΔΣ Analog-to-Digital Converters (ADCs) which use charge-balance techniques to achieve 24-bit performance. The ADCs are optimized for measuring low-level unipolar or bipolar signals in weigh scale, process control, scientific, and medical applications.

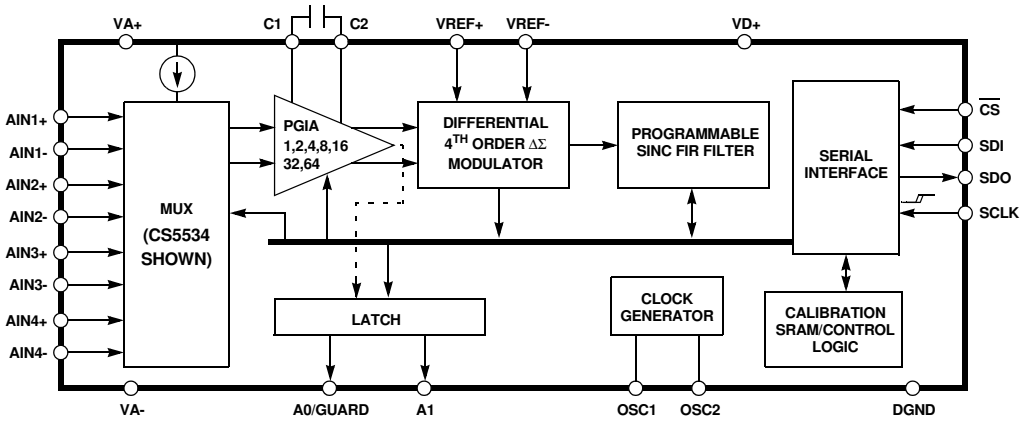
To accommodate these applications, the ADCs come as either two-channel (CS5532) or four-channel (CS5534) devices and include a very low-noise, chopper-stabilized instrumentation amplifier (6 nV/√Hz @ 0.1 Hz) with selectable gains of 1×, 2×, 4×, 8×, 16×, 32×, and 64×. These ADCs also include a fourth-order ΔΣ modulator followed by a digital filter which provides twenty selectable output word rates of 6.25, 7.5, 12.5, 15, 25, 30, 50, 60, 100, 120, 200, 240, 400, 480, 800, 960, 1600, 1920, 3200, and 3840 Sps (MCLK = 4.9152 MHz).

To ease communication between the ADCs and a microcontroller, the converters include a simple three-wire serial interface which is SPI™ and Microwire™ compatible with a Schmitt-trigger input on the serial clock (SCLK).

High dynamic range, programmable output rates, and flexible power supply options makes these ADCs ideal solutions for weigh scale and process control applications.

ORDERING INFORMATION

See page 47



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1. CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARACTERISTICS

(VA+, VD+ = 5 V ±5%; VREF+ = 5 V; VA-, VREF-, DGND = 0 V; MCLK = 4.9152 MHz;
OWR (Output Word Rate) = 60 Sps; Bipolar Mode; Gain = 32)
(See Notes 1 and 2.)

Parameter	Min	Typ	Max	Unit
Accuracy				
Linearity Error	-	±0.0007	±0.0015	%FS
No Missing Codes	24	-	-	Bits
Bipolar Offset	-	±16	±32	LSB_{24}
Unipolar Offset	-	±32	±64	LSB_{24}
Offset Drift (Notes 3 and 4)	-	640/G + 5	-	nV/°C
Bipolar Full-scale Error	-	±8	±31	ppm
Unipolar Full-scale Error	-	±16	±62	ppm
Full-scale Drift (Note 4)	-	2	-	ppm/°C

Notes:
1. Applies after system calibration at any temperature within -40 °C ~ +85 °C.
2. Specifications guaranteed by design, characterization, and/or test. LSB is 24 bits.
3. This specification applies to the device only and does not include any effects by external parasitic thermocouples. The PGIA contributes 5 nV of offset drift, and the modulator contributes 640/G nV of offset drift, where G is the amplifier gain setting.
4. Drift over specified temperature range after calibration at power-up at 25 °C.

ANALOG CHARACTERISTICS (Continued)

(See Notes 1 and 2.)

Parameter			Min	Typ	Max	Unit
Analog Input						
Common Mode + Signal on AIN+ or AIN-Bipolar/Unipolar Mode						
	Gain = 1		VA-	-	VA+	V
	Gain = 2, 4, 8, 16, 32, 64	(Note 5)	VA- + 0.7	-	VA+ - 1.7	V
CVF Current on AIN+ or AIN-	Gain = 1	(Note 6, 7)	-	50	-	nA
	Gain = 2, 4, 8, 16, 32, 64		-	1200	-	pA
Input Current Noise	Gain = 1		-	200	-	pA/√Hz
	Gain = 2, 4, 8, 16, 32, 64		-	1	-	pA/√Hz
Input Leakage for Mux when Off (at 25 °C)			-	10	-	pA
Off-channel Mux Isolation			-	120	-	dB
Open Circuit Detect Current			100	300	-	nA
Common Mode Rejection	dc, Gain = 1		-	90	-	dB
	dc, Gain = 64		-	130	-	dB
	50, 60 Hz		-	120	-	dB
Input Capacitance			-	60	-	pF
Guard Drive Output			-	20	-	µA
Voltage Reference Input						
Range	(VREF+) - (VREF-)		1	2.5	(VA+)-(VA-)	V
CVF Current		(Note 6, 7)	-	50	-	nA
Common Mode Rejection	dc		-	120	-	dB
	50, 60 Hz		-	120	-	dB
Input Capacitance			11	-	22	pF
System Calibration Specifications						
Full-scale Calibration Range	Bipolar/Unipolar Mode		3	-	110	%FS
Offset Calibration Range	Bipolar Mode		-100	-	100	%FS
Offset Calibration Range	Unipolar Mode		-90	-	90	%FS

Notes:
5. The voltage on the analog inputs is amplified by the PGIA, and becomes $V_{CM} \pm$ Gain*(AIN+ - AIN-)/2 at the differential outputs of the amplifier. In addition to the input common mode + signal requirements for the analog input pins, the differential outputs of the amplifier must remain between (VA- + 0.1 V) and (VA+ - 0.1 V) to avoid saturation of the output stage.
6. See the section of the data sheet which discusses input models.
7. Input current on AIN+ or AIN- (with Gain = 1), or VREF+ or VREF- may increase to 250 nA if operated within 50 mV of VA+ or VA-. This is due to the rough charge buffer being saturated under these conditions.

ANALOG CHARACTERISTICS (Continued)

(See Notes 1 and 2.)

Parameter			Min	Typ	Max	Unit
Power Supplies						
DC Power Supply Currents (Normal Mode)	I_{A+}, I_{A-}		-	13	15	mA
	I_{D+}		-	0.5	1	mA
Power Consumption	Normal Mode	(Notes 8 and 9)	-	70	80	mW
	Standby		-	4	-	mW
	Sleep		-	500	-	µW
Power Supply Rejection		(Note 10)				
	dc Positive Supplies		-	115	-	dB
	dc Negative Supply		-	115	-	dB

8. All outputs unloaded. All input CMOS levels.
9. Power is specified when the instrumentation amplifier (Gain ≥ 2) is on. Analog supply current is reduced by approximately 1/2 when the instrumentation amplifier is off (Gain = 1).
10. Tested with 100 mV change on VA+ or VA-.

TYPICAL RMS NOISE (nV)

(See notes 11, 12, 13 and 14)

Output Word Rate (Sps)	-3 dB Filter Frequency (Hz)	Instrumentation Amplifier Gain						
		x64	x32	x16	x8	x4	x2	x1
7.5	1.94	8.5	9	10	15	26	50	99
15	3.88	12	13	15	21	37	70	139
30	7.75	17	18	21	30	52	99	196
60	15.5	24	25	29	42	73	140	277
120	31	34	36	42	59	103	198	392
240	62	80	136	260	514	1020	2050	4090
480	122	113	194	369	730	1450	2900	5810
960	230	159	274	523	1030	2060	4110	8230
1,920	390	260	470	912	1810	3620	7230	14500
3,840	780	1360	2690	5380	10800	21500	43000	86000

Notes: 11. The -B devices provide the best noise specifications.

12. Wideband noise aliased into the baseband. Referred to the input. Typical values shown for 25 °C.

13. For Peak-to-Peak Noise multiply by 6.6 for all ranges and output rates.

14. Word rates and -3dB points with FRS = 0. When FRS = 1, word rates and -3dB points scale by 5/6.

TYPICAL NOISE-FREE RESOLUTION(BITS)

(See Notes 15 and 16)

Output Word Rate (Sps)	-3 dB Filter Frequency (Hz)	Instrumentation Amplifier Gain						
		x64	x32	x16	x8	x4	x2	x1
7.5	1.94	20	21	22	23	23	23	23
15	3.88	20	21	22	22	22	22	22
30	7.75	19	20	21	22	22	22	22
60	15.5	19	20	21	21	21	21	21
120	31	18	19	20	21	21	21	21
240	62	17	17	18	18	18	18	18
480	122	17	17	17	17	17	17	17
960	230	16	16	17	17	17	17	17
1,920	390	16	16	16	16	16	16	16
3,840	780	13	13	13	13	13	13	13

15. Noise-free resolution listed is for bipolar operation, and is calculated as LOG((Input Span)/(6.6xRMS Noise))/LOG(2) rounded to the nearest bit. For unipolar operation, the input span is 1/2 as large, so one bit is lost. The input span is calculated in the analog input span section of the data sheet. The noise-free resolution table is computed with a value of 1.0 in the gain register. Values other than 1.0 will scale the noise, and change the noise-free resolution accordingly.

16. “Noise-free resolution” is not the same as “effective resolution”. Effective resolution is based on the RMS noise value, while noise-free resolution is based on a peak-to-peak noise value specified as 6.6 times the RMS noise value. Effective resolution is calculated as LOG((Input Span)/(RMS Noise))/LOG(2).

Specifications are subject to change without notice.

5 V DIGITAL CHARACTERISTICS

(VA+, VD+ = 5 V ±5%; VA-, DGND = 0 V; See Notes 2 and 17.)

Parameter		Symbol	Min	Typ	Max	Unit
High-level Input Voltage	All Pins Except SCLK SCLK	V_{IH}	0.6 VD+ (VD+) - 0.45	- -	VD+ VD+	V
Low-level Input Voltage	All Pins Except SCLK SCLK	V_{IL}	0.0 0.0	-	0.8 0.6	V
High-level Output Voltage	A0 and A1, I_{out} = -1.0 mA SDO, I_{out} = -5.0 mA	V_{OH}	(VA+) - 1.0 (VD+) - 1.0	-	-	V
Low-level Output Voltage	A0 and A1, I_{out} = 1.0 mA SDO, I_{out} = 5.0 mA	V_{OL}	-	-	(VA-) + 0.4 0.4	V
Input Leakage Current		I_{in}	-	±1	±10	µA
SDO Tri-State Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

3 V DIGITAL CHARACTERISTICS

(T_A = 25 °C; VA+ = 5V ±5%; VD+ = 3.0V±10%; VA-, DGND = 0V; See Notes 2 and 17.)

Parameter		Symbol	Min	Typ	Max	Unit
High-level Input Voltage	All Pins Except SCLK SCLK	V_{IH}	0.6 VD+ (VD+) - 0.45	-	VD+ VD+	V
Low-level Input Voltage	All Pins Except SCLK SCLK	V_{IL}	0.0 0.0	-	0.8 0.6	V
High-level Output Voltage	A0 and A1, I_{out} = -1.0 mA SDO, I_{out} = -5.0 mA	V_{OH}	(VA+) - 1.0 (VD+) - 1.0	-	-	V
Low-level Output Voltage	A0 and A1, I_{out} = 1.0 mA SDO, I_{out} = 5.0 mA	V_{OL}	-	-	(VA-) + 0.4 0.4	V
Input Leakage Current		I_{in}	-	±1	±10	µA
SDO Tri-State Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

17. All measurements performed under static conditions.

DYNAMIC CHARACTERISTICS

Parameter	Symbol	Ratio	Unit
Modulator Sampling Rate	f_s	MCLK/16	Sps
Filter Settling Time to 1/2 LSB (Full Scale Step Input) Single Conversion mode (Notes 18, 19, and 20) Continuous Conversion mode, OWR < 3200 Sps Continuous Conversion mode, OWR ≥ 3200 Sps	 t_s t_s t_s	 $1/OWR_{SC}$ $5/OWR_{sinc5} + 3/OWR$ $5/OWR$	 s s s

18. The ADCs use a $Sinc^5$ filter for the 3200 Sps and 3840 Sps output word rate (OWR) and a $Sinc^5$ filter followed by a $Sinc^3$ filter for the other OWRs. OWR_{sinc5} refers to the 3200 Sps (FRS = 1) or 3840 Sps (FRS = 0) word rate associated with the $Sinc^5$ filter.
19. The single conversion mode only outputs fully settled conversions. See Table 1 for more details about single conversion mode timing. OWR_{SC} is used here to designate the different conversion time associated with single conversions.
20. The continuous conversion mode outputs every conversion. This means that the filter's settling time with a full scale step input in the continuous conversion mode is dictated by the OWR.

ABSOLUTE MAXIMUM RATINGS

(DGND = 0 V; See Note 21.)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	(Notes 22 and 23) Positive Digital Positive Analog Negative Analog	 VD+ VA+ VA-	 -0.3 -0.3 +0.3	 - - -	 +6.0 +6.0 -3.75	 V V V
Input Current, Any Pin Except Supplies	(Notes 24 and 25)	I_{IN}	-	-	±10	mA
Output Current		I_{OUT}	-	-	±25	mA
Power Dissipation	(Note 26)	PDN	-	-	500	mW
Analog Input Voltage	VREF pins AIN Pins	V_{INR} V_{INA}	(VA-) -0.3 (VA-) -0.3	- -	(VA+) + 0.3 (VA+) + 0.3	V V
Digital Input Voltage		V_{IND}	-0.3	-	(VD+) + 0.3	V
Ambient Operating Temperature		T_A	-40	-	85	°C
Storage Temperature		T_{stg}	-65	-	150	°C

Notes: 21. All voltages with respect to ground.

22. VA+ and VA- must satisfy {(VA+) - (VA-)} ≤ +6.6 V.
23. VD+ and VA- must satisfy {(VD+) - (VA-)} ≤ +7.5 V.
24. Applies to all pins including continuous overvoltage conditions at the analog input (AIN) pins.
25. Transient current of up to 100 mA will not cause SCR latch-up. Maximum input current for a power supply pin is ±50 mA.
26. Total power dissipation, including all input currents and output currents.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS

(VA+ = 2.5 V or 5 V ±5%; VA- = -2.5V±5% or 0 V; VD+ = 3.0 V ±10% or 5 V ±5%;DGND = 0 V; Levels: Logic 0 = 0 V, Logic 1 = VD+; C_L = 50 pF; See Figures 1 and 2.)

Parameter	Symbol	Min	Typ	Max	Unit
Master Clock Frequency (Note 27) External Clock or Crystal Oscillator	MCLK	1	4.9152	5	MHz
Master Clock Duty Cycle		40	-	60	%
Rise Times (Note 28) Any Digital Input Except SCLK SCLK Any Digital Output	t_{rise}	 - - -	 - - 50	 1.0 100 -	 µs µs ns
Fall Times (Note 28) Any Digital Input Except SCLK SCLK Any Digital Output	t_{fall}	 - - -	 - - 50	 1.0 100 -	 µs µs ns
Start-up					
Oscillator Start-up Time XTAL = 4.9152 MHz (Note 29)	t_{ost}	-	20	-	ms
Serial Port Timing					
Serial Clock Frequency	SCLK	0	-	2	MHz
Serial Clock Pulse Width High Pulse Width Low	t_1 t_2	250 250	- -	- -	ns ns
SDI Write Timing					
$\overline{CS}$ Enable to Valid Latch Clock	t_3	50	-	-	ns
Data Set-up Time prior to SCLK rising	t_4	50	-	-	ns
Data Hold Time After SCLK Rising	t_5	100	-	-	ns
SCLK Falling Prior to $\overline{CS}$ Disable	t_6	100	-	-	ns
SDO Read Timing					
$\overline{CS}$ to Data Valid	t_7	-	-	150	ns
SCLK Falling to New Data Bit	t_8	-	-	150	ns
$\overline{CS}$ Rising to SDO Hi-Z	t_9	-	-	150	ns

Notes: 27. Device parameters are specified with a 4.9152 MHz clock.

28. Specified using 10% and 90% points on waveform of interest. Output loaded with 50 pF.

29. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.

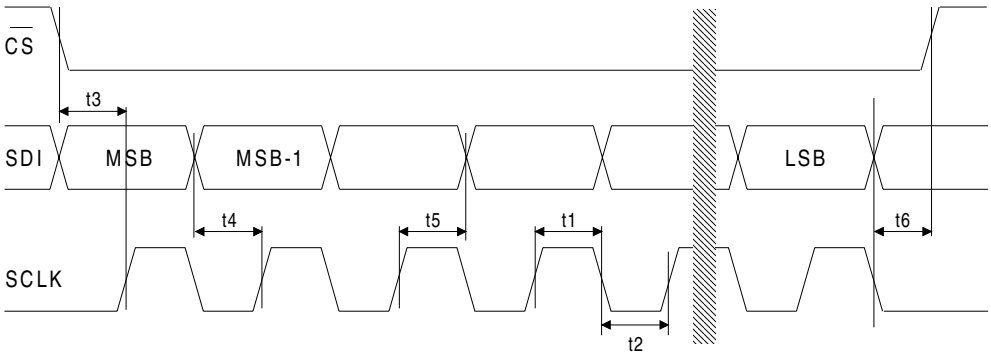


Figure 1. SDI Write Timing (Not to Scale)

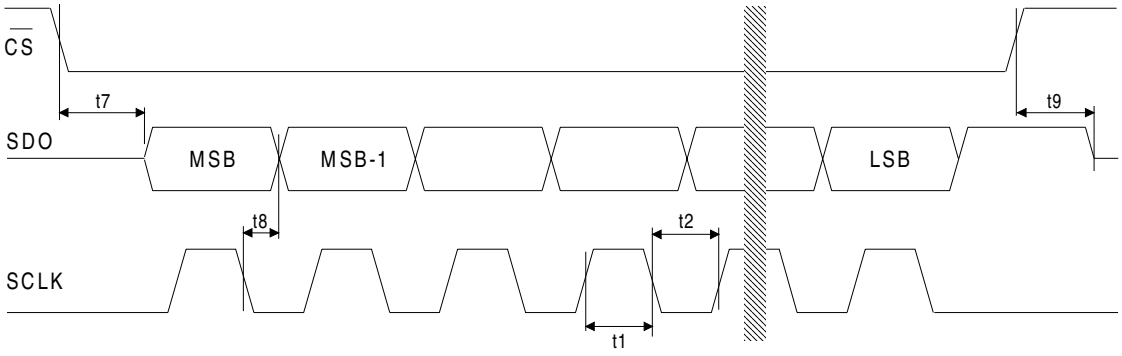


Figure 2. SDO Read Timing (Not to Scale)

2. GENERAL DESCRIPTION

The CS5532/34 are highly integrated ΔΣ Analog-to-Digital Converters (ADCs) which use charge-balance techniques to achieve 24-bit performance. The ADCs are optimized for measuring low-level unipolar or bipolar signals in weigh scale, process control, scientific, and medical applications.

To accommodate these applications, the ADCs come as either two-channel (CS5532) or four-channel (CS5534) devices and include a very-low-noise, chopper-stabilized, programmable-gain instrumentation amplifier (PGIA, 6 nV/$\sqrt{\text{Hz}}$ @ 0.1 Hz) with selectable gains of 1×, 2×, 4×, 8×, 16×, 32×, and 64×. These ADCs also include a fourth-order ΔΣ modulator followed by a digital filter which provides twenty selectable output word rates of 6.25, 7.5, 12.5, 15, 25, 30, 50, 60, 100, 120, 200, 240, 400, 480, 800, 960, 1600, 1920, 3200, and 3840 Samples per second (MCLK = 4.9152 MHz).

To ease communication between the ADCs and a microcontroller, the converters include a simple three-wire serial interface which is SPI and Microwire compatible with a Schmitt-trigger input on the serial clock (SCLK).

2.1. Analog Input

Figure 3 illustrates a block diagram of the CS5532/34. The front end consists of a multiplexer, a unity gain coarse/fine charge input buffer, and a programmable-gain, chopper-stabilized instrumentation amplifier. The unity gain buffer is activated any time conversions are performed with a gain of one and the instrumentation amplifier is activated any time conversions are performed with gain settings greater than one.

The unity gain buffer is designed to accommodate rail-to-rail input signals. The common mode plus signal range for the unity gain buffer amplifier is VA- to VA+. Typical CVF (sampling) current for the unity gain buffer amplifier is about 50 nA (MCLK = 4.9152 MHz, see Figure 4).

The instrumentation amplifier is chopper stabilized and operates with a chop-clock frequency of MCLK/128. The CVF (sampling) current into the

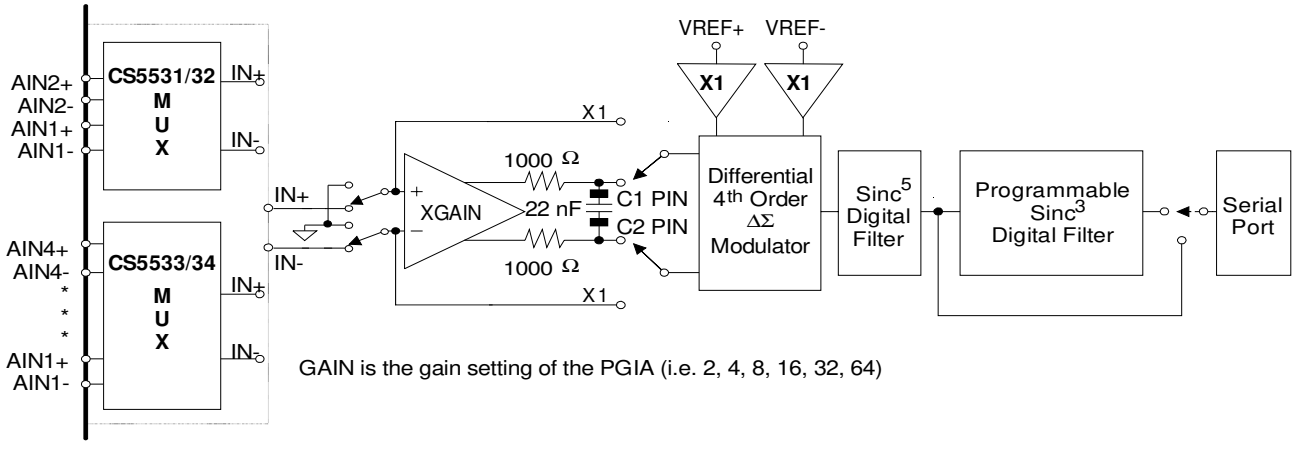


Figure 3. Multiplexer Configuration

instrumentation amplifier is typically 1200 pA over -40°C to +85°C (MCLK=4.9152 MHz). The common-mode plus signal range of the instrumentation amplifier is (VA-) + 0.7 V to (VA+) - 1.7 V.

Figure 4 illustrates the input models for the amplifiers. The dynamic input current for each of the pins can be determined from the models shown.

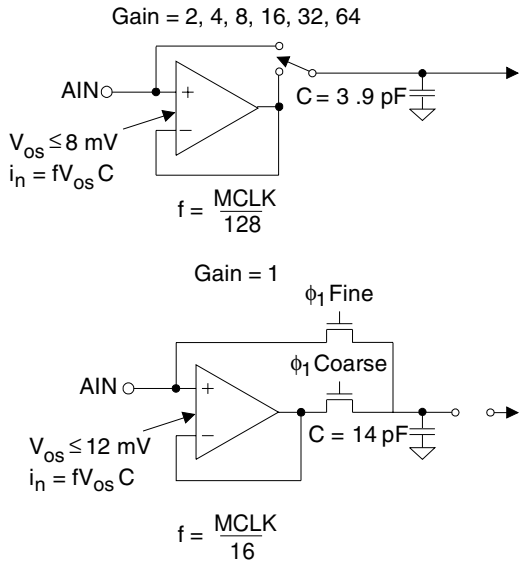


Figure 4. Input models for AIN+ and AIN- pins

Note: The C=3.9pF and C = 14pF capacitors are for input current modeling only. For physical input capacitance see 'Input Capacitance' specification under *Analog Characteristics*.

2.1.1. Analog Input Span

The full-scale input signal that the converter can digitize is a function of the gain setting and the reference voltage connected between the VREF+ and VREF- pins. The full-scale input span of the converter is ((VREF+) - (VREF-))/(GxA), where G is the gain of the amplifier and A is 2 for VRS = 0, or A is 1 for VRS = 1. VRS is the Voltage Reference Select bit, and must be set according to the differential voltage applied to the VREF+ and VREF- pins on the part. See section 2.3.5 for more details.

After reset, the unity gain buffer is engaged. With a 2.5 V reference this would make the full-scale input range default to 2.5 V. By activating the instrumentation amplifier (i.e. a gain setting other than 1) and using a gain setting of 32, the full-scale input range can quickly be set to 2.5/32 or about 78 mV. Note that these input ranges assume the calibration registers are set to their default values (i.e. Gain = 1.0 and Offset = 0.0).

2.1.2. Multiplexed Settling Limitations

The settling performance of the CS5532/34 in multiplexed applications is affected by the single-pole, low-pass filter which follows the instrumentation amplifier (see Figure 3). To achieve data sheet settling and linearity specifications, it is recommended that a 22 nF C0G capacitor be used. Capacitors as low as 10 nF or X7R type capacitors can also be used with some minor increase in distortion for AC signals.

2.1.3. Voltage Noise Density Performance

Figure 5 illustrates the measured voltage noise density versus frequency from 0.025 Hz to 10 Hz of a CS5532-BS. The device was powered with ±2.5 V supplies, using 30 Sps OWR, the 64x gain range, bipolar mode, and with the input short bit enabled.

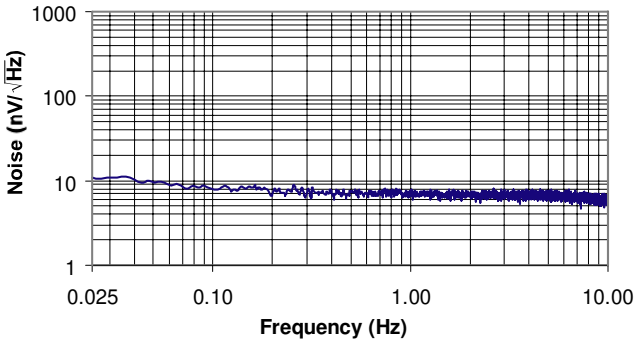


Figure 5. Measured Voltage Noise Density, 64x

2.1.4. No Offset DAC

An offset DAC was not included in the CS553X family because the high dynamic range of the converter eliminates the need for one. The offset register can be manipulated by the user to mimic the function of a DAC if desired.

2.2. Overview of ADC Register Structure and Operating Modes

The CS5532/34 ADCs have an on-chip controller, which includes a number of user-accessible registers. The registers are used to hold offset and gain calibration results, configure the chip's operating modes, hold conversion instructions, and to store conversion data words. Figure 6 depicts a block diagram of the on-chip controller's internal registers.

Each of the converters has 32-bit registers to function as offset and gain calibration registers for each channel. The CS5532 has two offset and two gain calibration registers, the CS5534 has four offset and four gain calibration registers. These registers hold calibration results. The contents of these registers can be read or written by the user. This allows calibration data to be off-loaded into an external EEPROM. The user can also manipulate the contents of these registers to modify the offset or the gain slope of the converter.

The converters include a 32-bit configuration register which is used for setting options such as the power down modes, resetting the converter, shorting the analog inputs, and enabling diagnostic test bits like the guard signal.

A group of registers, called Channel Setup Registers, are used to hold pre-loaded conversion instructions. Each channel setup register is 32 bits wide, and holds two 16-bit conversion instructions referred to as Setups. Upon power up, these registers can be initialized by the system microcontroller with conversion instructions. The user can then instruct the converter to perform single or multiple

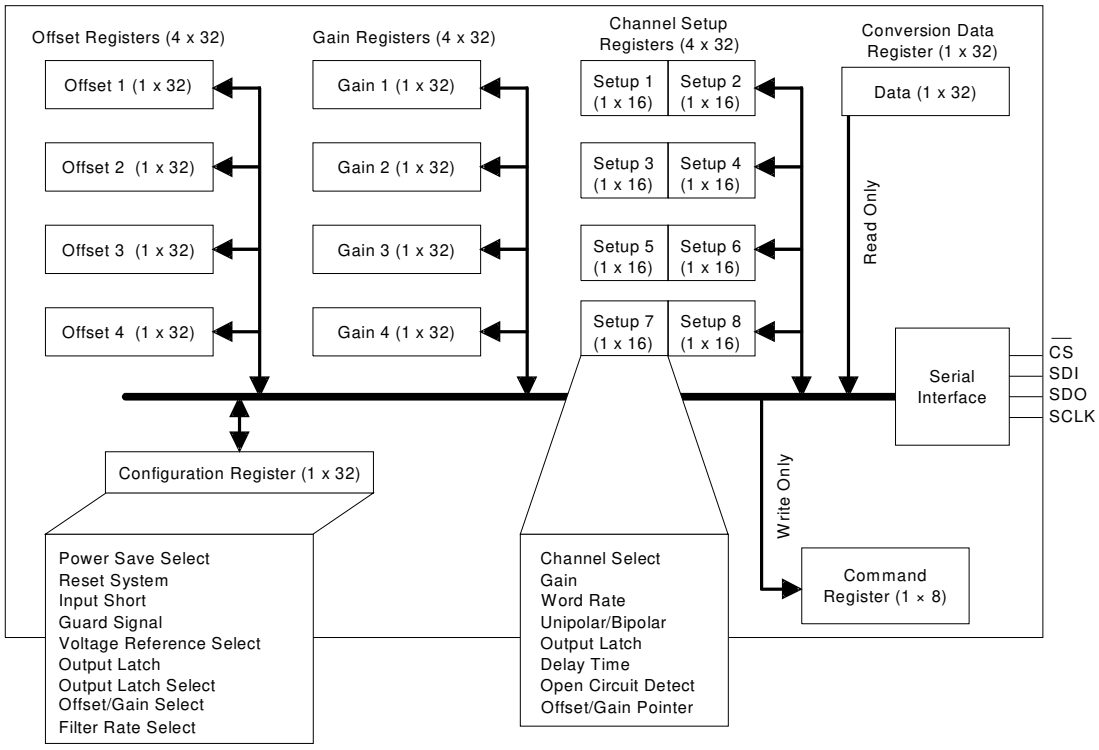


Figure 6. CS5532/34 Register Diagram

conversions or calibrations with the converter in the mode defined by one of these Setups.

Using the single conversion mode, an 8-bit command word can be written into the serial port. The command includes pointer bits which 'point' to a 16-bit command in one of the Channel Setup Registers which is to be executed. The 16-bit Setups can be programmed to perform a conversion on any of the input channels of the converter. More than one of the 16-bit Setups can be used for the same analog input channel. This allows the user to convert on the same signal with either a different conversion speed, a different gain range, or any of the other options available in the channel setup registers. Alternately, the user can set up the registers to perform different conversion conditions on each of the input channels.

The ADCs also include continuous conversion capability. The ADCs can be instructed to continuously convert, referencing one 16-bit command Setup. In the continuous conversions mode, the conversion data words are loaded into a shift register. The converter issues a flag on the SDO pin when a conversion cycle is completed so the user can read the register, if need be. See "Performing Conversions" on page 33 for more details.

The following pages document how to initialize the converter, perform offset and gain calibrations, and how to configure the converter for the various conversion modes. Each of the bits of the configuration register and of the Channel Setup Registers is described. A list of examples follows the description section. Also the *Command Register Quick Reference* can be used to decode all valid commands (the first 8 bits into the serial port).

2.2.1. System Initialization

The CS5532/34 provide no power-on-reset function. To initialize the ADCs, the user must perform a software reset by resetting the ADC's serial port with the Serial Port Initialization sequence. This sequence resets the serial port to the command mode and is accomplished by transmitting at least 15 SYNC1 command bytes (0xFF hexadecimal), followed by one SYNC0 command (0xFE hexadecimal). Note that this sequence can be initiated at anytime to reinitialize the serial port. To complete the system initialization sequence, the user must also perform a system reset sequence which is as follows: Write a logic 1 into the RS bit of the configuration register. This will reset the calibration registers and other logic (but not the serial port). A valid reset will set the RV bit in the configuration register to a logic 1. After writing the RS bit to a logic 1, wait 20 microseconds, then write the RS bit back to logic 0. While this involves writing an entire word into the configuration register, the RV bit is a read-only bit, therefore a write to the configuration register will not overwrite the RV bit. After clearing the RS bit back to logic 0, read the configuration register to check the state of the RV bit as this indicates that a valid reset occurred. Reading the configuration register clears the RV bit back to logic 0.

Completing the reset cycle initializes the on-chip registers to the following states:

Configuration Register:	00000000(H)
Offset Registers:	00000000(H)
Gain Registers:	01000000(H)
Channel Setup Registers:	00000000(H)

Note: Previous datasheets stated that the RS bit would clear itself back to logic 0 and therefore the user was not required to write the RS bit back to logic 0. The current data sheet instruction that requires the user to write into the configuration register to clear the RS bit has been added to insure that the RS bit is cleared. Characterization across multiple lots of silicon has indicated some chips do not automatically reset the RS bit to logic 0 in the configuration register, although the reset function is completed. This occurs only on small number of chips when the VA- supply is negative with respect to DGND. This has not caused an operational issue for customers because their start-up sequence includes

writing a word (with RS=0) into the configuration register after performing a reset. The change in the reset sequence to include writing the RS bit back to 0 insures the clearing of the RS bit in the event that a user does not write into the configuration register after the RS bit has been set.

The RV bit in the Configuration Register is set to indicate a valid reset has occurred. The RS bit should be written back to logic 0 to complete the reset cycle. After a system initialization or reset, the on-chip controller is initialized into command mode where it waits for a valid command (the first 8 bits written into the serial port are shifted into the command register). Once a valid command is received and decoded, the byte instructs the converter to either acquire data from or transfer data to an internal register(s), or perform a conversion or a calibration. The *Command Register Descriptions* section can be used to decode all valid commands.

2.2.2. Command Register Quick Reference

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	ARA	CS1	CS0	R/$\overline{W}$	RSB2	RSB1	RSB0

BIT	NAME	VALUE	FUNCTION
D7	Command Bit, C	0	Must be logic 0 for these commands.
		1	These commands are invalid if this bit is logic 1.
D6	Access Registers as Arrays, ARA	0	Ignore this function.
		1	Access the respective registers, offset, gain, or channel-setup, as an array of registers. The particular registers accessed are determined by the RS bits. The registers are accessed MSB first with physical channel 0 accessed first followed by physical channel 1 next and so forth.
D5-D4	Channel Select Bits, CS1-CS0	00 01 10 11	CS1-CS0 provide the address of one of the two (four for CS5534) physical input channels. These bits are also used to access the calibration registers associated with the respective physical input channel. Note that these bits are ignored when reading data register.
D3	Read/$\overline{Write}$, R/$\overline{W}$	0	Write to selected register.
		1	Read from selected register.
D2-D0	Register Select Bit, RSB3-RSB0	000	Reserved
		001	Offset Register
		010	Gain Register
		011	Configuration Register
		101	Channel-Setup Registers
		110	Reserved
		111	Reserved

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	MC	CSRP2	CSRP1	CSRP0	CC2	CC1	CC0

BIT	NAME	VALUE	FUNCTION
D7	Command Bit, C	0	These commands are invalid if this bit is logic 0.
		1	Must be logic 1 for these commands.
D6	Multiple Conversions, MC	0	Perform fully settled single conversions.
		1	Perform conversions continuously.
D5-D3	Channel-Setup Register Pointer Bits, CSRP	000 ... 111	These bits are used as pointers to the channel-setup registers. Either a single conversion or continuous conversions are performed on the channel setup register pointed to by these bits.
D2-D0	Conversion/Calibration Bits, CC2-CC0	000	Normal Conversion
		001	Self-Offset Calibration
		010	Self-Gain Calibration
		011	Reserved
		100	Reserved
		101	System-Offset Calibration
		110	System-Gain Calibration
		111	Reserved

2.2.3. Command Register Descriptions

READ/$\overline{\text{WRITE}}$ ALL OFFSET CALIBRATION REGISTERS

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	R/$\overline{W}$	0	0	1

Function: *These commands are used to access the offset registers as arrays.*

R/$\overline{W}$ (Read/$\overline{Write}$)

0 Write to selected registers.

1 Read from selected registers.

READ/$\overline{\text{WRITE}}$ ALL GAIN CALIBRATION REGISTERS

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	R/$\overline{W}$	0	1	0

Function: *These commands are used to access the gain registers as arrays.*

R/$\overline{W}$ (Read/$\overline{Write}$)

0 Write to selected registers.

1 Read from selected registers.

READ/$\overline{\text{WRITE}}$ ALL CHANNEL-SETUP REGISTERS

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	R/$\overline{W}$	1	0	1

Function: *These commands are used to access the channel-setup registers as arrays.*

R/$\overline{W}$ (Read/$\overline{Write}$)

0 Write to selected registers.

1 Read from selected registers.

READ/$\overline{\text{WRITE}}$ INDIVIDUAL OFFSET REGISTER

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	0	CS1	CS0	R/W	0	0	1

Function: *These commands are used to access each offset register separately. CS1 - CS0 decode the registers accessed.*

R/$\overline{W}$ (Read/$\overline{Write}$)

0 Write to selected register.

1 Read from selected register.

CS[1:0] (Channel Select Bits)

00 Offset Register 1

01 Offset Register 2

10 Offset Register 3 (CS5534 only)

11 Offset Register 4 (CS5534 only)

READ/$\overline{\text{WRITE}}$ INDIVIDUAL GAIN REGISTER

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	0	CS1	CS0	R/$\overline{W}$	0	1	0

Function: *These commands are used to access each gain register separately. CS1 - CS0 decode the registers accessed.*

R/$\overline{W}$ (Read/$\overline{\text{Write}}$)

0 Write to selected register.

1 Read from selected register.

CS[1:0] (Channel Select Bits)

00 Gain Register 1

01 Gain Register 2

10 Gain Register 3 (CS5534 only)

11 Gain Register 4 (CS5534 only)

READ/$\overline{\text{WRITE}}$ INDIVIDUAL CHANNEL-SETUP REGISTER

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	0	CS1	CS0	R/$\overline{W}$	1	0	1

Function: *These commands are used to access each channel-setup register separately. CS1 - CS0 decode the registers accessed.*

R/$\overline{W}$ (Read/$\overline{\text{Write}}$)

0 Write to selected register.

1 Read from selected register.

CS[1:0] (Channel Select Bits)

00 Channel-Setup Register 1

01 Channel-Setup Register 2

10 Channel-Setup Register 3

11 Channel-Setup Register 4

READ/$\overline{\text{WRITE}}$ CONFIGURATION REGISTER

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	R/$\overline{W}$	0	1	1

Function: *These commands are used to read from or write to the configuration register.*

R/$\overline{W}$ (Read/$\overline{\text{Write}}$)

0 Write to selected register.

1 Read from selected register.

PERFORM CONVERSION

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	MC	CSRP2	CSRP1	CSRP0	0	0	0

Function: *These commands instruct the ADC to perform either a single, fully-settled conversion or continuous conversions on the physical input channel pointed to by the pointer bits (CSRP2 - CRSP0) in the channel-setup register.*

MC (Multiple Conversions)

0 Perform a single conversion.

1 Perform continuous conversions.

CSRP [2:0] (Channel Setup Register Pointer Bits)

000 Setup 1

001 Setup 2

010 Setup 3

011 Setup 4

100 Setup 5

101 Setup 6

110 Setup 7

111 Setup 8

PERFORM CALIBRATION

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	0	CSRP2	CSRP1	CSRP0	CC2	CC1	CC0

Function: *These commands instruct the ADC to perform a calibration on the physical input channel selected by the setup register which is chosen by the command byte pointer bits (CSRP2 - CSRP0).*

CSRP [2:0] (Channel Setup Register Pointer Bits)

000 Setup 1
001 Setup 2
010 Setup 3
011 Setup 4
100 Setup 5
101 Setup 6
110 Setup 7
111 Setup 8

CC [2:0] (Calibration Control Bits)

000 Reserved
001 Self-Offset Calibration
010 Self-Gain Calibration
011 Reserved
100 Reserved
101 System-Offset Calibration
110 System-Gain Calibration
111 Reserved

SYNC1

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Function: *Part of the serial port re-initialization sequence.*

SYNC0

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	0

Function: *End of the serial port re-initialization sequence.*

NULL

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

Function: *This command is used to clear a port flag and keep the converter in the continuous conversion mode.*

2.2.4. Serial Port Interface

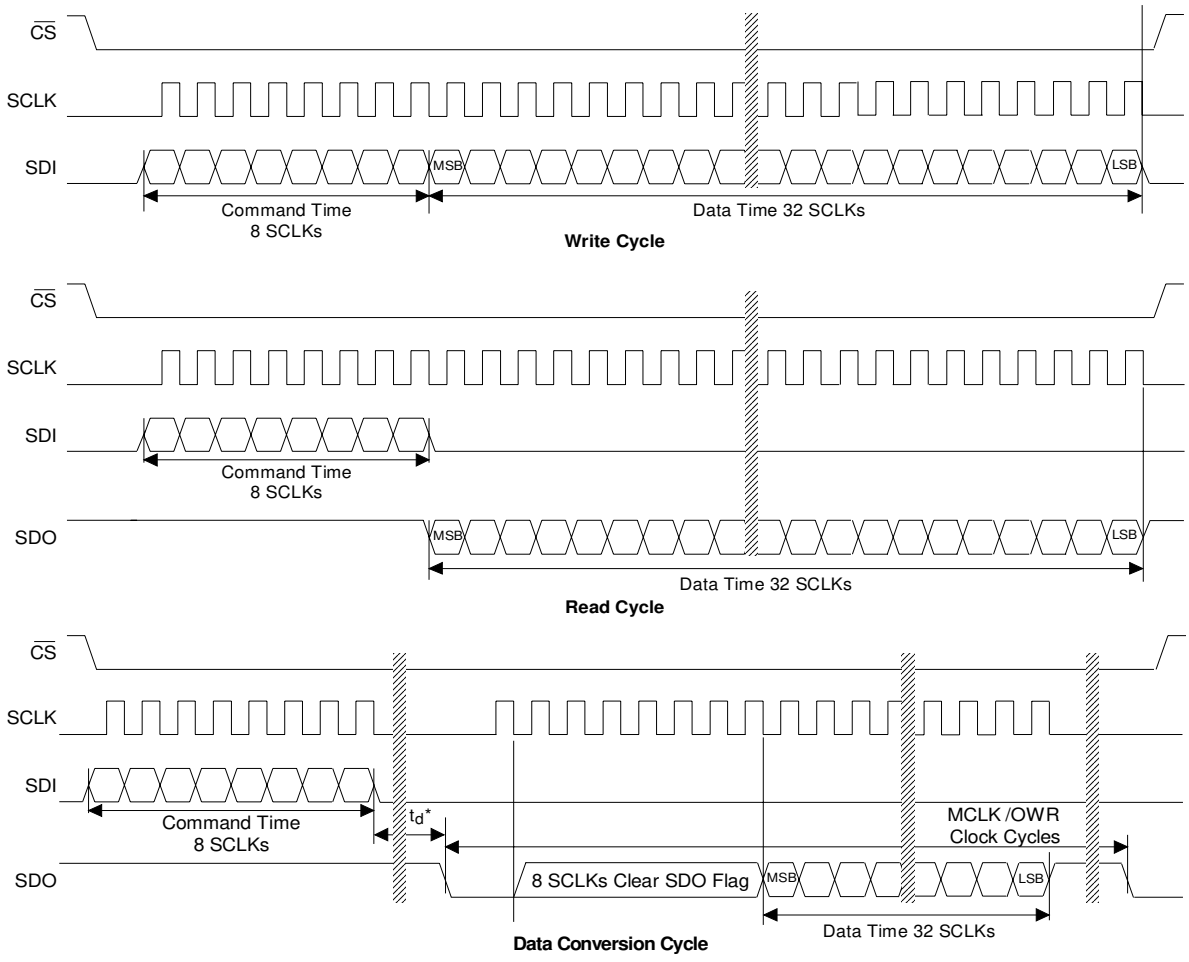
The CS5532/34's serial interface consists of four control lines: $\overline{CS}$, SDI, SDO, SCLK. Figure 7 details the command and data word timing.

$\overline{CS}$, Chip Select, is the control line which enables access to the serial port. If the $\overline{CS}$ pin is tied low, the port can function as a three wire interface.

SDI, Serial Data In, is the data signal used to transfer data to the converters.

SDO, Serial Data Out, is the data signal used to transfer output data from the converters. The SDO output will be held at high impedance any time $\overline{CS}$ is at logic 1.

SCLK, Serial Clock, is the serial bit-clock which controls the shifting of data to or from the ADC's serial port. The $\overline{CS}$ pin must be held low (logic 0) before SCLK transitions can be recognized by the port logic. To accommodate optoisolators SCLK is designed with a Schmitt-trigger input to allow an optoisolator with slower rise and fall times to directly drive the pin. Additionally, SDO is capable of sinking or sourcing up to 5 mA to directly drive an optoisolator LED. SDO will have less than a 400 mV loss in the drive voltage when sinking or sourcing 5 mA.



* td is the time it takes the ADC to perform a conversion. See the Single Conversion and Continuous Conversion sections of the data sheet for more details about conversion timing.

Figure 7. Command and Data Word Timing

2.2.5. Reading/Writing On-Chip Registers

The CS5532/34's offset, gain, configuration, and channel-setup registers are readable and writable while the conversion data register is read only.

As shown in Figure 7, to write to a particular register the user must transmit the appropriate write command and then follow that command by 32 bits of data. For example, to write 0x80000000 (hexadecimal) to physical channel one's gain register, the user would first transmit the command byte 0x02 (hexadecimal) followed by the data 0x80000000 (hexadecimal). Similarly, to read a particular register the user must transmit the appropriate read command and then acquire the 32 bits of data. Once a register is written to or read from, the serial port returns to the command mode.

In addition to accessing the internal registers one at a time, the gain and offset registers as well as the channel setup registers can be accessed as arrays (i.e. the entire register set can be accessed with one command). In the CS5532, there are two gain and offset registers, and in the CS5534, there are four gain and offset registers. There are four channel setup registers in both devices. As an example, to write 0x80000000 (hexadecimal) to all four gain registers in the CS5534, the user would transmit the command 0x42 (hexadecimal) followed by four iterations of 0x80000000 (hexadecimal), (i.e. 0x42 followed by 0x80000000, 0x80000000, 0x80000000, 0x80000000). The registers are written to or read from in sequential order (i.e, 1, followed by 2, 3, and 4). Once the registers are written to or read from, the serial port returns to the command mode.

2.3. Configuration Register

To ease the architectural design and simplify the serial interface, the configuration register is thirty-two bits long, however, only eleven of the thirty-two bits are used. The following sections detail the bits in the configuration register.

2.3.1. Power Consumption

The CS5532/34 accommodate three power consumption modes: normal, standby, and sleep. The default mode, "normal mode", is entered after power is applied. In this mode, the CS5532/34-BS devices typically consume 70 mW. The other two modes are referred to as the power save modes. They power down most of the analog portion of the chip and stop filter convolutions. The power save modes are entered whenever the power down (PDW) bit of the configuration register is set to logic 1. The particular power save mode entered depends on state of the PSS (Power Save Select) bit. If PSS is logic 0, the converter enters the standby mode reducing the power consumption to 4 mW. The standby mode leaves the oscillator and the on-chip bias generator for the analog portion of the chip active. This allows the converter to quickly return to the normal mode once PDW is set back to a logic 1. If PSS and PDW are both set to logic 1, the sleep mode is entered reducing the consumed power to around 500 µW. Since this sleep mode disables the oscillator, approximately a 20 ms oscillator start-up delay period is required before returning to the normal mode. If an external clock is used, there will be no delay. Further note that when the chips are used in the Gain = 1 mode, the PGIA is powered down. With the PGIA powered down, the power consumed in the normal power mode is reduced by approximately 1/2. Power consumption in the sleep and standby modes is not affected by the amplifier setting.

2.3.2. System Reset Sequence

The reset system (RS) bit permits the user to perform a system reset. A system reset can be initiated at any time by writing a logic 1 to the RS bit in the configuration register. After the RS bit has been set, the internal logic of the chip will be initialized to a reset state. The reset valid (RV) bit is set indicating that the internal logic was properly reset. The RV bit is cleared after the configuration regis-

ter is read. The on-chip registers are initialized to the following default states:

Configuration Register:	00000000(H)
Offset Registers:	00000000(H)
Gain Registers:	01000000(H)
Channel Setup Registers:	00000000(H)

After reset, the RS bit should be written back to logic 0 to complete the reset cycle. The ADC will return to the command mode where it waits for a valid command. Also, the RS bit is the only bit in the configuration register that can be set when initiating a reset (i.e. a second write command is needed to set other bits in the Configuration Register after the RS bit has been cleared).

2.3.3. Input Short

The input short bit allows the user to internally ground all the inputs of the multiplexer. This is a useful function because it allows the user to easily test the grounded input performance of the ADC and eliminate the noise effects due to the external system components.

2.3.4. Guard Signal

The guard signal bit modifies the function of A0. When set, this bit outputs the common mode voltage of the instrumentation amplifier on A0. This feature is useful when the user wants to connect an external shield to the common mode potential of the instrumentation amplifier to protect against leakage. Figure 8 illustrates a typical connection diagram for the guard signal.

2.3.5. Voltage Reference Select

The voltage reference select (VRS) bit selects the size of the sampling capacitor used to sample the voltage reference. The bit should be set based upon the magnitude of the reference voltage to achieve optimal performance. Figures 9 and 10 model the effects on the reference's input impedance and input current for each VRS setting. As the models show, the reference includes a coarse/fine charge buffer which reduces the dynamic current demand of the external reference.

The reference's input buffer is designed to accommodate rail-to-rail (common-mode plus signal) input voltages. The differential voltage between the VREF+ and VREF- can be any voltage from 1.0 V up to the analog supply (depending on how VRS is configured), however, the VREF+ cannot go above VA+ and the VREF- pin can not go below VA-. Note that the power supplies to the chip should be established before the reference voltage.

2.3.6. Output Latch Pins

The A1-A0 pins of the ADCs mimic the D21-D20/D5-D4 bits of the channel-setup registers if the output latch select (OLS) bit is logic 0 (default). If the OLS bit is logic 1, A1-A0 mimic the output latch bit settings in the configuration register. These two options give the user a choice of allowing the latch outputs to change anytime a different CSR is selected for a conversion, or to allow the latch bits to remain latched to a fixed state (determined by the configuration register bit) for all CSR selections. In either case, A1-A0 can be used to control external multiplexers and other logic functions outside the converter. The A1-A0 outputs can sink or source at least 1 mA, but it is recommended to limit drive currents to less than 20 µA to reduce self-heating of the chip. These outputs are powered

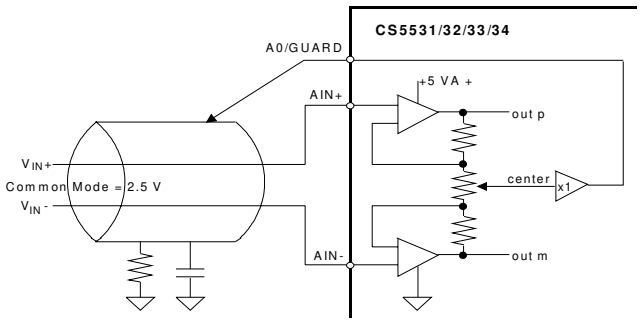


Figure 8. Guard Signal Shielding Scheme

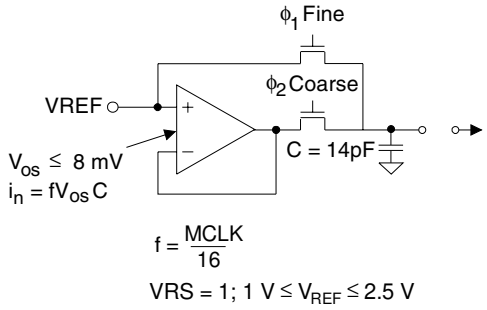


Figure 9. Input Reference Model when VRS = 1

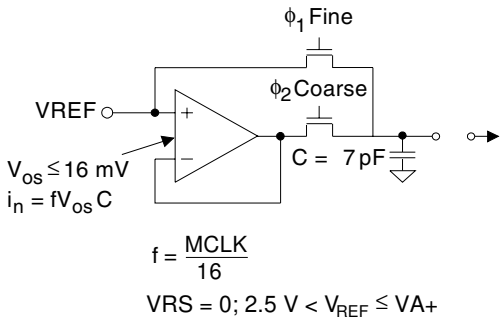


Figure 10. Input Reference Model when VRS = 0

from VA+ and VA-. Their output voltage will be limited to the VA+ voltage for a logic 1 and VA- for a logic 0.

2.3.7. Offset and Gain Select

The Offset and Gain Select bit (OGS) is used to select the source of the calibration registers to use when performing conversions and calibrations. When the OGS bit is set to '0', the offset and gain registers corresponding to the desired physical channel (CS1-CS0 in the selected Setup) will be accessed. When the OGS bit is set to '1', the offset and gain registers pointed to by the OG1-OG0 bits in the selected Setup will be accessed. This feature allows multiple calibration values (e.g. for different gain settings) to be used on a single physical channel without having to re-calibrate or manipulate the calibration registers.

2.3.8. Filter Rate Select

The Filter Rate Select bit (FRS) modifies the output word rates of the converter to allow either 50 Hz or 60 Hz rejection when operating from a 4.9152 MHz crystal. If FRS is cleared to logic 0, the word rates and corresponding filter characteristics can be selected (using the Channel Setup Registers) from 7.5, 15, 30, 60, 120, 240, 480, 960, 1920, or 3840 Sps when using a 4.9152 MHz clock. If FRS is set to logic 1, the word rates and corresponding filter characteristics scale by a factor of 5/6, making the selectable word rates 6.25, 12.5, 25, 50, 100, 200, 400, 800, 1600, and 3200 Sps when using a 4.9152 MHz clock. When using other clock frequencies, these selectable word rates will scale linearly with the clock frequency that is used.