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±2.5 V / 5 V, 200 kSps, 16-bit, High-throughput ΔΣ ADC

Features

- Single-ended Analog Input
- On-chip Buffers for High Input Impedance
- Conversion Time = 5 μS
- Settles in One Conversion
- Linearity Error = 0.0008%
- Signal-to-Noise = 80 dB
- S/(N + D) = 80 dB
- DNL = ±0.1 LSB Max.
- Simple three/four-wire serial interface
- Power Supply Configurations:
    - Analog: +5V/GND; IO: +1.8V to +3.3V
    - Analog: ±2.5V; IO: +1.8V to +3.3V
- Power Consumption:
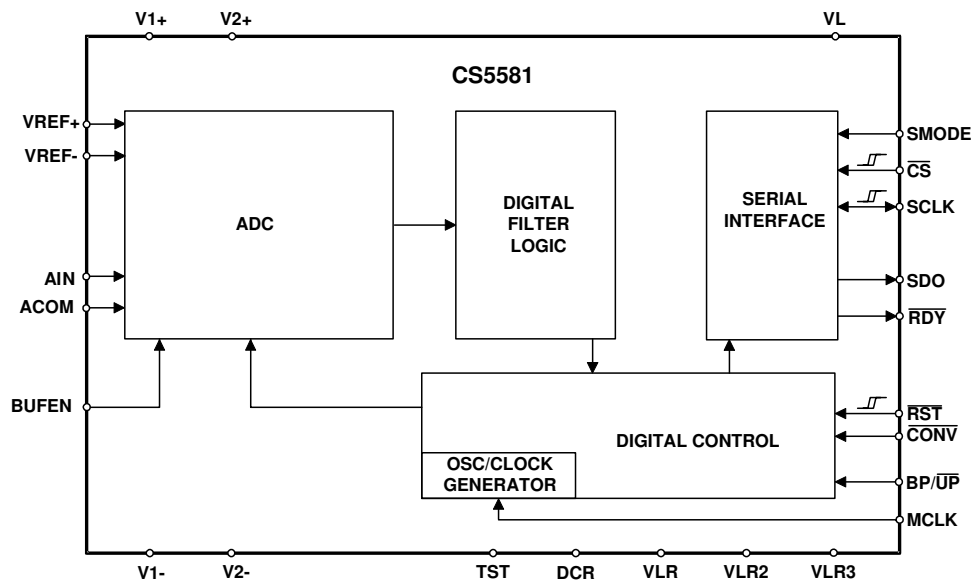   - ADC Input Buffers On: 85 mW
    - ADC Input Buffers Off: 60 mW

General Description

The CS5581 is a single-channel, 16-bit analog-to-digital converter capable of 200 kSps conversion rate. The input accepts a single-ended analog input signal. On-chip buffers provide high input impedance for both the AIN input and the VREF+ input. This significantly reduces the drive requirements of signal sources and reduces errors due to source impedances. The CS5581 is a delta-sigma converter capable of switching multiple input channels at a high rate with no loss in throughput. The ADC uses a low-latency digital filter architecture. The filter is designed for fast settling and settles to full accuracy in one conversion. The converter's 16-bit data output is in serial format, with the serial port acting as either a master or a slave. The converter is designed to support bipolar, ground-referenced signals when operated from ±2.5V analog supplies.

The converter can operate from an analog supply of 0-5V or from ±2.5V. The digital interface supports standard logic operating from 1.8, 2.5, or 3.3 V.

ORDERING INFORMATION:

MAR '08
DS796PP1

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LIST OF FIGURES

LIST OF TABLES

1. CHARACTERISTICS AND SPECIFICATIONS

• Min / Max characteristics and specifications are guaranteed over the specified operating conditions.

• Typical characteristics and specifications are measured at nominal supply voltages and T_A = 25°C.

• VLR = 0 V. All voltages measured with respect to 0 V.

ANALOG CHARACTERISTICS T_A = -40 to +85 °C; V1+ = V2+ = +2.5 V, ±5%; V1- = V2- = -2.5 V, ±5%; VL -VLR = 3.3 V, ±5%; VREF = (VREF+) - (VREF-) = 4.096V; MCLK = 16 MHz; SMODE = VL, unless otherwise stated; BUFEN = V1+ unless otherwise stated. Connected per Figure 6. Bipolar mode unless otherwise stated.

Parameter		Min	Typ	Max	Unit
Accuracy					
Linearity Error		-	0.0008	-	±%FS
Differential Linearity Error	(Note 1)	-	-	±0.1	LSB$_{16}$
Positive Full-scale Error		-	1.0	-	%FS
Negative Full-scale Error		-	1.0	-	%FS
Full-scale Drift	(Note 2, 3)	-	±1	-	LSB$_{16}$
Bipolar Offset	(Note 3)	-	±15	-	LSB$_{16}$
Bipolar Offset Drift	(Note 2, 3)	-	±1	-	LSB$_{16}$
Noise		-	140	-	μVrms
Dynamic Performance					
Peak Harmonic or Spurious Noise	1 kHz, -0.5 dB Input	-	-96	-	dB
	12 kHz, -0.5 dB Input	-	-96	-	dB
Total Harmonic Distortion	1 kHz, -0.5 dB Input	-	-95	-82	dB
Signal-to-Noise		77	80	-	dB
S/(N + D) Ratio	-0.5 dB Input, 1 kHz	-	80	-	dB
	-60 dB Input, 1 kHz	-	21	-	dB
-3 dB Input Bandwidth	(Note 4)	-	168	-	kHz

1. No missing codes is guaranteed at 16 bits resolution over the specified temperature range.
2. Total drift over specified temperature range after reset at power-up, at 25º C.
3. One LSB is equivalent to VREF ÷ 2^{16} or 4.096 ÷ 65536 = 62.5 μV.
4. Scales with MCLK.

ANALOG CHARACTERISTICS (CONTINUED)

T_A = -40 to +85 °C; V1+ = V2+ = +2.5 V, ±5%; V1- = V2- = -2.5 V, ±5%; VL -VLR = 3.3 V, ±5%; VREF = (VREF+) - (VREF-) = 4.096V; MCLK = 16 MHz; SMODE = VL, unless otherwise stated; BUFEN = V1+ unless otherwise stated. Connected per Figure 6.

Parameter		Min	Typ	Max	Unit
Analog Input					
Analog Input Range	Unipolar		0 to +VREF / 2		V
	Bipolar		±VREF / 2		V
Input Capacitance		-	10	-	pF
CVF Current (Note 5)	AIN Buffer On (BUFEN = V+)	-	600	-	nA
	AIN Buffer Off (BUFEN = V-)	-	130	-	µA
	ACOM	-	130	-	µA
Voltage Reference Input					
Voltage Reference Input Range (VREF+) – (VREF-) (Note 6)		2.4	4.096	4.2	V
Input Capacitance		-	10	-	pF
CVF Current	VREF+ Buffer On (BUFEN = V+)	-	3	-	µA
	VREF+ Buffer Off (BUFEN = V-)	-	1	-	mA
	VREF-	-	1	-	mA
Power Supplies					
DC Power Supply Currents	I_{V1}	-	-	18	mA
	I_{V2}	-	-	1.8	mA
	I_{VL}	-	-	0.6	mA
Power Consumption	Normal Operation Buffers On	-	85	101	mW
	Buffers Off	-	60	80	mW
Power Supply Rejection	(Note 7) V1+ , V2+ Supplies	-	80	-	dB
	V1-, V2- Supplies	-	80	-	dB

5.   Measured using an input signal of 1 V DC.

6.   For optimum performance, VREF+ should always be less than (V+) - 0.2 volts to prevent saturation of the VREF+ input buffer.

7.   Tested with 100 mVP-P on any supply up to 1 kHz. V1+ and V2+ supplies at the same voltage potential, V1- and V2- supplies at the same voltage potential.

SWITCHING CHARACTERISTICS

T_A = -40 to +85 °C; V1+ = V2+ = +2.5 V, ±5%; V1- = V2- = -2.5 V, ±5%;

VL - VLR = 3.3 V, ±5%, 2.5 V, ±5%, or 1.8 V, ±5%

Input levels: Logic 0 = 0V = Low; Logic 1 = VD+ = High; CL = 15 pF.

Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Frequency	Internal Oscillator	XIN	12	14	16	MHz
	External Clock	f_{clk}	0.5	16	16.2	MHz
Master Clock Duty Cycle			40	-	60	%
Reset						
$\overline{RST}$ Low Time (Note 8)		t_{res}	1	-	-	µs
$\overline{RST}$ rising to $\overline{RDY}$ falling	Internal Oscillator	t_{wup}	-	120	-	µs
	External Clock		-	1536	-	MCLKs
Conversion						
$\overline{CONV}$ Pulse Width		t_{cpw}	4	-	-	MCLKs
BP/$\overline{UP}$ setup to $\overline{CONV}$ falling (Note 9)		t_{scn}	0	-	-	ns
$\overline{CONV}$ low to start of conversion		t_{scn}	-	-	2	MCLKs
Perform Single Conversion ($\overline{CONV}$ high before $\overline{RDY}$ falling)		t_{bus}	20	-	-	MCLKs
Conversion Time (Note 10) Start of Conversion to $\overline{RDY}$ falling		t_{buh}	-	-	84	MCLKs

8. Reset must not be released until the power supplies and the voltage reference are within specification.

9. BP/$\overline{UP}$ can be changed coincident $\overline{CONV}$ falling. BP/$\overline{UP}$ must remain stable until $\overline{RDY}$ falls.

10. If $\overline{CONV}$ is held low continuously, conversions occur every 80 MCLK cycles.
    If $\overline{RDY}$ is tied to $\overline{CONV}$, conversions will occur every 82 MCLKs.
    If $\overline{CONV}$ is operated asynchronously to MCLK, a conversion may take up to 84 MCLKs.
    $\overline{RDY}$ falls at the end of conversion.

SWITCHING CHARACTERISTICS (CONTINUED)

T_A = -40 to +85 °C; V1+ = V2+ = +2.5 V, ±5%; V1- = V2- = -2.5 V, ±5%;

VL - VLR = 3.3 V, ±5%, 2.5 V, ±5%, or 1.8 V, ±5%

Input levels: Logic 0 = 0V = Low; Logic 1 = VD+ = High; CL = 15 pF.

Parameter		Symbol	Min	Typ	Max	Unit
Serial Port Timing in SSC Mode (SMODE = VL)						
$\overline{RDY}$ falling to MSB stable		t_1	-	-2	-	MCLKs
Data hold time after SCLK rising		t_2	-	10	-	ns
Serial Clock (Out) (Note 11, 12)	Pulse Width (low) Pulse Width (high)	t_3 t_4	50 50	- -	- -	ns ns
$\overline{RDY}$ rising after last SCLK rising		t_5	-	8	-	MCLKs

11. SDO and SCLK will be high impedance when $\overline{CS}$ is high. In some systems SCLK and SDO may require pull-down resistors.
12. SCLK = MCLK/2.
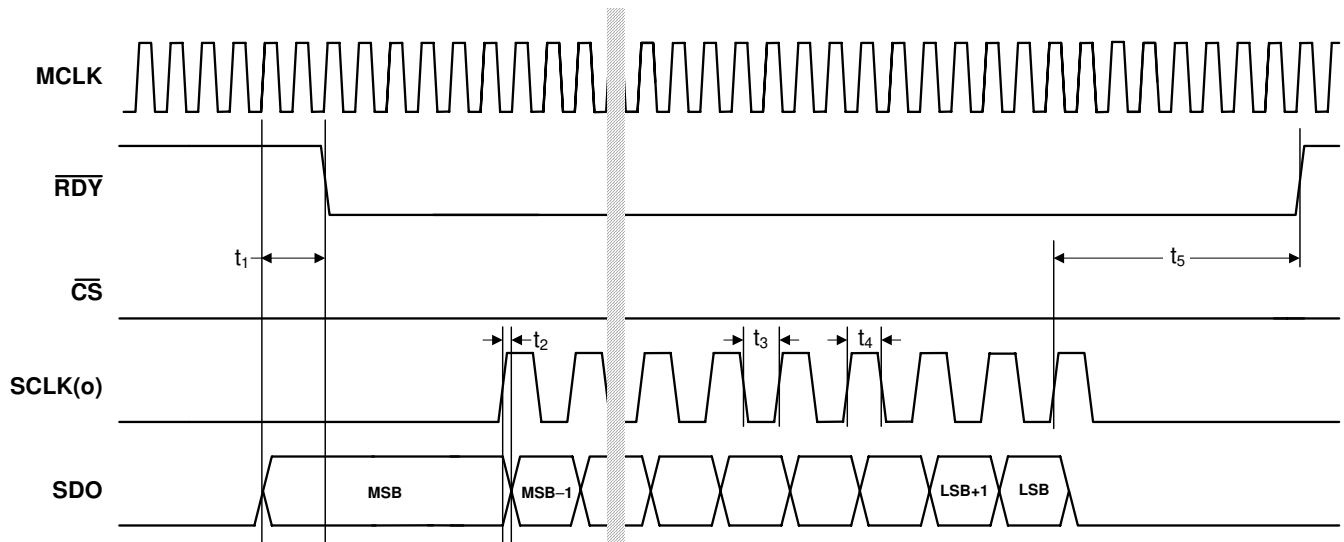
Figure 1. SSC Mode - Read Timing, $\overline{CS}$ remaining low (Not to Scale)

SWITCHING CHARACTERISTICS (CONTINUED)

T_A = -40 to +85 °C; V1+ = V2+ = +2.5 V, ±5%; V1- = V2- = -2.5 V, ±5%;

VL - VLR = 3.3 V, ±5%, 2.5 V, ±5%, or 1.8 V, ±5%

Input levels: Logic 0 = 0V = Low; Logic 1 = VD+ = High; CL = 15 pF.

Parameter		Symbol	Min	Typ	Max	Unit
Serial Port Timing in SSC Mode (SMODE = VL)						
Data hold time after SCLK rising		t_7	-	10	-	ns
Serial Clock (Out) (Note 13, 14)	Pulse Width (low)	t_8	50	-	-	ns
	Pulse Width (high)	t_9	50	-	-	ns
$\overline{RDY}$ rising after last SCLK rising		t_{10}	-	8	-	MCLKs
$\overline{CS}$ falling to MSB stable		t_{11}	-	10	-	ns
First SCLK rising after $\overline{CS}$ falling		t_{12}	-	8	-	MCLKs
$\overline{CS}$ hold time (low) after SCLK rising		t_{13}	10	-	-	ns
SCLK, SDO tristate after $\overline{CS}$ rising		t_{14}	-	5	-	ns

13. SDO and SCLK will be high impedance when $\overline{CS}$ is high. In some systems SCLK and SDO may require pull-down resistors.

14. SCLK = MCLK/2.

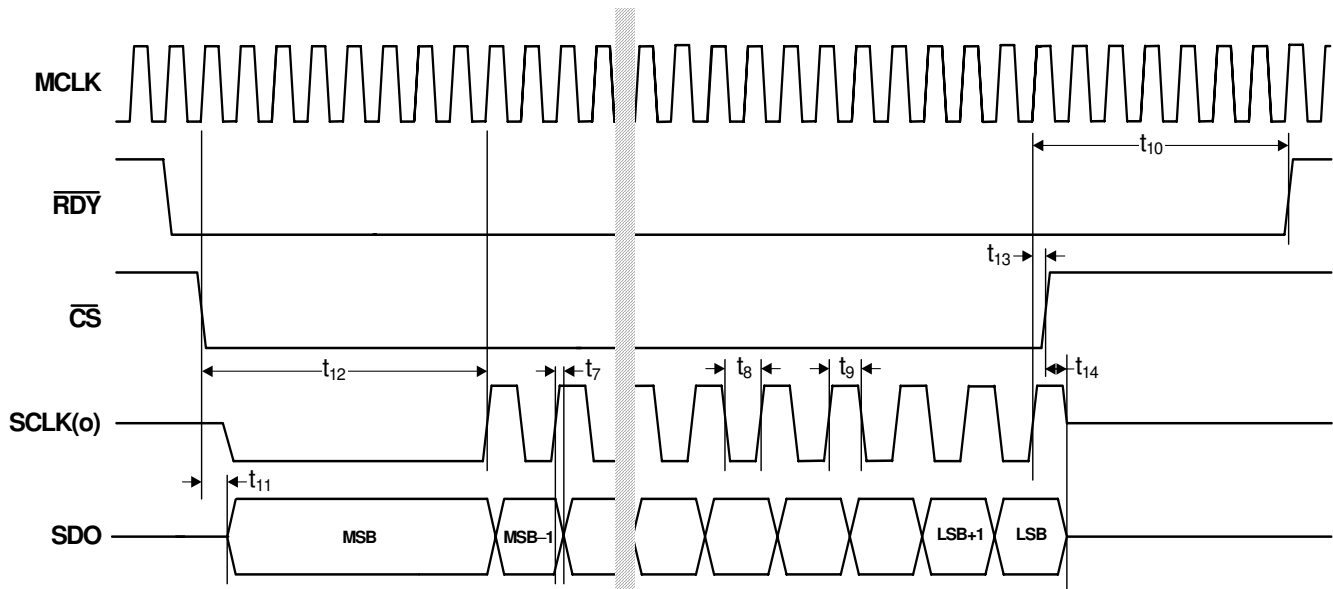**Figure 2. SSC Mode - Read Timing, $\overline{CS}$ falling after $\overline{RDY}$ falls (Not to Scale)**

SWITCHING CHARACTERISTICS (CONTINUED)

T_A = -40 to +85 °C; V1+ = V2+ = +2.5 V, ±5%; V1- = V2- = -2.5 V, ±5%;

VL - VLR = 3.3 V, ±5%, 2.5 V, ±5%, or 1.8 V, ±5%

Input levels: Logic 0 = 0V = Low; Logic 1 = VD+ = High; CL = 15 pF.

Parameter	Symbol	Min	Typ	Max	Unit
Serial Port Timing in SEC Mode (SMODE = VLR)					
SCLK(in) Pulse Width (High)	-	30	-	-	ns
SCLK(in) Pulse Width (Low)	-	30	-	-	ns
$\overline{CS}$ hold time (high) after $\overline{RDY}$ falling	t_{15}	10	-	-	ns
$\overline{CS}$ hold time (high) after SCLK rising	t_{16}	10	-	-	ns
$\overline{CS}$ low to SDO out of Hi-Z (Note 15)	t_{17}	-	10	-	ns
Data hold time after SCLK rising	t_{18}	-	10	-	ns
Data setup time before SCLK rising	t_{19}	10	-	-	ns
$\overline{CS}$ hold time (low) after SCLK rising	t_{20}	10	-	$\frac{1}{SCLK}-10$	ns
$\overline{RDY}$ rising after SCLK falling	t_{21}	-	10	-	ns

15. SDO will be high impedance when $\overline{CS}$ is high. In some systems SDO may require a pull-down resistor.
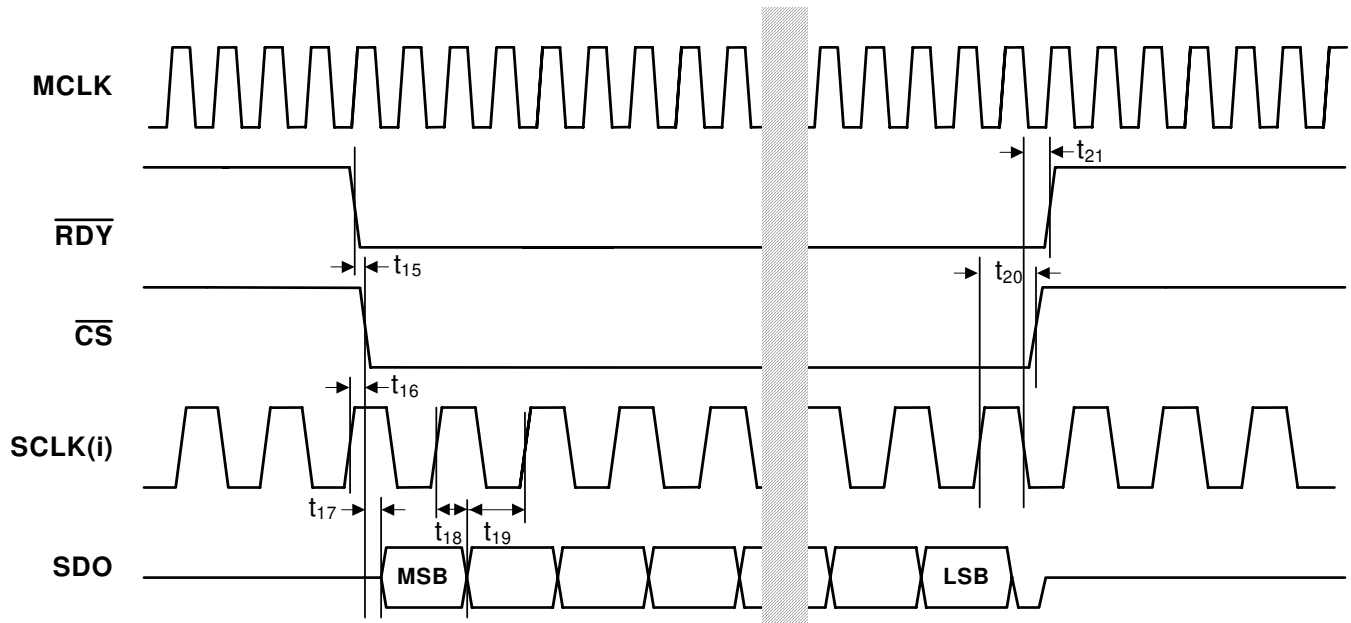
Figure 3. SEC Mode - Continuous SCLK Read Timing (Not to Scale)
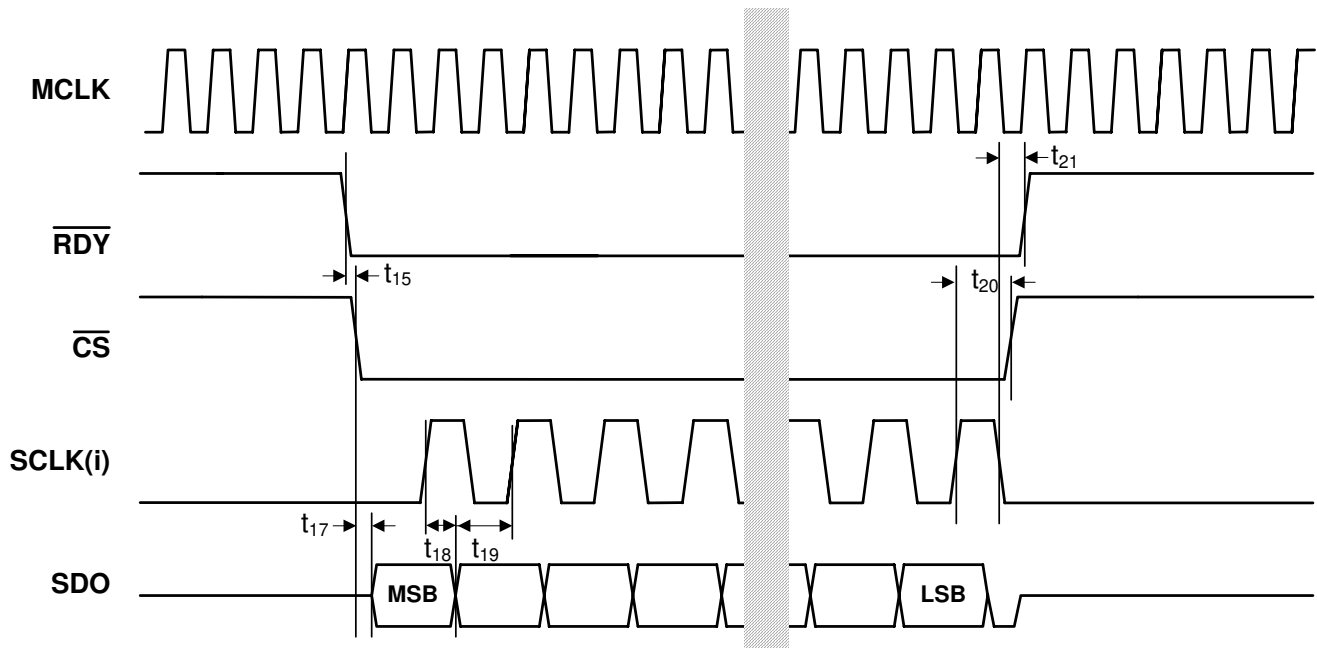
Figure 4. SEC Mode - Discontinuous SCLK Read Timing (Not to Scale)

DIGITAL CHARACTERISTICS

T_A = TMIN to TMAX; VL = 3.3V, ±5% or VL = 2.5V, ±5% or 1.8V, ±5%; VLR = 0V

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current	I_{in}	-	-	2	µA
Digital Input Pin Capacitance	C_{in}	-	3	-	pF
Digital Output Pin Capacitance	C_{out}	-	3	-	pF

GUARANTEED LOGIC LEVELS

T_A = -40 to +85 °C; V1+ = V2+ = +2.5 V, ±5%; V1- = V2- = -2.5 V, ±5%;
VL - VLR = 3.3 V, ±5%, 2.5 V, ±5%, or 1.8 V, ±5%
Input levels: Logic 0 = 0V = Low; Logic 1 = VD+ = High; CL = 15 pF.

Parameter	Sym	VL	Guaranteed Limits			Unit	Conditions
			Min	Typ	Max		
Logic Inputs							
Minimum High-level Input Voltage:	V_{IH}	3.3	1.9			V	
		2.5	1.6				
		1.8	1.2				
Maximum Low-level Input Voltage:	V_{IL}	3.3			1.1	V	
		2.5			0.95		
		1.8			0.6		
Logic Outputs							
Minimum High-level Output Voltage:	V_{OH}	3.3	2.9			V	I_{OH} = -2 mA
		2.5	2.1				
		1.8	1.65				
Maximum Low-level Output Voltage:	V_{OL}	3.3			0.36	V	I_{OH} = -2 mA
		2.5			0.36		
		1.8			0.44		

RECOMMENDED OPERATING CONDITIONS

(VLR = 0V, see Note 16)

Parameter		Symbol	Min	Typ	Max	Unit
Single Analog Supply						
DC Power Supplies:	(Note 16)					
	V1+	V1+	4.75	5.0	5.25	V
	V2+	V2-	4.75	5.0	5.25	V
	V1-	V1+	-	0	-	V
	V2-	V2-	-	0	-	V
Dual Analog Supplies						
DC Power Supplies:	(Note 16)					
	V1+	V1+	+2.375	+2.5	+2.625	V
	V2+	V2-	+2.375	+2.5	+2.625	V
	V1-	V1+	-2.375	-2.5	-2.625	V
	V2-	V2-	-2.375	-2.5	-2.625	V
Analog Reference Voltage	(Note 17) [VREF+] – [VREF-]	VREF	2.4	4.096	4.2	V

16. The logic supply can be any value VL – VLR = +1.71 to +3.465 volts as long as VLR ≥ V2- and VL ≤ 3.465 V.
17. The differential voltage reference magnitude is constrained by the V1+ or V1- supply magnitude.

ABSOLUTE MAXIMUM RATINGS

(VLR = 0V)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies:						
	[V1+] – [V1-] (Note 18)	-	0	-	5.5	V
	VL + [|V1-|] (Note 19)	-	0	-	6.1	V
Input Current, Any Pin Except Supplies	(Note 20)	I_{IN}	-	-	±10	mA
Analog Input Voltage	(AIN and VREF pins)	V_{INA}	(V1-) – 0.3	-	(V1+) + 0.3	V
Digital Input Voltage		V_{IND}	VLR – 0.3	-	VL + 0.3	V
Storage Temperature		T_{stg}	-65	-	150	°C

Notes: 18. V1+ = V2+; V1- = V2-
       19. V1- = V2-
       20. Transient currents of up to 100 mA will not cause SCR latch-up.

<center>WARNING:</center>

Recommended Operating Conditions indicate limits to which the device is functionally operational. Absolute Maximum Ratings indicate limits beyond which permanent damage to the device may occur. The Absolute Maximum Ratings are stress ratings only and the device should not be operated at these limits. Operation at conditions beyond the Recommended Operating Conditions may affect device reliability, and functional operation beyond Recommended Operating Conditions is not implied. Performance specifications are intended for the conditions specified for each table in the Characteristics and Specifications section.

2. OVERVIEW

The CS5581 is a 16-bit analog-to-digital converter capable of 200 kSps conversion rate. The analog input accepts a single-ended input with a magnitude of ±VREF / 2 volts. The ADC uses a low-latency digital filter architecture. The filter is designed for fast settling and settles to full accuracy in one conversion.

The converter is a serial output device. The serial port can be configured to function as either a master or a slave.

The converter can operate from an analog supply of 5V or from ±2.5V. The digital interface supports standard logic operating from 1.8, 2.5, or 3.3 V.

The CS5581 may convert at rates up to 200 kSps when operating from a 16 MHz input clock.

3. THEORY OF OPERATION

The CS5581 converter provides high-performance measurement of DC or AC signals. The converter can be used to perform single conversions or continuous conversions upon command. Each conversion is independent of previous conversions and settles to full specified accuracy, even with a full-scale input voltage step. This is due to the converter architecture which uses a combination of a high-speed delta-sigma modulator and a low-latency filter architecture.

Once power is established to the converter, a reset must be performed. A reset initializes the internal converter logic.

If $\overline{CONV}$ is held low, the converter will convert continuously with $\overline{RDY}$ falling every 80 MCLKs. This is equivalent to 200 kSps if MCLK = 16.0 MHz. If $\overline{CONV}$ is tied to $\overline{RDY}$, a conversion will occur every 82 MCLKs. If $\overline{CONV}$ is operated asynchronously to MCLK, it may take up to 84 MCLKs from $\overline{CONV}$ falling to $\overline{RDY}$ falling.

Multiple converters can operate synchronously if they are driven by the same MCLK source and $\overline{CONV}$ to each converter falls on the same MCLK falling edge. Alternately, $\overline{CONV}$ can be held low and all devices can be synchronized if they are reset with $\overline{RST}$ rising on the same falling edge of MCLK.

The output coding of the conversion word is a function of the BP/$\overline{UP}$ pin.

3.1 Converter Operation

The converter should be reset after the power supplies and voltage reference are stable.

The CS5581 converts at 200 kSps when synchronously operated ($\overline{CONV}$ = VLR) from a 16.0 MHz master clock. Conversion is initiated by taking $\overline{CONV}$ low. A conversion lasts 80 master clock cycles, but if $\overline{CONV}$ is asynchronous to MCLK there may be an uncertainty of 0-4 MCLK cycles after $\overline{CONV}$ falls to when a conversion actually begins. This may extend the throughput to 84 MCLKs per conversion.

When the conversion is completed, the output word is placed into the serial port and $\overline{RDY}$ goes low. To convert continuously, $\overline{CONV}$ should be held low. In continuous conversion mode with $\overline{CONV}$ held low, a conversion is performed in 80 MCLK cycles. Alternately $\overline{RDY}$ can be tied to $\overline{CONV}$ and a conversion will occur every 82 MCLK cycles.

To perform only one conversion, $\overline{CONV}$ should return high at least 20 master clock cycles before $\overline{RDY}$ falls.

Once a conversion is completed and $\overline{\text{RDY}}$ falls, $\overline{\text{RDY}}$ will return high when all the bits of the data word are emptied from the serial port or if the conversion data is not read and $\overline{\text{CS}}$ is held low, $\overline{\text{RDY}}$ will go high two MCLK cycles before the end of conversion. $\overline{\text{RDY}}$ will fall at the end of the next conversion when new data is put into the port register.

See *Serial Port* on page 24 for information about reading conversion data.

Conversion performance can be affected by several factors. These include the choice of clock source for the chip, the timing of $\overline{\text{CONV}}$, and the choice of the serial port mode.

The converter can be operated from an internal oscillator. This clock source has greater jitter than an external crystal-based clock. Jitter may not be an issue when measuring DC signals, or very-low-frequency AC signals, but can become an issue for higher frequency AC signals. For maximum performance when digitizing AC signals, a low-jitter MCLK should be used.

To maximize performance, the $\overline{\text{CONV}}$ pin should be held low in the continuous conversion state to perform multiple conversions, or $\overline{\text{CONV}}$ should occur synchronous to MCLK, falling when MCLK falls.

If the converter is operated at maximum throughput, the SSC serial port mode is less likely to cause interference to measurements as the SCLK output is synchronized to the MCLK. Alternately, any interference due to serial port clocking can also be minimized if data is read in the SEC serial port mode when a conversion is not in progress.

3.2 Clock

The CS5581 can be operated from its internal oscillator or from an external master clock. The state of MCLK determines which clock source will be used. If MCLK is tied low, the internal oscillator will start and be used as the clock source for the converter. If an external CMOS-compatible clock is input into MCLK, the converter will power down the internal oscillator and use the external clock. If the MCLK pin is held high, the internal oscillator will be held in the stopped state. The MCLK input can be held high to delete clock cycles to aid in synchronizing multiple converters in different phase relationships.

The internal oscillator can be used if the signals to be measured are essentially DC. The internal oscillator exhibits jitter at about 500 picoseconds rms. If the CS5581 is used to digitize AC signals, an external low-jitter clock source should be used.

If the internal oscillator is used as the clock for the CS5581, the maximum conversion rate will be dictated by the oscillator frequency.

If driven from an external MCLK source, the fast rise and fall times of the MCLK signal can result in clock coupling from the internal bond wire of the IC to the analog input. Adding a 50 ohm resistor on the external MCLK source significantly reduces this effect.
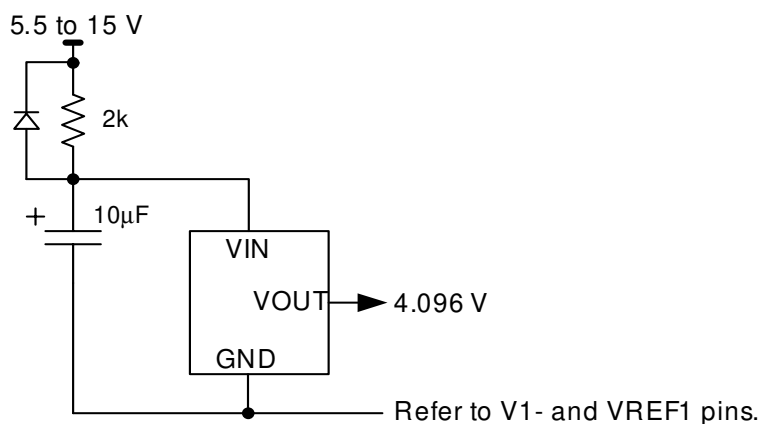
3.3 Voltage Reference

The voltage reference for the CS5581 can range from 2.4 volt to 4.2 volts. A 4.096 volt reference is required to achieve the specified signal-to-noise performance. Figure 6 and Figure 7 illustrate the connection of the voltage reference with either a single +5 V analog supply or with ±2.5 V.

For optimum performance, the voltage reference device should be one that provides a capacitor connection to provide a means of noise filtering, or the output should include some type of bandwidth-limiting filter.

Some 4.096 volt reference devices need only 5 volts total supply for operation and can be connected as shown in Figure 6 or Figure 7. The reference should have a local bypass capacitor and an appropriate output capacitor.

Some older 4.096 voltage reference designs require more headroom and must operate from an input voltage of 5.5 to 6.5 volts. If this type of voltage reference is used ensure that when power is applied to the system, the voltage reference rise time is slower than the rise time of the V1+ and V1- power supply voltage to the converter. An example circuit to slow the output startup time of the reference is illustrated in Figure 5.

Figure 5. Voltage Reference Circuit

3.4 Analog Input

The analog input of the converter is single-ended with a full-scale input of ±2.048 volts, relative to the ACOM pin. This is illustrated in Figure 6 and Figure 7. These diagrams also illustrate a differential buffer amplifier configuration for driving the CS5581.

The capacitors at the outputs of the amplifiers provide a charge reservoir for the dynamic current from the A/D inputs while the resistors isolate the dynamic current from the amplifier. The amplifiers can be powered from higher supplies than those used by the A/D but precautions should be taken to ensure that the op amp output voltage remains within the power supply limits of the A/D, especially under start-up conditions.

3.5 Output Coding Format

The reference voltage directly defines the input voltage range in both the unipolar and bipolar configurations. In the unipolar configuration (BP/$\overline{UP}$ low), the first code transition occurs 0.5 LSB above zero, and the final code transition occurs 1.5 LSBs below VREF. In the bipolar configuration (BP/$\overline{UP}$ high), the first code transition occurs 0.5 LSB above -VREF and the last transition occurs 1.5 LSBs below +VREF. See Table 1 for the output coding of the converter.

Table 1. Output Coding, Two's Complement

Bipolar Input Voltage	Two's Complement
>(VREF-1.5 LSB)	7F FF
VREF-1.5 LSB	7F FF / 7F FE
-0.5 LSB	00 00 / FF FF
-VREF+0.5 LSB	80 01 / 80 00
<(-VREF+0.5 LSB)	80 00

NOTE: VREF = [(VREF+) - (VREF-)] / 2

Table 2. Output Coding, Offset Binary

Unipolar Input Voltage	Offset Binary
>(VREF-1.5 LSB)	FF FF
VREF-1.5 LSB	FF FF / FF FE
(VREF/2)-0.5 LSB	80 00 / 7F FF
+0.5 LSB	00 01 / 00 00
<(+0.5 LSB)	00 00

NOTE: VREF = [(VREF+) - (VREF-)] / 2

3.6 Typical Connection Diagrams

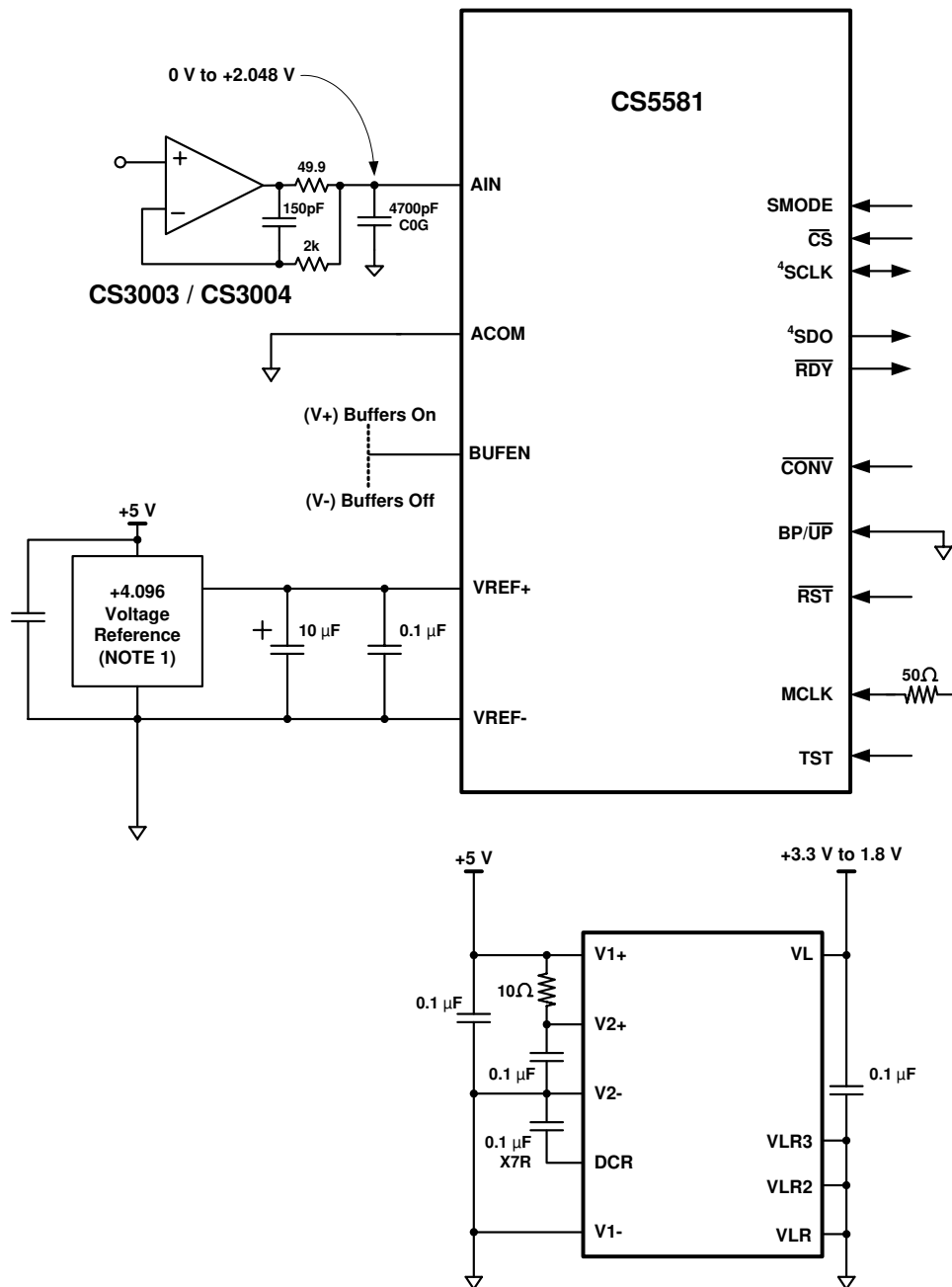The following figure depicts the CS5581 powered from bipolar analog supplies, +2.5 V and - 2.5 V.
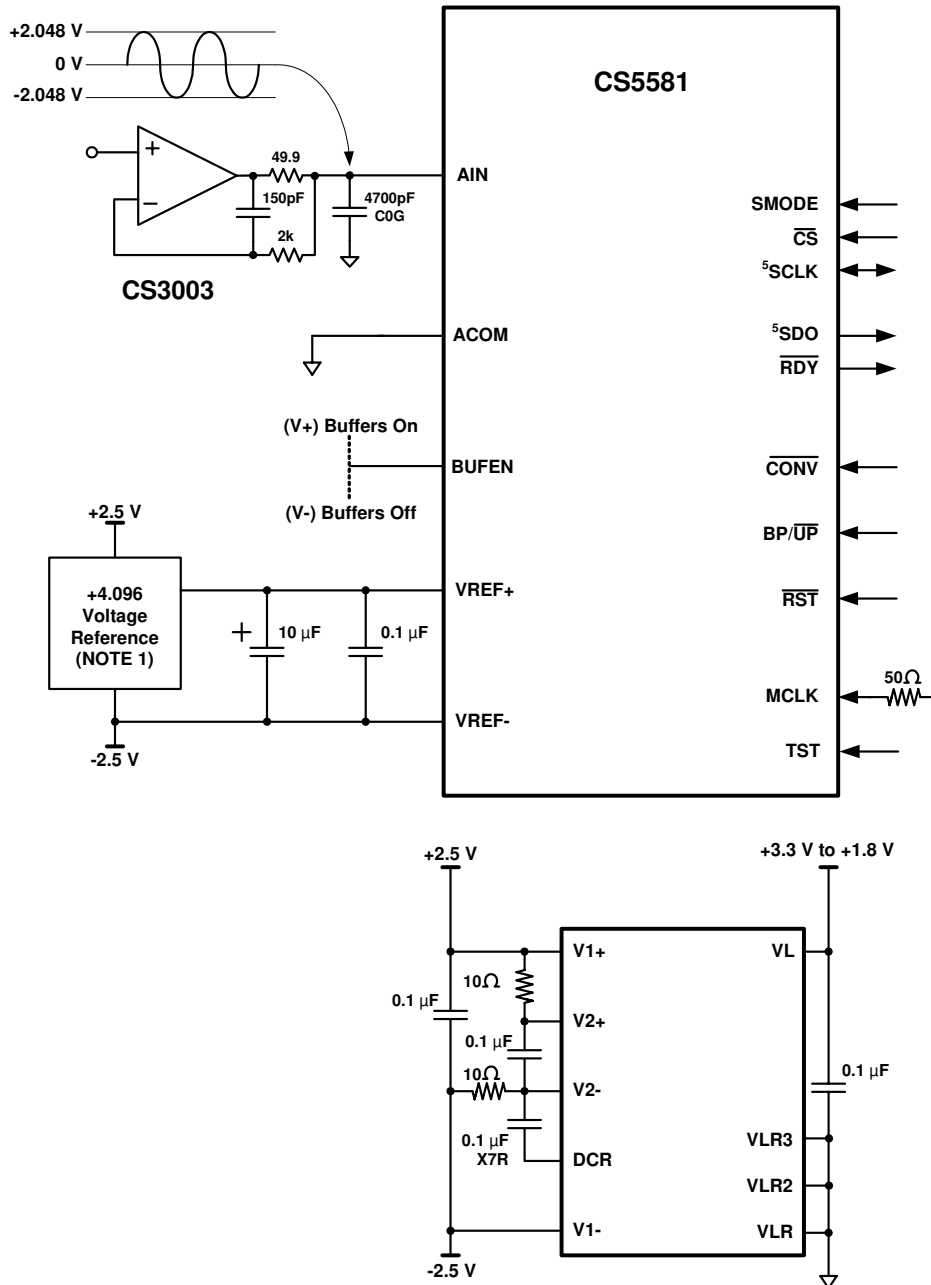
NOTES
1. See Section 3.3 Voltage Reference for information on required voltage reference performance criteria.
2. Locate capacitors so as to minimize loop length.
3. The ±2.5 V supplies should also be bypassed to ground at the converter.
4. VLR and the power supply ground for the ±2.5 V should be connected to the same ground plane under the chip.
5. SCLK and SDO may require pull-down resistors in some applications.

Figure 6. CS5581 Configured Using ±2.5V Analog Supplies

The following figure depicts the CS5581 part powered from a single 5V analog supply and configured for unipolar measurement.
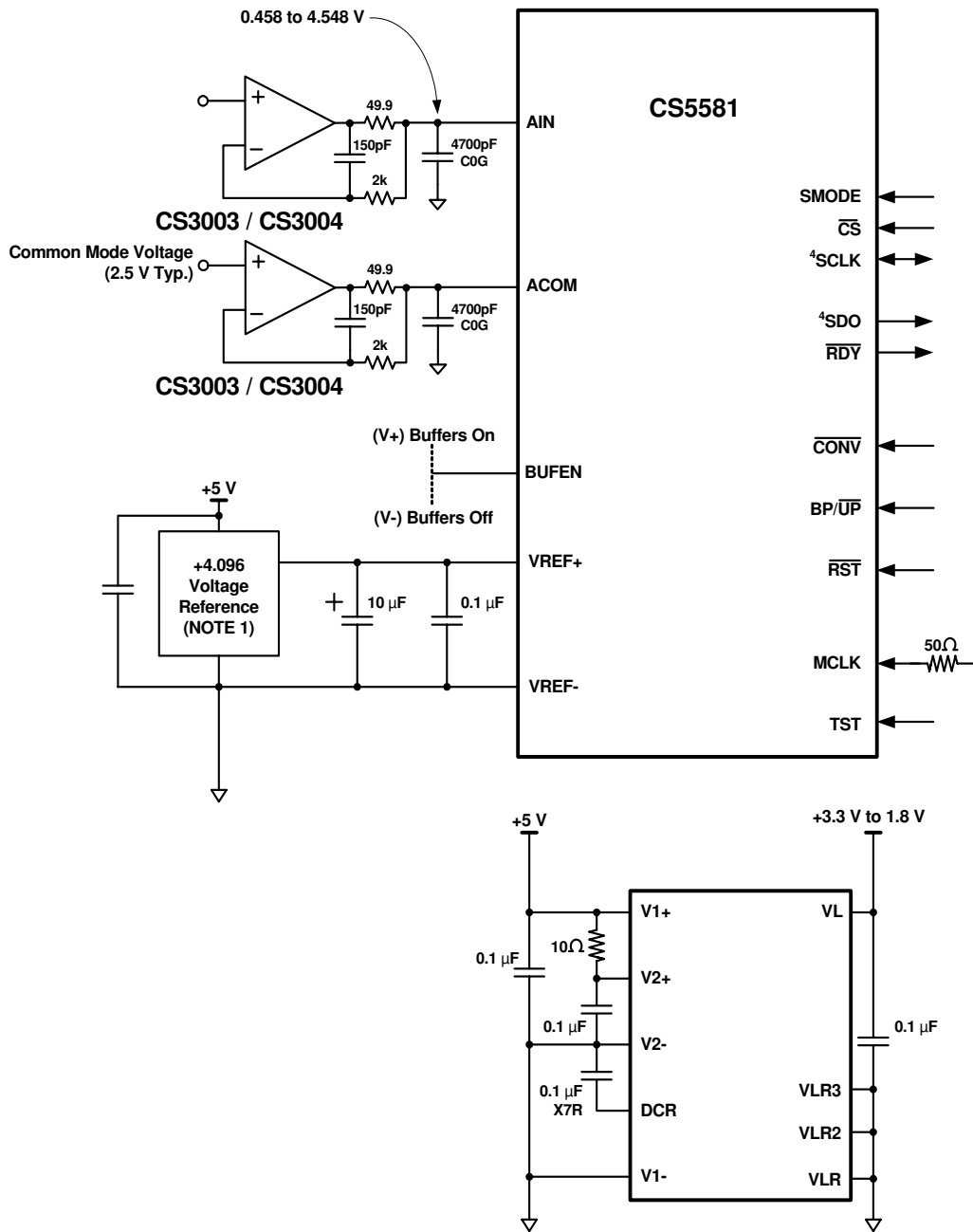
CS5581

0 V to +2.048 V

49.9
150pF
2k
4700pF
C0G

AIN

CS3003 / CS3004

SMODE
$\overline{CS}$
[4]SCLK
[4]SDO
$\overline{RDY}$

ACOM

(V+) Buffers On

BUFEN

$\overline{CONV}$

(V-) Buffers Off

BP/$\overline{UP}$

+5 V

$\overline{RST}$

+4.096
Voltage
Reference
(NOTE 1)

VREF+

10 μF   0.1 μF

MCLK   50Ω

VREF-

TST

+5 V   +3.3 V to 1.8 V

V1+   VL

0.1 μF   10Ω

V2+

0.1 μF

V2-   0.1 μF

0.1 μF
X7R   DCR   VLR3

VLR2

V1-   VLR

NOTES
1. See Section 3.3 Voltage Reference for information on required voltage reference performance criteria.
2. Locate capacitors so as to minimize loop length.
3. V1-, V2-, and VLR should be connected to the same ground plane under the chip.
4. SCLK and SDO may require pull-down resistors in some applications.

Figure 7. CS5581 Configured for Unipolar Measurement Using a Single 5V Analog Supply

The following figure depicts the CS5581 part powered from a single 5V analog supply and configured for bipolar measurement, referenced to a common mode voltage of 2.5 V.

0.458 to 4.548 V

CS5581

49.9
150pF
2k
4700pF
C0G
AIN

SMODE
$\overline{CS}$
[4]SCLK

[4]SDO
$\overline{RDY}$

CS3003 / CS3004

Common Mode Voltage
(2.5 V Typ.)

49.9
150pF
2k
4700pF
C0G
ACOM

CS3003 / CS3004

(V+) Buffers On

BUFEN

$\overline{CONV}$

BP/$\overline{UP}$

$\overline{RST}$

+5 V

(V-) Buffers Off

+4.096
Voltage
Reference
(NOTE 1)

10 μF   0.1 μF

VREF+

VREF-

MCLK   50Ω

TST

+5 V   +3.3 V to 1.8 V

0.1 μF   10Ω

V1+   VL

V2+

0.1 μF   V2-

0.1 μF
X7R   DCR

0.1 μF

V1-

VLR3

VLR2

VLR

NOTES
1. See Section 3.3 Voltage Reference for information on required voltage reference performance criteria.
2. Locate capacitors so as to minimize loop length.
3. V1-, V2-, and VLR should be connected to the same ground plane under the chip.
4. SCLK and SDO may require pull-down resistors in some applications.

Figure 8. CS5581 Configured for Bipolar Measurement Using a Single 5V Analog Supply

3.7 AIN & VREF Sampling Structures

The CS5581 uses on-chip buffers on the AIN and the VREF+ inputs. Buffers provide much higher input impedance and therefore reduce the amount of drive current required from an external source. This helps minimize errors.

The Buffer Enable (BUFEN) pin determines if the on-chip buffers are used or not. If the BUFEN pin is connected to the V1+ supply, the buffers will be enabled.   If the BUFEN pin is connected to the V1- pin, the buffers are off. The converter will consume about 30 mW less power when the buffers are off, but the input impedances of AIN, ACOM and VREF+ will be significantly less than with the buffers enabled.

3.8 Converter Performance

The CS5581 achieves excellent differential nonlinearity (DNL) as shown in Figures 9 and 10. Figure 9 illustrates the code widths on the typical scale of ±1 LSB. Figure 10 illustrates a zoomed scale of ±0.1 LSB. The DNL error histogram in Figure 10 indicates that more than half the codes are accurate to better than ±0.01 LSB.
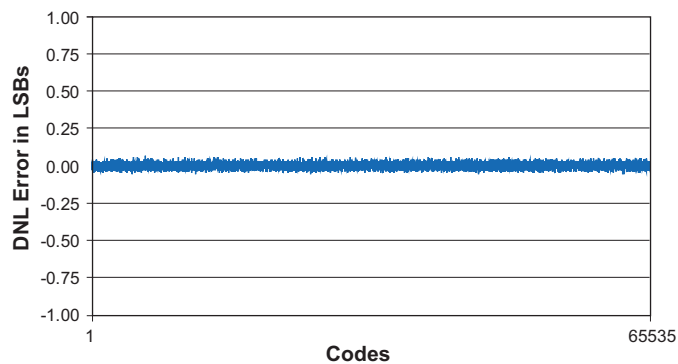

Figure 9. CS5581 DNL Plot
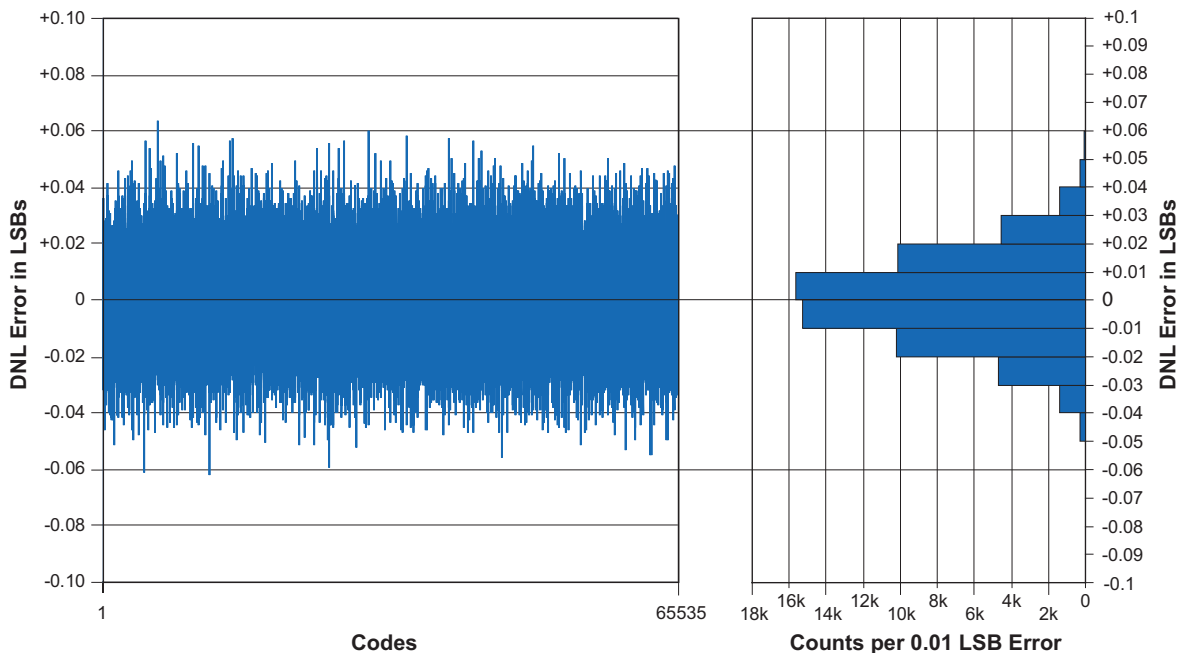
Figure 10. CS5581 DNL Error Plot with DNL Histogram

![Cirrus Logic logo]

CS5581

Figures 11 through 16 illustrate the performance of the CS5581 when driven by a 5.55 kHz sine wave at various amplitudes. In each case, the captured data was windowed with a seven-term window function that exhibits 4.3 dB of attenuation before being processed by the FFT.

Figure 14 illustrates the converter performance with an input that is 1/10,000 of full scale. This is a signal magnitude of about 6.5 codes, peak to peak.
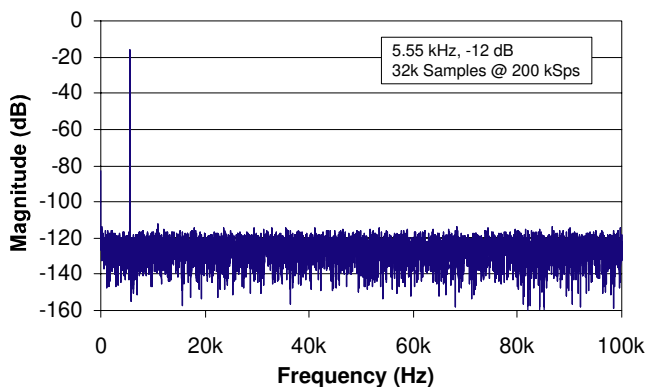
Figure 15 illustrates the converter performance with an input that is 1/100,000 of full scale, or about 0.65 of a code, peak to peak. These plots illustrate that this converter has excellent small-signal performance due to the near-perfect DNL of the converter.
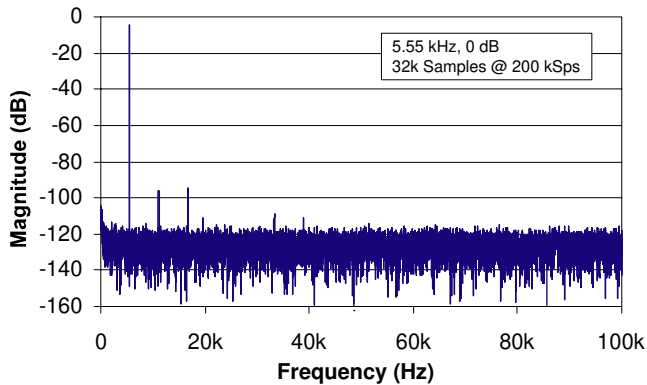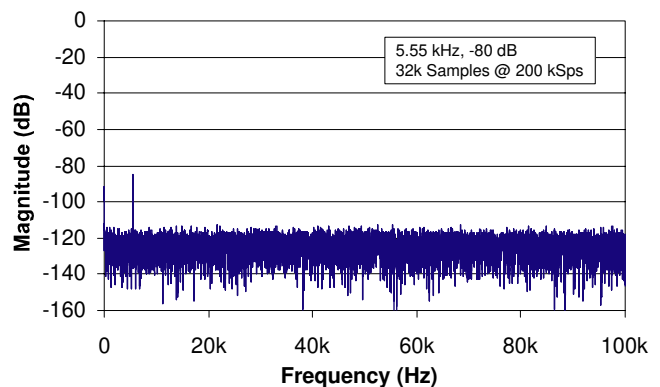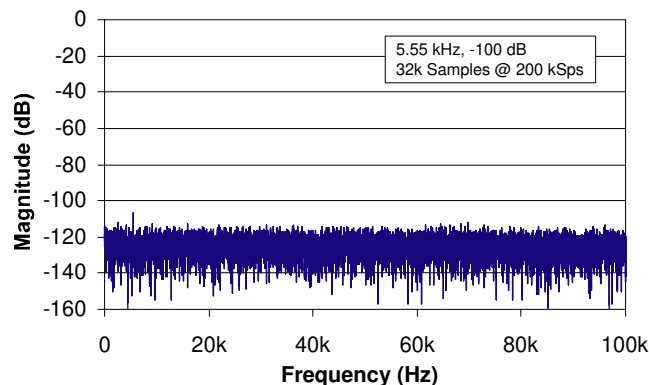

Figure 11. Spectral Performance, 0 dB
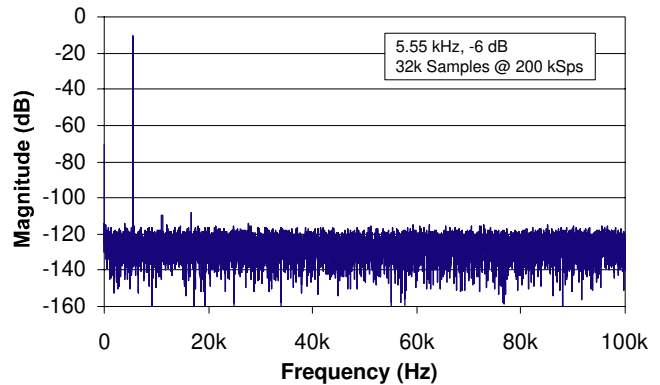
Figure 12. Spectral Performance, -6 dB

Figure 13. Spectral Performance, -12 dB

Figure 14. Spectral Performance, -80 dB

Figure 15. Spectral Performance, -100 dB

![CS5581 logo](Cirrus Logic)

Figure 16 illustrates the noise floor of the converter from 0.1 Hz to 100 kHz. While the plot does exhibit some 1/f noise at lower frequencies, the noise floor is entirely free of spurious frequency content due to digital activity inside the chip.

Figure 17 illustrates a noise histogram of 4096 samples.
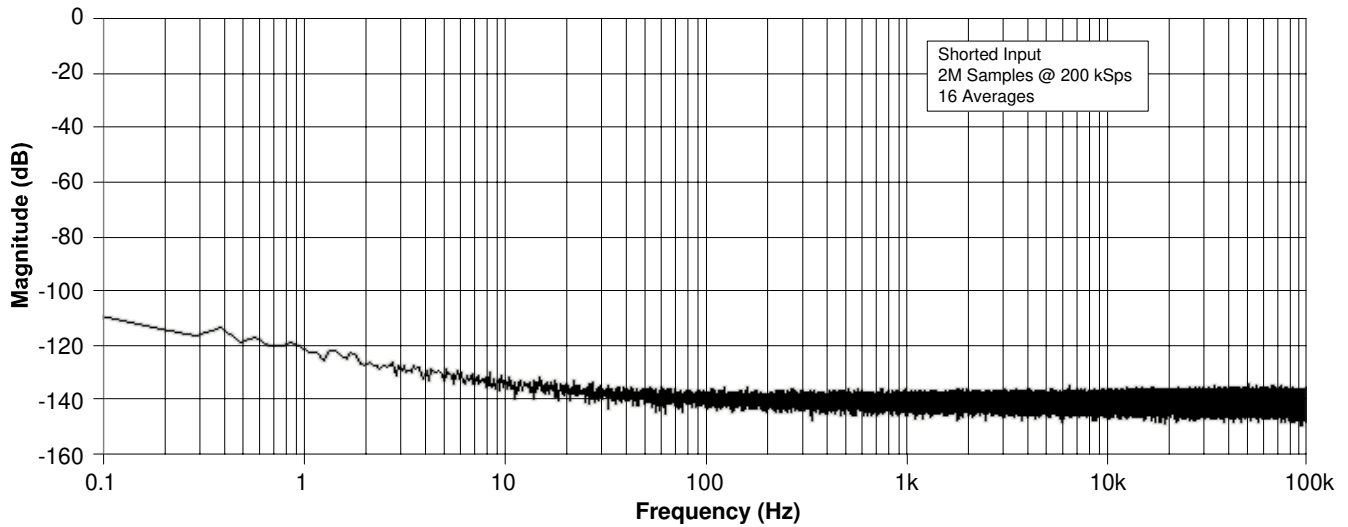
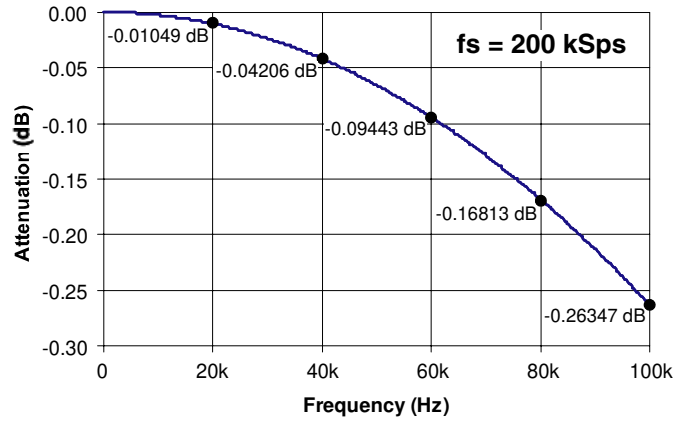**Figure 16. Spectral Plot of Noise with Shorted Input**
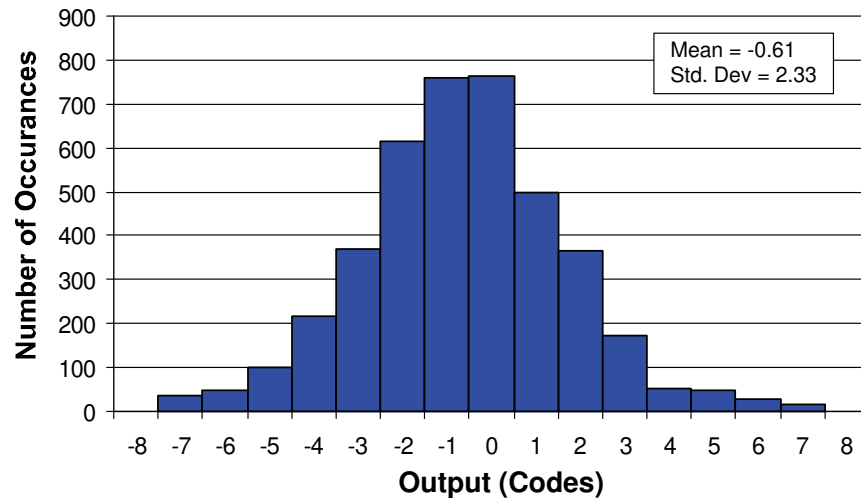
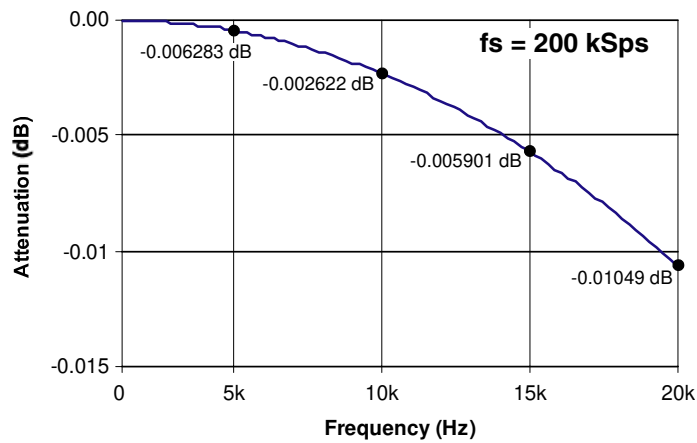**Figure 17. Noise Histogram (4096 Conversions)**
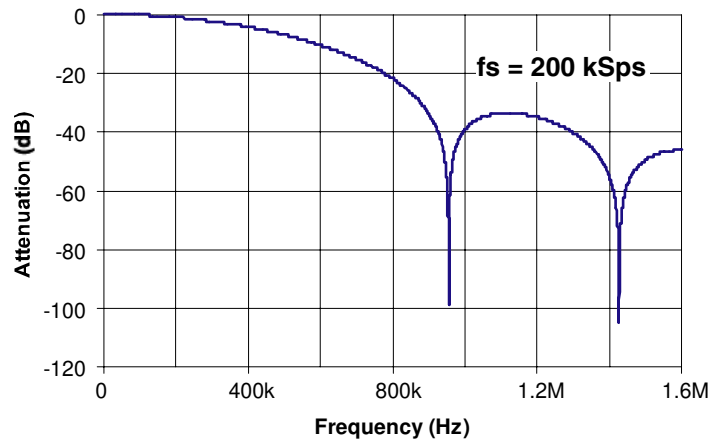
3.9 Digital Filter Characteristics

The digital filter is designed for fast settling, therefore it exhibits very little in-band attenuation. The filter attenuation is 0.26347 dB at 100 kHz when sampling at 200 kSps.

Figure 18. CS5581 Spectral Response (DC to fs/2)

Figure 19. CS5581 Spectral Response (DC to 20 kHz)

Figure 20. CS5581 Spectral Response (DC to 8fs)

3.10 Serial Port

The serial port on the CS5581 can operate in two different modes: synchronous self clock (SSC) mode & synchronous external clock (SEC) mode.

3.10.1 SSC Mode

If the SMODE pin is high (SMODE = VL), the serial port operates in the SSC (Synchronous Self Clock) mode. In the SSC mode the port shifts out conversion data words with SCLK as an output. SCLK is generated inside the converter from MCLK. Data is output from the SDO (Serial Data Output) pin. If CS is high, the SDO and SCLK pins will stay in a high-impedance state. If CS is low when RDY falls, the conversion data word will be output from SDO MSB first. Data is output on the rising edge of SCLK and should be latched into the external logic on the subsequent rising edge of SCLK. When all bits of the conversion word are output from the port the RDY signal will return to high.

3.10.2 SEC Mode

If the SMODE pin is low (SMODE = VLR), the serial port operates in the SEC (Synchronous External Clock mode). In this mode, the user usually monitors RDY. When RDY falls at the end of a conversion, the conversion data word is placed into the output data register in the serial port. CS is then activated low to enable data output. Note that CS can be held low continuously if it is not necessary to have the SDO output operate in the high impedance state. When CS is taken low (after RDY falls) the conversion data word is then shifted out of the SDO pin by driving the SCLK pin from system logic external to the converter. Data bits are advanced on rising edges of SCLK and latched by the subsequent rising edge of SCLK.

If CS is held low continuously, the RDY signal will fall at the end of a conversion and the conversion data will be placed into the serial port. If the user starts a read, the user will maintain control over the serial port until the port is empty. However, if SCLK is not toggled, the converter will overwrite the conversion data at the completion of the next conversion. If CS is held low and no read is performed, RDY will rise just prior to the end of the next conversion and then fall to signal that new data has been written into the serial port.

3.11 Power Supplies & Grounding

The CS5581 can be configured to operate with its analog supply operating from 5V, or with its analog supplies operating from ±2.5V. The digital interface supports digital logic operating from either 1.8V, 2.5V, or 3.3V.

Figure 6 on page 17 illustrates the device configured to operate from ±2.5V analog. Figure 7 on page 18 illustrates the device configured to operate from 5V analog.

To maximize converter performance, the analog ground and the logic ground for the converter should be connected at the converter. In the dual analog supply configuration, the analog ground for the ±2.5V supplies should be connected to the VLR pin at the converter with the converter placed entirely over the analog ground plane.

In the single analog supply configuration (+5V), the ground for the +5V supply should be directly tied to the VLR pin of the converter with the converter placed entirely over the analog ground plane. Refer to Figure 7 on page 18.

3.12 Using the CS5581 in Multiplexing Applications

The CS5581 is a delta-sigma A/D converter. Delta-sigma converters use oversampling as means to achieve high signal to noise. This means that once a conversion is started, the converter takes many samples to compute the resulting output word. The analog input for the signal to be converted must remain active during the entire conversion until RDY falls.

The CS5581 can be used in multiplexing applications, but the system timing for changing the multiplexer channel and for starting a new conversion will depend upon the multiplexer system architecture.

The simplest system is illustrated in Figure 21. Any time the multiplexer is changed, the analog signal presented to the converter must fully settle. After the signal has settled, the CONV signal is issued to the converter to start a conversion. Being a delta-sigma converter, the signal must remain present at the input of the converter until the conversion is completed. Once the conversion is completed, RDY falls. At this time the multiplexer can be changed to the next channel and the data can be read from the serial port. The CONV signal should be delayed until after the data is read and until the new analog signal has settled. In this configuration, the throughput of the converter will be dictated by the settling time of the analog input circuit and the conversion time of the converter. The conversion data can be read from the serial port after the multiplexer is changed to the new channel while the analog input signal is settling.
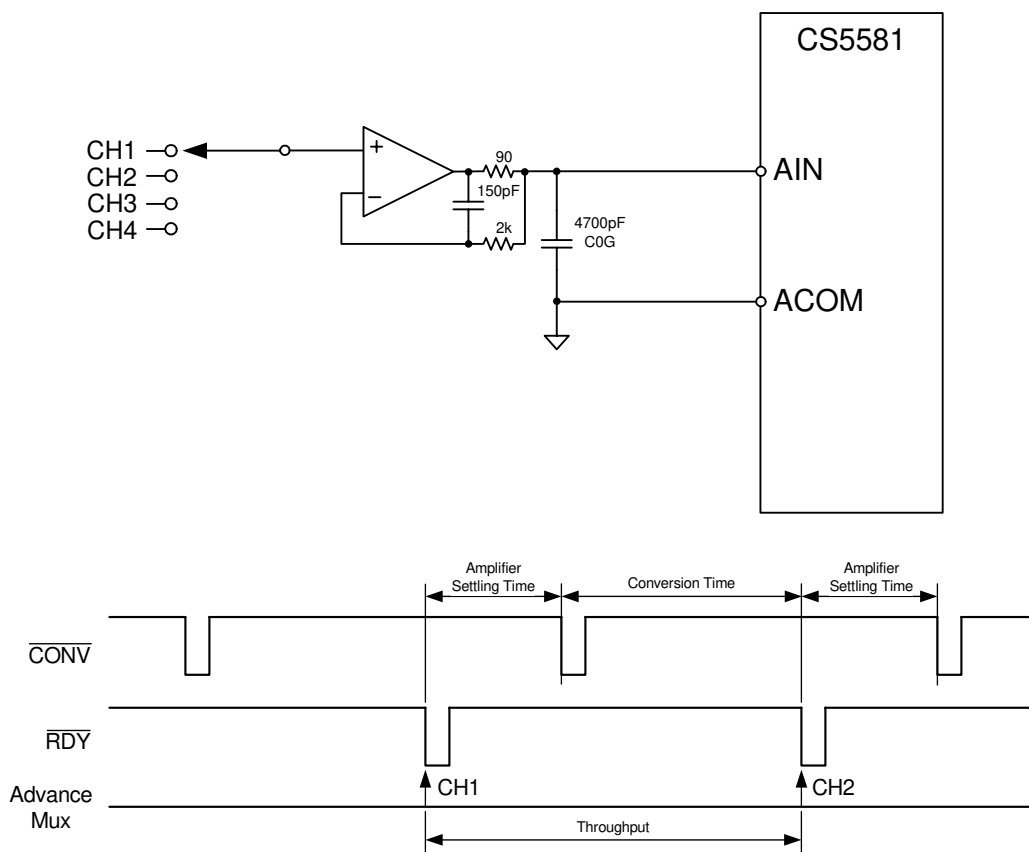
Figure 21. Simple Multiplexing Scheme

A more complex multiplexing scheme can be used to increase the throughput of the converter is illustrated in Figure 22. In this circuit, two banks of multiplexers are used.