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CS61574A
CS61575

T1/E1 Line Interface

Features

- Provides Analog Transmission Line Interface for T1 and E1 Applications
- Provides Line Driver, Jitter Attenuator and Clock Recovery Functions
- Fully Compliant with AT&T 62411 Stratum 4 Jitter Requirements
- Low Power Consumption (typically 175 mW)
- B8ZS/HDB3/AMI Encoder/Decoder
- 14 dB of Transmitter Return Loss

General Description

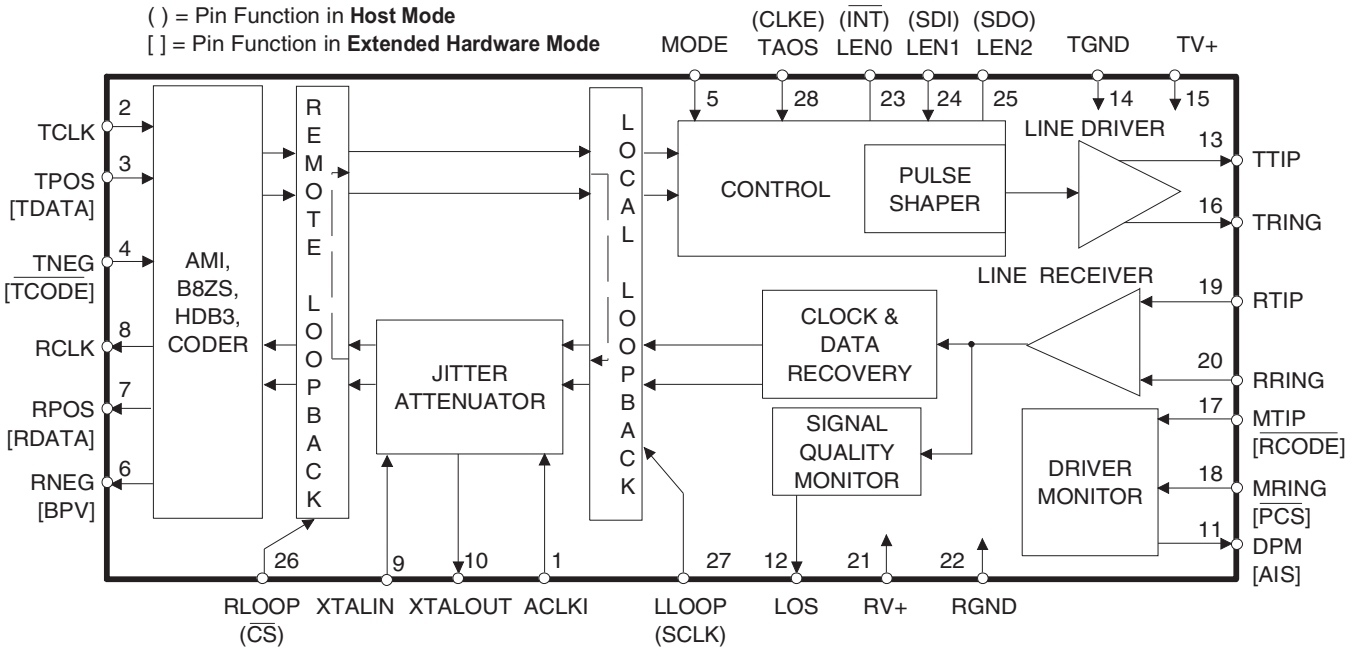
The CS61574A and CS61575 combine the complete analog transmit and receive line interface for T1 or E1 applications in a low power, 28-pin device operating from a +5V supply. Both devices support processor-based or stand-alone operation and interface with industry standard T1 and E1 framers.

The receiver uses a digital Delay-Locked-Loop which is continuously calibrated from a crystal reference to provide excellent stability and jitter tolerance. The CS61574A has a receiver jitter attenuator optimized for minimum delay in switching and transmission applications, while the CS61575 attenuator is optimized for CPE applications subject to AT&T 62411 requirements. The transmitter features internal pulse shaping and a matched, constant impedance output stage to insure signal quality on mismatched, poorly terminated lines.

Applications

- Interfacing Network Equipment such as DACS and Channel Banks to a DSX-1 Cross Connect
- Interfacing Customer Premises Equipment to a CSU
- Building Channel Service Units

ORDERING INFORMATION - See page 26.



ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Supply (referenced to RGND, TGND=0V)		RV+ TV+	- -	6.0 (RV+) + 0.3	V V
Input Voltage, Any Pin	(Note 1)	V_{in}	RGND-0.3	(RV+) + 0.3	V
Input Current, Any Pin	(Note 2)	I_{in}	-10	10	mA
Ambient Operating Temperature		T_A	-40	85	°C
Storage Temperature		T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:
1. Excluding RTIP, RRING, which must stay within -6V to (RV+) + 0.3V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. Also TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Units
DC Supply	(Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature		T_A	-40	25	85	°C
Power Consumption	(Notes 4,5)	P_C	-	290	350	mW
Power Consumption	(Notes 4,6)	P_C	-	175	-	mW

Notes:
3. TV+ must not exceed RV+ by more than 0.3V.
4. Power consumption while driving line load over operating temperature range. Includes IC and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
5. Assumes 100% ones density and maximum line length at 5.25V.
6. Assumes 50% ones density and 300ft. line length at 5.0V.

DIGITAL CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage PINS 1-4, 17, 18, 23-28	(Notes 7, 8)	V_{IH}	2.0	-	-	V
Low-Level Input Voltage PINS 1-4, 17, 18, 23-28	(Notes 7, 8)	V_{IL}	-	-	0.8	V
High-Level Output Voltage I_{OUT} = -40 µA PINS 6-8, 11, 12, 25	(Notes 7, 8, 9)	V_{OH}	4.0	-	-	V
Low-Level Output Voltage I_{OUT} = 1.6 mA PINS 6-8, 11, 12, 23, 25	(Notes 7, 8, 9)	V_{OL}	-	-	0.4	V
Input Leakage Current (Except Pin 5)			-	-	±10	µA
Low-Level Input Voltage, PIN 5		V_{IL}	-	-	0.2	V
High-Level Input Voltage, PIN 5		V_{IH}	(RV+) - 0.2	-	-	V
Mid-Level Input Voltage, PIN 5	(Note 10)	V_{IM}	2.3	-	2.7	V

Notes:
7. In Extended Hardware Mode, pins 17 and 18 are digital inputs. In Host Mode, pin 23 is an open drain output and pin 25 is a tristate output.
8. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ I_{OUT} = -40µA).
9. Output drivers will drive CMOS logic levels into a CMOS load.
10. As an alternative to supplying a 2.3-to-2.7V input, this pin may be left floating.

ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter		Min	Typ	Max	Units
Transmitter					
AMI Output Pulse Amplitudes	(Note 11)				
E1, 75 Ω	(Note 12)	2.14	2.37	2.6	V
E1, 120 Ω	(Note 13)	2.7	3.0	3.3	V
T1, FCC Part 68	(Note 14)	2.7	3.0	3.3	V
T1, DSX-1	(Note 15)	2.4	3.0	3.6	V
E1 Zero (space) level (LEN2/1/0 = 0/0/0)					
1:1 transformer and 75Ω load		-0.237	-	0.237	V
1:1.26 transformer and 120Ω load		-0.3	-	0.3	V
Recommended Output Load at TTIP and TRING		-	75	-	Ω
Jitter Added During Remote Loopback	(Note 16)				
10Hz - 8kHz		-	0.005	0.02	UI
8kHz - 40kHz		-	0.008	0.025	UI
10Hz - 40kHz		-	0.010	0.025	UI
Broad Band		-	0.015	0.05	UI
Power in 2kHz band about 772kHz	(Notes 11, 17)	12.6	15	17.9	dBm
Power in 2kHz band about 1.544MHz (referenced to power in 2kHz band at 772kHz)	(Notes 11, 17)	-29	-38	-	dB
Positive to Negative Pulse Imbalance	(Notes 11, 17)				
T1, DSX-1		-	0.2	0.5	dB
E1 amplitude at center of pulse		-5	-	5	%
E1 pulse width at 50% of nominal amplitude		-5	-	5	%
Transmitter Return Loss	(Notes 11, 17, 18)				
51 kHz to 102 kHz		8	-	-	dB
102 kHz to 2.048 MHz		14	-	-	dB
2.048 MHz to 3.072 MHz		10	-	-	dB
Transmitter Short Circuit Current	(Notes 11, 19)	-	-	50	mA RMS
Driver Performance Monitor					
MTIP/MRING Sensitivity: Differential Voltage Required for Detection		-	0.6	-	V

Notes:
11. Using a 0.47 µF capacitor in series with the primary of a transformer recommended in the Applications section.
12. Pulse amplitude measured at the output of a 1:1 or 1:1.26 transformer across a 75 Ω load for line length setting LEN2/1/0 = 0/0/0.
13. Pulse amplitude measured at the output of a 1:1.26 transformer across a 120 Ω load for line length setting LEN2/1/0 = 0/0/0.
14. Pulse amplitude measured at the output of a 1:1.15 transformer across a 100 Ω load for line length setting LEN2/1/0 = 0/1/0.
15. Pulse amplitude measured at the DSX-1 cross-connect across a 100 Ω load for line length settings LEN2/1/0 = 0/1/1, 1/0/0, 1/0/1, 1/1/0, or 1/1/1 using a 1:1.15 transformer and the length of #22 AWG, ABAM, or equivalent cable specified in Table 3.
16. Input signal to RTIP/RRING is jitter free. Values will reduce slightly if jitter free clock is input to TCLK.
17. Not production tested. Parameters guaranteed by design and characterization.
18. Return loss = 20 $\log_{10}$ ABS($(z_1 + z_0)/(z_1 - z_0)$) where z_1 = impedance of the transmitter, and z_0 = impedance of line load. Measured with a repeating 1010 data pattern with LEN2/1/0 = 0/0/0 and a 1:1 transformer terminated with a 75Ω load, or a 1:1.26 transformer terminated with a 120Ω load.
19. Measured broadband through a 0.5 Ω resistor across the secondary of a 1:1.26 transformer during the transmission of an all ones data pattern for LEN2/1/0 = 0/0/0.

ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter		Min	Typ	Max	Units
Receiver					
RTIP/RRING Input Impedance		-	50k	-	Ω
Sensitivity Below DSX (0dB = 2.4V)		-13.6 500	- -	- -	dB mV
Data Decision Threshold					
T1, DSX-1	(Note 20)	60	65	70	% of peak
T1, DSX-1	(Note 21)	53	65	77	% of peak
T1, FCC Part 68 and E1	(Note 22)	45	50	55	% of peak
Allowable Consecutive Zeros before LOS		160	175	190	bits
Receiver Input Jitter Tolerance	(Note 23)				
10kHz - 100kHz		0.4	-	-	UI
2kHz		6.0	-	-	UI
10Hz and below		300	-	-	UI
Loss of Signal Threshold	(Note 24)	0.25	0.30	0.50	V

Notes: 20. For input amplitude of 1.2 V_{pk} to 4.14 V_{pk}.
21. For input amplitude of 0.5 V_{pk} to 1.2 V_{pk} and from 4.14 V_{pk} to RV+.
22. For input amplitude of 1.05 V_{pk} to 3.3 V_{pk}.
23. Jitter tolerance increases at lower frequencies. See Figure 11.
24. The analog input squelch circuit shall operate when the input signal amplitude above ground on the RTIP and RRING pins falls within the range of 0.25V to 0.50V. Operation of the squelch results in the recovery of zeros. During receive LOS, the RPOS, RNEG or RDATA outputs are forced low.

ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter		Min	Typ	Max	Units
Jitter Attenuator					
Jitter Attenuation Curve Corner Frequency	(Notes 17, 25)				
CS61574A		-	6	-	Hz
CS61575		-	3	-	Hz
CS61574A T1 Receiver Jitter Transfer	(Notes 25, 26)				
Jitter Freq. [Hz]	Amplitude [UIpp]				
10	10	3.0	6.0	-	dB
100	10	20	30	-	dB
500	10	35	40	-	dB
1k	5	40	50	-	dB
10k, 40k	0.3	40	50	-	dB
CS61575 T1 Receiver Jitter Transfer	(Notes 25, 26)				
Jitter Freq. [Hz]	Amplitude [UIpp]				
10	10	6.0	9.0	-	dB
100	10	23	33	-	dB
500	10	38	43	-	dB
1k	5	40	50	-	dB
10k, 40k	0.3	40	50	-	dB
CS61574A E1 Receiver Jitter Transfer	(Notes 26, 27, 28)				
Jitter Freq. [Hz]	Amplitude [UIpp]				
10	1.5	3.0	6.0	-	dB
20	1.5	6.0	12	-	dB
100	1.5	20	32	-	dB
400	1.5	30	40	-	dB
1k	1.5	35	45	-	dB
10k, 100k	0.2	35	45	-	dB
CS61575 E1 Receiver Jitter Transfer	(Notes 26, 27, 28)				
Jitter Freq. [Hz]	Amplitude [UIpp]				
10	1.5	6.0	12	-	dB
20	1.5	12	18	-	dB
100	1.5	22	29	-	dB
400	1.5	30	39	-	dB
1k	1.5	35	45	-	dB
10k, 100k	0.2	35	45	-	dB
Attenuator Input Jitter Tolerance (Before Onset of FIFO Overflow or Underflow Protection)	(Notes 17, 28)				
CS61574A		12	23	-	UI
CS61575		138	-	-	UI

Notes: 25. Attenuation measured at the demodulator output of an HP3785B with input jitter equal to 3/4 of measured jitter tolerance using a measurement bandwidth of 1 Hz (10<f<100Hz), 4Hz (100<f<1000 Hz) and 10 Hz (f> 1kHz) centered around the jitter frequency. With a 2^{15}-1 PRBS data pattern.

26. Crystal must meet specifications described in Appendix A.

27. Jitter measured at the demodulator output of an HP3785A (or equivalent) using a measurement bandwidth not to exceed 20 Hz centered around the jitter frequency. With a 2^{15}-1 PRBS data pattern.

28. Jitter below 100 kHz and within the attenuator's input jitter tolerance is not translated or aliased to other frequencies. Output jitter increases significantly when attenuator input jitter tolerance is exceeded.

T1 SWITCHING CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%;

GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+; See Figures 1, 2, & 3)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 26)	f_c	-	6.176000	-	MHz
TCLK Frequency		f_{tclk}	-	1.544	-	MHz
TCLK Pulse Width	(Note 29)	t_{pwh2}	150	-	500	ns
ACLKI Duty Cycle		t_{pwh3}/t_{pw3}	40	-	60	%
ACLKI Frequency	(Note 30)	f_{aclki}	-	1.544	-	MHz
RCLK Duty Cycle	(Note 31)	t_{pwh1}/t_{pw1}	45	50	55	%
Rise Time, All Digital Outputs	(Note 32)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 32)	t_f	-	-	85	ns
TPOS/TNEG (TDATA) to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG (TDATA) Hold Time		t_{h2}	25	-	-	ns
RPOS/RNEG Valid Before RCLK Falling	(Note 33)	t_{su1}	150	274	-	ns
RDATA Valid Before RCLK Falling	(Note 34)	t_{su1}	150	274	-	ns
RPOS/RNEG Valid Before RCLK Rising	(Note 35)	t_{su1}	150	274	-	ns
RPOS/RNEG Valid After RCLK Falling	(Note 33)	t_{h1}	150	274	-	ns
RDATA Valid After RCLK Falling	(Note 34)	t_{h1}	150	274	-	ns
RPOS/RNEG Valid After RCLK Rising	(Note 35)	t_{h1}	150	274	-	ns

Notes: 29. The transmitted pulse width does not depend on the TCLK duty cycle.
30. ACLKI provided by an external source or TCLK.
31. RCLK duty cycle will be 62.5% or 37.5% when jitter attenuator limits are reached.
32. At max load of 1.6 mA and 50 pF.
33. Host Mode (CLKE = 1).
34. Extended Hardware Mode.
35. Hardware Mode, or Host Mode (CLKE = 0).

E1 SWITCHING CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%;

GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+; See Figures 1, 2, & 3)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 26)	f_c	-	8.192000	-	MHz
TCLK Frequency		f_{tclk}	-	2.048	-	MHz
TCLK Pulse Width	(Note 29)	t_{pwh2}	150	-	340	ns
ACLKI Duty Cycle		t_{pwh3}/t_{pw3}	40	-	60	%
ACLKI Frequency	(Note 30)	f_{aclki}	-	2.048	-	MHz
RCLK Duty Cycle	(Note 31)	t_{pwh1}/t_{pw1}	45	50	55	%
Rise Time, All Digital Outputs	(Note 32)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 32)	t_f	-	-	85	ns
TPOS/TNEG (TDATA) to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG (TDATA) Hold Time		t_{h2}	25	-	-	ns
RPOS/RNEG Valid Before RCLK Falling	(Note 33)	t_{su1}	100	194	-	ns
RDATA Valid Before RCLK Falling	(Note 34)	t_{su1}	100	194	-	ns
RPOS/RNEG Valid Before RCLK Rising	(Note 35)	t_{su1}	100	194	-	ns
RPOS/RNEG Valid After RCLK Falling	(Note 33)	t_{h1}	100	194	-	ns
RDATA Valid After RCLK Falling	(Note 34)	t_{h1}	100	194	-	ns
RPOS/RNEG Valid After RCLK Rising	(Note 35)	t_{h1}	100	194	-	ns

SWITCHING CHARACTERISTICS (TA = -40° to 85°C; TV+, RV+ = ±5%;

Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter	Symbol	Min	Typ	Max	Units
SDI to SCLK Setup Time	t_{dc}	50	-	-	ns
SCLK to SDI Hold Time	t_{cdh}	50	-	-	ns
SCLK Low Time	t_{cl}	240	-	-	ns
SCLK High Time	t_{ch}	240	-	-	ns
SCLK Rise and Fall Time	t_r, t_f	-	-	50	ns
CS to SCLK Setup Time	t_{cc}	50	-	-	ns
SCLK to CS Hold Time	t_{cch}	50	-	-	ns
CS Inactive Time	t_{cwh}	250	-	-	ns
SCLK to SDO Valid (Note 36)	t_{cdv}	-	-	200	ns
CS to SDO High Z	t_{cdz}	-	100	-	ns
Input Valid To PCS Falling Setup Time	t_{su4}	50	-	-	ns
PCS Rising to Input Invalid Hold Time	t_{h4}	50	-	-	ns
PCS Active Low Time	t_{pcsl}	250	-	-	ns

Notes: 36. Output load capacitance = 50pF.

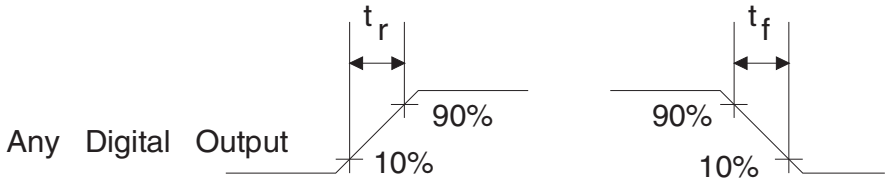


Figure 1. Signal Rise and Fall Characteristics

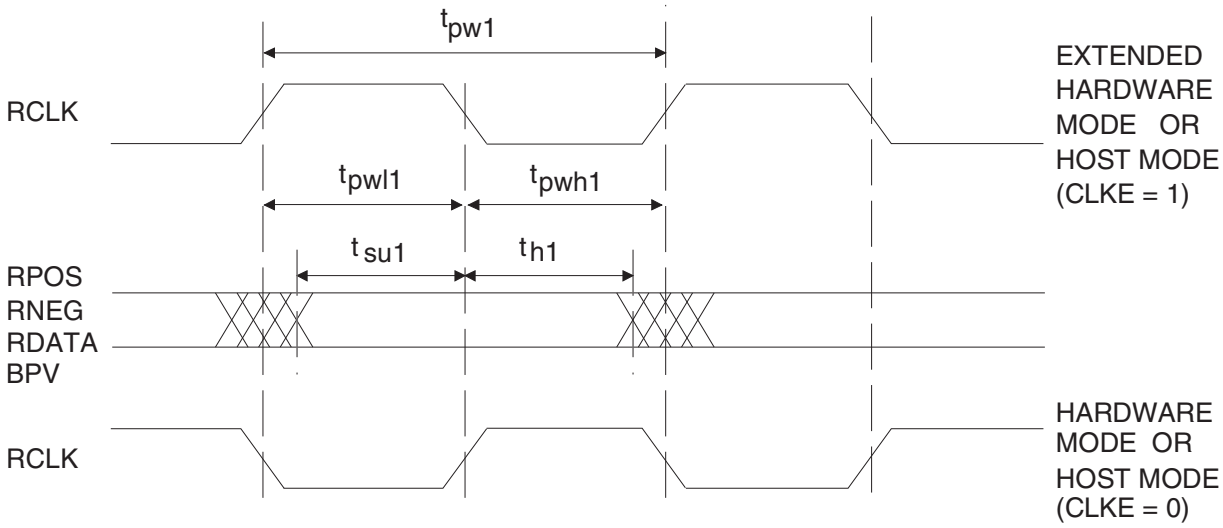


Figure 2. Recovered Clock and Data Switching Characteristics

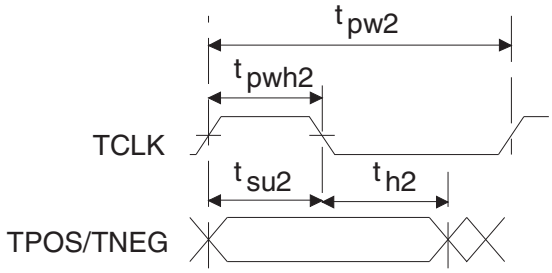


Figure 3a. Transmit Clock and Data Switching Characteristics

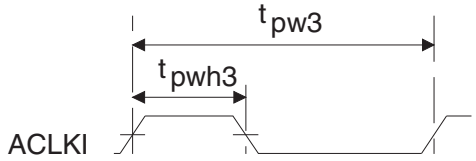


Figure 3b. Alternate External Clock Characteristics

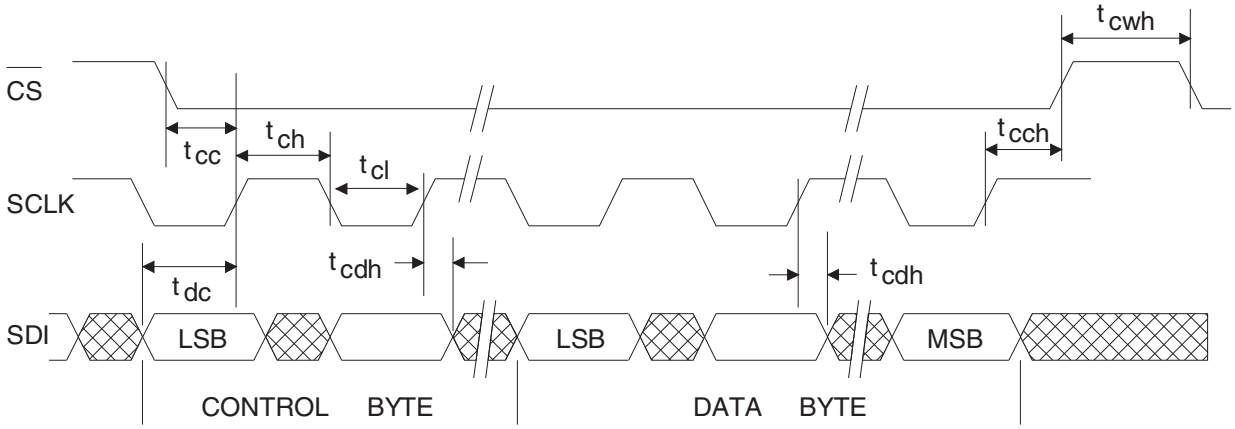


Figure 4. Serial Port Write Timing Diagram

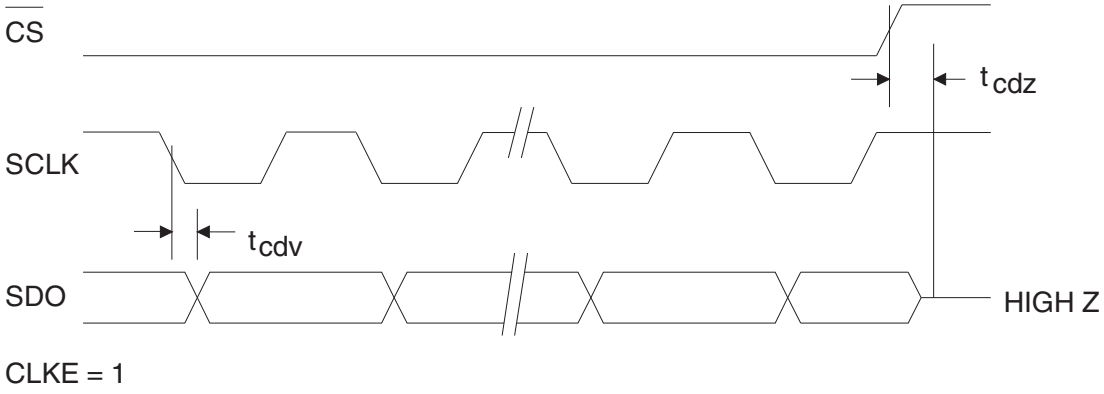


Figure 5. Serial Port Read Timing Diagram

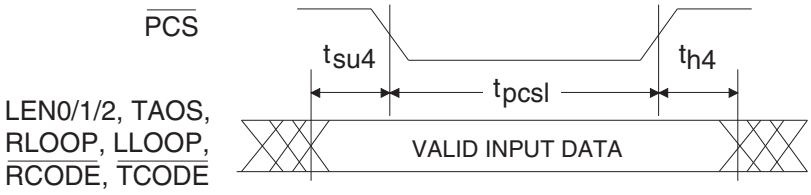


Figure 6. Extended Hardware Mode Parallel Chip Select Timing Diagram

THEORY OF OPERATION

Enhancements in CS61575 and CS61574A

The CS61574A and CS61575 provide higher performance and more features than the CS61574 including:

- AT&T 62411, Stratum 4 compliant jitter attenuation over the full range of operating frequency and jitter amplitude (CS61575),
- 50% lower power consumption,
- Internally matched transmitter output impedance for improved signal quality,
- Optional AMI, B8ZS, HDB3 encoder/decoder or external line coding support,
- Receiver AIS (unframed all ones) detection,
- ANSI T1.231-1993 compliant receiver LOS (Loss of Signal) handling,
- Transmitter TTIP and TRING outputs are forced low when TCLK is static,
- The Driver Performance Monitor operates over a wider range of input signal levels.

Existing designs using the CS61574 can be converted to the higher performance, pin-compatible CS61574A or CS61575 if the transmit transformer is replaced by a pin-compatible transformer with a new turns ratio.

Understanding the Difference Between the CS61575 and CS61574A

The CS61574A and CS61575 provide receiver jitter attenuation performance optimized for different applications. The CS61575 is optimized to attenuate large amplitude, low frequency jitter for T1 Customer Premises Equipment (CPE) applications as required by AT&T 62411. The CS61574A is optimized to minimize data delay in T1 and E1 switching or transmission applications. Refer to the "Jitter Attenuator" section for additional information.

Introduction to Operating Modes

The CS61574A and CS61575 support three operating modes which are selected by the level of the MODE pin as shown in Tables 1 and 2, Figure 7, and Figures A1-A3 of the Applications section.

The modes are Hardware Mode, Extended Hardware Mode, and Host Mode. In Hardware and Extended Hardware Modes, discrete pins are used to configure and monitor the device. The Extended Hardware Mode provides a parallel chip select input which latches the control inputs allowing individual ICs to be configured using a common set of control lines. In the Host Mode, an external processor monitors and configures the device through a serial interface. There are thirteen multi-function pins whose functionality is determined by the operating mode. (see Table 2).

	Hardware Mode	Extended Hardware Mode	Host Mode
Control Method	Control Pins	Control Pins with Parallel Chip Select	Serial Interface
MODE Pin Level	<0.2 V	Floating or 2.5 V	>(RV+)-0.2 V
Line Coding	External	Internal-AMI, B8ZS, or HDB3	External
AIS Detection	No	Yes	No
Driver Performance Monitor	Yes	No	Yes

Table 1. Differences Between Operating Modes

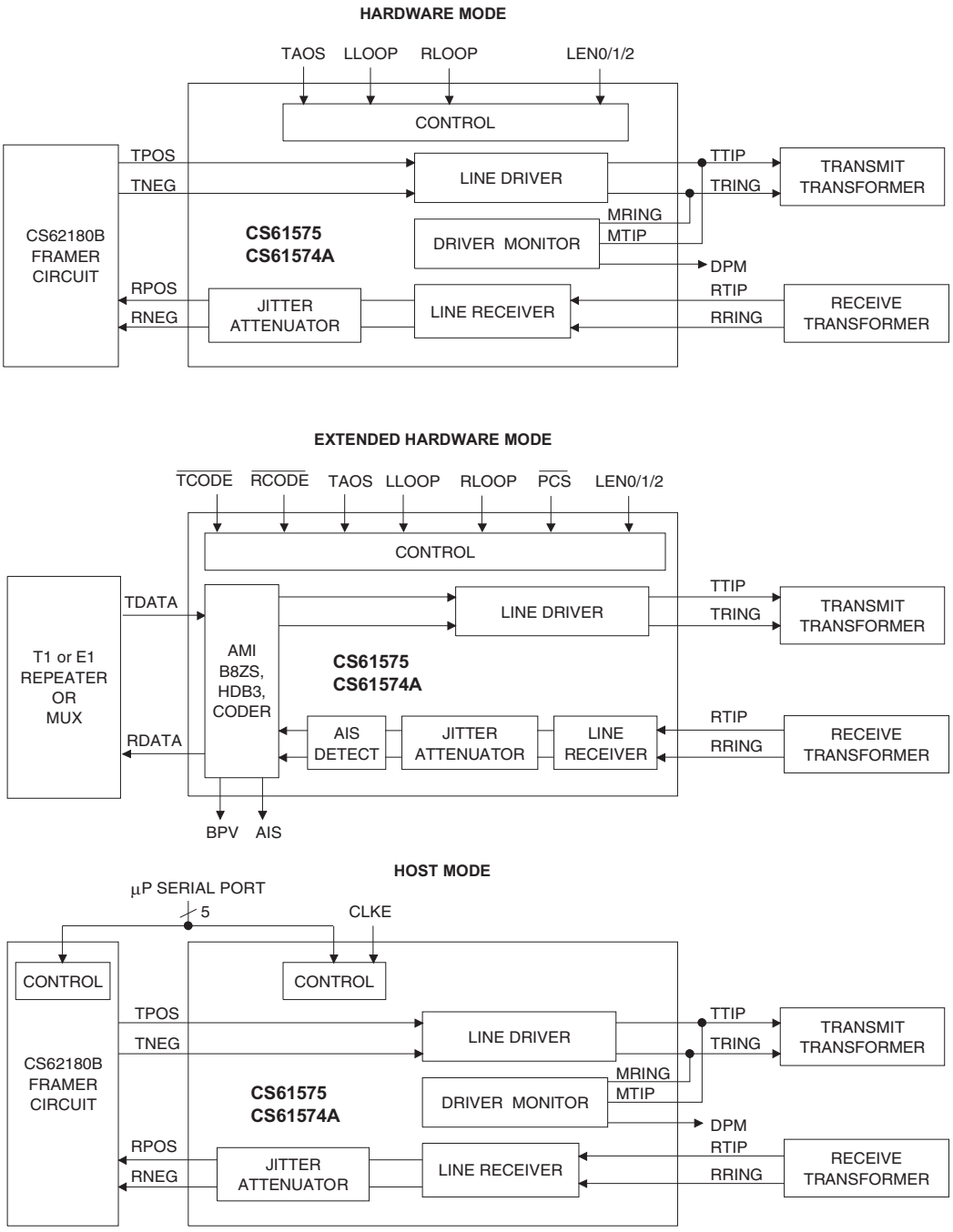


Figure 7. Overview of Operating Modes

FUNCTION	PIN	MODE HARDWARE	MODE EXTENDED HARDWARE	MODE HOST
TRANSMITTER	3	TPOS	TDATA	TPOS
	4	TNEG	$\overline{\text{TCODE}}$	TNEG
RECEIVER/DPM	6	RNEG	BPV	RNEG
	7	RPOS	RDATA	RPOS
	11	DPM	AIS	DPM
	17	MTIP	$\overline{\text{RCODE}}$	MTIP
	18	MRING	-	MRING
CONTROL	18	-	$\overline{\text{PCS}}$	-
	23	LEN0	LEN0	$\overline{\text{INT}}$
	24	LEN1	LEN1	SDI
	25	LEN2	LEN2	SDO
	26	RLOOP	RLOOP	$\overline{\text{CS}}$
	27	LLOOP	LLOOP	SCLK
	28	TAOS	TAOS	CLKE

Table 2. Pin Definitions

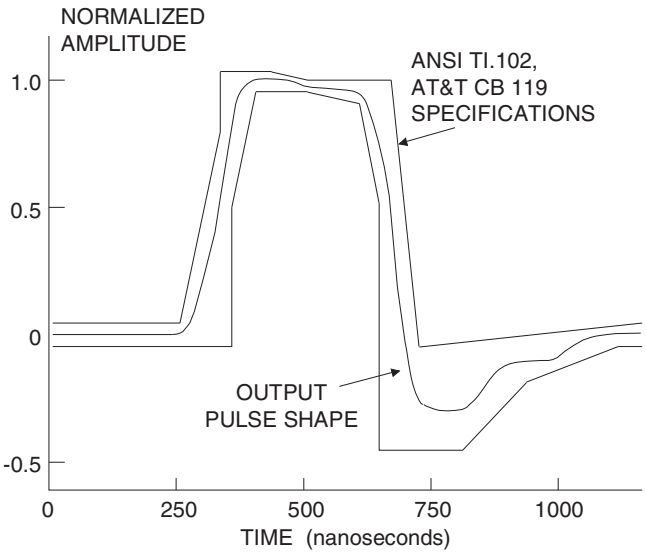


Figure 8. Typical Pulse Shape at DSX-1 Cross Connect

Transmitter

The transmitter takes digital T1 or E1 input data and drives appropriately shaped bipolar pulses onto a transmission line. The transmit data (TPOS & TNEG or TDATA) is supplied synchronously and sampled on the falling edge of the input clock, TCLK.

Either T1 (DSX-1 or Network Interface) or E1 CCITT G.703 pulse shapes may be selected. Pulse shaping and signal level are controlled by "line length select" inputs as shown in Table 3.

LEN2	LEN1	LEN0	Option Selected	Application
0	1	1	0-133 FEET	DSX-1 ABAM (AT&T 600B or 600C)
1	0	0	133-266 FEET	
1	0	1	266-399 FEET	
1	1	0	399-533 FEET	
1	1	1	533-655 FEET	
0	0	0	120Ω (1:1.26) 75Ω (1:1)	E1 CCITT G.703
0	0	1	AT&T CB113	Repeater
0	1	0	FCC PART 68, OPT. A	Network Interface
0	1	1	ANSI 1.403	

Table 3. Line Length Selection

The CS61575 and CS61574A line drivers are designed to drive a 75 Ω equivalent load.

For E1 applications, the CS61574A and CS61575 drivers provide 14 dB of return loss during the transmission of both marks and spaces. This improves signal quality by minimizing reflections off the transmitter. Similar levels of return loss are provided for T1 applications.

For T1 DSX-1 applications, line lengths from 0 to 655 feet (as measured from the transmitter to the DSX-1 cross connect) may be selected. The five partition arrangement in Table 3 meets ANSI T1.102 and AT&T CB-119 requirements when using #22 ABAM cable. A typical output pulse is shown in Figure 8. These pulse settings can also be used to meet CCITT pulse shape requirements for 1.544 MHz operation.

For T1 Network Interface applications, two additional options are provided. Note that the optimal pulse width for Part 68 (324 ns) is narrower than the optimal pulse width for DSX-1 (350 ns). The CS61575 and CS61574A automatically adjusts the pulse width based upon the "line length" selection made.

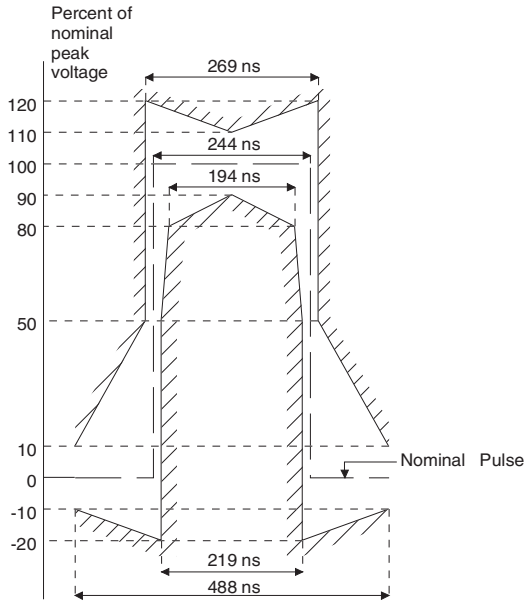


Figure 9. Mask of the Pulse at the 2048 kbps Interface

The E1 G.703 pulse shape is supported with line length selection LEN2/1/0=0/0/0. The pulse width will meet the G.703 pulse shape template shown in Figure 9, and specified in Table 4.

The CS61574A and CS61575 will detect a static TCLK, and will force TTIP and TRING low to prevent transmission when data is not present. When any transmit control pin (TAOS, LEN0-2 or LLOOP) is toggled, the transmitter outputs will require approximately 22 bit periods to stabilize. The transmitter will take longer to stabilize when RLOOP is selected because the timing circuitry must adjust to the new frequency.

Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of TCLK. Transmit all ones is selected when TAOS goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING). In this mode, the TPOS and TNEG (or TDATA) inputs are ignored. If Remote Loopback is in effect, any TAOS request will be ignored.

Receiver

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver is sensitive to signals over the entire range of ABAM cable lengths and requires no equalization or ALBO (Automatic Line Build Out) circuits. The signal is received on both ends of a center-tapped, center-grounded transformer. The transformer is center tapped on the IC side. The clock and data recovery circuit exceeds the jitter tolerance specifications of Publications 43802, 43801, AT&T 62411, TR-TSY-000170, and CCITT REC. G.823.

	For coaxial cable, 75Ω load and transformer specified in Application Section.	For shielded twisted pair, 120Ω load and transformer specified in Application Section.
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ±0.237 V	0 ±0.30 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval	0.95 to 1.05*	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05*	

* When configured with a 0.47 µF nonpolarized capacitor in series with the TX transformer primary as shown in Figures A1, A2 and A3.

Table 4. CCITT G.703 Specifications

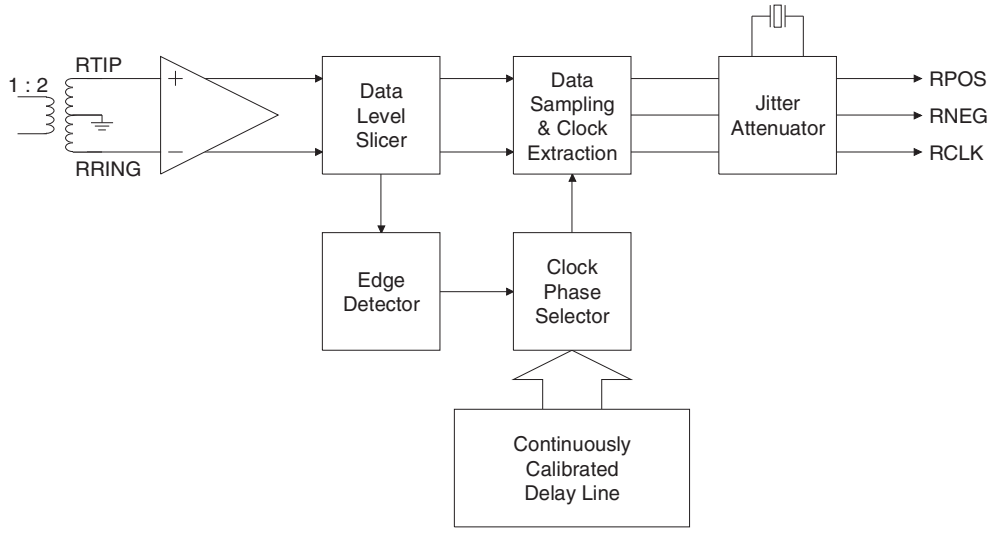


Figure 10. Receiver Block Diagram

A block diagram of the receiver is shown in Figure 10. The two leads of the transformer (RTIP and RRING) have opposite polarity allowing the receiver to treat RTIP and RRING as unipolar signals. Comparators are used to detect pulses on RTIP and RRING. The comparator thresholds are dynamically established at a percent of the peak level (50% of peak for E1, 65% of peak for T1; with the slicing level selected by LEN2/1/0 inputs).

The leading edge of an incoming data pulse triggers the clock phase selector. The phase selector chooses one of the 13 available phases which the delay line produces for each bit period. The output from the phase selector feeds the clock and data recovery circuits which generate the recovered clock and sample the incoming signal at appropriate intervals to recover the data.

Data sampling will continue at the periods selected by the phase selector until an incoming pulse deviates enough to cause a new phase to be selected for data sampling. The phases of the delay line are selected and updated to allow as much as 0.4 UI of jitter from 10 kHz to 100 kHz, without error. The jitter tolerance of the receiver exceeds that shown in Figure 11. Additionally, this method of clock and data recovery is tolerant of long strings of consecutive zeros. The data sampler will continuously sample data based on its last input until a new pulse arrives to update the clock phase selector.

The delay line is continuously calibrated using the crystal oscillator reference clock. The delay line produces 13 phases for each cycle of the reference clock. In effect, the 13 phases are analogous to a 20 MHz clock when the reference clock is 1.544 MHz. This implementation utilizes the benefits of a 20 MHz clock for clock recovery without actually having the clock present to impede analog circuit performance.

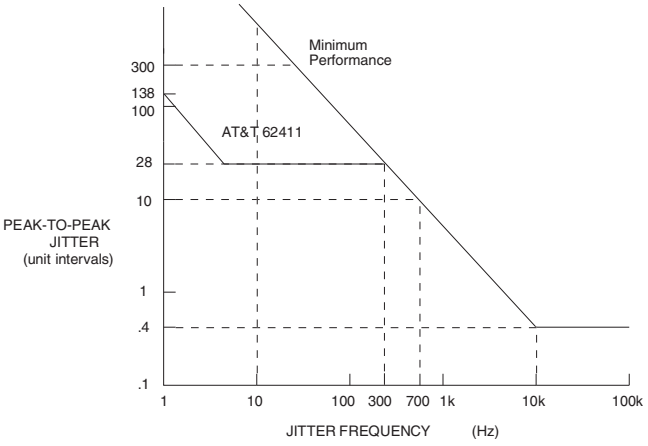


Figure 11. Minimum Input Jitter Tolerance of Receiver

In the Hardware Mode, data at RPOS and RNEG should be sampled on the rising edge of RCLK, the recovered clock. In the Extended Hardware Mode, data at RDATA should be sampled on the falling edge of RCLK. In the Host Mode, CLKE determines the clock polarity for which output data should be sampled as shown in Table 5.

MODE (pin 5)	CLKE (pin 28)	DATA	CLOCK	Clock Edge for Valid Data
LOW (<0.2V)	X	RPOS RNEG	RCLK RCLK	Rising Rising
HIGH (>(V+) - 0.2V)	LOW	RPOS RNEG SDO	RCLK RCLK SCLK	Rising Rising Falling
HIGH (>(V+) - 0.2V)	HIGH	RPOS RNEG SDO	RCLK RCLK SCLK	Falling Falling Rising
MIDDLE (2.5V)	X	RDATA	RCLK	Falling

X = Don't care

Table 5. Data Output/Clock Relationship

Loss of Signal

The receiver will indicate loss of signal after power-up, reset or upon receiving 175 consecutive zeros. A digital counter counts received zeros, based on RCLK cycles. A zero is received when the RTIP and RRING inputs are below the input comparator slicing threshold level established by the peak detector. After the signal is removed for a period of time the data slicing threshold level decays to approximately 300 mV_{peak}.

If ACLKI is present during the LOS state, ACLKI is switched into the input of the jitter attenuator, resulting in RCLK matching the frequency of ACLKI. The jitter attenuator buffers any instantaneous changes in phase between the last recovered clock and the ACLKI reference clock. This means that RCLK will smoothly transition to the new frequency. If ACLKI is not present, then the crystal oscillator of the jitter attenuator is forced to its center frequency. Table 6 shows the status of RCLK upon LOS.

Crystal present?	ACLKI present?	Source of RCLK
No	Yes	ACLKI
Yes	No	Centered Crystal
Yes	Yes	ACLKI via the Jitter Attenuator

Table 6. RCLK Status at LOS

Jitter Attenuator

The jitter attenuator reduces wander and jitter in the recovered clock signal. It consists of a 32 or 192-bit FIFO, a crystal oscillator, a set of load capacitors for the crystal, and control logic. The jitter attenuator exceeds the jitter attenuation requirements of Publications 43802 and REC. G.742. A typical jitter attenuation curve is shown in Figure 12. The CS61575 fully meets AT&T 62411 jitter attenuation requirements. The CS61574A will have a discontinuity in the jitter transfer function when the incoming jitter amplitude exceeds approximately 23 UIs.

The jitter attenuator works in the following manner. The recovered clock and data are input to the FIFO with the recovered clock controlling the FIFO's write pointer. The crystal oscillator controls the FIFO's read pointer which reads data out of the FIFO and presents it at RPOS and RNEG (or RDATA). RCLK is equivalent to the oscillator's output. By changing the load capacitance that the IC presents to the crystal, the oscillatior frequency (and RCLK) is adjusted to the average frequency of the recovered signal. Logic determines the phase relationship between the read and write pointers and decides how to adjust the load capacitance of the crystal. Jitter is absorbed in the FIFO according to the jitter transfer characteristic shown in Figure 12.

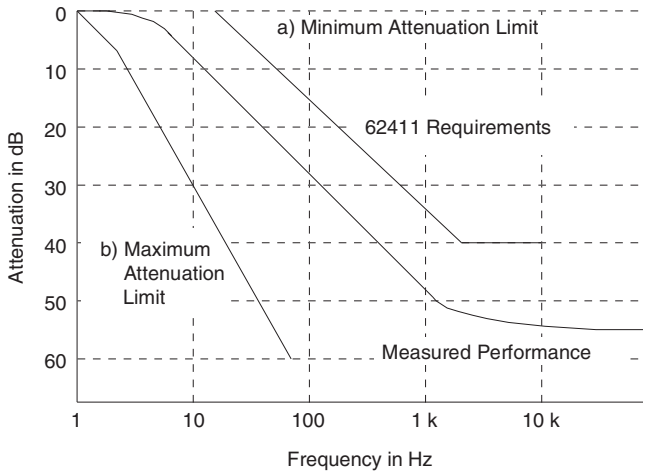


Figure 12. Typical Jitter Transfer Function

The FIFO in the jitter attenuator is designed to prevent overflow and underflow. If the jitter amplitude becomes very large, the read and write pointers may get very close together. Should they attempt to cross, the oscillator's divide by four circuit adjusts by performing a divide by 3 1/2 or divide by 4 1/2 to prevent the overflow or underflow. During this activity, data will never be lost.

The difference between the CS61575 and CS61574A is the depth of the FIFO in the jitter attenuator. The CS61575 has a 192-bit FIFO which allows it to attenuate large amplitude, low frequency jitter as required by AT&T 62411 (e.g., 28 UIpp @ 300 Hz). This makes the CS61575 ideal for use in T1 Customer Premises Equipment which must be compatible with AT&T 62411 requirements. In single-line Stratum 4, Type II systems which are loop-timed, he CS61575 recovered clock can be used as the transmit clock eliminating the need for an external system clock synchronizer. In Stratum 4, Type I systems which transfer timing and require a clock synchronizer, the CS61575 simplifies the design of the synchronizer by absorbing large amplitude low frequency jitter before it reaches the synchronizer.

The CS61574A has a 32-bit FIFO which allows it to absorb jitter with minimum data delay in T1 and E1 switching or transmission applications. The CS61574A will tolerate large amplitude jitter by tracking rather than attenuating it, preventing data errors so that the jitter may be absorbed in external frame buffers. With large amplitude input jitter, the CS61574A jitter transfer function may exhibit some jitter peaking, but will offer performance comparable to the CS61574.

The jitter attenuator may be bypassed by pulling XTALIN to RV+ through a 1 kΩ resistor and providing a 1.544 MHz (or 2.048 MHz) clock on ACLKI. RCLK may exhibit quantization jitter of approximately 1/13 UIpp and a duty cycle of approximately 30% (70%) when the attenuator is disabled.

Local Loopback

Local loopback is selected by taking LLOOP, pin 27, high or by setting the LLOOP register bit via the serial interface.

The local loopback mode takes clock and data presented on TCLK, TPOS, and TNEG (or TDATA), sends it through the jitter attenuator and outputs it at RCLK, RPOS and RNEG (or RDATA). If the jitter attenuator is disabled, it is bypassed. Inputs to the transmitter are still transmitted on TTIP and TRING, unless TAOS has been selected in which case, AMI-coded continuous ones are transmitted at the TCLK frequency. The receiver RTIP and RRING inputs are ignored when local loopback is in effect.

Remote Loopback

Remote loopback is selected by taking RLOOP, pin 26, high or by setting the RLOOP register bit via the serial interface.

In remote loopback, the recovered clock and data input on RTIP and RRING are sent through the jitter attenuator and back out on the line via TTIP and TRING. Selecting remote loopback overrides any TAOS request (see Table 7). The recovered incoming signals are also sent to RCLK, RPOS and RNEG (or RDATA). Simultaneous selection of local and remote loopback modes is not valid (see Reset).

RLOOP Input Signal	TAOS Input Signal	Source of Data for TTIP & TRING	Source of Clock for TTIP & TRING
0	0	TDATA	TCLK
0	1	all 1s	TCLK
1	X	RTIP & RRING	RTIP & RRING (RCLK)

Notes: 1. X = Don't care. The identified All Ones Select input is ignored when the indicated loopback is in effect.
2. Logic 1 indicates that Loopback or All Ones option is selected.

Table 7. Interaction of RLOOP with TAOS

In the Extended Hardware Mode the transmitted data is looped before the AMI/B8ZS/HDB3 encoder/decoder during remote loopback so that the transmitted signal matches the received signal, even in the presence of received bipolar violations. Data output on RDATA is decoded, however, if $\overline{\text{RCODE}}$ is low.

Driver Performance Monitor

To aid in early detection and easy isolation of non-functioning links, the IC is able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring driver. The driver performance monitor indicator is normally low, and goes high upon detecting a driver failure.

The driver performance monitor consists of an activity detector that monitors the transmitted signal when MTIP is connected to TTIP and MRING is connected to TRING. DPM will go high if the absolute difference between MTIP and MRING does not transition above or below a threshold level within a time-out period. In the Host Mode, DPM is available from both the register and pin 11.

Whenever more than one line interface IC resides on the same circuit board, the effectiveness of the driver performance monitor can be maximized by having each IC monitor performance of a neighboring IC, rather than having it monitor its own performance. Note that a CS61574A or CS61575 can not be used to monitor a CS61574 due to output stage differences.

Line Code Encoder/Decoder

In the Extended Hardware Mode, three line codes are available: AMI, B8ZS and HDB3. The input to the encoder is TDATA. The outputs from the decoder are RDATA and BPV (Bipolar Violation Strobe). The encoder and decoder are selected using the LEN2, LEN1, LEN0, $\overline{\text{TCODE}}$ and $\overline{\text{RCODE}}$ pins as shown in Table 8.

		LEN 2/1/0	
		000	010-111
TCODE (Transmit Encoder Selection)	LOW	HDB3 Encoder	B8ZS Encoder
	HIGH	AMI Encoder	
RCODE (Receiver Decoder Selection)	LOW	HDB3 Decoder	B8ZS Decoder
	HIGH	AMI Decoder	

Table 8. Encoder/Decoder Selection

Alarm Indication Signal

In the Extended Hardware Mode, the receiver sets the output pin AIS high when less than 9 zeros are detected out of 8192 bit periods. AIS returns low when 9 or more zeros are detected out of 8192 bit periods.

Parallel Chip Select

In the Extended Hardware Mode, $\overline{\text{PCS}}$ can be used to gate the digital control inputs: $\overline{\text{TCODE}}$, $\overline{\text{RCODE}}$, LEN0, LEN1, LEN2, RLOOP, LLOOP and TAOS. Inputs are accepted on these pins only when $\overline{\text{PCS}}$ is low and will immediately change the operating state of the device. Therefore, when cycling $\overline{\text{PCS}}$ to update the operating state, the digital control inputs should be stable for the entire $\overline{\text{PCS}}$ low period. The digital control inputs are ignored when $\overline{\text{PCS}}$ is high.

Power On Reset / Reset

Upon power-up, the IC is held in a static state until the supply crosses a threshold of approximately 3 Volts. When this threshold is crossed, the device will delay for about 10 ms to allow the power supply to reach operating voltage. After this delay, calibration of the delay lines used in the transmit and receive sections commences. The delay lines can be calibrated only if a reference clock is present. The reference clock for the receiver is provided by the crystal oscillator, or ACLKI if the oscillator is disabled. The reference clock for the transmitter is provided by TCLK. The initial calibration should take less than 20 ms.

In operation, the delay lines are continuously calibrated, making the performance of the device independent of power supply or temperature variations. The continuous calibration function forgoes any requirement to reset the line interface when in operation. However, a reset function is available which will clear all registers.

In the Hardware and Extended Hardware Modes, a reset request is made by simultaneously setting both the RLOOP and LLOOP pins high for at least 200 ns. Reset will initiate on the falling edge of the reset request (falling edge of RLOOP and LLOOP). In the Host Mode, a reset is initiated by simultaneously writing RLOOP and LLOOP to the register. In either mode, a reset will set all registers to 0 and force the oscillator to its center frequency before initiating calibration. A reset will also set LOS high.

Serial Interface

In the Host Mode, pins 23 through 28 serve as a microprocessor/microcontroller interface. One on-board register can be written to via the SDI pin or read from via the SDO pin at the clock rate determined by SCLK. Through this register, a host controller can be used to control operational characteristics and monitor device status. The serial port read/write timing is independent of the system transmit and receive timing.

Data transfers are initiated by taking the chip select input, $\overline{\text{CS}}$, low ($\overline{\text{CS}}$ must initially be high). Address and input data bits are clocked in on the rising edge of SCLK. The clock edge on which output data is stable and valid is determined by CLKE as shown in Table 5. Data transfers are terminated by setting $\overline{\text{CS}}$ high. $\overline{\text{CS}}$ may go high no sooner than 50 ns after the rising edge of the SCLK cycle corresponding to the last write bit. For a serial data read, $\overline{\text{CS}}$ may go high any time to terminate the output.

Figure 13 shows the timing relationships for data transfers when CLKE = 1. When CLKE = 1, data bit D7 is held until the falling edge of the 16th clock cycle. When CLKE = 0, data bit D7 is held until the rising edge of the 17th clock cycle. SDO goes High-Z after $\overline{\text{CS}}$ goes high *or* at the end of the hold period of data bit D7.

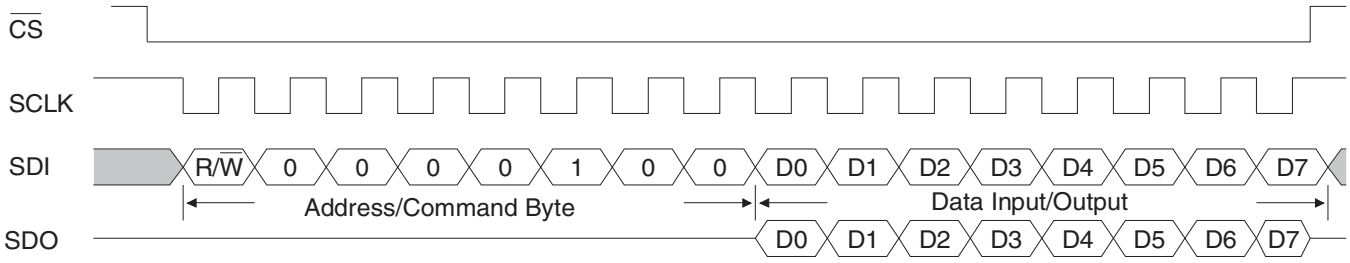


Figure 13. Input/Output Timing

An address/command byte, shown in Table 9, precedes a data register. The first bit of the address/command byte determines whether a read or a write is requested. The next six bits contain the address. The line interface responds to address 16 (0010000). The last bit is ignored.

LSB, first bit	0	R/$\overline{W}$	Read/Write Select; 0 = write, 1 = read
	1	ADDP	LSB of address, Must be 0
	2	ADD1	Must be 0
	3	ADD2	Must be 0
	4	ADD3	Must be 0
	5	ADD4	Must be 1
	6	-	Reserved - Must be 0
MSB, last bit	7	X	Don't Care

Table 9. Address/Command Byte

The data register, shown in Table 10, can be written to the serial port. Data is input on the eight clock cycles immediately following the address/command byte. Bits 0 and 1 are used to clear an interrupt issued from the $\overline{INT}$ pin, which occurs in response to a loss of signal or a problem with the output driver.

LSB, first bit in	0	clr LOS	Clear Loss Of Signal
	1	clr DPM	Clear Driver Performance
	2	LEN0	Bit 0 - Line Length Select
	3	LEN1	Bit 1 - Line Length Select
	4	LEN2	Bit 2 - Line Length Select
	5	RLOOP	Remote Loopback
	6	LLOOP	Local Loopback
MSB, last bit in	7	TAOS	Transmit All Ones Select

Table 10. Input Data Register

Writing a "1" to either "Clear LOS" or "Clear DPM" over the serial interface has three effects:

1) The current interrupt on the serial interface will be cleared. (Note that simply reading the register bits will not clear the interrupt).
2) Output data bits 5, 6 and 7 will be reset as appropriate.
3) Future interrupts for the corresponding LOS or DPM will be prevented from occurring.

Writing a "0" to either "Clear LOS" or "Clear DPM" enables the corresponding interrupt for LOS or DPM.

Output data from the serial interface is presented as shown in Tables 11 and 12. Bits 2, 3 and 4 can be read to verify line length selection. Bits 5, 6 and 7 must be decoded. Codes 101, 110 and 111 (Bits 5, 6 and 7) indicate intermittent loss of signal and/or driver problems.

SDO goes to a high impedance state when not in use. SDO and SDI may be tied together in applications where the host processor has a bi-directional I/O port.

LSB, first bit in	0	LOS	Loss Of Signal
	1	DPM	Driver Performance
	2	LEN0	Bit 0 - Line Length Select
	3	LEN1	Bit 1 - Line Length Select
	4	LEN2	Bit 2 - Line Length Select

Table 11. Output Data Bits 0 - 4

Bits			Status
5	6	7	
0	0	0	Reset has occurred or no program input.
0	0	1	TAOS n effect.
0	1	0	LLOOP in effect
0	1	1	TAOS/LLOOP in effect.
1	0	0	RLOOP in effect.
1	0	1	DPM changed state since last "clear DPM" occurred.
1	1	0	LOS changed state since last "clear LOS" occurred.
1	1	1	LOS and DPM have changed state since last "clear LOS" and "clear DPM".

Table 12. Coding for Serial Output bits 5,6,7

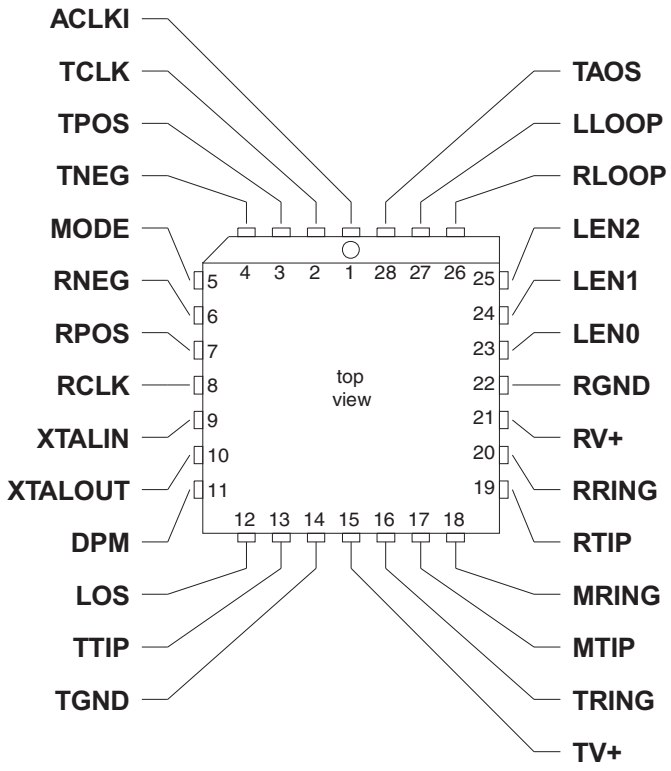
Power Supply

The device operates from a single +5 Volt supply. Separate pins for transmit and receive supplies provide internal isolation. These pins should be connected externally near the device and decoupled to their respective grounds. TV+ must not exceed RV+ by more than 0.3V.

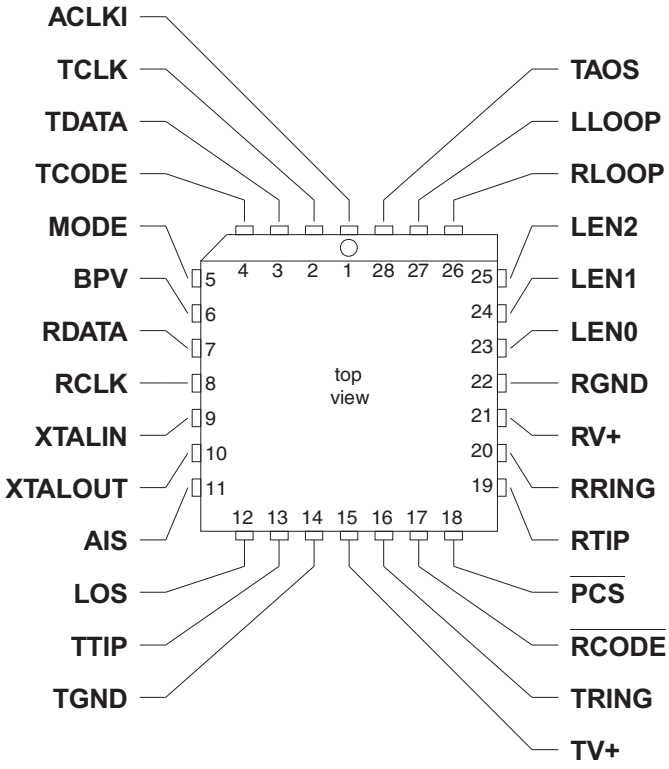
Decoupling and filtering of the power supplies is crucial for the proper operation of the analog circuits in both the transmit and receive paths. A 1.0 µF capacitor should be connected between TV+ and TGND, and a 0.1 µF capacitor should be connected between RV+ and RGND. Use mylar or ceramic capacitors and place them as closely as possible to their respective power supply pins. A 68 µF tantalum capacitor should be added close to the RV+/RGND supply. Wire-wrap breadboarding of the line interface is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

PIN DESCRIPTIONS

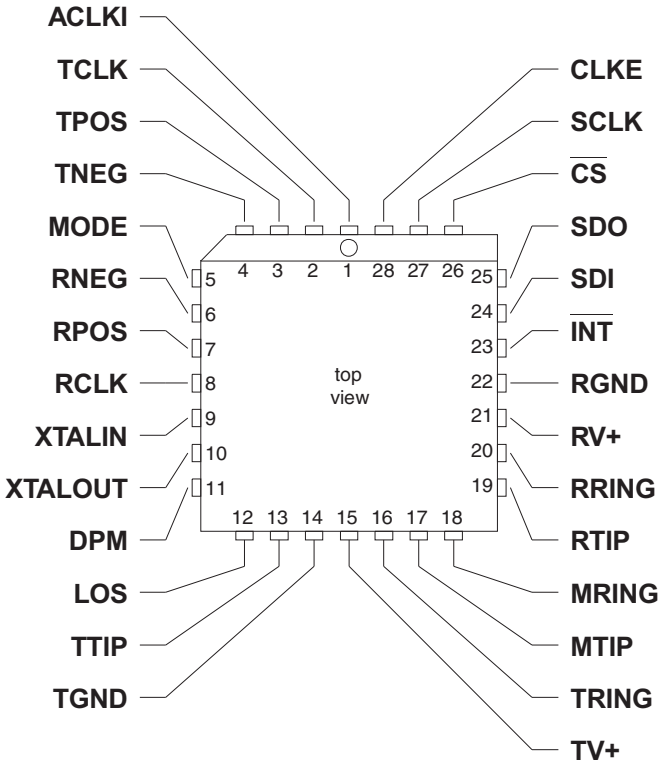
Hardware Mode



Extended Hardware Mode



Extended Hardware Mode



Power Supplies

RGND - Ground, Pin 22.

Power supply ground for all subcircuits except the transmit driver; typically 0 Volts.

RV+ - Power Supply, Pin 21.

Power supply for all subcircuits except the transmit driver; typically +5 Volts.

TGND - Ground, Transmit Driver, Pin 14.

Power supply ground for the transmit driver; typically 0 Volts.

TV+ - Power Supply, Transmit Driver, Pin 15.

Power supply for the transmit driver; typically +5 Volts. TV+ must not exceed RV+ by more than 0.3 V.

Oscillator

XTALIN, XTALOUT - Crystal Connections, Pins 9 and 10.

A 6.176 MHz (or 8.192 MHz) crystal should be connected across these pins. If a 1.544 MHz (or 2.048 MHz) clock is provided on ACLKI (pin 1), the jitter attenuator may be disabled by tying XTALIN, Pin 9 to RV+ through a 1 kΩ resistor, and floating XTALOUT, Pin 10.

Overdriving the oscillator with an external clock is not supported. See Appendix A.

Control

ACLKI - Alternate External Clock Input, Pin 1.

A 1.544 MHz (or 2.048 MHz) clock may be input to ACLKI, or this pin must be tied to ground. During LOS, the ACLKI input signal, if present, is output on RCLK through the jitter attenuator.

CLKE - Clock Edge, Pin 28. (Host Mode)

Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. Conversely, setting CLKE to logic 0 causes RPOS and RNEG to be valid on the rising edge of RCLK, and SDO to be valid on the falling edge of SCLK.

$\overline{\text{CS}}$ - Chip Select, Pin 26. (Host Mode)

This pin must transition from high to low to read or write the serial port.

$\overline{\text{INT}}$ - Receive Alarm Interrupt, Pin 23. (Host Mode)

Goes low when LOS or DPM change state to flag the host processor. $\overline{\text{INT}}$ is cleared by writing "clear LOS" or "clear DPM" to the register. $\overline{\text{INT}}$ is an open drain output and should be tied to the power supply through a resistor.

LEN0, LEN1, LEN2 - Line Length Selection, Pins 23, 24 and 25. (Hardware and Extended Hardware Modes)

Determines the shape and amplitude of the transmitted pulse to accommodate several cable types and lengths. See Table 3 for information on line length selection. Also controls the receiver slicing level and the line code in Extended Hardware Mode.

LLOOP - Local Loopback, Pin 27. (Hardware and Extended Hardware Modes)

Setting LLOOP to a logic 1 routes the transmit clock and data through the jitter attenuator to the receive clock and data pins. TCLK and TPOS/TNEG (or TDATA) are still transmitted unless overridden by a TAOS request. Inputs on RTIP and RRING are ignored.

MODE - Mode Select, Pin 5.

Driving the MODE pin high puts the line interface in the Host Mode. In the host mode, a serial control port is used to control the line interface and determine its status. Grounding the MODE pin puts the line interface in the Hardware Mode, where configuration and status are controlled by discrete pins. Floating the MODE pin or driving it to +2.5 Vselects the Extended Hardware Mode, where configuration and status are controlled by discrete pins. When floating MODE, there should be no external load on the pin. MODE defines the status of 13 pins (see Table 2).

$\overline{\text{PCS}}$ - Parallel Chip Select, Pin 18. (Extended Hardware Mode)

Setting $\overline{\text{PCS}}$ high causes the line interface to ignore the $\overline{\text{TCODE}}$, $\overline{\text{RCODE}}$, LEN0, LEN1, LEN2, RLOOP, LLOOP and TAOS inputs.

$\overline{\text{RCODE}}$ - Receiver Decoder Select, Pin 17. (Extended Hardware Mode)

Setting $\overline{\text{RCODE}}$ low enables B8ZS or HDB3 zero substitution in the receiver decoder. Setting $\overline{\text{RCODE}}$ high enables the AMI receiver decoder (see Table 8).

RLOOP - Remote Loopback, Pin 26. (Hardware and Extended Hardware Modes)

Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the jitter attenuator (if active) and through the driver back to the line. The recovered signal is also sent to RCLK and RPOS/RNEG (or RDATA). Any TAOS request is ignored.

Simultaneously taking RLOOP and LLOOP high for at least 200 ns initiates a device reset.

SCLK - Serial Clock, Pin 27. (Host Mode)

Clock used to read or write the serial port registers. SCLK can be either high or low when the line interface is selected using the $\overline{\text{CS}}$ pin.

SDI - Serial Data Input, Pin 24. (Host Mode)

Data for the on-chip register. Sampled on the rising edge of SCLK.

SDO - Serial Data Output, Pin 25. (Host Mode)

Status and control information from the on-chip register. If CLKE is high SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to or after bit D7 is output.

TAOS - Transmit All Ones Select, Pin 28. (Hardware and Extended Hardware Modes)

Setting TAOS to a logic 1 causes continuous ones to be transmitted at the frequency determined by TCLK.

$\overline{\text{TCODE}}$ - Transmitter Encoder Select, Pin 4. (Extended Hardware Mode)

Setting $\overline{\text{TCODE}}$ low enables B8ZS or HDB3 zero substitution in the transmitter encoder. Setting $\overline{\text{TCODE}}$ high enables the AMI transmitter encoder .

Data

RCLK - Recovered Clock, Pin 8.

The receiver recovered clock generated by the jitter attenuator is output on this pin.When in the loss of signal state ACLKI (if present) is output on RCLK via the jitter attenuator. If ACLKI is not present during LOS, RCLK is forced to the center frequency of the crystal oscillator..

RDATA - Receive Data - Pin 7. (Extended Hardware Mode)

Data recovered from the RTIP and RRING inputs is output at this pin, after being decoded by the line code decoder. RDATA is NRZ. RDATA is stable and valid on the falling edge of RCLK.

RPOS, RNEG - Receive Positive Data, Receive Negative Data, Pins 6 and 7. (Hardware and Host Modes)

The receiver recovered NRZ digital data is output on these pins. In the Hardware Mode, RPOS and RNEG are stable and valid on the rising edge of RCLK. In the Host Mode, CLKE determines the clock edge for which RPOS and RNEG are stable and valid. See Table 5. A positive pulse (with respect to ground) received on the RTIP pin generates a logic 1 on RPOS, and a positive pulse received on the RRING pin generates a logic 1 on RNEG.

RTIP, RRING - Receive Tip, Receive Ring, Pins 19 and 20.

The AMI receive signal is input to these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A1 in the *Applications* section. Data and clock are recovered and output on RCLK and RPOS/RNEG or RDATA.

TCLK - Transmit Clock, Pin 2.

The1.544 MHz (or 2.048 MHz) transmit clock is input on this pin. TPOS/TNEG or TDATA are sampled on the falling edge of TCLK.

TDATA - Transmit Data, Pin 3. (Extended Hardware Mode)

Transmitter NRZ input data which passes through the line code encoder, and is then driven on to the line through TTIP and TRING. TDATA is sampled on the falling edge of TCLK.

TPOS, TNEG - Transmit Positive Data, Transmit Negative Data, Pins 3 and 4. (Hardware and Host Modes)

Inputs for clock and data to be transmitted. The signal is driven on to the line through TTIP and TRING. TPOS and TNEG are sampled on the falling edge of TCLK. A TPOS input causes a positive pulse to be transmitted, while a TNEG input causes a negative pulse to be transmitted.