Chipsmall

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

CRYSTAL
A Cirrus Logic Company

CS61583

Dual T1/E1 Line Interface

Features

- Dual T1/E1 Line Interface

- Low Power Consumption
  (Typically 220mW per Line Interface)

- Matched Impedance Transmit Drivers

- Common Transmit and Receive Transformers for all Modes

- Selectable Jitter Attenuation for Transmit or Receive Paths

- Supports JTAG Boundary Scan

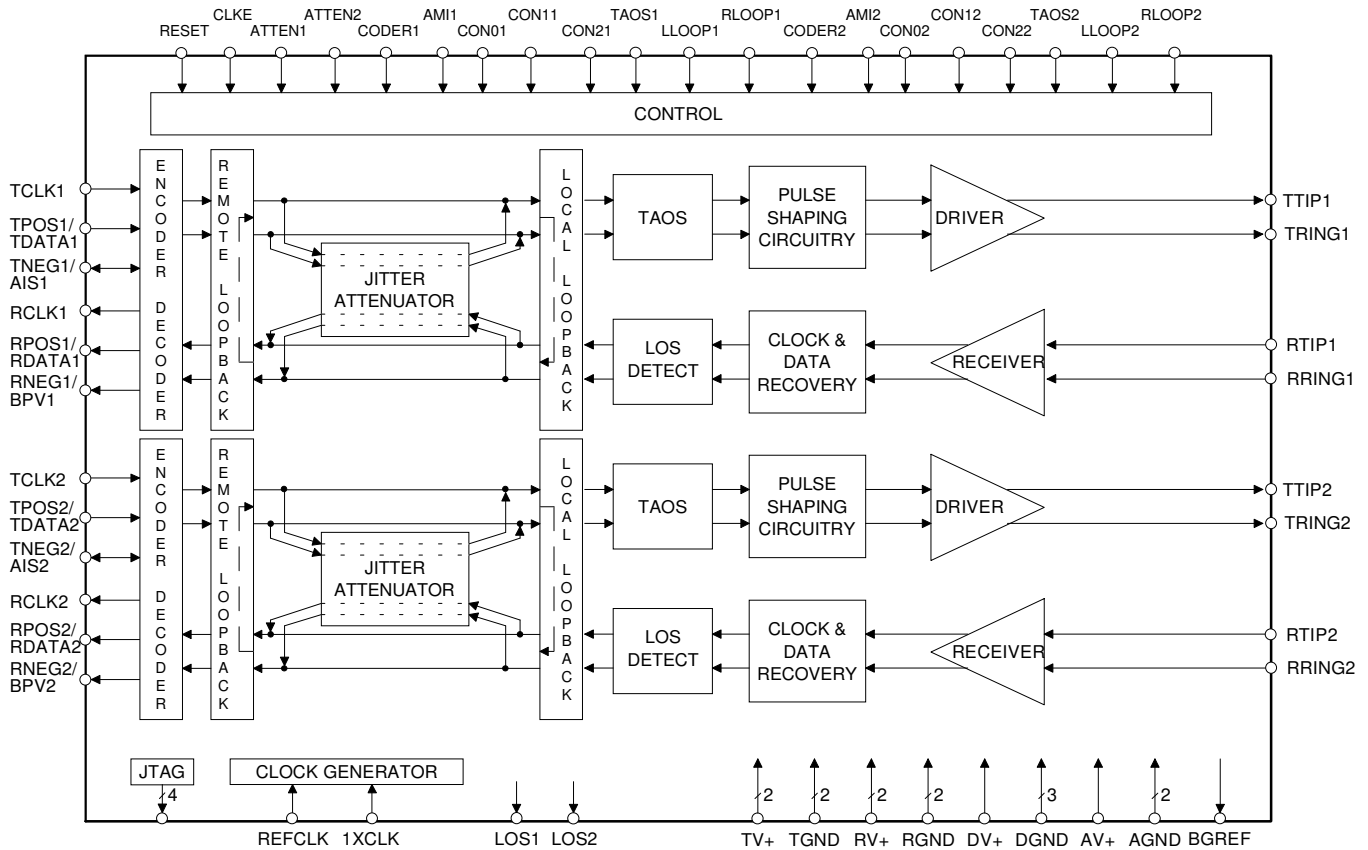- Hardware Mode Derivative of the CS61584

General Description

The CS61583 is a dual line interface for T1/E1 applications, designed for high-volume cards where low power and high density are required. Each channel features individual control and status pins which eliminates the need for external microprocessor support. The matched impedance drivers reduce power consumption and provide substantial return loss to insure superior T1/E1 pulse quality.

The CS61583 provides JTAG boundary scan to enhance system testability and reliability. The CS61583 is a 5 volt device and is a hardware mode derivative of the CS61584.

ORDERING INFORMATION
CS61583-IL5: 68-pin PLCC, -40 to +85 °C
CS61583-IQ5: 64-pin TQFP, -40 to +85 °C

Table of Contents

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Supply (TV+1, TV+2, RV+1, RV+2, AV+, DV+) (Note 1)			-	6.0	V
Input Voltage (Any Pin)		V_{in}	RGND - 0.3	(RV+) + 0.3	V
Input Current (Any Pin)	(Note 2)	I_{in}	-10	10	mA
Ambient Operating Temperature		T_A	-40	85	°C
Storage Temperature		T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

Notes: 1. Referenced to RGND1, RGND2, TGND1, TGND2, AGND, DGND at 0V.
2. Transient currents of up to 100 mA will not cause SCR latch-up.

RECOMMENDED OPERATING CONDITIONS

Parameter			Symbol	Min	Typ	Max	Units
DC Supply (TV+1, TV+2, AV+, DV+, RV+1, RV+2) (Note 3)				4.75	5.0	5.25	V
Ambient Operating Temperature			T_A	-40	25	85	°C
Power Consumption (Each Channel)	T1	(Notes 4 and 5)	P_C	-	310	-	mW
	T1	(Notes 4 and 6)		-	220	-	mW
	E1, 75Ω	(Notes 4 and 5)		-	275	-	mW
	E1, 120Ω	(Notes 4 and 5)		-	275	-	mW
REFCLK Frequency	T1	1XCLK = 1		1.544 - 100 ppm	1.544	1.544 + 100 ppm	MHz
	T1	1XCLK = 0		12.352 - 100 ppm	12.352	12.352 + 100 ppm	MHz
	E1	1XCLK = 1		2.048 - 100 ppm	2.048	2.048 + 100 ppm	MHz
	E1	1XCLK = 0		16.384 - 100 ppm	16.384	16.384 + 100 ppm	MHz

Notes: 3. TV+1, TV+2, AV+, DV+, RV+1, RV+2 should be connected together. TGND1, TGND2, RGND1, RGND2, DGND1, DGND2, DGND3 should be connected together.
4. Power consumption while driving line load over operating temperature range. Includes IC and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
5. Assumes 100% ones density and maximum line length at 5.25V.
6. Assumes 50% ones density and 300ft. line length at 5.0V.

DIGITAL CHARACTERISTICS (T_A = -40 to 85 °C; power supply pins within ±5% of nominal)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	(Note 7)	V_{IH}	(DV+)-0.5	-	-	V
Low-Level Input Voltage	(Note 7)	V_{IL}	-	-	0.5	V
High-Level Output Voltage (Digital pins) I_{OUT} = -40 μA	(Note 8)	V_{OH}	(DV+)-0.3	-	-	V
Low-Level Output Voltage (Digital pins) I_{OUT} = 1.6 mA	(Note 8)	V_{OL}	-	-	0.3	V
Input Leakage Current (Digital pins except J-TMS, and J-TDI)			-	-	±10	μA

Notes: 7. Digital inputs are designed for CMOS logic levels.
       8. Digital outputs are TTL compatible and drive CMOS levels into a CMOS load.

ANALOG SPECIFICATIONS (T_A = -40 to 85 °C; power supply pins within ±5% of nominal)

Parameter		Min	Typ	Max	Units
Receiver					
RTIP/RRING Differential Input Impedance		-	20k	-	Ω
Sensitivity Below DSX-1 (0 dB = 2.4 V)		-13.6	-	-	dB
Loss of Signal Threshold		-	0.3	-	V
Data Decision Threshold T1, DSX-1 (Note 9)		60	65	70	% of Peak
(Note 10)		55	-	75	
E1 (Note 11)		45	50	55	
(Note 12)		40	-	60	
Allowable Consecutive Zeros before LOS		160	175	190	bits
Receiver Input Jitter 10 Hz and below (Note 13)		300	-	-	UI
Tolerance (DSX-1, E1) 2 kHz		6.0	-	-	UI
10 kHz - 100 kHz		0.4	-	-	UI
Receiver Return Loss 51 kHz - 102 kHz (Notes 14,		12	-	-	dB
102 kHz - 2.048 MHz 21, and 22)		18	-	-	dB
2.048 MHz - 3.072 MHz		14	-	-	dB
Jitter Attenuator					
Jitter Attenuation Curve T1 (Notes 14 and 15)		-	4	-	Hz
Corner Frequency E1		-	5.5	-	Hz
Attenuation at 10 kHz Jitter Frequency (Notes 14 and 15)		-	60	-	dB
Attenuator Input Jitter Tolerance (Note 14) (Before Onset of FIFO Overflow or Underflow Protection)		28	43	-	UI_{pk-pk}

Notes: 9. For input amplitude of 1.2 V_{pk} to 4.14 V_{pk}
    10. For input amplitude of 0.5 V_{pk} to 1.2 V_{pk}, and 4.14 V_{pk} to 5.0 V_{pk}
    11. For input amplitude of 1.07 V_{pk} to 4.14 V_{pk},
    12. For input amplitude of 4.14 V_{pk} to 5.0 V_{pk},
    13. Jitter tolerance increases at lower frequencies. Refer to the Receiver section.
    14. Not production tested. Parameters guaranteed by design and characterization.
    15. Attenuation measured with sinusoidal input jitter equal to 3/4 of measured jitter tolerance.
        Circuit attenuates jitter at 20 dB/decade above the corner frequency. Output jitter
        can increase significantly when more than 28 UI's are input to the attenuator. Refer to the
        Jitter Attenuator section.

ANALOG SPECIFICATIONS (T_A = -40 to 85 °C; power supply pins within ±5% of nominal)

Parameter		Min	Typ	Max	Units
Transmitter					
AMI Output Pulse Amplitudes (Note 16)					
E1, 75Ω (Note 17)		2.14	2.37	2.6	V
E1, 120Ω (Note 18)		2.7	3.0	3.3	V
T1, DSX-1 (Note 19)		2.4	3.0	3.6	V
Recommended Transmitter Output Load (Note 16)					
T1		-	76.6	-	Ω
E1, 75Ω		-	57.4	-	Ω
E1, 120Ω		-	90.6	-	Ω
Jitter Added During Remote Loopback	10 Hz - 8 kHz	-	0.005	-	UI
	8 kHz - 40 kHz	-	0.008	-	UI
	10 Hz - 40 kHz	-	0.010	-	UI
	Broad Band (Note 20)	-	0.015	-	UI
Power in 2 kHz band about 772 kHz (Notes 14 and 21) (DSX-1 only)		12.6	15	17.9	dBm
Power in 2 kHz band about 1.544 MHz (Notes 14 and 21)) (referenced to power in 2 kHz band at 772 kHz) (DSX-1 only)		-29	-38	-	dB
Positive to Negative Pulse Imbalance (Notes 14 and 21)					
T1, DSX-1		-	0.2	0.5	dB
E1, amplitude at center of pulse interval		-5	-	+5	%
E1, width at 50% of nominal amplitude		-5	-	+5	%
Transmitter Return Loss (Notes 14, 21, and 22)					
51 kHz - 102 kHz		18	25	-	dB
102 kHz - 2.048 MHz		14	18	-	dB
2.048 MHz - 3.072 MHz		10	12	-	dB
E1 Short Circuit Current (Note 23)		-	-	50	mA$_{rms}$
E1 and DSX-1 Output Pulse Rise/Fall Times (Note 24)		-	25	-	ns
E1 Pulse Width (at 50% of peak amplitude)		-	244	-	ns
E1 Pulse Amplitude	E1, 75Ω	-0.237	-	0.237	V
for a space	E1, 120Ω	-0.3	-	0.3	V

Notes: 16. Using a transformer that meets the specifications in the Applications section.

17. Measured across 75 Ω at the output of the transmit transformer for CON2/1/0 = 0/0/0.

18. Measured across 120 Ω at the output of the transmit transformer for CON2/1/0 = 0/0/1.

19. Measured at the DSX-1 cross-connect for line length settings CON2/1/0 = 0/1/0, 0/1/1, 1/0/0, 1/0/1, and 1/1/0 after the appropriate length of #22 ABAM cable specified in Table 1.

20. Input signal to RTIP/RRING is jitter free. Values will reduce slightly if jitter free clock is input to TCLK.

21. Typical performance using the line interface circuitry recommended in the Applications section.

22. Return loss = $20 \log_{10} ABS((z_1+z_0)/(z_1-z_0))$ where z_1=impedance of the transmitter or receiver, and z_0=cable impedance.

23. Transformer secondary shorted with 0.5 Ω resistor during the transmission of 100% ones.

24. At transformer secondary and measured from 10% to 90% of amplitude.

SWITCHING CHARACTERISTICS - T1 CLOCK/DATA (T_A = -40 to 85 °C; power supply pins within ±5% of nominal; Inputs: Logic 0 = 0V, Logic 1 = DV+) (See Figures 1, 2, and 3)

| Parameter		Symbol	Min	Typ	Max	Units
TCLK Frequency	(Note 25)	f_{tclk}	-	1.544	-	MHz
TCLK Duty Cycle		t_{pwh2}/t_{pw2}	30	50	70	%
RCLK Duty Cycle	(Note 26)	t_{pwh1}/t_{pw1}	45	50	55	%
Rise Time (All Digital Outputs)	(Note 27)	t_r	-	-	65	ns
Fall Time (All Digital Outputs)	(Note 27)	t_f	-	-	65	ns
RPOS/RNEG (RDATA) to RCLK Rising Setup Time		t_{su1}	-	274	-	ns
RCLK Rising to RPOS/RNEG (RDATA) Hold Time		t_{h1}	-	274	-	ns
TPOS/TNEG (TDATA) to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG (TDATA) Hold Time		t_{h2}	25	-	-	ns

Notes: 25. The maximum burst rate of a gapped TCLK input clock is 8.192 MHz. For the gapped clock to be tolerated by the CS61583, the jitter attenuator must be switched to the transmit path of the line interface. The maximum gap size that can be tolerated on TCLK is 28 UIp-p.
26. RCLK duty cycle may be outside the specified limits when the jitter attenuator is in the receive path, and when the jitter attenuator is employing the overflow/underflow protection mechanism.
27. At max load of 50 pF.

SWITCHING CHARACTERISTICS - E1 CLOCK/DATA (T_A = -40 to 85 °C; power supply pins within ±5% of nominal; Inputs: Logic 0 = 0V, Logic 1 = DV+) (See Figures 1, 2, and 3)

Parameter		Symbol	Min	Typ	Max	Units
TCLK Frequency	(Note 25)	f_{tclk}	-	2.048	-	MHz
TCLK Duty Cycle		t_{pwh2}/t_{pw2}	30	50	70	%
RCLK Duty Cycle	(Note 26)	t_{pwh1}/t_{pw1}	45	50	55	%
Rise Time (All Digital Outputs)	(Note 27)	t_r	-	-	65	ns
Fall Time (All Digital Outputs)	(Note 27)	t_f	-	-	65	ns
RPOS/RNEG (RDATA) to RCLK Rising Setup Time		t_{su1}	-	194	-	ns
RCLK Rising to RPOS/RNEG (RDATA) Hold Time		t_{h1}	-	194	-	ns
TPOS/TNEG (TDATA) to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG (TDATA) Hold Time		t_{h2}	25	-	-	ns
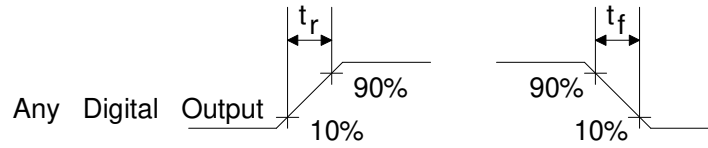
Figure 1. Signal Rise and Fall Characteristics
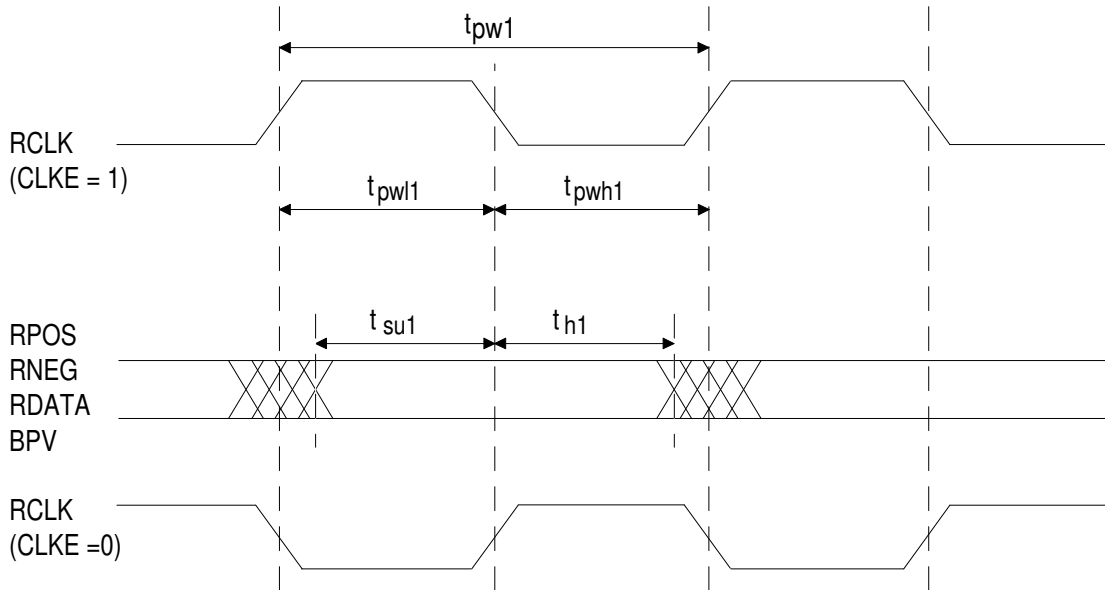
Figure 2. Recovered Clock and Data Switching Characteristics
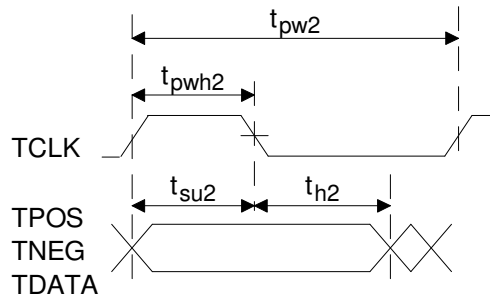
Figure 3. Transmit Clock and Data Switching Characteristics

SWITCHING CHARACTERISTICS - JTAG (T$_A$ = - 40 $°$ to 85 $°$ C;
TV+, RV+ = nominal ±0.3V; Inputs: Logic 0 = 0V, Logic 1 = RV+)   (See Figure 4)

Parameter	Symbol	Min	Typ	Max	Units
Cycle Time	t$_{cyc}$	200	-	-	ns
J-TMS/J-TDI to J-TCK rising setup time	t$_{su}$	50	-	-	ns
J-TCK rising to J-TMS/J-TDI hold time	t$_h$	50	-	-	ns
J-TCK falling to J-TDO valid	t$_{dv}$	-	-	50	ns
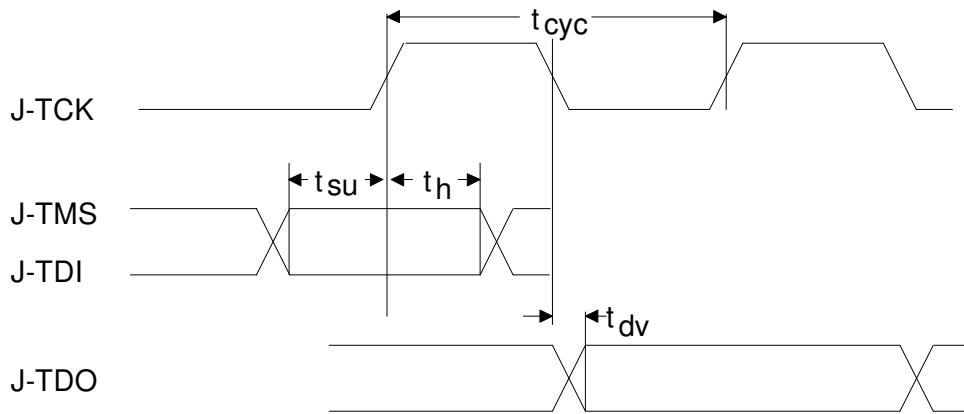
Figure 4. JAG Switching Characteristics

OVERVIEW

The CS61583 is a dual line interface for T1/E1 applications, designed for high-volume cards where low power and high density are required. One board design can support all T1/E1 short-haul modes by only changing component values in the receive and transmit paths (if REFCLK and TCLK are externally tied together). Figure 5 illustrates applications of the CS61583 in various environments.

All control of the device is achieved via external pins, eliminating the need for microprocessor support. The following pin control options are available on a per channel basis: line length selection, coder mode, jitter attenuator location, transmit all ones, local loopback, and remote loopback.

The line driver generates waveforms compatible with E1 (CCITT G.703), T1 short haul (DSX-1), and T1 FCC Part 68 Option A (DS1). A single transformer turns ratio is used for all waveform types. The driver internally matches the impedance of the load, providing excellent return loss to insure superior T1/E1 pulse quality. An addi-
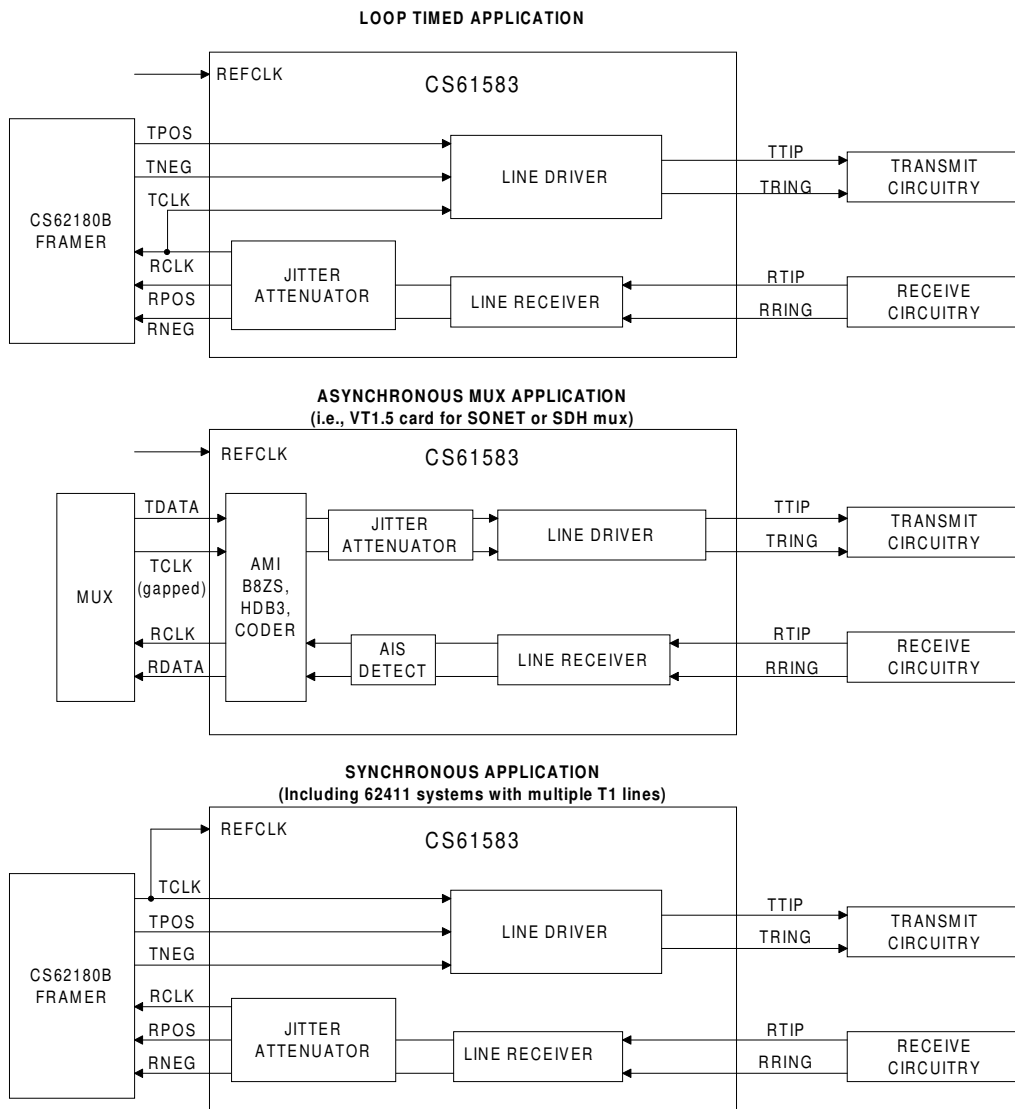
Figure 5. Examples of CS61583 Applications

tional benefit of the internal impedance matching is a 50 percent reduction in power consumption compared to implementing return loss using external resistors that causes the transmitter to drive the equivalent of two line loads.

The line receiver contains all the necessary clock and data recovery circuits.

The jitter attenuator meets AT&T 62411 requirements when using a 1X or 8X reference clock supplied by either a crystal oscillator or external reference at the REFCLK input pin.

AT&T 62411 Customer Premises Application

The AT&T 62411 specification applies to the T1 interface between the customer premises and the carrier, and must be implemented by the customer premises equipment in order to connect to the AT&T network.

In 62411 applications, the management of jitter is a very important design consideration. Typically, the jitter attenuator is placed in the receive path of the CS61583 to reduce the jitter input to the system synchronizer. The jitter attenuated recovered clock is used as the input to the transmit clock to implement a loop-timed system. A Stratum 4 (±32 ppm) quality clock or better should be input to REFCLK. Note that any jitter present on the reference clock will not be filtered by the jitter attenuator.

Asynchronous Multiplexer Application

Asynchronous multiplexers accept multiple T1/E1 lines (which are asynchronous to each other), and combine them into a higher speed transmission rate (e.g. M13 muxes and SONET muxes). In these systems, the jitter attenuator is placed in the transmit path of the CS61583 to remove the gapped clock jitter input by the multiplexer to TCLK. Because the transmit clock is jittered, the reference clock to the CS61583 is provided by an external source operating at 1X or 8X the data rate. Because T1/E1 framers are

not usually required in asynchronous multiplexers, the B8ZS/AMI/HDB3 coders in the CS61583 are activated to provide data interfaces on TDATA and RDATA.

Synchronous Application

A typical example of a synchronous application is a T1 card in a central office switch or a 0/1 digital cross-connect system. These systems place the jitter attenuator in the receive path to reduce the jitter presented to the system. A Stratum 3 or better system clock is input to the CS61583 transmit and reference clocks.

TRANSMITTER

The transmitter accepts data from a T1 or E1 system and outputs pulses of appropriate shape to the line. The transmit clock (TCLK) and transmit data (TPOS & TNEG, or TDATA) are supplied synchronously. Data is sampled on the falling edge of the TCLK input.

The configuration pins CON[2:0] control transmitted pulse shapes, transmitter source impedance, and receiver slicing level as shown in Table 1. Typical output pulses are shown in Figures 6 and 7. These pulse shapes are fully pre-defined by circuitry in the CS61583, and are fully compliant with appropriate standards when used with our application guidelines in standard installations. Both channels must be operated at the same line rate (both T1 or both E1).

Note that the pulse width for Part 68 Option A (324 ns) is narrower than the optimal pulse width for DSX-1 (350 ns). The CS61583 automatically adjusts the pulse width based on the configuration selection.

The transmitter impedance changes with the line length options in order to match the load impedance (75Ω for E1 coax, 100Ω for T1, 120Ω for E1 shielded twisted pair), providing a minimum of 14 dB return loss for T1 and E1 frequencies
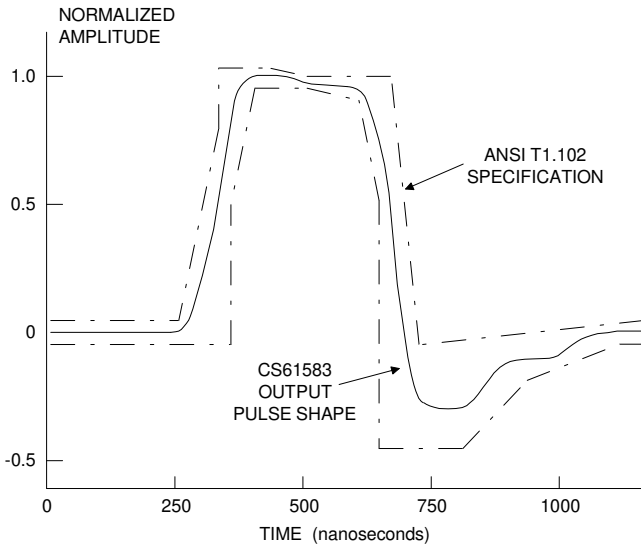
Figure 6. Typical Pulse Shape at DSX-1 Cross Connect

Figure 7. Pulse Mask at the 2048 kbps Interface

during the transmission of both marks and spaces. This improves signal quality by minimizing reflections from the transmitter. Impedance matching also reduces load power consumption by a factor of two when compared to the return loss achieved by using external resistors.
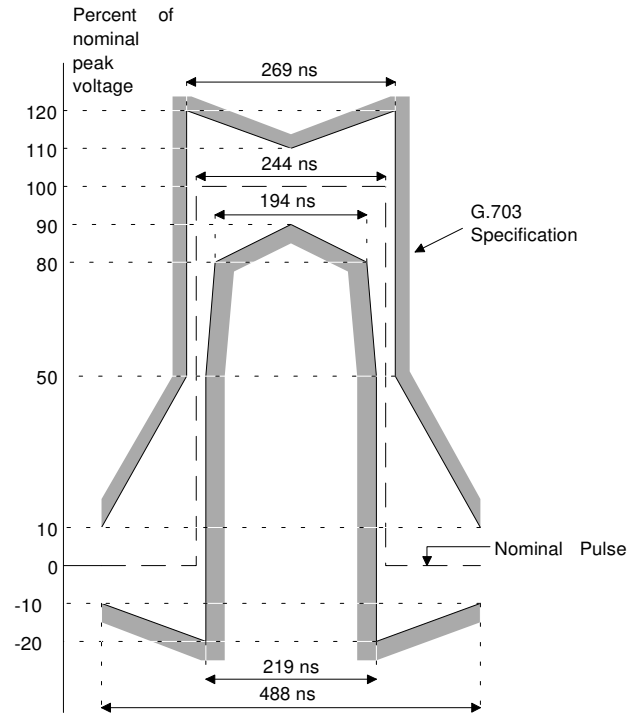
The CS61583 driver will automatically detect an inactive TLCK input (i.e., no valid data is being clocked to the driver). When this condition is detected, the driver is forced low (except during remote loopback) to output spaces and prevent TTIP and TRING from entering a constant transmit-mark state.

When any transmit configuration established by CON[2:0], TAOS, or LLOOP changed states, the transmitter stabilizes within 22 TCLK bit periods. The transmitter takes longer to stabilize when RLOOP1 or RLOOP2 is selected because the timing circuitry must adjust to the new frequency from RCLK.

When the transmitter transformer secondaries are shorted through a 0.5 ohm resistor, the transmit-

C O N 2	C O N 1	C O N 0	Transmit Pulse Width at 50% Amplitude	Transmit Pulse Shape	Receiver Slicing Level
0	0	0	244 ns (50%)	E1: square, 2.37 Volts into 75 Ω	50%
0	0	1	244 ns (50%)	E1: square, 3.00 Volts into 120 Ω	50%
0	1	0	350 ns (54%)	DSX-1: 0-133 ft. / or DS1 FCC Part 68 Option A with undershoot	65%
0	1	1	350 ns (54%)	DSX-1: 133-266 ft.	65%
1	0	0	350 ns (54%)	DSX-1: 266-399 ft.	65%
1	0	1	350 ns (54%)	DSX-1: 399-533 ft.	65%
1	1	0	350 ns (54%)	DSX-1: 533-655 ft.	65%
1	1	1	324 ns (50%)	DS1: FCC Part 68 Option A (0 dB)	65%

Table 1. Configuration Selection

ter will output a maximum of 50 mA-rms, as required by European specification BS6450.

RECEIVER

The receiver extracts data and clock from the T1/E1 signal on the line interface and outputs clock and synchronized data to the system. The signal is detected differentially across the receive transformer and can be recovered over the entire range of short haul cable lengths. The transmit and receive transfomer specifications are identical and are presented in the Applications section.

As shown in Table 1, the receiver slicing level is set at 65% for DS1/DSX-1 short-haul and at 50% for all other applications.

The clock recovery circuit is a second-order phase locked loop that can tolerate up to 0.4 UI of jitter from 10 kHz to 100 kHz without generating errors (Figure 8). The clock and data recovery circuit is tolerant of long strings of consecutive zeros and will successfully recover a 1-in-175 jitter-free line input signal.

Recovered data at RPOS and RNEG (or RDATA) is stable and may be sampled using the recovered clock RCLK. The CLKE input determines the clock polarity for which output data is stable and valid as shown in Table 2. When CLKE is low, RPOS and RNEG (or RDATA) are valid on the rising edge of RCLK. When CLKE is high, RPOS and RNEG (or RDATA) are valid on the falling edge of RCLK.

CLKE	DATA	CLOCK	Clock Edge for Valid Data
LOW	RPOS, RNEG or RDATA	RCLK RCLK	Rising Rising
HIGH	RPOS, RNEG or RDATA	RCLK RCLK	Falling Falling

Table 2. Recovered Data/Clock Options

JITTER ATTENUATOR

The jitter attenuator can be switched into either the receive or transmit paths. Alternatively, it can also be removed from both paths to reduce the propagation delay.

The location of the attenuators for both channels is controlled by the ATTEN0 and ATTEN1 pins. Table 3 shows how these pins are decoded.

ATTEN1	ATTEN0	Location of Jitter Attenuator
0	0	Receiver
0	1	Disabled
1	0	Transmitter
1	1	Reserved

Table 3. Jitter Attenuation Control

The attenuator consists of a 64-bit FIFO, a narrow-band monolithic PLL, and control logic. Signal jitter is absorbed in the FIFO which is designed to neither overflow nor underflow. If overflow or underflow is imminent, the jitter transfer function is altered to insure that no bit-errors occur. Under this condition, jitter gain may occur and jitter should be attenuated externally in a frame buffer. The jitter attenuator will typically tolerate 43 UIs before the overflow/underflow mechanism occurs. If the jitter attenuator has not had time to "lock" to the aver-

Figure 8. Minimum Input Jitter Tolerance of Receiver (Clock Recovery Circuit and Jitter Attenuator)

age incoming frequency (e.g. following a device reset) the attenuator will tolerate a minimum of 22 UIs before the overflow/underflow mechanism occurs.

For T1/E1 line cards used in high-speed mutiplexers (e.g., SONET and SDH), the jitter attenuator is typically used in the transmit path. The attenuator can accept a transmit clock with gaps ≤ 28 UIs and a transmit clock burst rate of ≤ 8 MHz.

When the jitter attenuator is in the receive path and loss of signal occurs, the frequency of the last recovered signal is held. When the jitter attenuator is not in the receive path, the last recovered frequency is not held and the output frequency becomes the frequency of the reference clock.

A typical jitter attenuation curve is shown in Figure 9.
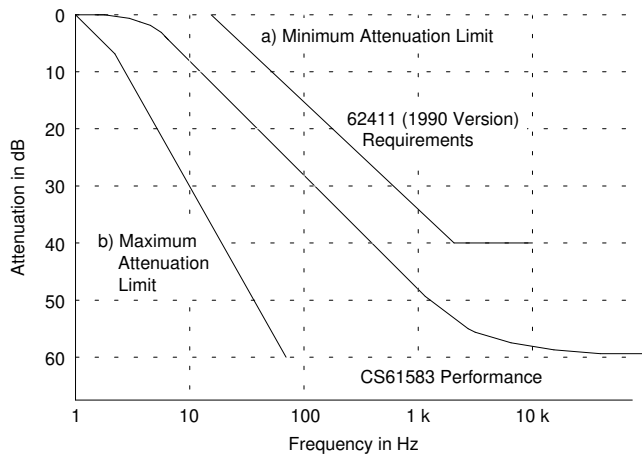
Figure 9. Typical Jitter Transfer Function

REFERENCE CLOCK

The CS61583 requires a reference clock with a minimum accuracy of ±100 ppm for T1 and E1 applications. This clock can be either a 1X clock (i.e., 1.544 MHz or 2.048 MHz), or can be a 8X clock (i.e., 12.352 MHz or 16.384 MHz) as selected by the 1XCLK pin. In systems with a

jittered transmit clock, the reference clock should not be tied to the transmit clock and a separate external oscillator should drive the reference clock input. Any jitter present on the reference clock will not be filtered by the jitter attenuator.

POWER-UP RESET

On power-up, the device is held in a static state until the power supply achieves approximately 60% of the power supply voltage. When this threshold is crossed, the device waits another 10 ms to allow the power supply to reach operating voltage and then calibrates the transmit and receive circuitry. This initial calibration takes less than 20 ms but can occur only if REFCLK and TCLK are present. The power-up reset performs the same functions as the RESET pin.

LINE CONTROL AND MONITORING

Line control and monitoring of the CS61583 is achieved using the control pins. The controls and indications available on the CS61583 are detailed below.

Line Code Encoder/Decoder

Coding may be transparent, AMI, B8ZS, or HDB3 and is selected using the CODER1, CODER2, AMI1, and AMI2 pins. In the coder mode, AMI, B8ZS, and HDB3 line codes are available. The input data to the encoder is on TDATA and the output data from the decoder is in NRZ format on RDATA. See Table 4.

CODER[2:1]=0	CODER[2:1]=1
Transparent Mode Enabled and AMI[2:1] Pin(s) Disabled	AMI[2:1]=0 B8ZS/HDB3 Encoder/Decoder Enabled
	AMI[2:1]=1 AMI Encoder/Decoder Enabled

Table 4. Coder Mode Options

Alarm Indication Signal

In coder mode, the TNEG pin becomes the alarm indication signal (AIS) output controlled by the receiver. The receiver detects the AIS condition on observation of 99.9% ones density in a 5.3 ms period (< 9 zeros in 8192 bits) and sets the AIS pin high. The AIS condition is exited when ≥ 9 zeros are detected in 8192 bits.

Bipolar Violation Detection

In coder mode, the RNEG pin becomes the bipolar violation (BPV) strobe output controlled by the receiver. The BPV pin goes high for one RCLK period when a bipolar violation is detected in the received signal. Note that B8ZS or HDB3 zero substitutions are not flagged as bipolar violations when the decoder is enabled.

Loss of Signal

The loss of signal (LOS) indication is detected by the receiver and reported when the LOS pin is high. Loss of signal is indicated when 175±15 consecutive zeros are received. The LOS condition is exited according to the ANSI T1.231-1993 criteria that requires 12.5% ones density over 175±75 bit periods with no more than 100 consecutive zeros. Note that bit errors may occur at RPOS and RNEG (or RDATA) prior to the LOS indication if the analog input level falls below the receiver sensitivity.

The LOS pin is set high when the device is reset or in powered up and returns low when data is recovered by the receiver.

Transmit All Ones

Transmit all ones is selected by setting the TAOS pin high. Selecting TAOS causes continuous ones to be transmitted to the line interface on TTIP and TRING at the frequency of REFCLK. In this mode, the transmit data inputs TPOS and TNEG (or TDATA) are ignored. A TAOS overrides the data transmitted to the line interface during local and remote loopbacks.

Local Loopback

A local loopback is selected by setting the LLOOP pin high. Selecting LLOOP causes the TCLK, TPOS, and TNEG (or TDATA) inputs to be looped back through the jitter attenuator (if enabled) to the RCLK, RPOS, and RNEG (or RDATA) outputs. Data received at the line interface is ignored, but data at TPOS and TNEG (or TDATA) continues to be transmitted to the line interface at TTIP and TRING.

A TAOS request overrides the data transmitted to the line interface during local loopback. Note that simultaneous selection of local and remote loopback modes is not valid.

Remote Loopback

A remote loopback is selected by setting the RLOOP pin high. Selecting RLOOP causes the data received from the line interface at RTIP and RRING to be looped back through the jitter attenuator (if enabled) and retransmitted on TTIP and TRING. Data transmitted at TPOS and TNEG (or TDATA) is ignored, but data recovered from RTIP and RRING continues to be transmitted on RPOS and RNEG (or RDATA).

Remote loopback is functional if TCLK is absent. A TAOS request overrides the data transmitted to the line interface during a remote loopback. Note that simultaneous selection of local and remote loopback modes is not valid.

Reset Pin

The CS61583 is continuously calibrated during operation to insure the performance of the device over power supply and temperature. The continuous calibration function eliminates the need to reset the line interface during operation.

A device reset may be selected by setting the RESET pin high for a minimum of 200 ns. The reset function initiates on the falling edge of RESET and takes less than 20 ms to complete. The control logic is initialized and the transmit and

receive circuitry is calibrated if REFCLK and TCLK are present.

JTAG BOUNDARY SCAN

Board testing is supported through JTAG boundary scan. Using boundary scan, the integrity of the digital paths between devices on a circuit board can be verified. This verification is supported by the ability to externally set the signals on the digital output pins of the CS61583, and to externally read the signals present on the input pins of the CS61583. Additionally, the manufacturer ID, part number and revision of the CS61583 can be read during board test using JTAG boundary scan.

As shown in Figure 10, the JTAG hardware consists of data and instruction registers plus a Test Access Port (TAP) controller. Control of the TAP is achieved through signals applied to the Test Mode Select (J-TMS) and Test Clock (J-TCK) input pins. Data is shifted into the registers via the Test Data Input (J-TDI) pin, and shifted out of the registers via the Test Data Output (J-TDO) pin. Both J-TDI and J-TDO are clocked at a rate determined by J-TCK. The Instruction register defines which data register is accessed in the

shift operation. Note that if J-TDI is floating, an internal pull-up resistor forces the pin high.

JTAG Data Registers (DR)

The test data registers are the Boundary-Scan Register (BSR), the Device Identification Register (DIR), and the Bypass Register (BR).

Boundary Scan Register: The BSR is connected in parallel to all the digital I/O pins, and provides the mechanism for applying/reading test patterns to/from the board traces. The BSR is 67 bits long and is initialized and read using the instruction SAMPLE/PRELOAD. The bit ordering for the BSR is the same as the top-view package pin out, beginning with the LOS1 pin and moving counter-clockwise to end with the CODER1 pin as shown in Table 5. Note that the analog, oscillator, power, ground, CLKE, and ATTEN0 pins are not included as part of the boundary-scan register.

The input pins require one bit in the BSR and only one J-TCK cycle is required to load test data for each input pin.

The output pins have two bits in the BSR to define output high, output low, or high impedance.

Figure 10. Block Diagram of JTAG Circuitry

The first bit (shifted in first) selects between an output-enabled state (bit set to 1) or high-impedance state (bit set to 0). The second bit shifted in contains the test data that may be output on the pin. Therefore, two J-TCK cycles are required to load test data for each output pin.

BSR bits	Pin Name	Pad Type
0-2	LOS1	bi-directional[2]
3-5	TNEG1/AIS1	bi-directional
6	TPOS1/TDATA1	input
7	TCLK1	input
8-9	RNEG1/BPV1	output
10-11	RPOS1/RDATA1	output
12-13	RCLK1	output
14-16	ATTEN1	bi-directional[1]
17-19	RLOOP1	bi-directional[1]
20	LLOOP1	input
21-23	LLOOP2	bi-directional[1]
24-26	TAOS1	bi-directional[1]
27-29	TAOS2	bi-directional[1]
30-32	CON01	bi-directional[1]
33-35	CON02	bi-directional[1]
36-38	CON11	bi-directional[1]
39-41	CON12	bi-directional[1]
42-44	CON21	bi-directional[1]
45	CON22	input
46-48	AMI1	bi-directional[1]
49-50	RCLK2	output
51-52	RPOS2/RDATA2	output
53-54	RNEG2/BPV2	output
55	TCLK2	input
56	TPOS2/TDATA2	input
57-59	TNEG2/AIS2	bi-directional
60-62	LOS2	bi-directional[2]
63	AMI2	input
64	CODER2	input
65	RLOOP2	input
66	CODER1	input

1. Configure pad as an input.
2. Configure pad as an output.

Table 5. Boundary Scan Register

The bi-directional pins have three bits in the BSR to define input, output high, output low, or high impedance. The first bit shifted into the BSR configures the output driver as high-impedance (bit set to 0) or active (bit set to 1). The second bit shifted into the BSR sets the output value when the first bit is 1. The third bit captures the value of the pin. This pin may have its value set externally as an input (if the first bit is 0) or set internally as an output (if the first bit is 1). To configure a pad as an input, the J-TDI pattern is 0X0. To configure a pad as an output, the J-TDI pattern is 1X1. Therefore, three J-TCK cycles are required to load test data for each bi-directional pin.

Device Identification Register: The DIR provides the manufacturer, part number, and version of the CS61583. This information can be used to verify that the proper version or revision number has been used in the system under test. The DIR is 32 bits long and is partitioned as shown in figure 11.

MSB   LSB
31   28 27   12 11   1 0
| 0 0 0 0 | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 | 0 0 0 0 1 1 0 0 1 0 0 | 1 |
 (4 bits)   (16 bits)   (11 bits)

BIT #(s)	FUNCTION	Total Bits
31-28	Version number	4
27-12	Part Number	16
11-1	Manufacturer Number	11
0	Constant Logic '1'	1

Figure 11. Device Identification Register

Data from the DIR is shifted out to J-TDO LSB first.

Bypass Register: The Bypass register consists of a single bit, and provides a serial path between J-TDI and J-TDO, bypassing the BSR. This allows bypassing specific devices during certain board-level tests. This also reduces test access times by reducing the total number of shifts required from J-TDI to J-TDO.

JTAG Instructions and Instruction Register (IR)

The instruction register (2 bits) allows the instruction to be shifted into the JTAG circuit. The instruction selects the test to be performed or the data register to be accessed or both. The valid instructions are shifted in LSB first and are listed below:

IR CODE	INSTRUCTION
00	EXTEST
01	SAMPLE/PRELOAD
10	IDCODE
11	BYPASS

EXTEST Instruction: The EXTEST instruction allows testing of off-chip circuitry and board-level interconnect. EXTEST connects the BSR to the J-TDI and J-TDO pins. The normal path between the CS61583 logic and I/O pins is broken. The signals on the output pins are loaded from the BSR and the signals on the input pins are loaded into the BSR.

SAMPLE/PRELOAD Instruction: The SAMPLE/PRELOAD instructions allows scanning of the boundary-scan register without interfering with the operation of the CS61583. This instruction connects the BSR to the J-TDI and J-TDO pins. The normal path between the CS61583 logic and its I/O pins is maintained. The signals on the I/O pins are loaded into the BSR. Additionally, this instruction can be used to latch values into the digital output pins.

IDCODE Instruction: The IDCODE instruction connects the device identification register to the J-TDO pin. The IDCODE instruction is forced into the instruction register during the Test-Logic-Reset controller state. The default instruction is IDCODE after a device reset.

BYPASS Instruction: The BYPASS instruction connects the minimum length bypass register between the J-TDI and J-TDO pins and allows data to be shifted in the Shift-DR controller state.

Internal Testing Considerations

Note that the INTEST instruction is not supported because of the difficulty in performing significant internal tests using JTAG.

The one test that could be easily performed using an arbitrary clock rate on TCLK and REFCLK is a local loopback with jitter attenuator disabled. However, this test provides limited fault coverage and is only useful in determining if the device had been catastrophically destroyed. Alternatively, catastrophic destruction of the device and/or surrounding board traces can be detected using EXTEST. Therefore, the INTEST instruction provides limited testing capability and was not included in the CS61583.

JTAG TAP Controller

Figure 12 shows the state diagram for the TAP state machine. A description of each state follows. Note that the figure contains two main branches to access either the data or instruction registers. The value shown next to each state transition in this figure is the value present at J-TMS at each rising edge of J-TCK.

Test-Logic-Reset State

In this state, the test logic is disabled to continue normal operation of the device. During initialization, the CS61583 initializes the instruction register with the IDCODE instruction.

Regardless of the original state of the controller, the controller enters the Test-Logic-Reset state when the J-TMS input is held high for at least five rising edges of J-TCK. The controller remains in this state while J-TMS is high. The CS61583 processor automatically enters this state at power-up.

Run-Test/Idle State

This is a controller state between scan operations. Once in this state, the controller remains in the state as long as J-TMS is held low. The

instruction register and all test data registers retain their previous state. When J-TMS is high and a rising edge is applied to J-TCK, the controller moves to the Select-DR state.

Select-DR-Scan State

This is a temporary controller state. The test data register selected by the current instruction retains its previous state. If J-TMS is held low and a rising edge is applied to J-TCK when in this state, the controller moves into the Capture-DR state and a scan sequence for the selected test data register is initiated. If J-TMS is held high and a rising edge applied to J-TCK, the controller moves to the Select-IR-Scan state.

The instruction does not change in this state.

Capture-DR State

In this state, the Boundary Scan Register captures input pin data if the current instruction is EXTEST or SAMPLE/PRELOAD. The other test data registers, which do not have parallel input, are not changed.

The instruction does not change in this state.

When the TAP controller is in this state and a rising edge is applied to J-TCK, the controller enters the Exit1-DR state if J-TMS is high or the Shift-DR state if J-TMS is low.

Shift-DR State

In this controller state, the test data register connected between J-TDI and J-TDO as a result of the current instruction shifts data on stage toward its serial output on each rising edge of J-TCK.

The instruction does not change in this state.

When the TAP controller is in this state and a rising edge is applied to J-TCK, the controller enters the Exit1-DR state if J-TMS is high or remains in the Shift-DR state if J-TMS is low.

Exit1-DR State

This is a temporary state. While in this state, if J-TMS is held high, a rising edge applied to J-TCK causes the controller to enter the Update-DR state, which terminates the scanning process. If J-TMS is held low and a rising edge is applied to J-TCK, the controller enters the Pause-DR state.
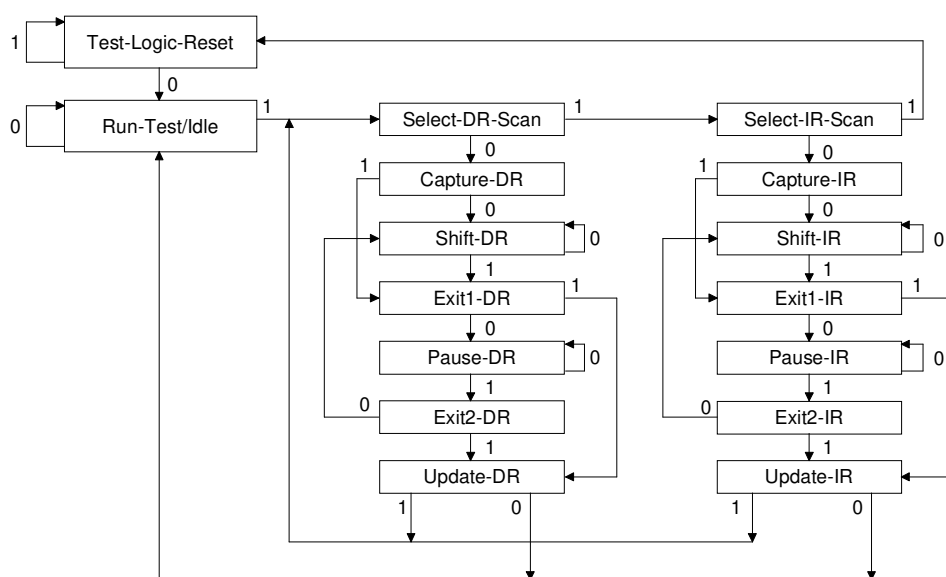
Figure 12. TAP Controller State Diagram

The test data register selected by the current instruction retains its previous value during this state. The instruction does not change in this state.

Pause-DR State

The pause state allows the test controller to temporarily halt the shifting of data through the test data register in the serial path between J-TDI and J-TDO. For example, this state could be used to allow the tester to reload its pin memory from disk during application of a long test sequence.

The test data register selected by the current instruction retains its previous value during this state. The instruction does not change in this state.

The controller remains in this state as long as J-TMS is low. When J-TMS goes high and a rising edge is applied to J-TCK, the controller moves to the Exit2-DR state.

Exit2-DR State

This is a temporary state. While in this state, if J-TMS is held high, a rising edge applied to J-TCK causes the controller to enter the Update-DR state, which terminates the scanning process. If J-TMS is held low and a rising edge is applied to J-TCK, the controller enters the Shift-DR state.

The test data register selected by the current instruction retains its previous value during this state. The instruction does not change in this state.

Update-DR State

The Boundary Scan Register is provided with a latched parallel output to prevent changes while data is shifted in response to the EXTEST and SAMPLE/PRELOAD instructions. When the TAP controller is in this state and the Boundary Scan Register is selected, data is latched into the

parallel output of this register from the shift-register path on the falling edge of J-TCK. The data held at the latched parallel output changes only in this state.

All shift-register stages in the test data register selected by the current instruction retains their previous value during this state. The instructions does not change in this state.

Select-IR-Scan State

This is a temporary controller state. The test data register selected by the current instruction retains its previous state. If J-TMS is held low and a rising edge is applied to J-TCK when in this state, the controller moves into the Capture-IR state, and a scan sequence for the instruction register is initiated. If J-TMS is held high and a rising edge is applied to J-TCK, the controller moves to the Test-Logic-Reset state. The instruction does not change in this state.

Capture-IR State

In this controller state, the shift register contained in the instruction register loads a fixed value of "01" on the rising edge of J-TCK. This supports fault-isolation of the board-level serial test data path.

Data registers selected by the current instruction retain their value during this state. The instructions does not change in this state.

When the controller is in this state and a rising edge is applied to J-TCK, the controller enters the Exit1-IR state if J-TMS is held high, or the Shift-IR state if J-TMS is held low.

Shift-IR State

In this state, the shift register contained in the instruction register is connected between J-TDI and J-TDO and shifts data one stage towards its serial output on each rising edge of J-TCK.

The test data register selected by the current instruction retains its previous value during this state. The instruction does not change in this state.

When the controller is in this state and a rising edge is applied to J-TCK, the controller enters the Exit1-IR state if J-TMS is held high, or remains in the Shift-IR state if J-TMS is held low.

Exit1-IR State

This is a temporary state. While in this state, if J-TMS is held high, a rising edge applied to J-TCK causes the controller to enter the Update-IR state, which terminates the scanning process. If J-TMS is held low and a rising edge is applied to J-TCK, the controller enters the Pause-IR state.

The test data register selected by the current instruction retains its previous value during this state. The instruction does not change in this state.

Pause-IR State

The pause state allows the test controller to temporarily halt the shifting of data through the instruction register.

The test data register selected by the current instruction retains its previous value during this state. The instruction does not change in this state.

The controller remains in this state as long as J-TMS is low. When J-TMS goes high and a rising edge is applied to J-TCK, the controller moves to the Exit2-IR state.

Exit2-IR State

This is a temporary state. While in this state, if J-TMS is held high, a rising edge applied to J-TCK causes the controller to enter the Update-IR state, which terminates the scanning process. If

J-TMS is held low and a rising edge is applied to J-TCK, the controller enters the Shift-IR state.

The test data register selected by the current instruction retains its previous value during this state. The instruction does not change in this state.

Update-IR State

The instruction shifted into the instruction register is latched into the parallel output from the shift-register path on the falling edge of J-TCK. When the new instruction has been latched, it becomes the current instruction.

Test data registers selected by the current instruction retain their previous value.

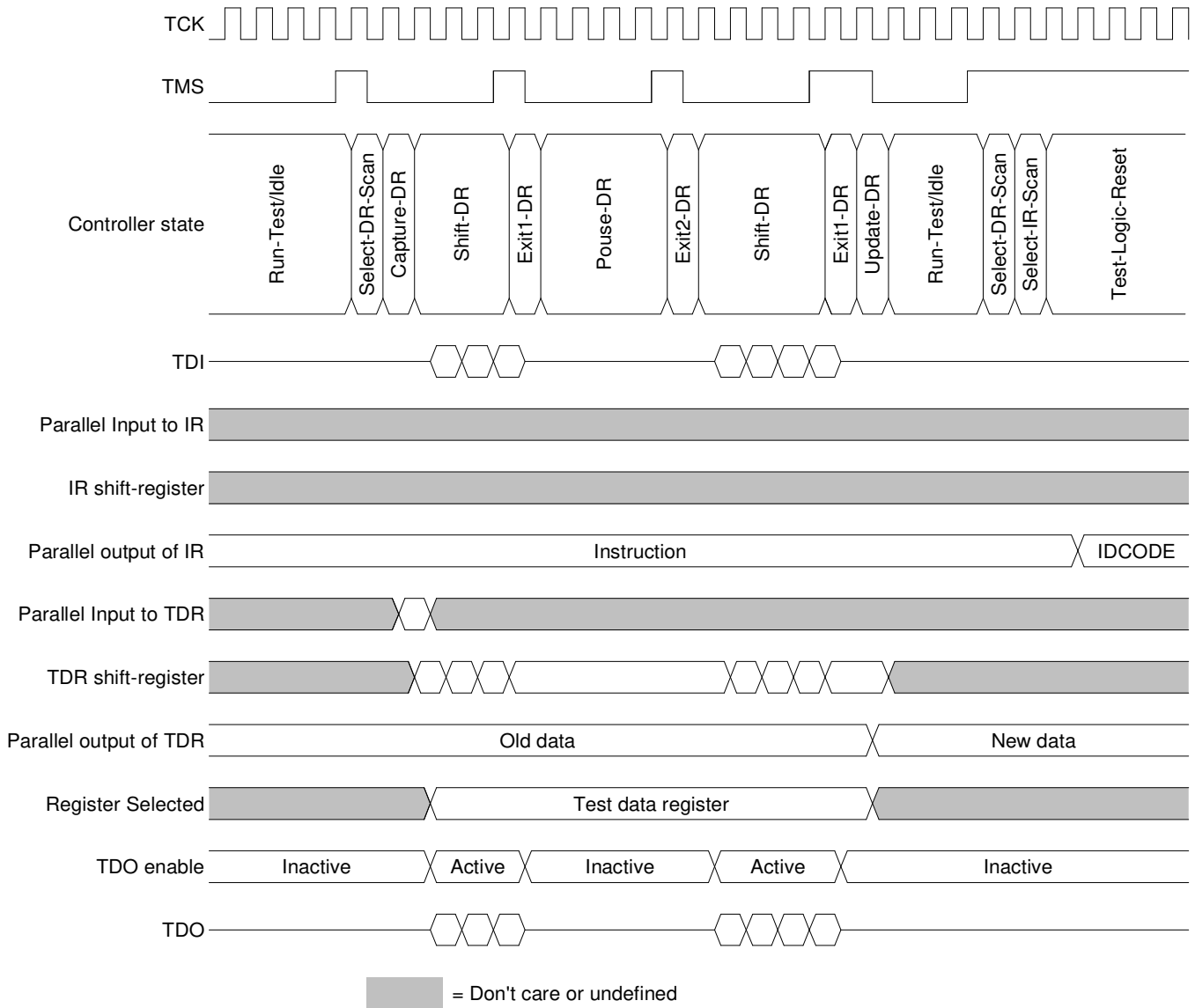### JTAG Application Examples

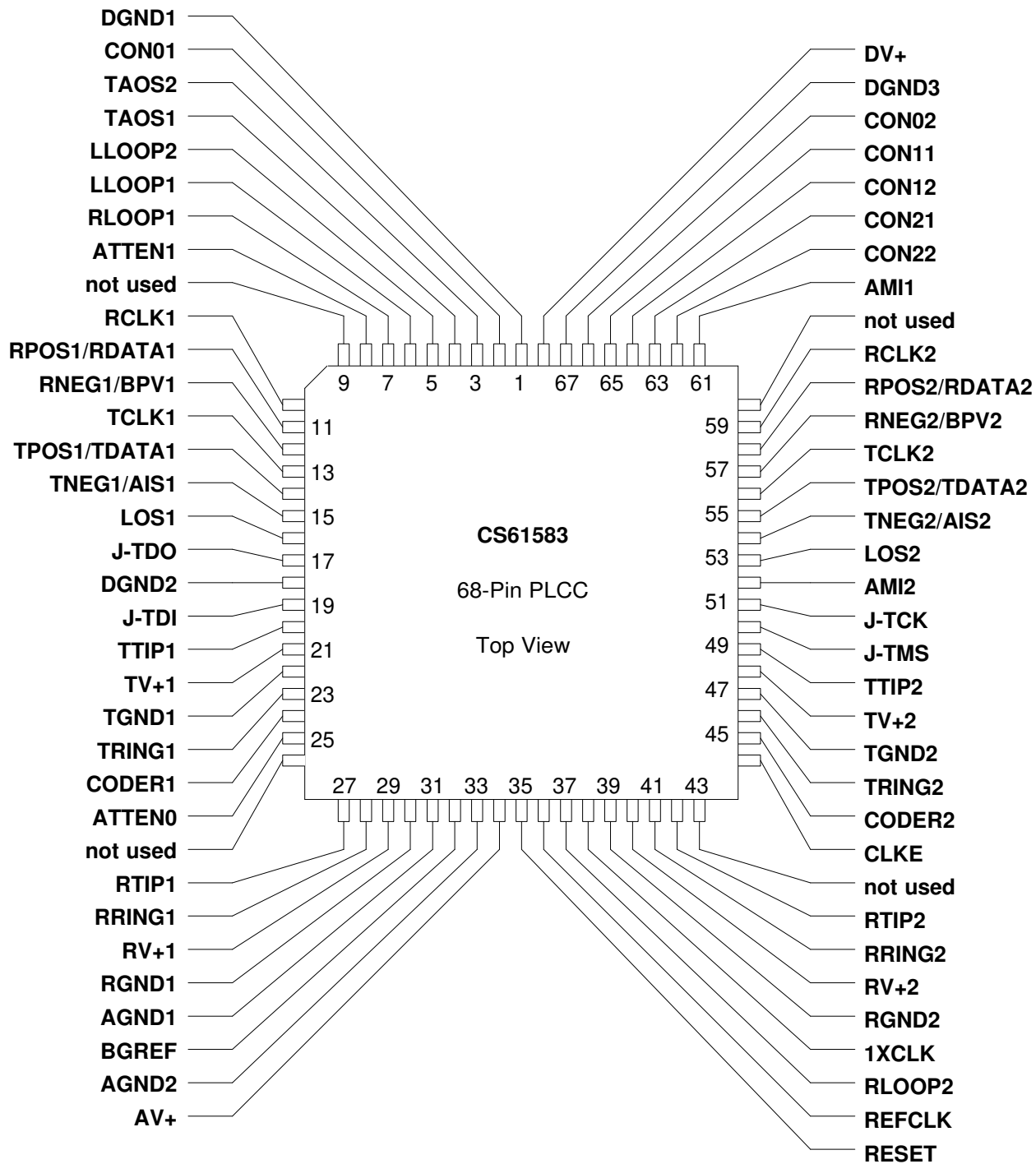Figures 13 and 14 illustrate examples of updating the instruction and data registers during JTAG operation.
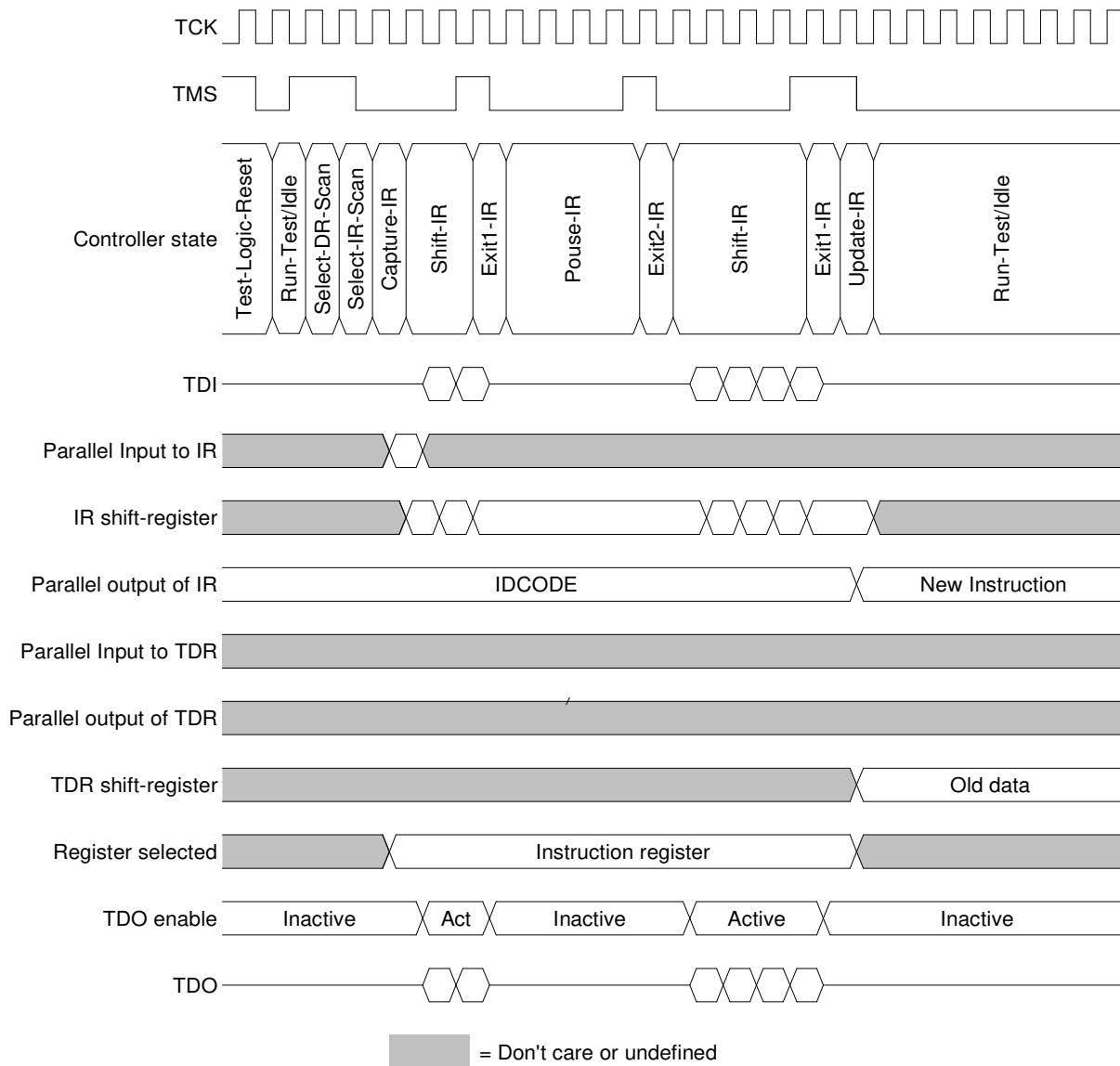
Figure 13. JTAG Instruction Register Update

Figure 14. JTAG Data Register Update

PIN DESCRIPTIONS

Left pins		Right pins
DGND1		DV+
CON01		DGND3
TAOS2		CON02
TAOS1		CON11
LLOOP2		CON12
LLOOP1		CON21
RLOOP1		CON22
ATTEN1		AMI1
not used		not used
RCLK1		RCLK2
RPOS1/RDATA1		RPOS2/RDATA2
RNEG1/BPV1		RNEG2/BPV2
TCLK1		TCLK2
TPOS1/TDATA1		TPOS2/TDATA2
TNEG1/AIS1		TNEG2/AIS2
LOS1		LOS2
J-TDO		AMI2
DGND2		J-TCK
J-TDI		J-TMS
TTIP1		TTIP2
TV+1		TV+2
TGND1		TGND2
TRING1		TRING2
CODER1		CODER2
ATTEN0		CLKE
not used		not used
RTIP1		RTIP2
RRING1		RRING2
RV+1		RV+2
RGND1		RGND2
AGND1		1XCLK
BGREF		RLOOP2
AGND2		REFCLK
AV+		RESET

Top pins: 9 7 5 3 1 67 65 63 61
Left numbers: 11 13 15 17 19 21 23 25
Right numbers: 59 57 55 53 51 49 47 45
Bottom pins: 27 29 31 33 35 37 39 41 43

CS61583

68-Pin PLCC

Top View

Note: Pins labeled as "not used" should be tied to ground.

DGND1

CON01

TAOS2

TAOS1

LLOOP2

LLOOP1

RLOOP1

ATTEN1

RCLK1

RPOS1/RDATA1

RNEG1/BPV1

TCLK1

TPOS1/TDATA1

TNEG1/AIS1

LOS1

J-TDO

DGND2

J-TDI

TTIP1

TV+1

TGND1

TRING1

CODER1

ATTEN0

RTIP1

RRING1

RV+1

RGND1

AGND1

BGREF

AGND2

AV+

DV+

DGND3

CON02

CON11

CON12

CON21

CON22

AMI1

RCLK2

RPOS2/RDATA2

RNEG2/BPV2

TCLK2

TPOS2/TDATA2

TNEG2/AIS2

LOS2

AMI2

J-TCK

J-TMS

TTIP2

TV+2

TGND2

TRING2

CODER2

CLKE

RTIP2

RRING2

RV+2

RGND2

1XCLK

RLOOP2

REFCLK

RESET

CS61583

64-Pin TQFP

Top View

64 62 60 58 56 54 52 50

1

2

4

6

8

10

12

14

16

48

46

44

42

40

38

36

34

18 20 22 24 26 28 30 32

Power Supplies

AGND1, AGND2 : Analog Ground (PLCC pins 31, 33; TQFP pins 21, 23)
Analog supply ground pins.

AV+ : Analog Power Supply (PLCC pin 34; TQFP pin 24)
Analog supply pin for the internal bandgap reference and timing generation circuits.

BGREF : Bandgap Reference (PLCC pin 32; TQFP pin 22)
This pin is used by the internal bandgap reference and must be connected to ground by a 4.99kΩ ±1% resistor to provide an internal current reference.

DGND1, DGND2, DGND3 : Digital Ground (PLCC pins 1, 18, 67; TQFP pins 57, 9, 55)
Power supply ground pins for the digital circuitry of both channels.

DV+ : Power Supply (PLCC pin 68; TQFP pin 56)
Power supply pin for the digital circuitry of both channels.

RGND1, RGND2 : Receiver Ground (PLCC pins 30, 39; TQFP pins 20, 29)
Power supply ground pins for the receiver circuitry.

RV+1, RV+2 : Receiver Power Supply (PLCC pins 29, 40; TQFP pins 19, 30)
Power supply pins for the analog receiver circuitry.

TGND1, TGND2 : Transmit Ground (PLCC pins 22, 47; TQFP pins 13, 36)
Power supply ground pins for the transmitter circuitry.

TV+1, TV+2 : Transmit Power Supply (PLCC pins 21, 48; TQFP pins 12, 37)
Power supply pins for the analog transmitter circuitry.

T1/E1 Data

RCLK1, RCLK2 : Receive Clock (PLCC pins 10, 59; TQFP pins 1, 48)
RPOS1, RPOS2 : Receive Positive Data (PLCC pins 11, 58; TQFP pins 2, 47)
RNEG1, RNEG2 : Receive Negative Data (PLCC pins 12, 57; TQFP pins 3, 46)
The receiver recovered clock and NRZ digital data from RTIP and RRING is output on these pins. The CLKE pin determines the clock edge on which RPOS and RNEG are stable and valid. A positive pulse (with respect to ground) received on RTIP generates a logic 1 on RPOS, and a positive pulse received on RRING generates a logic 1 on RNEG.

RDATA1, RDATA2 : Receive Data (PLCC pins 11, 58; TQFP pins 2, 47)
In coder mode (CODER = 1), the decoded digital data stream from RTIP and RRING is output on RDATA in NRZ format. The CLKE pin determines the clock edge on which RDATA is stable and valid.

RTIP1, RTIP2 : Receive Tip (PLCC pins 27, 42; TQFP pins 17, 32)
RRING1, RRING2 : Receive Ring (PLCC pins 28, 41; TQFP pins 18, 31)
The receive AMI signal from the line interface is input on these pins. The recovered clock and data are output on RCLK, RPOS, and RNEG (or RDATA).